

Flexible Fullerene Field-Effect Transistors Fabricated Through Solution Processing

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Recent research into organic semiconductors for organic thin-film transistors (OTFTs) – as alternatives to amorphous silicon-based systems – has yielded improved synthetic and fabrication techniques for devices with great potential for the use in consumable electronic applications.^[1–3] To realize the advantages of organic semiconductors in practical applications, OTFTs fabricated through solution processing (spin-coating, casting, or printing) on flexible substrates are strongly desired. Although many groups have developed OTFTs incorporating soluble small-molecule or polymer semiconductors, the number of available hole-transporting materials overwhelms the number of electron-transporting materials.^[4–6] Preparing efficient organic integrated circuits at low cost requires soluble hole- and electron-transporting materials that ideally exhibit comparable electrical performance. At present, the development of high-performance n-channel OTFTs remains a challenge, especially when using attractive fabrication processes (e.g., solution processing).

Since 1995, when C₆₀ was first suggested as a promising material for n-channel thin-film transistors,^[7] the electronic properties of these devices have improved dramatically, achieving field-effect mobilities of the order of 1 cm² V⁻¹ s⁻¹.^[8–10] Unfortunately, C₆₀ thin films have been prepared most commonly using complicated and time-consuming thermal evaporation processes. Recently, C₆₀ derivatives have gained much attention for the use in TFTs and bulk heterojunction solar cells because of their reasonable carrier mobilities and high solubilities in organic solvents,^[11–13] which makes device fabrication feasible through simple, low-cost spin-coating and printing processes. Despite these advantages, films prepared

from soluble C₆₀ derivatives, such as the fullerene derivative [6,6]-phenyl-C₆₁-butyric acid methyl ester (PCBM), have much lower mobilities than those obtained through thermal evaporation of C₆₀ thin films. In addition, the complicated syntheses of soluble C₆₀ derivatives are expensive.^[14]

C₆₀ is reasonably soluble in some organic solvents.^[15,16] Therefore, in addition to vacuum sublimation processing, it is likely that C₆₀ films could be formed through solution processing. Moreover, serious electron trapping has been observed recently on hydroxyl gate-dielectric surfaces, resulting in an instability of the corresponding n-channel transistors, which leads to a poor device performance under ambient conditions.^[17–19] Additionally, the relatively high electron affinity of C₆₀ (~4.5 eV) means that it readily forms low-resistance contacts with metals.^[20] In this study, we present C₆₀-based TFTs on rigid and flexible substrates through solution processing. Although we obtained C₆₀ in the amorphous phase after solution processing, the resulting transistors exhibit high performance, with field-effect mobilities as high as 0.21 cm² V⁻¹ s⁻¹ in the saturation regime.

Figure 1a and b displays typical transfer- and output-curve characteristics, respectively, of the C₆₀-based TFTs on a rigid indium tin oxide (ITO) glass substrate with Al source/drain (S/D) electrodes. The devices exhibit typical n-channel characteristics with a good linear/saturation behavior. We have observed a strong field-effect modulation of the channel conductance, with ON/OFF current ratios (*I*_{on}/*I*_{off}) as high as 5 × 10⁵ (measured for gate voltages (*V*_G) from –10 to +60 V). The field-effect mobility (*μ*) and the threshold voltage (*V*_T) were extracted from the measured transfer curve by comparing it with the standard current–voltage equation for a transistor in the saturation regime:

$$I_{DS} = (WC_i/2L)\mu(V_G - V_T)^2 \quad (1)$$

where *I*_{DS} is the saturated drain current.^[21] The transistors display mobilities as high as 0.21 cm² V⁻¹ s⁻¹ and a value of *V*_T of 0.7 V. Although the mobilities in our devices are slightly lower than those of OTFTs prepared through vacuum deposition, our devices perform much better than those prepared through solution processing.^[22–24] There are many factors that influence the value of *V*_T, such as bulk traps (unintentional doping), interfacial states (organic/dielectric interfacial traps), and the crystallinity of the materials. C₆₀ was purchased from Materials Technologies Research at >99.5% purity; however, because impurities (e.g., voids) are also formed during the fabrication process, unintentional doping is inevitable, leading to a lower

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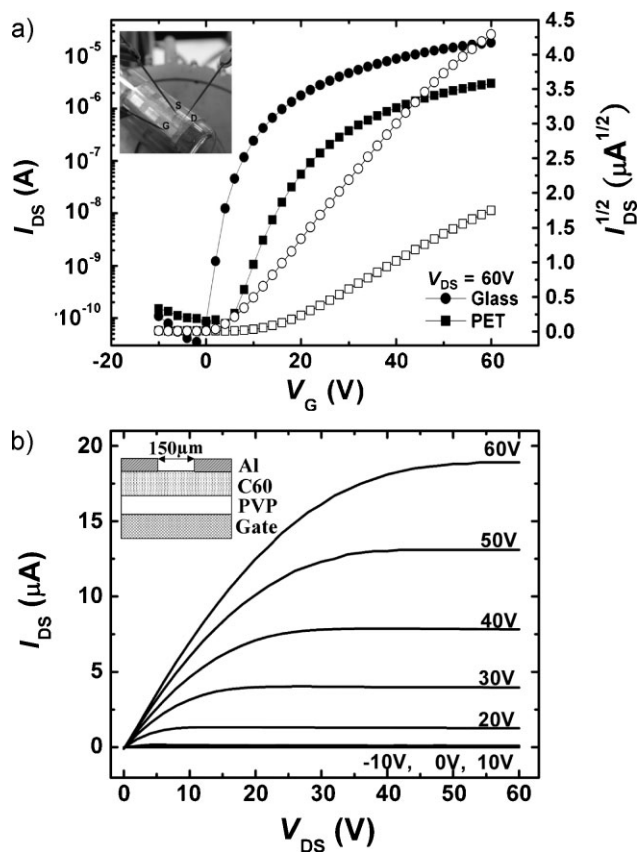


Figure 1. a) Transfer curves of C_{60} devices (at a saturated drain voltage (V_{DS}) of 60 V) prepared on flexible and rigid substrates obtained with real-time measurements; inset: photograph of a flexible device. b) Output characteristics of C_{60} devices grown on ITO glass; inset: device structure.

value of V_T , as had been observed by Dinelli et al.^[25] The presence of organic–dielectric interfacial traps also plays an important role in affecting the value of V_T . SiO_2 is traditionally employed as the gate dielectric in OTFTs, even though protonation of the siloxyl groups on the SiO_2 surface can generate some OH groups at the interface between SiO_2 and the organic semiconductor layer that can behave as electron traps.^[17] Several approaches have been examined to overcome such issues, including the use of self-assembled monolayers^[26] or polymers^[19,27] at SiO_2 –organic semiconductor interfaces. In this study, we use crosslinked poly-4-vinylphenol (PVP), rather than SiO_2 , as the gate dielectric to reduce the number of interfacial traps. Therefore, in our system, the low value of V_T is most likely related to unintentional doping and a lower number of organic–dielectric interfacial traps. The subthreshold slope (SS) is also strongly dependent on the interfacial trap density – it increases upon increasing the interfacial trap density. From the transfer curve, an SS of 1.4 V decade⁻¹ is extracted, which is not close to the theoretical minimum of 58 meV decade⁻¹ [$kT/q \ln(10)$] (k is the Boltzmann constant, T the absolute temperature, and q the magnitude of electrical charge), presumably because of the presence of the OH

groups of PVP that were not utilized in the crosslinking process. Hence, we anticipate that the value of SS is reduced if we use an OH-free gate dielectric.

For comparison, Figure 1a presents the transfer curves of devices prepared on rigid and flexible substrates. The mobilities in the flexible devices are approximately one order of magnitude lower than those of the devices prepared on rigid glass substrates. For the flexible devices, the transfer curves provide values of μ , SS, and V_T of 0.057 cm² V⁻¹ s⁻¹, 11 V, and 4.1 V decade⁻¹, respectively, thus, the threshold voltages of the flexible devices are higher than those of conventional devices formed on rigid substrates.^[28] A greater substrate roughness is likely to cause a greater density of trap states in the gate dielectric and at the dielectric–semiconductor interface; such phenomena may explain the observed decrease in mobility and the increase in the threshold voltage.^[29] The poorer characteristics of the flexible devices might also result from the high-temperature processing used to crosslink the polymer dielectrics, during which the flexible substrate may have undergone tensile/compressive stress. From a practical point of view, the need remains to prepare higher-performance organic transistors. Lowering the driving voltage and increasing the operating speed for solution-processable C_{60} TFTs can be achieved by incorporating high- k dielectrics^[30] or reducing the thickness of the dielectric.^[31,32] These approaches open up further applications for such devices. Overall, the devices prepared on flexible substrates exhibited good field-effect modulation with an ON/OFF ratio greater than 10⁴, sufficient for some practical applications.^[33]

Field-effect mobility is the key device parameter affecting the performance of TFTs. We found that the characteristics of TFTs, fabricated using C_{60} semiconductors, are dependent on the annealing temperature for the conversion from amorphous to crystalline C_{60} . Figure 2 displays the extracted plot of the mobilities of the devices prepared on both conventional glass and flexible substrates as a function of the annealing temperature. The trends in the variation of the mobility with respect to the temperature are similar for the devices prepared on the rigid and flexible substrates, indicating the compatibility of the flexible devices.^[34] In each case, the mobility reaches a maximum value at 90 °C. The decrease in mobility at annealing temperatures higher than 90 °C might be due to a change in the crystalline structure or an increase in grain size. The X-ray diffraction (XRD) pattern of a C_{60} thin film displays strong peaks that correspond to the (111)

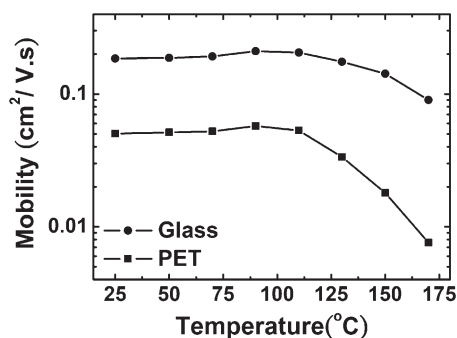


Figure 2. Mobilities of OTFTs featuring C_{60} semiconductor films annealed at temperatures between 25 and 170 °C.

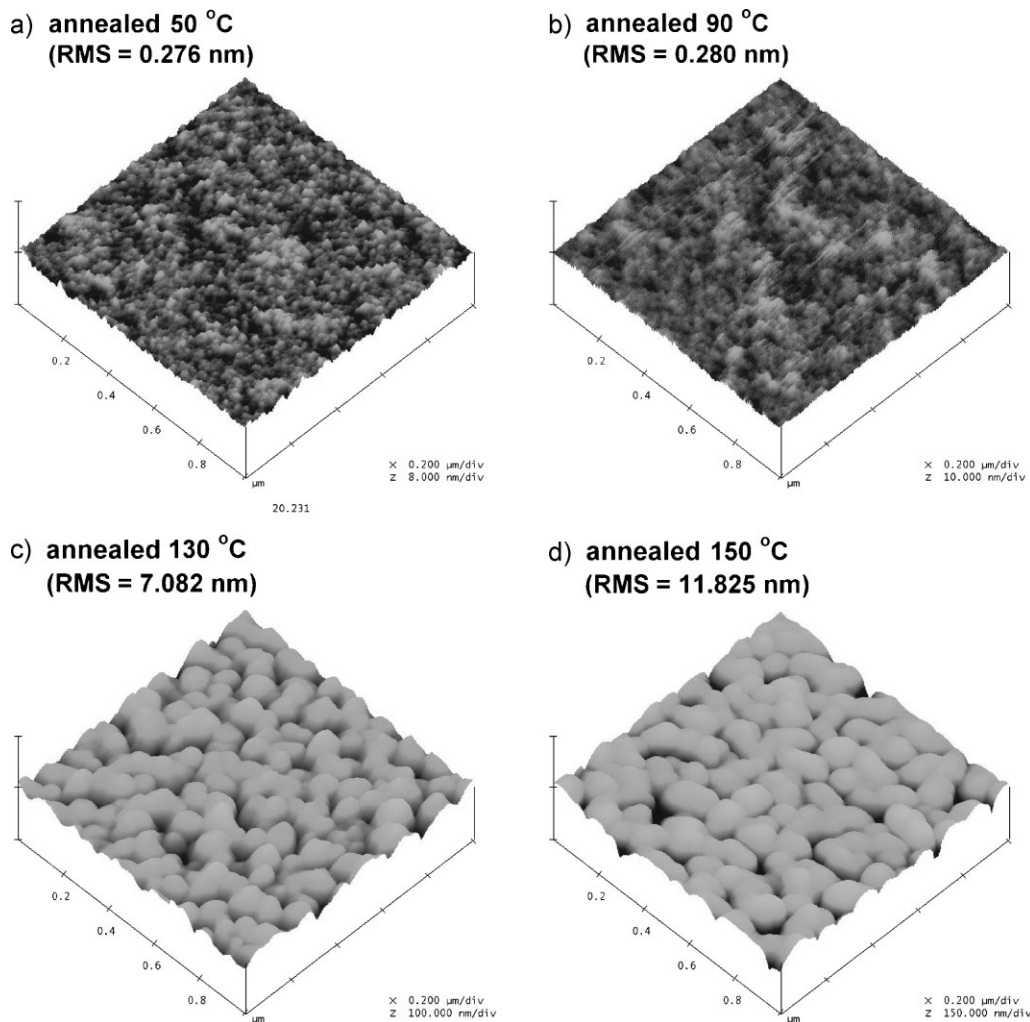


Figure 3. AFM images of C_{60} thin films on ITO glass/PVP substrates annealed at a) 50, b) 90, c) 130, and d) 150 °C. RMS stands for root mean square.

and (311) reflections of the face-centered cubic (fcc) phase of C_{60} , revealing the crystalline nature of the sample. Although crystallinity generally favors an enhancement in mobility, the opposite trend is observed in our case, presumably because of pronounced grain-boundary effects, which act as carrier scattering centers across the drain–source interface. Because such scattering seriously affects transport across the drain–source interface, the mobility decreases at high temperatures.

Figure 3a–d displays atomic force microscopy (AFM) images of the C_{60} films annealed at temperatures ranging from 50 to 150 °C. The surface morphologies of the films annealed at 50 and 90 °C are very smooth. In contrast, the faceted crystalline C_{60} film obtained after annealing at 130 °C exhibits a very rough surface morphology. The average grain size increases upon increasing the annealing temperature but the mobility is not obviously related to the annealing temperature. The AFM images reveal that high temperatures support the crystallization of the C_{60} molecules. Figure 4 presents XRD patterns of the C_{60} thin films after thermal treatment at 50–150 °C. The C_{60} films subjected to annealing at 50 and 90 °C possess amorphous features, whereas those annealed at 130 and 150 °C exhibit the strong diffraction

peaks of crystalline C_{60} . Crystallization phenomena dominate the behavior of transistors at high temperatures and, thus, determine the performance of the devices. The correlation between the grain size and the mobility is an interesting phenomenon. For planar

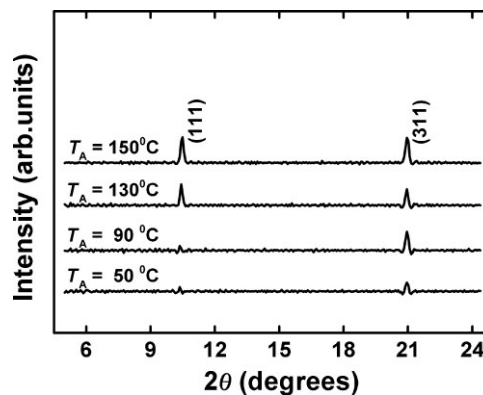


Figure 4. XRD patterns of C_{60} thin films grown on ITO/PVP substrates after annealing at 50, 90, 130, and 150 °C (T_A : annealing temperature).

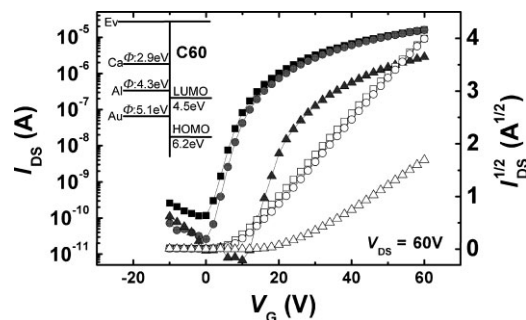


Figure 5. Typical transfer characteristics of C_{60} OTFTs featuring Au (triangles), Al (circles), and Ca (squares) as S/D electrodes at a constant drain voltage of 60 V.

molecules (e.g., pentacene) the mobility should increase with an increase in grain size. However, for spherical molecules (e.g., C_{60}), even when the grain size is small, nearest-neighbor hopping could lead to carrier transport, thus, our observed high mobility originates from the molecular assembly of the spherical molecules. When the annealing temperature is higher than 90 °C, pronounced grain-boundary effects become apparent (see the AFM images), thereby resulting in a marginal decrease in mobility. Grain-boundary effects in spherical molecules such as C_{60} are interesting phenomena that require further investigation. Our results suggest that the grain size has a less pronounced effect on the mobility of the device.

To study the effect of the work function of the metal electrodes on the performance of the C_{60} -based OTFTs, three metals (Ca, Al, and Au), possessing different work functions (5.1, 4.3, and 2.9 eV, respectively), have been used as the S/D electrodes. The Ca electrodes were covered by an Al layer to protect them from oxidation. The energy level of the lowest occupied molecular orbital (LUMO) for C_{60} is 4.5 eV.^[35,36] Figure 5 displays the transfer characteristics of C_{60} -based TFTs incorporating the various metals as the S/D electrodes. The values of μ and V_T are $0.22 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and -3 V , respectively, for the device incorporating Ca/Al S/D electrodes, $0.21 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 0.7 V , respectively, for that featuring Al electrodes, and $0.035 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 22 V , respectively, for that featuring Au electrodes. The maximum currents increase as the work function of the metal electrodes decreases. For devices grown under similar conditions and having a top-contact structure, the variation in mobility should result mainly from the value of the contact resistance between the organic semiconductor and the metal electrodes. The expected Schottky-barrier height at the interface between Au electrodes and C_{60} is 0.6 eV, with virtually no barrier for Ca and Al electrodes. We anticipated that the performance of C_{60} -based TFTs would be affected by a large contact resistance between the electrodes and the C_{60} channel, resulting in lower values of mobility in the case of high-work-function metals (e.g., Au). The mobility increases upon decreasing the work function of the electrode and we have observed a low-resistive ohmic characteristic of the Ca and Al contacts lacking a Schottky barrier. Because the work functions of Ca and Al are lower than the LUMO energy level of C_{60} , no energy barrier exists for carrier injection across the metal-semiconductor contact. As a result, the mobility is more than five times higher than that obtained with the Au electrodes. To

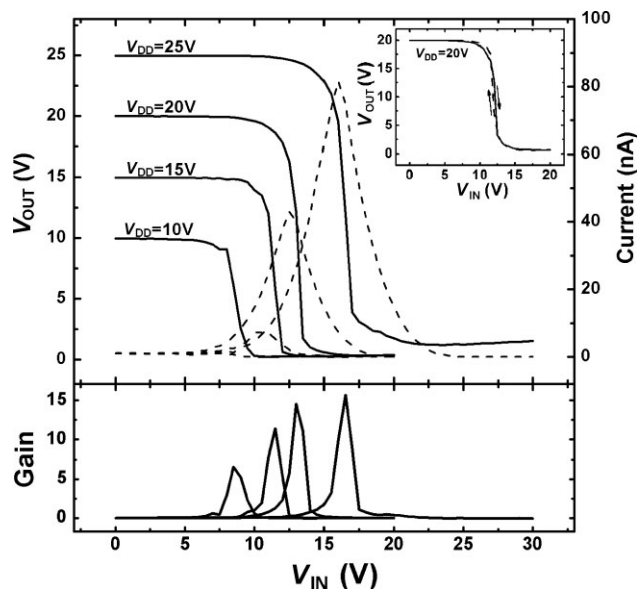


Figure 6. Output voltage (top, solid line), current (top, dashed line), and small-signal gain (bottom, solid line) plotted with respect to the input voltage for supply voltages between 10 and 25 V. The inverter featured a small-signal gain of 15. Inset: Transfer characteristics of the inverter in forward and back scans at a supply voltage of 20 V.

study the atmospheric stability of the devices, they were exposed to air for 30 min and then returned to the glove box. The mobility of these devices decreased by $\sim 50\%$; however, when the devices are maintained either in vacuum or under an inert atmosphere, their mobilities are stable for several weeks. Surface passivation might be one way to minimize the degradation of the mobilities of devices in air.

When preparing high-performance organic complementary inverters with reasonable gain, it is highly desirable that both p- and n-type transistors have high and comparable device performances. Figure 6 displays the voltage transfer characteristics of an organic complementary inverter incorporating pentacene and C_{60} as p- and n-type semiconductors, respectively. The performance of the pentacene-based TFT was tested separately; its mobility is $0.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. At a small input voltage (V_{IN}), the p- and n-type transistors are in ON and OFF states, respectively; as a result, the device functions as an inverter. Consequently, the output voltage (V_{OUT}) is almost equal to the supply voltage (V_{DD}) when the latter is varied between 10 and 25 V. When the value of V_{IN} exceeds the threshold voltage of the inverters, the p-type transistor turns off and the n-type transistor turns on. As a result, the value of V_{OUT} switches to become almost equal to zero. The small-signal gain, defined as the maximum value of the slope of the transfer curve, is 15. The small-signal gain increases as the value of V_{DD} augments. The corresponding increase in current, when the inverter is switched eventually, leads to power consumption, thus, when the inverter is switched, the power consumption deteriorates with an increase in V_{DD} . Most importantly, the hysteresis effect in the inverter circuit is negligible for a supply voltage of 20 V (inset of Fig. 6). Further enhancement to the performance of our complementary circuits might be achieved by incorporating a high- k dielectric^[37,38] or reducing the thickness of the dielectric.^[20,39]

In summary, we have fabricated C₆₀-based TFTs through solution processing. XRD and AFM analyses have revealed that the solution-processed films possess an amorphous C₆₀ phase. Crystalline C₆₀ was not essential to achieve the highest field-effect mobility. We have also fabricated C₆₀-based TFTs incorporating S/D electrodes of three different materials (Ca, Al, and Au). The highest mobility (0.21 cm² V⁻¹ s⁻¹) occurs in the C₆₀ field-effect transistors featuring Ca and Al electrodes and is approximately one order of magnitude higher than that obtained using Au electrodes. Our results demonstrate that complementary circuits can be fabricated using solution-processed small-molecule organic semiconductors.

Experimental

Devices were fabricated on ITO-coated glass substrates (<10 Ω sq⁻¹ sheet resistance) and ITO-coated poly(ethylene terephthalate) (PEN) substrates (8–12 Ω sq⁻¹ sheet resistance). The ITO on the glass substrate was used as the gate electrode. After routine solvent cleaning, the substrates were treated with UV-ozone for 15 min. The cleaned ITO substrates were then covered with a 680-nm-thick polymer dielectric insulator, prepared by spin-coating a solution of PVP (11 wt%) and poly(melamine-co-formaldehyde) (4 wt%) in propyleneglycol monomethyl ether acetate (PGMEA). The substrate was then prebaked at 100 °C for 5 min, followed by baking at 200 °C for 20 min, to crosslink the polymer. The resulting capacitance per unit area of the film (C_i) is 5.47 nF cm⁻². For deposition of the active layer, a 1 wt% C₆₀ solution was prepared in trichlorobenzene. The active layers of C₆₀ (Materials Technologies Research, >99.5%) thin films were spin-coated over the crosslinked PVP-covered ITO glass substrates under a N₂ atmosphere inside a glove box. To induce crystallization in the films, prior to S/D electrode deposition, the devices were thermally annealed on a hot plate at various temperatures (50–150 °C) for 10 min. Finally, Al was thermally evaporated onto the C₆₀ film through a shadow mask to form the S/D electrodes. To study the effect of the electrode materials on the performance of the devices, other metal electrodes (Ca and Au) were also deposited. For the construction of complementary circuits, as *p*-type partners to the solution-processed C₆₀ devices, pentacene TFTs were fabricated through vacuum evaporation. A schematic cross section of the top-contact OTFTs is presented in the inset of Figure 1a; the channel length is 150 μm and the width is 2 mm. The electrical performance of the devices was measured under a N₂ atmosphere inside a glove box using a Keithley 4200 semiconductor parameter analyzer and an HP 4980A Precision LCR meter.

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