國立交通大學

電機資訊學院　電子與光電學程

碩 士 論 文

應用於 IEEE 802.11A 之射頻前端發射器設計

RF Transmitter Front-End Design for IEEE 802.11A

研 究 生：陳聯興

指導教授：溫瓌岸 教授

中 華 民 國 九 十 三 年 六 月

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摘要

在本篇論文中完成了適用於 IEEE 802.11a 之前端發射器設計，本設計採用聯電 0.18-μm 1P6M CMOS 製程完成晶片製作，並以矽品 QFN20 完成封裝,。此顆 IC 的特點有二點，一是工作的頻寬相當寬(5G~6GHz)， 可包含 U-NII (5.15G~5.825 GHz)內的所有頻帶。二是所需的外部元件非常少，不再需要 balun 跟 SAW 濾波器。IC 中包含了兩個 balun、直接升頻混波器以及三級的前置放大器。模擬的結果可以達到輸出 1-dB 點為 10.5dBm(在 5.5GHz)，其旁波抑制為 38.7dB，轉換增益為 13.8 dB。在實際的封裝量測中，輸出 1-dB 點為 3.8dBm(在 5.5GHz)，旁波抑制有 34.3dB，轉換增益為 10.5 dB。

Abstract

In this thesis, a direct-conversion transmitter front-end for IEEE 802.11a has been designed and fabricated in UMC 0.18-μm 1P6M CMOS technology and packaged in SPIL QFN20. There are two features in this chip. First, it operates in the 5 to 6 GHz which covers the U-NII frequency band (5.15 to 5.825GHz). Secondly, it reduces the needs for external component. No external baluns and SAW filters are required. The transmitter front-end contains two baluns, an up-conversion mixer and a three-stage pre-amplifier. The simulation achieves an output 1-dB compression of 10.5 dBm at 5.5GHz with 38.7 dB sideband rejection and 13.8 dB conversion gain. The result of measurement exhibits an output 1-dB compression of 3.8 dBm at 5.5GHz with 34.3dB sideband rejection and 10.5dB conversion gain.

誌謝

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誌于　　2004

陳聯興

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Chap 1.

Introduction

1.1 Motivation

Owing to the fast development of wireless communications, the low cost, high performance and high integration technology is necessary for system-on-chip (SoC) design. The CMOS technology has been explored for RF IC design is a possible solution of low cost and high integration. However, there are enormous challenges to RF designer in CMOS technology as follows: higher NF, lower gm, higher parasitic output capacitance, inaccurate device model, low-Q passive components, etc. Therefore, these issues must be considered carefully during design. In this thesis, to design and fabricate a transmitter front-end chip in CMOS 0.18μm processes which meets IEEE 802.11a standard is presented.

The function block diagram of entire transceiver is shown in Fig. 1.1. The transceiver employees direct conversion architectures to reduce the number of off-chip components by eliminating requirements of IF filters. In transmit path, the baseband signal is filtered by a low-pass filter and up-converted to RF signal by a quadrature mixer. The power amplifier boosts RF signal and outputs to the

antenna. We will focus on the design and analysis for the transmitter front-end stage in the thesis.

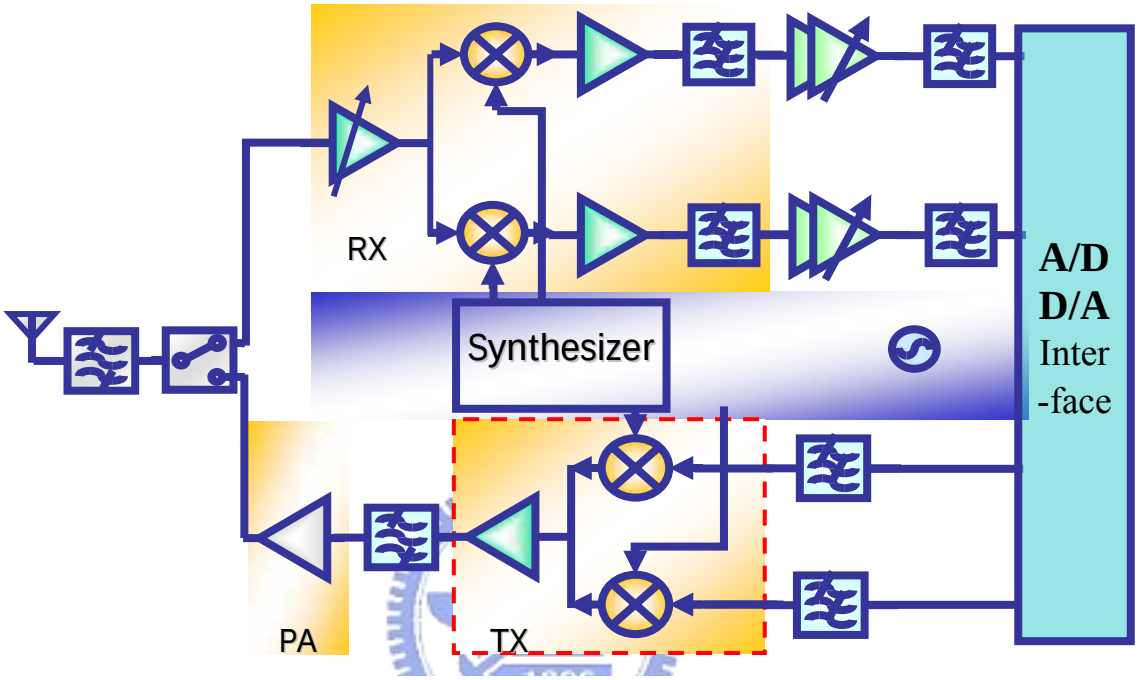


Fig. 1.1 Transceiver function block

1.2 IEEE 802.11a standard

As shown in Fig. 1.2, the IEEE 802.11a standard operates in the 5-GHz unlicensed national information infrastructure (U-NII) band [1]. It provides a total bandwidth of 300 MHz which is nearly four times to the 802.11b. The lower and middle U-NII sub-bands accommodate eight channels in a total bandwidth of 200MHz. The upper U-NII band accommodates four channels in a 100MHz bandwidth. The centers of the outmost channel shall be at distance of 30MHz

from the band's edges for the lower and middle U-NII bands, and 20MHz for the upper U-NII band. The standard supports channel bandwidths of 20MHz, with each channel being OFDM modulated signal consisting of 52 subcarrries. Each of the subcarrier can be a BPSK, QPSK, 16-QAM, or 64-QAM modulated signal.

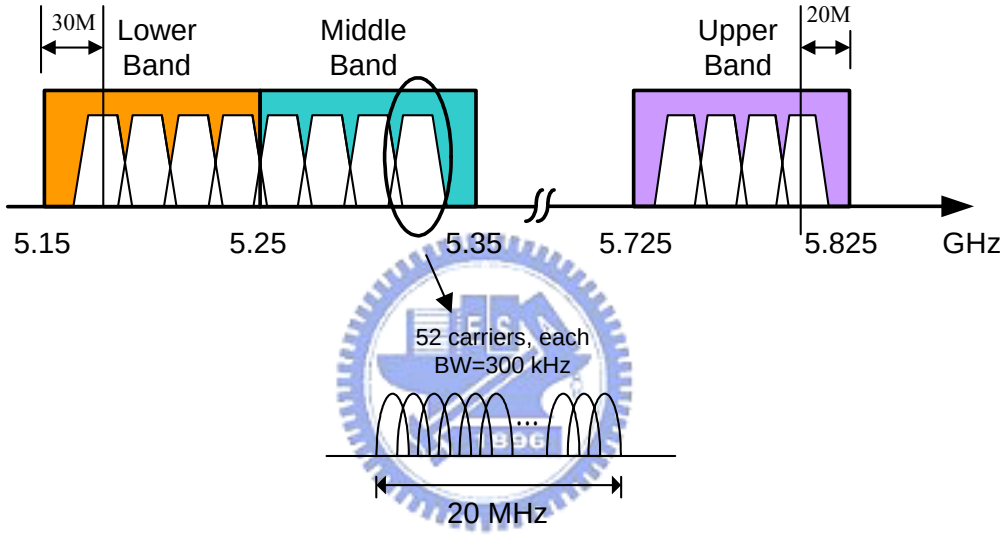


Fig. 1.2 Frequency cannel plan for 802.11a

The error vector magnitude (EVM) is used to indicate the quality of digitally modulated signal. EVM takes into account signal impairments such as phase and amplitude mismatches, phase noise, thermal noise and nonlinearity, etc. The modulation schemes and EVM requirements for transmitter are summarized in Table 1.1.

To prevent the out-of-channel emission leading to interference on the

adjacent channel or other wireless applications, IEEE 802.11a regulates maximum power level and transmit spectrum mask. The maximum allowable output power according to FCC regulations is illustrated in Table 1.2. The transmitted spectral density of the transmitted signal shall fall within the spectrum mask, as displayed in Fig. 1.3.

Table 1.1 Modulation scheme and EVM requirement

Data Rate (Mbits/s)	Modulation	Coding Rate	EVM (dB)	Minimum sensitivity (dBm)
6	BPSK	1/2	-5	-82
9	BPSK	2/3	-8	-81
12	QPSK	1/2	-10	-79
18	QPSK	3/4	-13	-77
24	16-QAM	1/2	-16	-74
36	16-QAM	3/4	-19	-70
48	64-QAM	1/2	-22	-66
54	64-QAM	3/4	-25	-65

Table 1.2 Transmit maximum power levels

Frequency band (GHz)	Maximum output power with up to 6dBi antenna gain (mW)
5.15~5.25	40 (2.5 mW/MHz)
5.25~5.35	200 (12.5mW/MHz)
5.725~5.825	800 (50 mW/MHz)

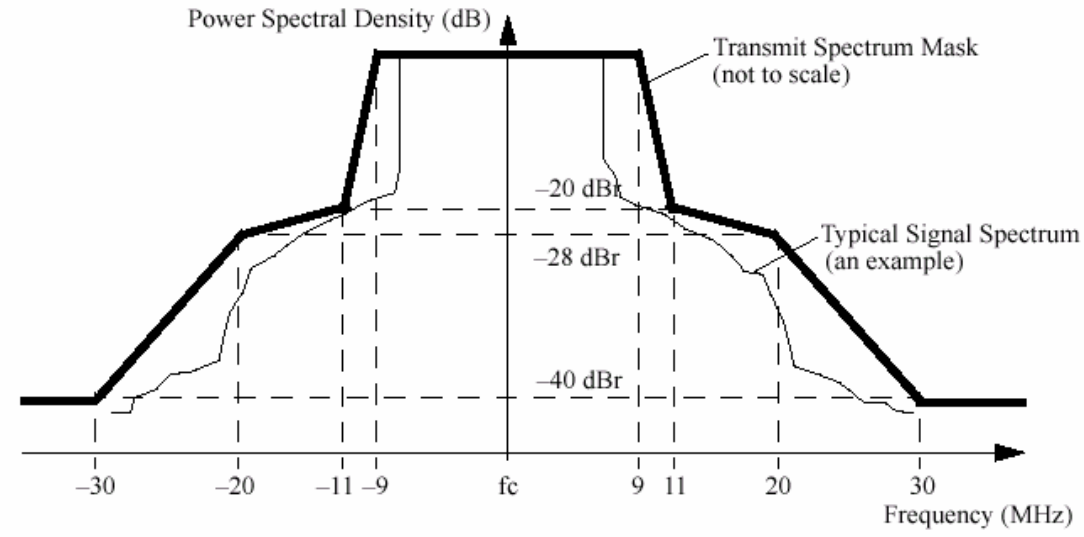


Fig. 1.3 Transmit spectrum mask

Chap 2.

Transmitter Architecture

The purpose of the wireless transmitter is to convey information to radio interface by modulation and up-conversion. The architecture plays an import role in the complexity and performance of the overall transmitter. The transmitter architectures are found in only a few forms, because those issues such as noise, interference rejection, and band selectivity are more relaxed in transmitter than in receivers [2]. In this chapter, we will introduce two types of transmitter architectures, whose advantages and drawbacks will be discussed in detail.

2.1 Superhetrodyne transmitter

Fig. 2.1 shows a traditional superhetrodyne architecture of transmitter. The transmitter up-converts baseband I and Q signal to RF using a carrier generated by mixing the outputs of two local oscillators, LO1and LO2. The first BPF rejects the harmonics of IF signal, while the second BPF remove unwanted sideband of RF signal.

Since the power amplifier (PA) output spectrum lies far from the operation

frequencies of the VCO, no injection pulling occurs. Another advantage of superhetrodyne transmitter is better I and Q matching because quadrature modulation is performed at lower frequencies, leading to less cross-talk between the two bit streams. Moreover, it is easier to control output power in a superhetrodyne transmitter than in direct conversion.

The transmitter suffers form a number of drawbacks as follows. First, The IF band-pass filter and RF band-pass filter are bulky and expensive. Next, the circuits of the superhetrodyne transmitter are more complex. Therefore it consumes higher power.

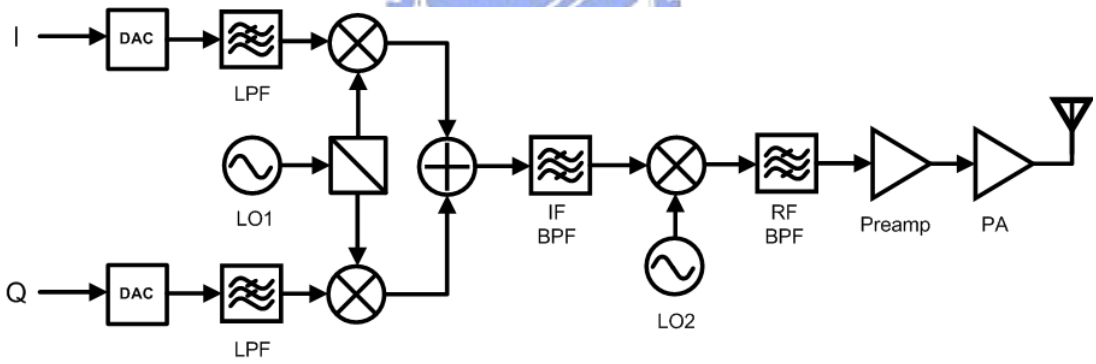


Fig. 2.1 Superhetrodyne transmitter

2.2 Direct-conversion transmitter

The direct-conversion transmitter only performs a single frequency conversion to RF as illustrated in Fig. 2.2. In this case, modulation and up-conversion occur in the same circuit. The direct-conversion transmitter is

usually preferred in a fully integrated design, because it avoids the need for an off-chip IF filter and demands only a single frequency synthesizer.

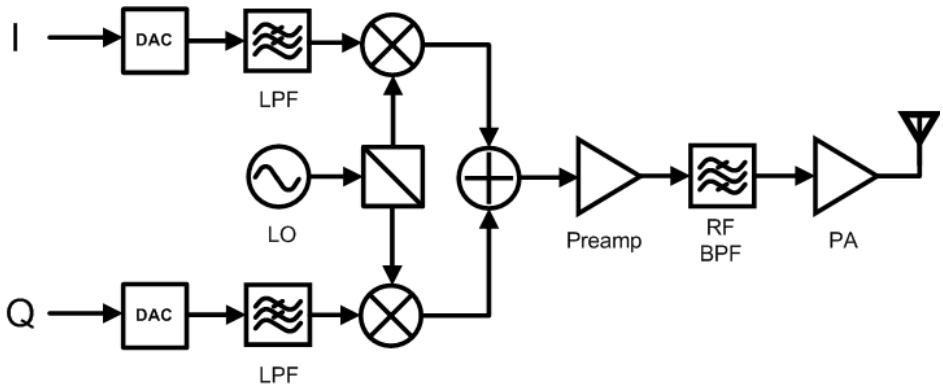
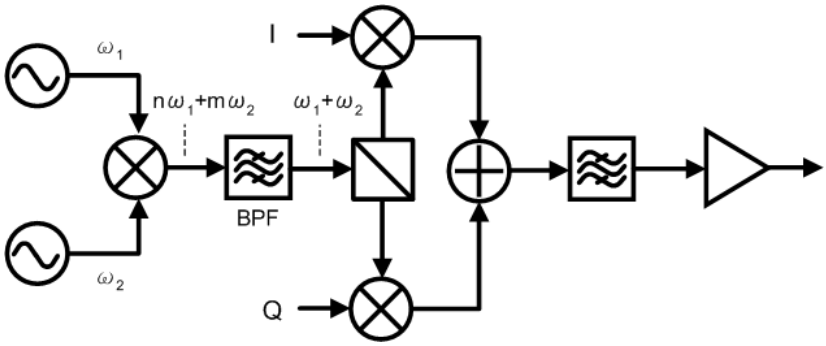


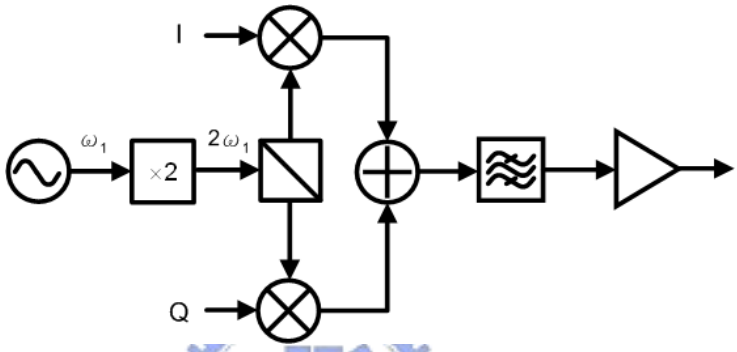
Fig. 2.2 Direct-conversion transmitter

The architecture of Fig. 2.2 suffers from an important drawback: local pulling or injection pulling. This issue arises because the PA output is a modulated waveform with high power and a spectrum centered around the LO frequency. If the high power signals feedback to the local oscillator through coupling or radiation, it becomes the noise injection to the oscillator. The problem worsens if the PA is turned on and off periodically to save power.

The phenomenon of LO pulling is alleviated if the PA output frequency is sufficiently higher or lower than the oscillator frequency. For quadrature modulation scheme, this can be accomplished by “offsetting the LO frequency” as shown in Fig. 2.3(a)(b).



(a)



(b)

Fig. 2.3 Offset the LO frequency (a) By adding two LO (b) by multiplying LO

Other issues of direct-conversion transmitter are not as critical as mentioned in the above discussion. First, the power control allocated at RF is harder to maintain accuracy and consumes more power. Second, the quadrature modulation occurs at RF frequency, thus I and Q matching become worse.

Chap 3.

Circuit Implementation

3.1 Circuit block diagram

Fig 3.1 shows a block diagram of the transmitter front-end using direct conversion architecture, the modulated I/Q baseband (BB) signal is directly mixed with a local frequency at the desired transmitted channel frequency. However, this architecture suffers from the VCO pulling due to the leakage of the power amplifier (PA) output. This drawback can be overcome by proper shielding (or separating) local oscillator and PA.

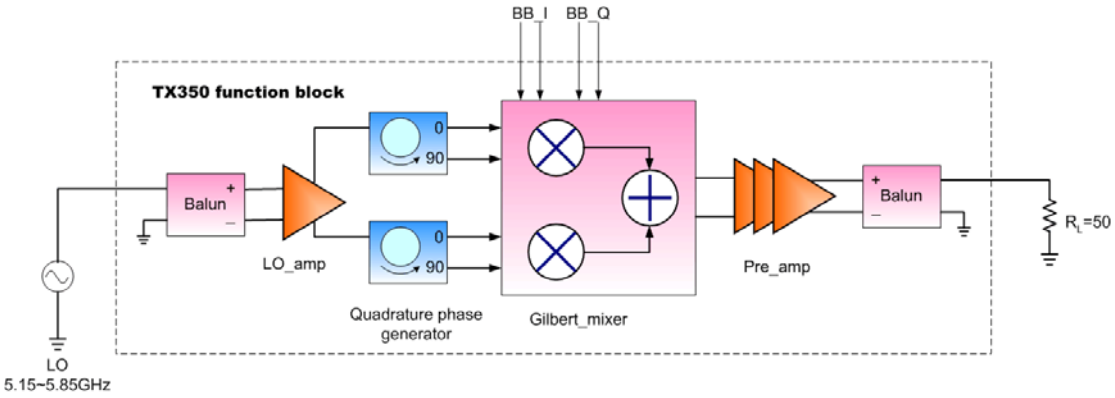


Fig 3.1 Block diagram of the transmitter front-end

In order to reduce size and cost of the transmitter, how to achieve a higher degree of integration of RF circuitry is one of the key design issues. The

transmitter front-end is comprised of two baluns, a local driver amplifier, two quadrature phase generators, an I/Q quadrature modulator (Gilbert cell mixer) and a three-stage pre-amplifier. The I/Q modulator take differential base-band input BB_I and BB_Q, frequency up-converts with the quadrature LO signals, and sums the output signals. On-chip inductors are used as loads at the mixer output to increase the voltage swing. The pre-amplifier boosts the output power to a level capable of driving the external power amplifier.

Precise quadrature LO signals are important for the direct conversion architecture. Any amplitude mismatches or phase differences apart from 90^{o} between LO_I and LO_Q causes degradation in the error vector magnitude (EVM). This design contains quadrature phase generators to reduce the amplitude mismatch and phase error. The purpose of LO amplifier is twofold: to improve the isolation between the mixer and LO, therefore reducing injection pulling of the LO, and to provide large LO level to optimize the mixer linearity and noise performance.

3.2 Specification

The 802.11a standard provides a total bandwidth of 300MHz in the 5GHz UNII band (5.15 to 5.825GHz), so operating in the 5 to 6 GHz which covers all the UNII frequency bands is our design goal [1]. The maximum allowed transmit

power is 16, 23, and 29dBm, respectively, for channels residing in the lower, middle and upper band. The specification of middle band is chosen in our design. Thus, the maximum output power through antenna is

$$P_{antenna\_out,\max} = 23 \text{ dBm}$$

which contains a 6-dB antenna gain. Hence, the final transmit power before antenna should be below

$$P_{TX\_OUT,\max} = 23 - 6 = 17 \text{ dBm}$$

The transmitter output power is thus determined as 16dBm with 1-dB margin. Notice that this value is the average output power. The peak-to-average power ratio (PAPR) is the problem to be concerned for OFDM system. In the worst case, suppose 52 peaks for the sinewaves add together, the PAPR will be 10log(52) ≈ 17dB. However, in practice, The PAPR is as low as 6 dB may meet the EVM and packet error rate (PER) requirement of the IEEE 802.11a specifications. Thus, the peak output power is

$$\begin{aligned} P_{out,peak} &= P_{out,avg} + PAPR \\ &= 16 + 6 \\ &= 22 \text{ dBm} \end{aligned}$$

With the P_{out} and gain of each stage, the output power of each module is obtained in Table 3.1. In general, the OP-1dB is the maximum operation boundary. After calculation, the OP-1dB of preamp and quadrature mixer are 4dBm and -11dBm, respectively. The relationship between OP-1dB and OIP3 can be

obtained

$$\frac{A_{O-P1dB}}{A_{OIP3}} \approx -10\,\text{dB} \tag{3.1}$$

The link budget of the entire transmitter system is listed in Table 3.1 and the specifications of transmitter front-end are summarized in Table 3.2.

Table 3.1 Link budget of the entire transmitter

Parameters	BPF1	T/R	PA	BPF2	Pre Amp	Mixer	LPF	DAC	Unit
Gain	-1	-2	22	-1	15	-5	-2		dB
Pout,avg	14	15	17	-3	-2	-17	-12	-10	dBm
Pout,peak	22	24	25	3	4	-13			dBm
OP-1dB	22	24	25		4	-11			dBm
OIP3			35		14	-1			dBm

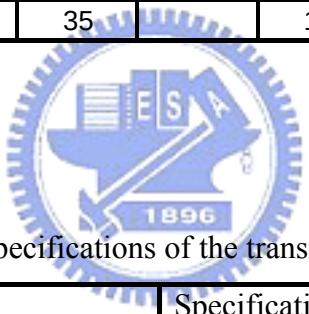


Table 3.2 Specifications of the transmitter front-end

Parameters	Specifications
Frequency Range	5-6 GHz
Conversion Gain	10 dB
IIP3	4 dBm
OIP3	14 dBm
OP1dB	4 dBm
Sideband rejection	>30 dB
Carrier rejection	>30 dB

3.3 Balun design

With today's CMOS IC technology, it can provide high frequency active devices for RF applications, but high quality passive components (e.g., inductors and transformer) present serious challenges for integration. Although significant progress toward the integration of high quality inductors has been reported, practical planar monolithic inductors achieves only moderate performance due to resistive losses in the metal traces and in the underlying substrate.

In this section, two types of baluns (balance to unbalance) which are suitable for CMOS implementation are described. A monolithic transformer comprising two coupled inductors occupies less area and exhibits a higher quality factor (Q) than LC-balun in differential circuits. However, modeling and parameter extraction of monolithic transformer is more difficult than the other. It also needs 3D electromagnetic simulator and spends much more time on simulation.

On-chip LC-balun is shown in Fig. 3.2. It is easy to be designed and fabricated in IC processes. Therefore, the LC-balun is used in our chip. The insertion loss of the LC-balun is higher

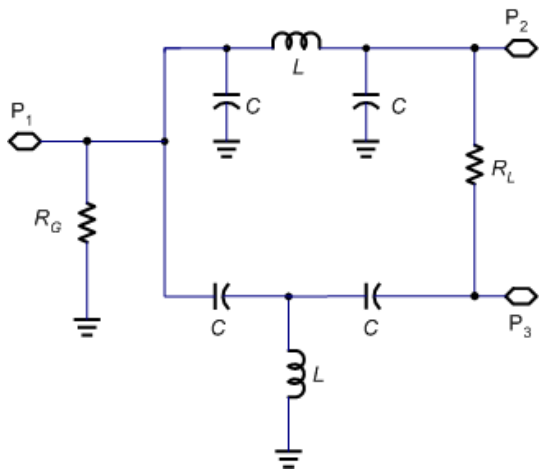


Fig. 3.2 LC-balun

than the monolithic transformer and need carefully design.

We will analyze this circuit by reducing it into two simple half-circuits driven by symmetric source, and redrew the circuit as shown in Fig. 3.3. Note that the port impedances differ from Fig. 3.2. ($R_G' = 2R_G$, *and* $R_L' = 1/2R_L$)

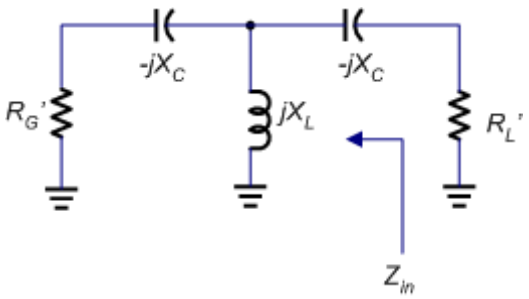


Fig. 3.3

To derive formulas for determining L and C value, let $X_L = X_C$ and the input impedance Z_{in} , seen at port 3 toward the port 1, equals R_L'

and

$$Z_{in} = (R_G' - jX_C) // jX_L - jX_C$$
$$= \frac{X_L X_C}{R_G'} = R_L' \qquad (3.2)$$

Thus $$X_L = \sqrt{R_G' \cdot R_L'} = \sqrt{R_G \cdot R_L} \qquad (3.3)$$

The balun is designed for the band around 5.5GHz. The frequency response of LC-balun is illustrated in Fig. 3.4, indicating that the phase error between port 2 and port 3 is less than 1.5^o and the amplitude mismatch is less than 0.5 dB.

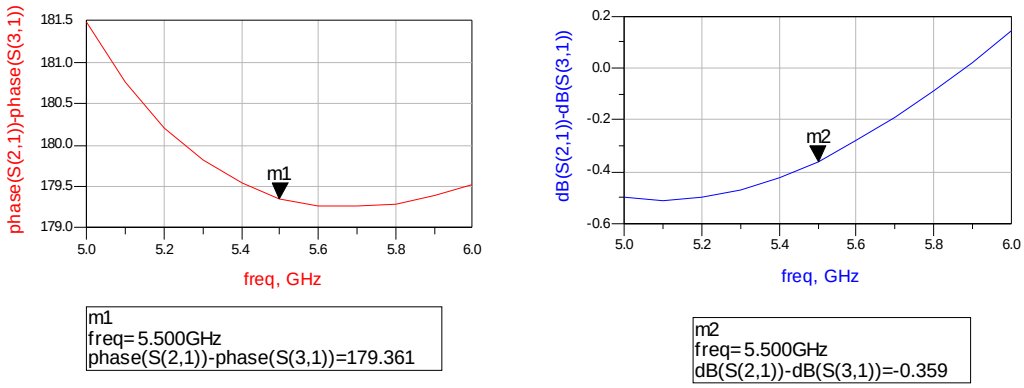


Fig 3.4 Frequency response of LC- balun

3.4 Quadrature generation design

Quadrature signals can be generated from a local oscillator in several different ways. The most common is the RC-CR network as shown in Fig. 3.5 [2].

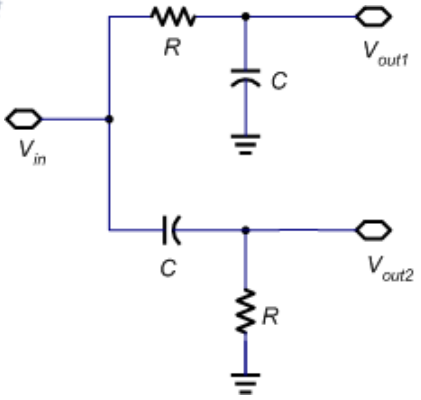


Fig.3.5 RC-CR network

Consider a sinusoidal with frequency ω applied at the input V_{in} , the outputs V_{out1} and V_{out2} is

$$V_{out1} = V_{in} * \frac{1}{1 + j\omega RC} \tag{3.4}$$

$$V_{out2} = V_{in} * \frac{j\omega RC}{1 + j\omega RC} \tag{3.5}$$

and hence

$$\begin{aligned} & Ang(V_{out2} - V_{out1}) \\ &= \frac{\pi}{2} - \tan^{-1}(\omega RC) + \tan^{-1}(\omega RC) \\ &= \frac{\pi}{2} \end{aligned} \tag{3.6}$$

Thus, V_{out1} and V_{out2} have 90^o phase difference at all frequencies, but the output amplitudes are equal only at $\omega = 1/(RC)$. Usually, it is difficult to achieve the accurate value of on-chip passive components and therefore amplitude mismatches arise. The amplitude mismatch, which is sensitive to variations in RC value, can be suppressed by limiting amplifiers.

Note that capacitive paths between the two outputs introduce phase error, demanding careful layout. Amplitude mismatches between the load capacitance also contribute to phase error.

Another issue in the circuit of Fig. 3.5 is the harmonic component of V_{in} . Suppose $V_{in} = A_1 \cos \omega t + A_n \cos n\omega t$, and therefore

$$\begin{aligned} V_{out1} = & \frac{A_1}{\sqrt{R^2C^2\omega^2 + 1}} \cos\left[\omega t - \tan^{-1}(RC\omega)\right] + \\ & \frac{A_2}{\sqrt{4R^2C^2\omega^2 + 1}} \cos\left[2\omega t - \tan^{-1}(2RC\omega)\right] \end{aligned} \tag{3.7}$$

$$\begin{aligned} V_{out2} = & \frac{A_1 RC\omega}{\sqrt{R^2C^2\omega^2 + 1}} \cos\left[\omega t - \tan^{-1}(RC\omega) + \frac{\pi}{2}\right] + \\ & \frac{2A_2 RC\omega}{\sqrt{4R^2C^2\omega^2 + 1}} \cos\left[2\omega t - \tan^{-1}(2RC\omega) + \frac{\pi}{2}\right] \end{aligned} \tag{3.8}$$

For a nominal value of $RC = \omega^{-1}$, we have

$$V_{out1} = \frac{A_1}{\sqrt{2}}\cos(\omega t - \frac{\pi}{4}) + \frac{A_2}{\sqrt{5}}\cos(2\omega t - \tan^{-1} 2) \quad (3.9)$$

$$V_{out1} = \frac{A_1}{\sqrt{2}}\cos(\omega t + \frac{\pi}{4}) + \frac{A_2}{\sqrt{5}}\cos(2\omega t - \tan^{-1} 2 + \frac{\pi}{2}) \quad (3.10)$$

The result indicates that it has a phase imbalance between V_{out1} and V_{out2}. Moreover, the magnitude of the harmonics also experiences unequal gains through the two paths, introducing amplitude mismatches at the output. If the LO harmonics are significant, the RC-CR network must be preceded by a lowpass filter.

The simulation results of RC-CR network are shown in Fig. 3.6, showing that the phase error is less than 0.5^{o} and the mismatch is less than 1 dB between 5 and 6GHz.

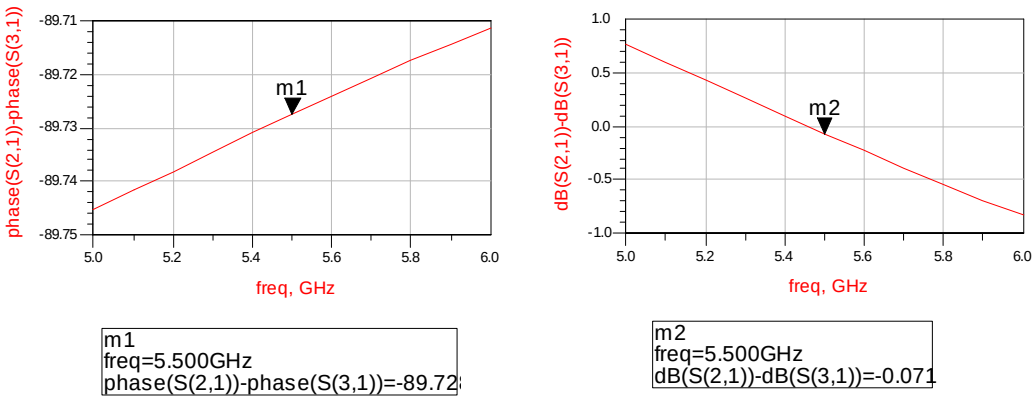


Fig. 3.6 Phase difference and amplitude mismatch

3.5 Mixer design

Mixers perform frequency translation by multiplying two signals (and their harmonics). Up-conversion mixers employed in the transmit path have two distinctly inputs, called the base-band (BB) port and the local oscillator (LO) port. Several up-conversion mixer topologies that can be realized in CMOS IC processes are presented. Since balanced mixer designs are more desirable due to its lower spurious outputs, higher common-mode noise rejection and higher port-port isolation, only balanced type mixer are discussed in this section[14].

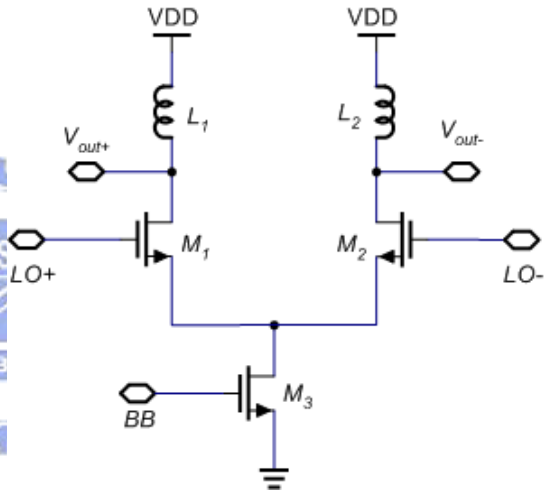


Fig 3.7 Single-balanced mixer

The single-balanced mixer shown in Fig. 3.7 is the simplest approach that can be implemented in most IC processes. The single balance mixer offers a desired single-ended RF input and it does not require a balun at the input. However, the drawback of single-balance mixer has low 1db compression point, low port-to-port isolation, low IIP3 and high input impedance.

If higher noise figure can be tolerated such as transmitter, the micro-mixer in Fig. 3.8 offers the best IIP3 due to its third-order harmonic distortion cancellation

mechanism. With proper biasing, the input impedance can be set close to 50 ohms which eliminates external matching network. However, using this topology, it would be difficult to increase the gain or reduce the noise figure. It achieves reasonable port-to-port isolation and eliminates the balun by using a current mirror. Because having three transistors in stack, limits the maximum signal swing and result in a lower output 1-dB compression point.

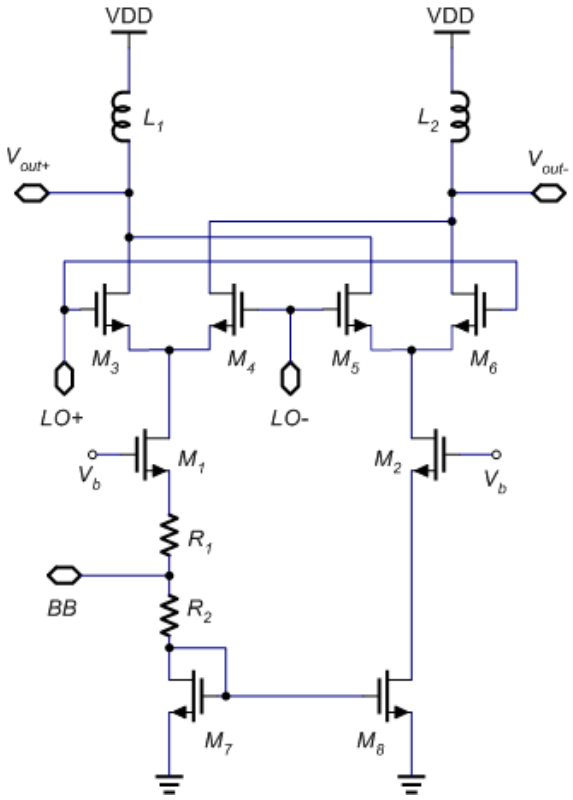


Fig.3.8 Micro-mixer

The Gilbert cell (double-balanced) mixer was invented in the 60's, but it still remains to be the most popular mixer circuit. A basic mixer circuit is shown in Fig. 3.9. Baseband (BB) signal is applied to the lower terminals of the stack, and LO

signal is connected to the upper ones. Thus RF signal is obtained as an output. It can prove high conversion gain and high port-to-to isolation. The linearity is reasonably good. Typically, the RF filter preceding this mixer is single-ended so a balun is needed to convert the single-ended signal to differential signal. However, balun having low insertion loss is very difficult to implement in IC processes.

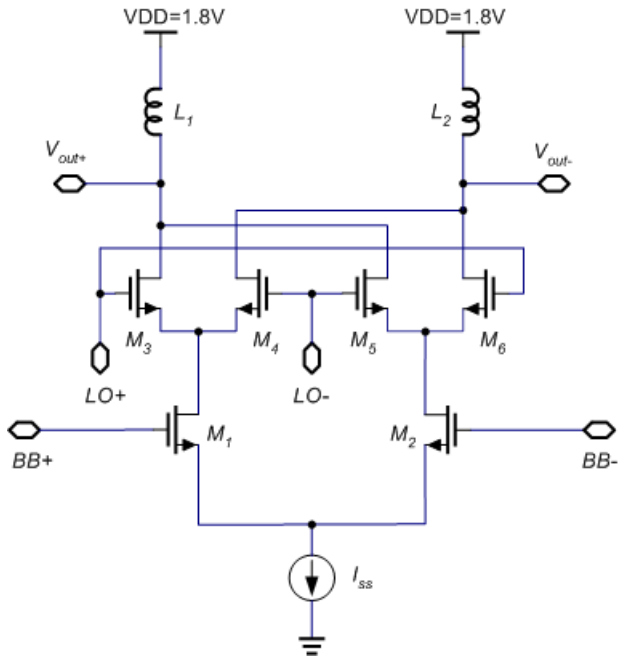


Fig. 3.9 Gilbert cell mixer

The distortion in RF signal is dominated by the lower BB differential pair rather than the upper LO differential pairs. This is because the BB signal is not a single tone signal [13]. Thus, harmonic distortions in the lower differential pair will cause intermodulation distortion, and these intermodulated components may appear at the same frequency of a wanted channel. This intermodulation distortion can be suppressed by improving the linearity of the mixer itself. Hence linearity is

an important parameter for the evaluation of a mixer performance, and it is usually indicated by 1 dB compression point and third-order intercept pointer (IP3).

The lower differential pair, called source coupled differential pair, is redrawn in Fig. 3.10. The general relationship between the input signal V_d and the output current I_d of the circuit is described as follows [3][13]

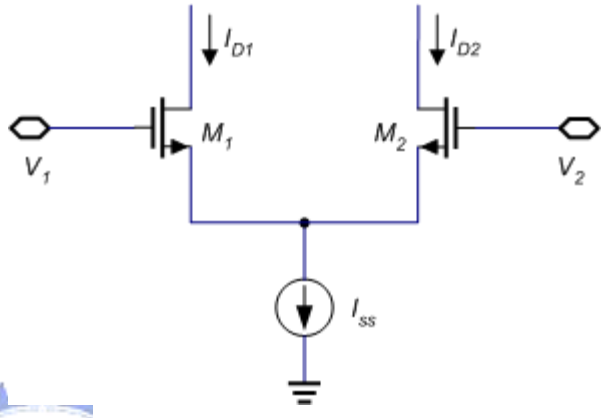


Fig 3.10 Source coupled

$$
\begin{aligned}
I_d &= I_{D1} - I_{D2} \\
&= \frac{1}{2}\beta V_d \sqrt{\frac{4I_{SS}}{\beta} - V_d^{\,2}} \\
&= 2V_d \sqrt{\frac{\beta I_{SS}}{4}} \left(1 - \frac{\beta V_d^{\,2}}{4I_{SS}}\right)^{0.5} \\
&= 2\sqrt{\frac{\beta I_{SS}}{4}} \left[V_d - \frac{1}{2}\left(\frac{\beta}{4I_{SS}}\right) V_d^{\,3} - \frac{1}{8}\left(\frac{\beta}{4I_{SS}}\right)^2 V_d^{\,5} - \frac{1}{16}\left(\frac{\beta}{4I_{SS}}\right)^3 V_d^{\,7} - \ldots \right]
\end{aligned}
\tag{3.11}
$$

where $V_d = V_1 - V_2$, $\beta = \mu_n C_{ox} \frac{W}{L}$

The first order term $(\beta I_{SS}/4)^{0.5} V_d$ in Eq. (3.11) is a desired component, which is called a fundamental in general. The rest higher order term (V_d^3, V_d^5, V_d^7, …), on the other hand , are distortion components that are not desirable and are often called harmonics. Eq. (3.11) reveals that the linearity of the source

coupled pair increases, if tail current source I_{SS} increases. Because the effect is slight, other linearization techniques have been developed.

A differential pair can be degenerated as shown in Figs 3.11 (a) and (b) [3]. In Fig. 3.11 (a), I_{SS} flows through the degeneration resistors, thereby consuming voltage headroom of $I_{SS}R_S$ / 2. The circuit of Fig. 3.11 (b), on the other hand, does not involve this issue but it suffers from a slightly higher noise and offset voltage because the two tail current sources introduce some differential error and noise.

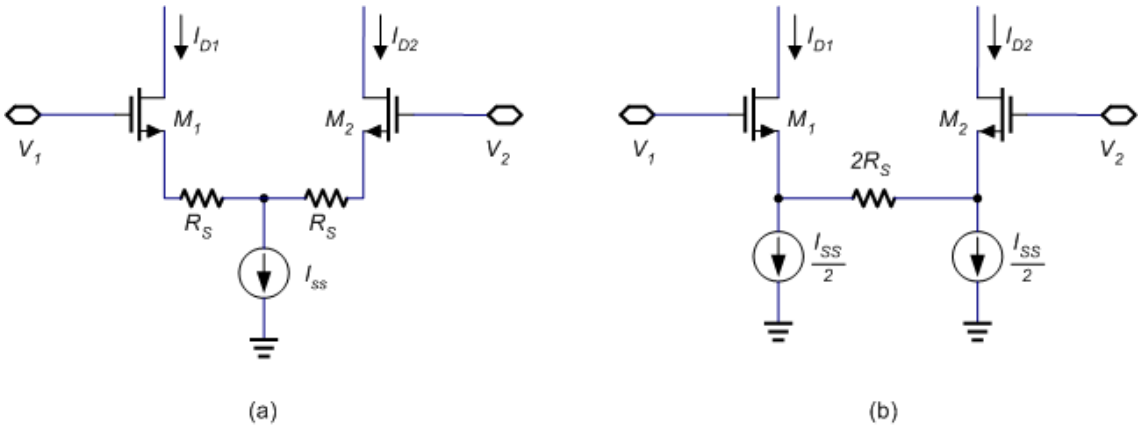


Fig. 3.11 Source degeneration applied to a differential pair

Resistive degeneration requires accuracy resistors, which is unavailable in today's IC technologies. As depicted in Fig.3.13, the resistor can be replaced by a NMOS operating in deep triode region. Recall the I-V relationship of the NMOS in triode region

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{3.12}$$

If in Eq. (3.12), $V_{DS} << 2(V_{GS} - V_{TH})$, the last term in Eq. (3.12) can be neglected and equivalent R_{ON} is obtained.

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)} \tag{3.13}$$

However, for large input swings, M_3 may experience substantial change in its on-resistance. The circuit of Fig. 3.13(a) can be further modified as Fig. 3.13(b). As the gate voltage of M_1 becomes more positive than the gate voltage of M_2, transistor M_3 stays in the triode region because $V_{D3} = V_{G3} - V_{G1}$ whereas M_4 eventually enter the saturation region because its drain voltage rises and its gate and source voltage fall. Thus, the circuit remains relatively linear even if one degeneration device goes into saturation.

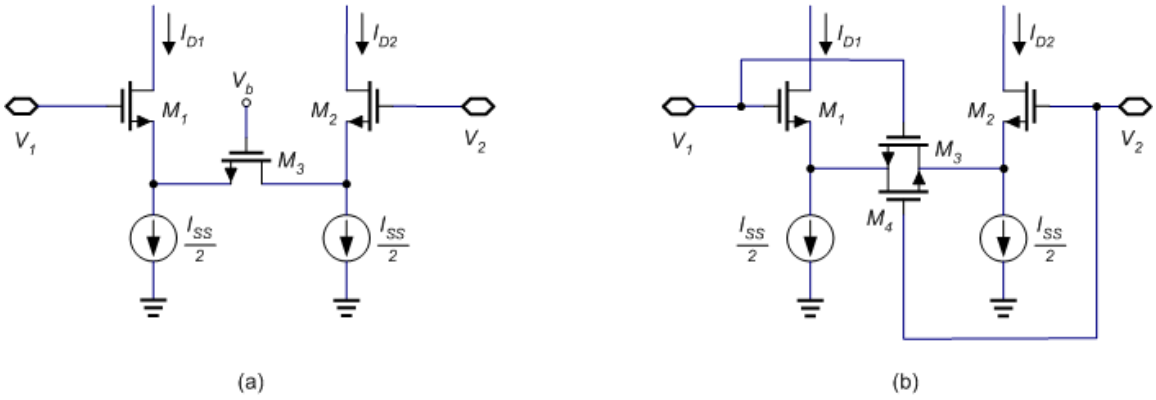


Fig. 3.12 Source degeneration with NMOS

The proposed mixer is illustrated in Fig. 3.13. Because quadrature modulation is required in modern digital communications, the mixer can be divided into two parts: in-phase and quadrature phase part. The in-phase and quadrature phase signal is combined by inductor load at output. The output of the mixer is chosen differential topology because it can eliminate even-order term harmonic distortion and have better common-mode rejection. The output of the mixer is ac-coupled and directly connected to the pre-amplifier input. The matching network of the inter-stage between mixer and preamplifier is not required because the impedances of mixer output and preamplifier input are close to conjugate match.

Fig. 3.14 and Fig. 3.15 show the performance of the proposed mixer. It achieves a -5.2dB conversion gain at 5.5GHz with 37.2 dB third-order harmonic rejection and the flatness is less than 0.5dB between 5 and 6 GHz. The proposed mixer dissipates 12.6mW which draws 7mA from 1.8V power supply.

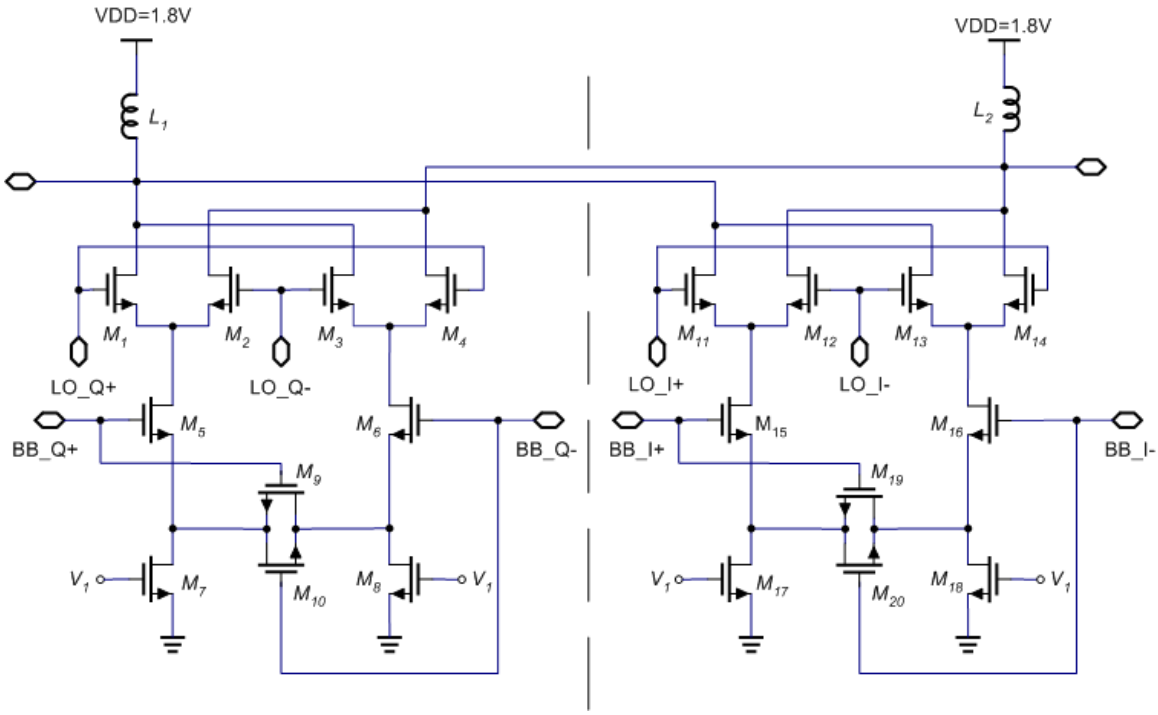


Fig. 3.13 The proposed mixer

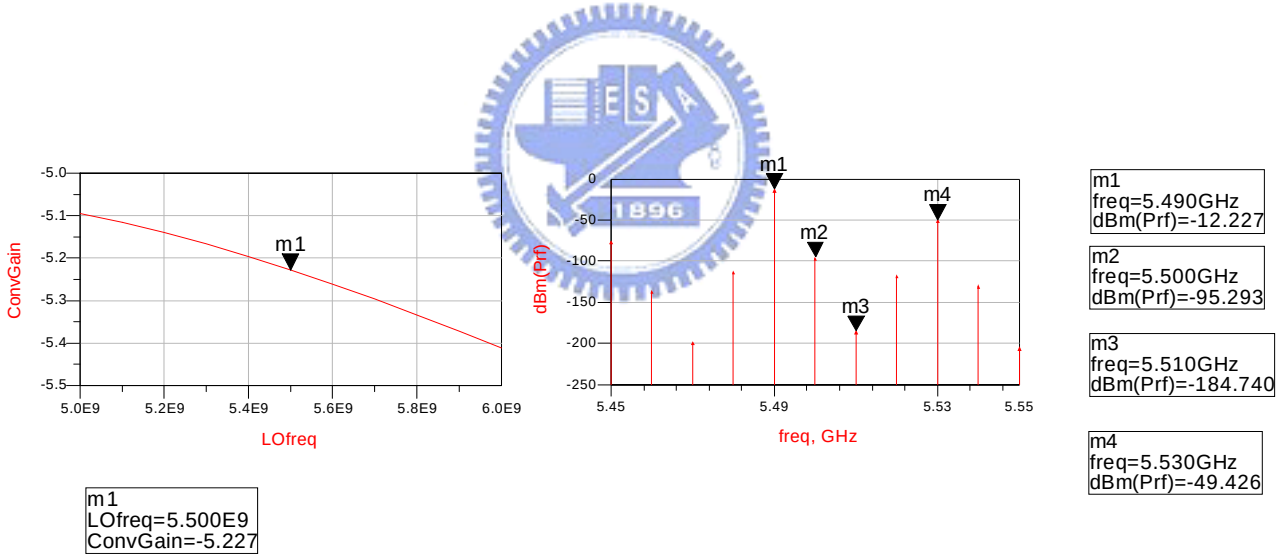


Fig 3.14 Frequency response

Fig 3.15 Harmonic

3.6 Pre-amplifier design

The pre-amplifier is used to boost the output power and to drive external high power amplifier. The proposed pre-amplifier, which consists of a three-stage differential amplifier, is shown in Fig. 3.23. For simplifying analysis, each stage will be discussed individually as follows.

3.6.1 First stage amplifier

The first stage amplifier is shown in Fig. 3.16. The circuit topology is full symmetric, so the half-circuit concept is used for simplifying analysis. Fig. 3.17 shows the equivalent half-circuit of Fig.3.16. It is called the cascode amplifier with single tuned load[5]. The cascode amplifier with tuned load provides selective amplification of wanted signals and a degree of degradation of unwanted signals. The use of inductor L_1 and L_4 not only increases the headroom but also cancels the parasitic drain-source and gate-source

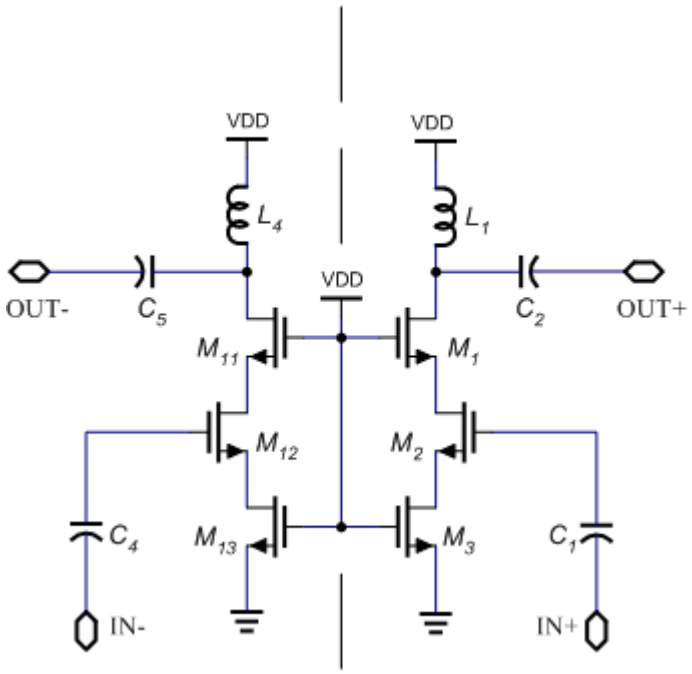


Fig. 3.16 The first stage amplifier

capacitance. We can resonate out this capacitance with an appropriate choice of inductance and obtain a maximum gain at arbitrary frequency ω_0. The cascode topology (M_1/M_2, M_{11}/M_{12}) eliminates the Miller effect and improves the amplifier reverse isolation. The NMOS M_3/M_{13} operate in deep triode region and its equivalent resistance R_{ON} is obtained by Eq.(3.13).

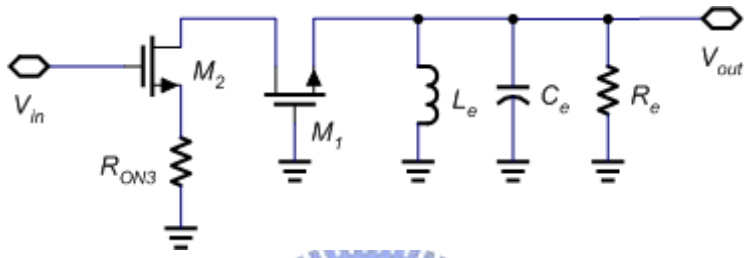


Fig 3.17 Equivalent half circuit of Fig. 3.16

For LC tank, the plot of magnitude function with frequency is shown in Fig. 3.18. The peak magnitude response occurs at the resonant frequency

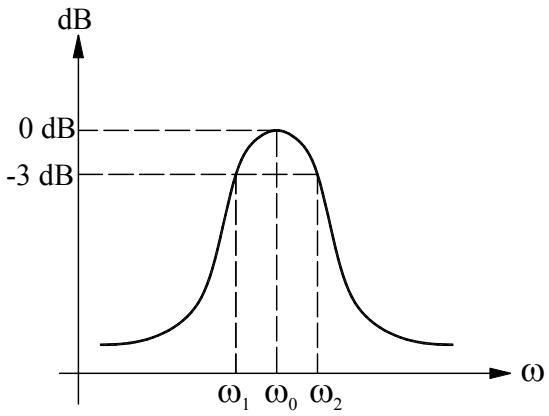


Fig. 3.18 Frequency response of LC tank

$$\omega_0 = \frac{1}{\sqrt{L_e C_e}} \tag{3.14}$$

where L_e is the parallel inductor, C_e is the parasitic capacitance. The -3dB bandwidth is

$$\omega_b = \omega_2 - \omega_1 = \frac{1}{C_e R_e} \tag{3.15}$$

where R_e is the parallel resistance in LC tank. Assuming $R_{ON3} << R_e$,

we obtain [3]

$$A_v \approx (g_{m1} + g_{mb1}) g_{m2} r_{o2} (r_{o1} // R_e) \quad \text{at } \omega_0 \tag{3.16}$$

It must be noted that Eq.(3.16) is certainly true only at low frequencies. At RF/microwave frequencies, the scattering (S) parameters, which are related to incident and reflected power, are more suitable to describe the two-port network.

This simplified schematic of a single stage amplifier is shown in Fig. 3.19. We can define the transducer power gain G_T, which quantifiers the gain of the amplifier placed between source and load [4].

$$\begin{aligned} G_T &= \frac{\text{Power delivered to the load}}{\text{Available power from the source}} = \frac{P_L}{P_A} \\ &= \frac{\left(1 - |\Gamma_L|^2\right)|S_{21}|^2 \left(1 - |\Gamma_S|^2\right)}{\left|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_S\Gamma_L\right|^2} \end{aligned} \tag{3.17}$$

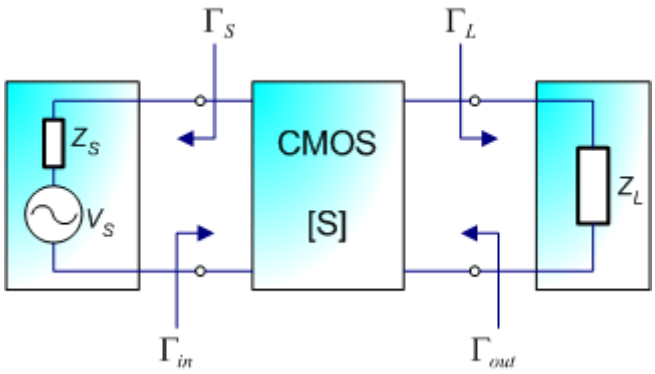


Fig. 3.19 Simplified schematic of a single stage amplifier

For amplifier designer, how to decide the reflection coefficients is an important issue. As examples, in a design requiring maximum transducer power gain, the reflection coefficients are selected as follows [7]

$$\begin{aligned} &\Gamma_S = \Gamma_{MS}^{*} \quad , \quad \Gamma_L = \Gamma_{ML}^{*} \qquad \text{for bilateral design } (S_{12} \neq 0) \\ &\Gamma_S = S_{11}^{*} \quad , \quad \Gamma_L = S_{22}^{*} \qquad \text{for unilateral design } (S_{12} = 0) \end{aligned} \tag{3.18}$$

where Γ_{MS}, Γ_{ML} are called simultaneous conjugate match.

$$\begin{aligned} &\Gamma_{MS} = \frac{B_1 \pm \sqrt{B_1^{\,2} - 4|C_1|}}{2C_1}, \quad \Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^{\,2} - 4|C_2|}}{2C_2} \\ &B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 , \quad B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \\ &C_1 = S_{11} - \Delta S_{22}^{*} , \quad C_2 = S_{22} - \Delta S_{11}^{*} , \quad \Delta = S_{11}S_{22} - S_{12}S_{21} \end{aligned} \tag{3.19}$$

In a high power amplifier design, the reflection coefficients are selected as follows

$$\Gamma_L = \Gamma_{OP} \tag{3.20}$$

where Γ_{OP} is the load reflection coefficients of maximum power.

In a low-noise design, the reflection coefficients are selected as follows

$$\Gamma_S = \Gamma_{opt} \tag{3.21}$$

where Γ_{opt} is the optimum noise reflection coefficients.

In a wideband amplifier design, it is usually necessary to reduce the gain-bandwidth constrains associated with the impedance to be matched by using resistive feedback or by loading the device with shut or series resistance [4][6]. To

design a wideband amplifier, two different design approaches are used: frequency compensated matching network and negative feedback. Frequency compensated matching network introduce an impedance mismatch to compensate for the frequency variation. Negative feedback allows a flat gain response and reduces the input and output VSWR over a wide frequency range. In our design, we sacrifice the impedance matching to get wider bandwidth. We also utilize negative feedback approach, for example, M_3 / M_{13} contributes a series feedback.

3.6.2 Second stage amplifier

The second stage amplifier, shown in Fig. 3.20, shares the same circuit topology as the first stage amplifier but remove two cascade NMOS. It can allow higher signal swing. As mentioned above, the circuit analysis is similar to the first stage amplifier.

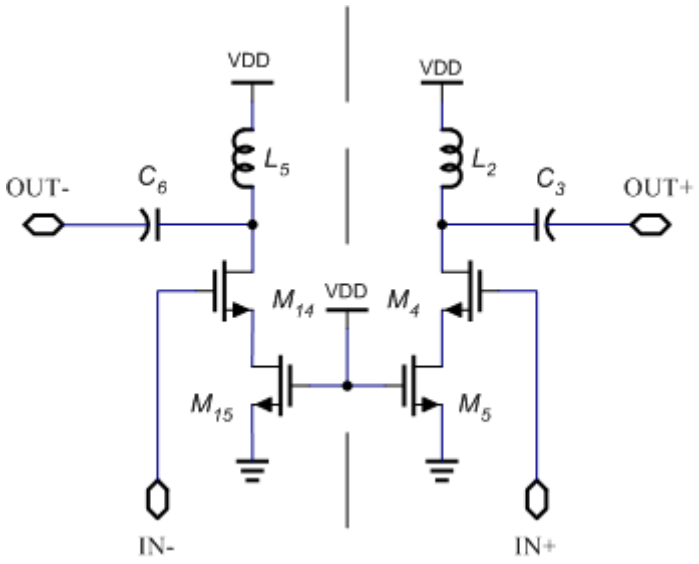


Fig 3.20 The second stage amplifier

3.6.3 Last stage amplifier

The last stage amplifier, serve as a power amplifier, is illustrated in Fig. 3.21. In order to increase the amplifier efficiency, the last stage operates in Class AB mode whose conduction angle is less than 180^{o}. This circuit, is called a push-pull amplifier, consists of four NMOS devices (M_6/M_7, M_{16}/M_{17}) to share the load current. The inductors (L_3/L_6) play the role of a RF choke providing DC biasing. The trace width of inductors must be wide enough to support large current density. Fig. 3.21 puts a balun transformer together and redraws the circuit as shown in Fig. 3.22.

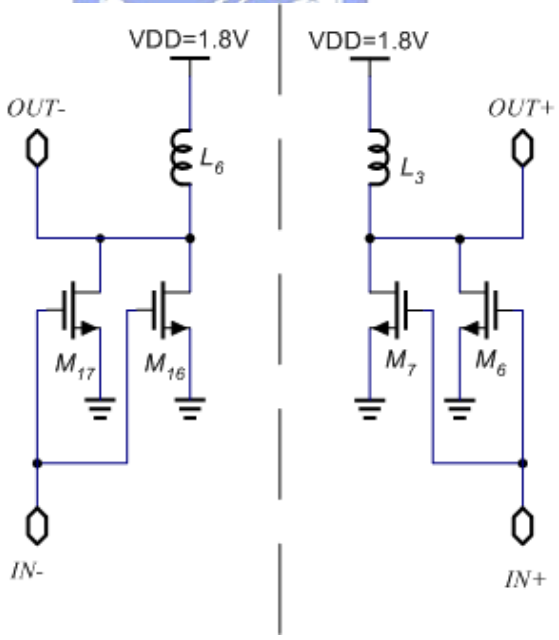


Fig.3.21 The last stage amplifier

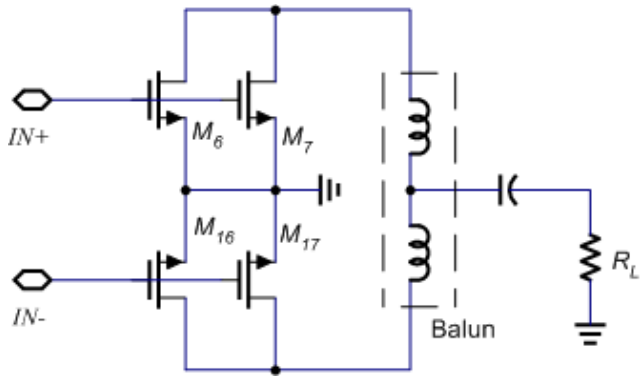


Fig. 3.22 Equivalent circuit of Fig. 3.21

The theoretical efficiency for true Class B operation with sinusoidal signals is 78.5%, which is greater than the 50% theoretical maximum obtainable with Class A operation. Although efficiencies near the theoretical limits are obtainable at low frequencies, it is difficult to achieve more than 50% efficiency at microwave frequencies. There are few Class B amplifiers in the microwave region proposed. This was due the fact that when an MOSFET is biased near pinch-off region, its gain is substantially less than when it is operated at maximum gain point. The efficiency and linearity of Class AB amplifier are intermediate between those of a Class A and Class B amplifiers.

3.6.4 Proposed pre-amplifier

The proposed pre-amplifier employs a fully differential three-stage amplifier as shown in Fig. 3.23. The fully differential topology has several advantages as follows: lower substrate noise and sensitivity, doubled signal swing, and linearization of transfer function (elimination the even harmonics). The cost will be higher power consumption. A three-stage amplifier offers sufficient gain and large bandwidth.

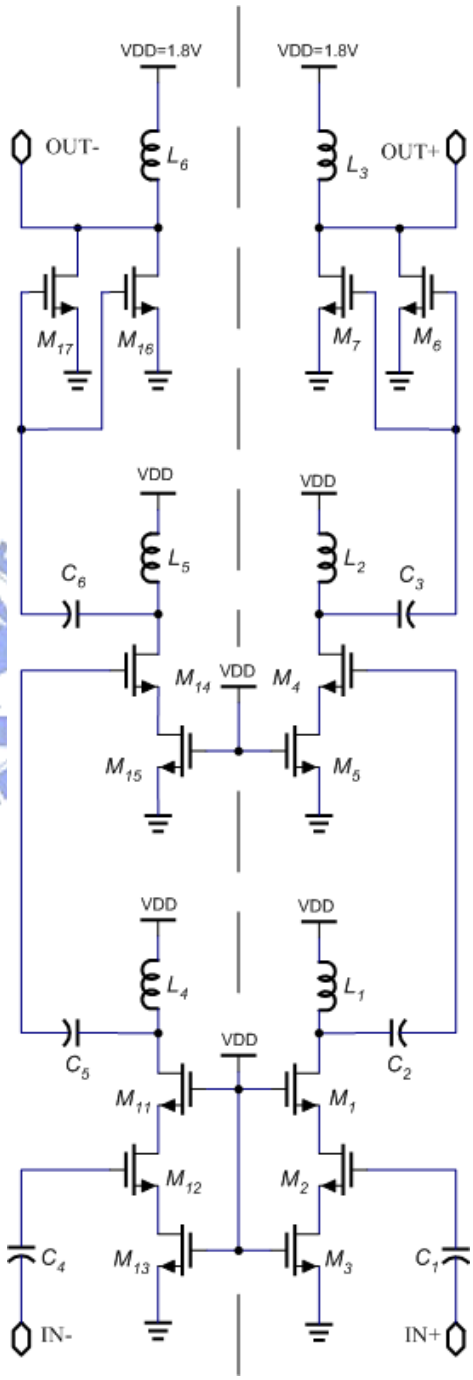


Fig. 3.23 The proposed pre-amplifier

Fig 3.24 demonstrates the frequency response of the proposed pre-amplifier. It achieves 20 dB transducer power gain at 5.5 GHz. Notice that the transducer power gain in upper bands is designed higher to compensate the frequency variation of a up-conversion mixer.

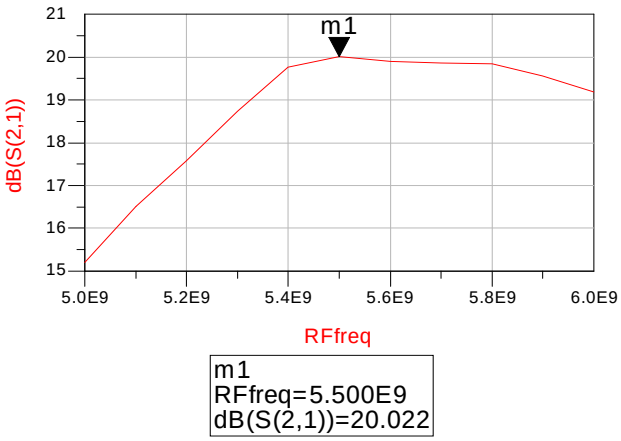


Fig 3.24 Frequency response of the proposed pre-amplifier

3.7 Simulation results

The simulation results of the entire transmitter front-end are shown in this section. Fig.3.25 exhibits the harmonics of in-band spectrum at 5.5GHz. This diagram tells us that sideband rejection is 38.7dB, carrier rejection is 33.4dB and three-order harmonic rejection is 36.9dB. Fig.3.26 and Fig. 3.27 show the in-band spectrum at 5GHz and 6GHz respectively. The harmonics of out-of-band spectrum are shown in Fig 3.28. Indicating that it achieves 23.2dB out-band rejection.

Fig. 3.29 and 3.30 illustrates the frequency response of the conversion gain and the output power, respectively. As the figure indicates, the conversion gain equals 13.8 dB at 5.5GHz, and the flatness is less than 3 dB over the entire band. Fig. 3.31 and 3.32 shows the output P1dB, IIP3 and OIP3 which are 10.5dBm, 5dBm and 15dBm, respectively. The entire transmitter front-end dissipates 54mW

which draws 30mA from 1.8V power supply.

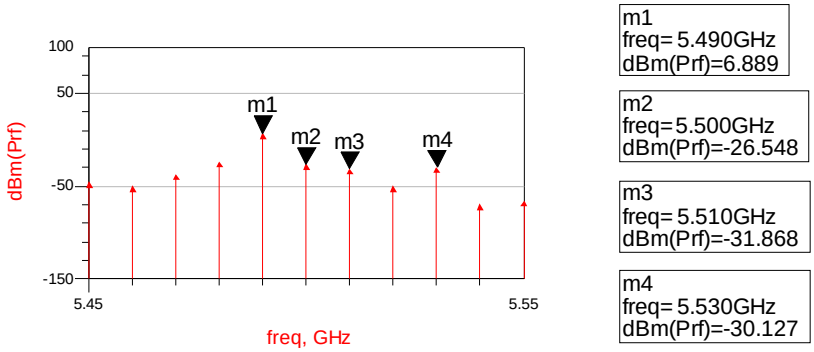


Fig. 3.25 Harmonics of in-band spectrum at 5.5GHz

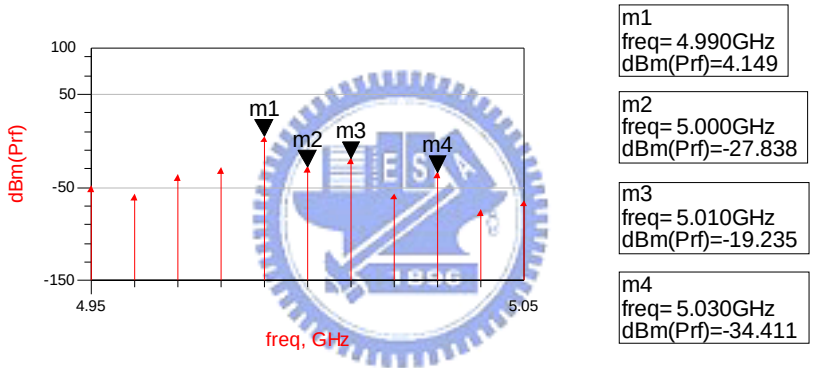


Fig. 3.26 Harmonics of in-band spectrum at 5GHz

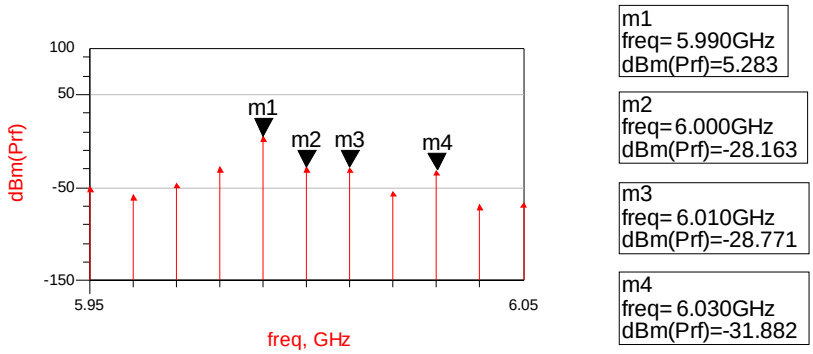


Fig. 3.27 Harmonics of in-band spectrum at 6GHz

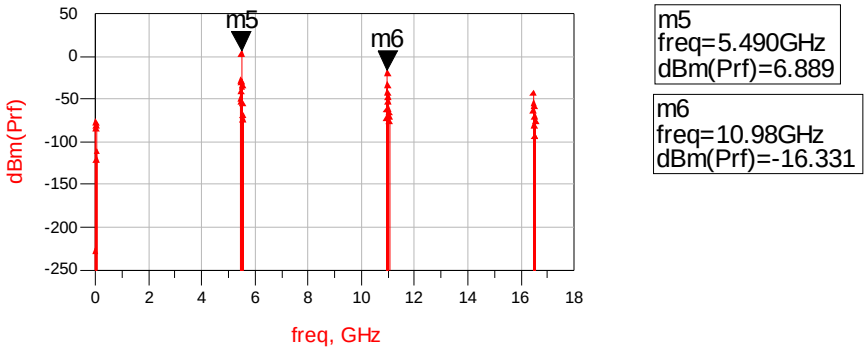


Fig. 3.28 Harmonics of out-band spectrum

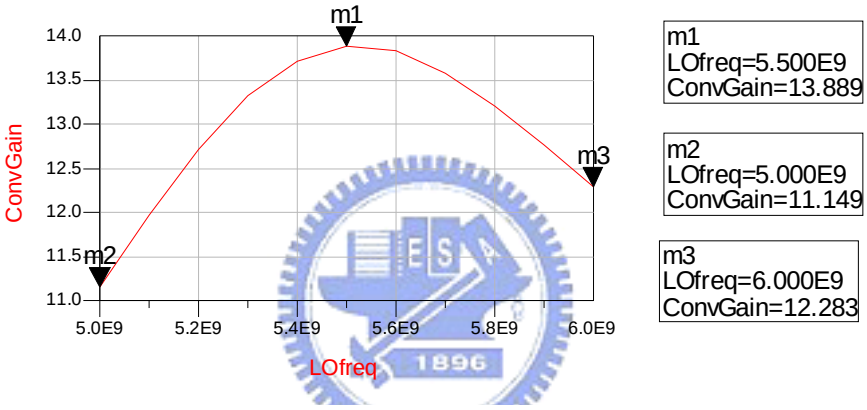


Fig 3.29 Frequency response of the conversion gain

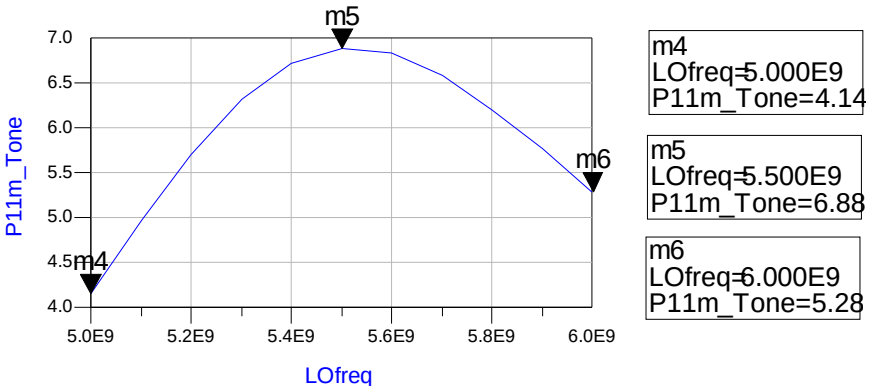


Fig 3.30 Frequency response of the output power

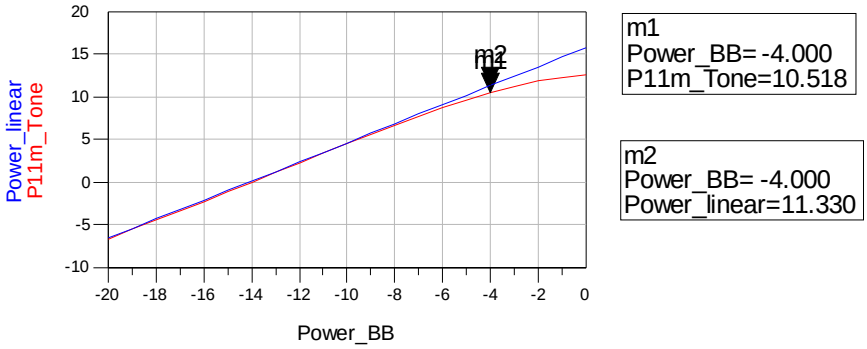


Fig 3.31 Ouput-1dB compression point

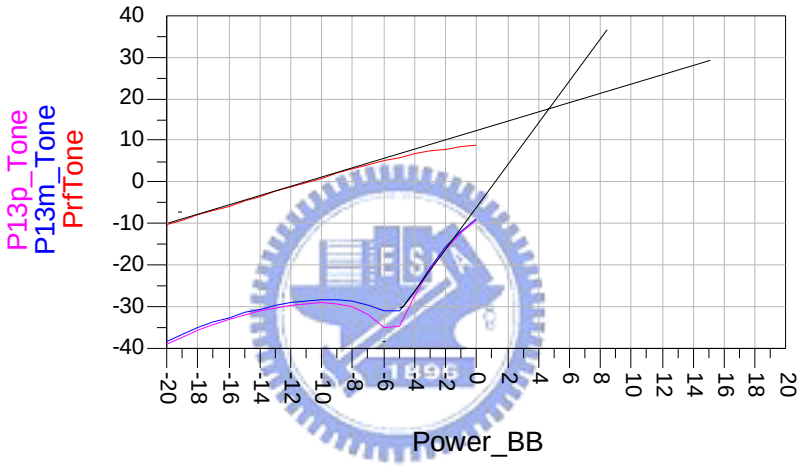


Fig 3.32 Input IP3 and Output IP3 point

3.8 Other applications

In this section, we utilize the same architecture of the transmitter, but change and optimize the component values for dual band and ultra-wide band applications.

3.8.1 Dual band (2.4GHz)

Fig.3.33 exhibits the harmonic of in-band spectrum at 2.45GHz. The sideband rejection is 7.8dB, carrier rejection is 38.7dB, three-order harmonic rejection is 45.3dB and the conversion gain is 10.2dB. The harmonic of out-band spectrum is shown in Fig 3.34. It reaches an 8.6dB out-band rejection.

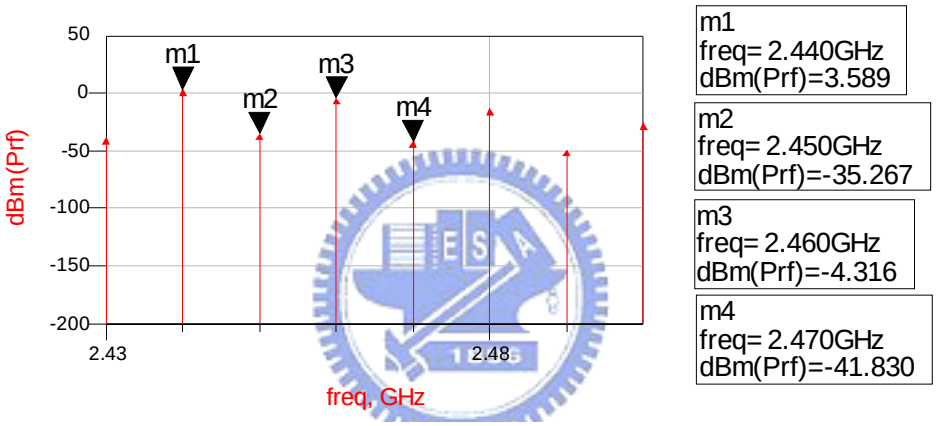


Fig 3.33 Harmonics of in-band spectrum at 2.45GHz

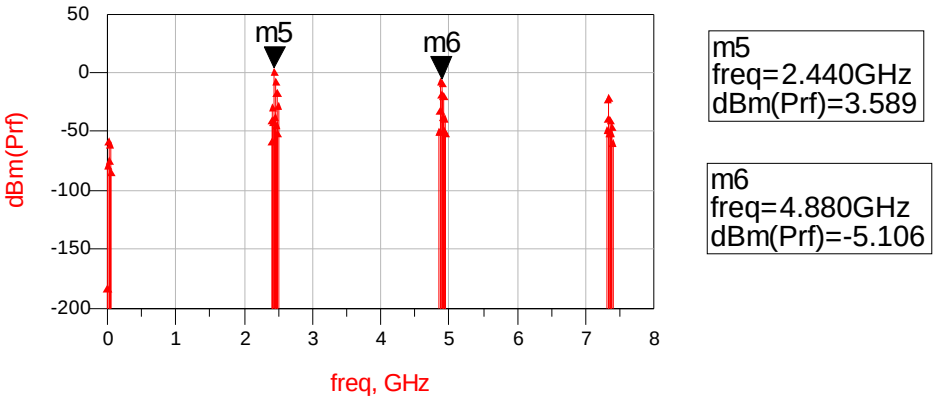


Fig 3.34 Harmonics of out-band spectrum

3.8.2 UWB Band (10GHz)

The harmonic of in-band spectrum at 9.5GHz is shown in Fig. 3.35. As the diagram indicates that sideband rejection is 37.2dB, carrier rejection is 30.7dB, three-order harmonic rejection is 35.7dB and the conversion gain is 6.1dB. Fig 3.36 shows the harmonic of out-band spectrum. It achieves a 32.9dB out-band rejection.

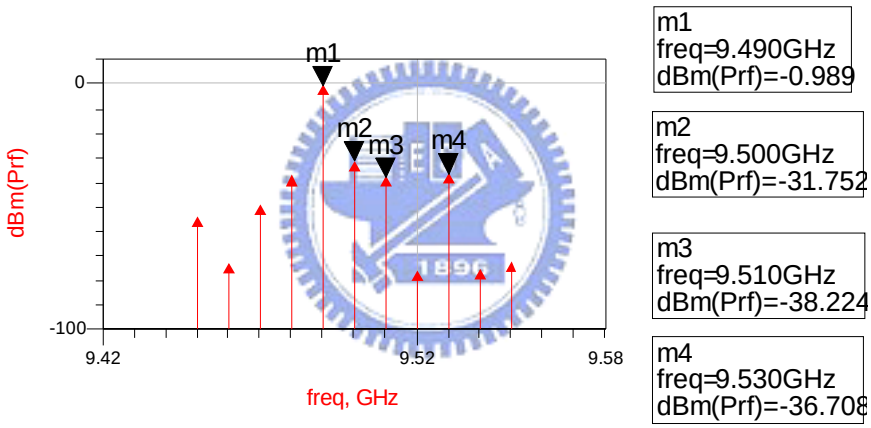


Fig 3.35 Harmonics of in-band spectrum

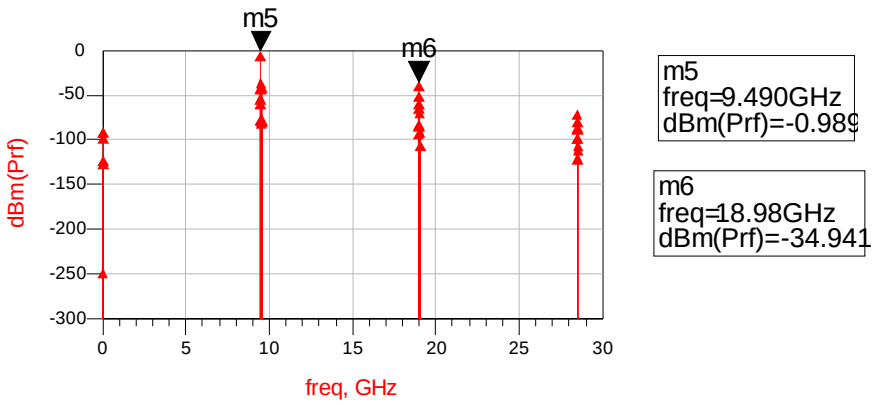


Fig 3.36 Harmonics of out-band spectrum

Chap 4.

Layout Considerations

4.1 Chip layout considerations

Someone said that making a layout is an art by itself. Some layouters claim that they have made a good layout when the layout-versus-schematic (LVS) check shows no error messages. This is a necessary, but not sufficient condition for a good RF layout. Poor layout causes the performance degradation of the circuits, or even result in wrong working. There are some design rules helping us to make a better layout, as follows.

First of all, in order to avoid the phenomenon of LO pulling, the RF output stage (PA) should be physically far away from the LO circuits. But it is difficult to do that in our chip. To minimize the effect, RF output stage and LO circuits are placed perpendicularly to each other. In IC processes, “guard rings” can also be employed to reduce the coupling.

Next, the fully differential topology is used in our design, the mismatch and symmetry should be concern. The common-centroid configuration is employed to

reduce device mismatch due to the effect of gradient. Moreover, the trace length of the connections for each stage must keep as equal as possible to minimize phase error.

Finally, how to determine the trace width of those connections is an important issue. For DC paths, it should be wide enough to support large current. For RF paths, the parasitic capacitor will be increased, if we increase the trace width. However, narrow trace raises parasitic inductor and the metal resistor. To solve this problem, we will introduce a transmission concept. For a lossless transmission line, the characteristic impedance is obtained as

$$Z_0 = \sqrt{\frac{L}{C}} \qquad (4.1)$$

where L is series inductance per unit length and C is shunt capacitance per unit length. Many CAD tools can provide the characteristic impedance of the planar transmission lines (e.g., coplanar waveguide, microstrip and stripline etc.). Our design employs a 50 Ω microstrip line, which characters are listed as follows: dielectric constant ε = 4.1 (SiO_2), the height is 2.1μm. Thus the width of a microstrip line can be obtained as 4 μm.

Consider the case of a bend in a microstrip line, is illustrated in Fig.4.1. The straightforward right-angle bend has a parasitic discontinuity capacitance. This effect could be minimized by mitering the corner. The optimum value of the miter

length a, depends on the characteristic impedance and the bend angle, but a value of $a = 1.8W$ is often used in practice. The chip layout is shown in Fig. 4.2, and the chip area occupied 2.5×2.5 mm^2.

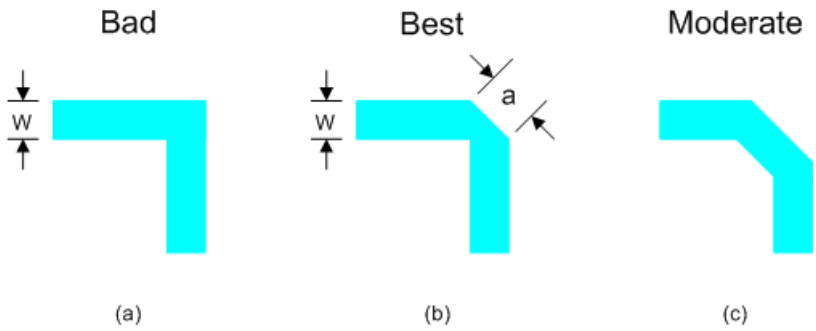


Fig. 4.1 Bend of a microstrip line

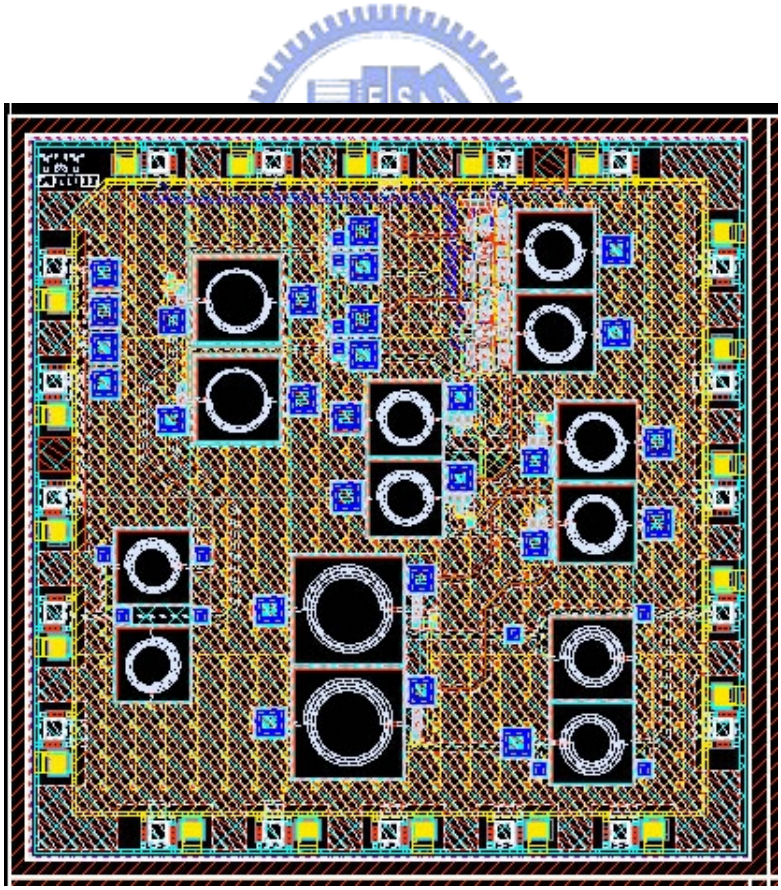


Fig. 4.2 Chip layout of the transmitter front-end

4.2 Package and ESD considerations

The 20-pin QFN package provided by SPIL is employed in our design as illustrated in Fig. 4.3. To prevent crosstalk due to adjacent pin coupling, the RF pins (LO and RF_out pin) are surrounded by ground wire, and the LO pins is allocated away from the RF_out pin. Fig 4.4 shows the simplified package model for each pin. Each pin exhibits a finite self-inductance which is about 1-nH. Multiple bond wires and pins are used to decrease the equivalent inductance and resistance on the V_{DD} and ground pins. A large on-chip capacitor, which is composed of four MIM capacitors in this chip, is used to stabilize the difference between V_{DD} and ground, and reduce the risk of inter-stage coupling.

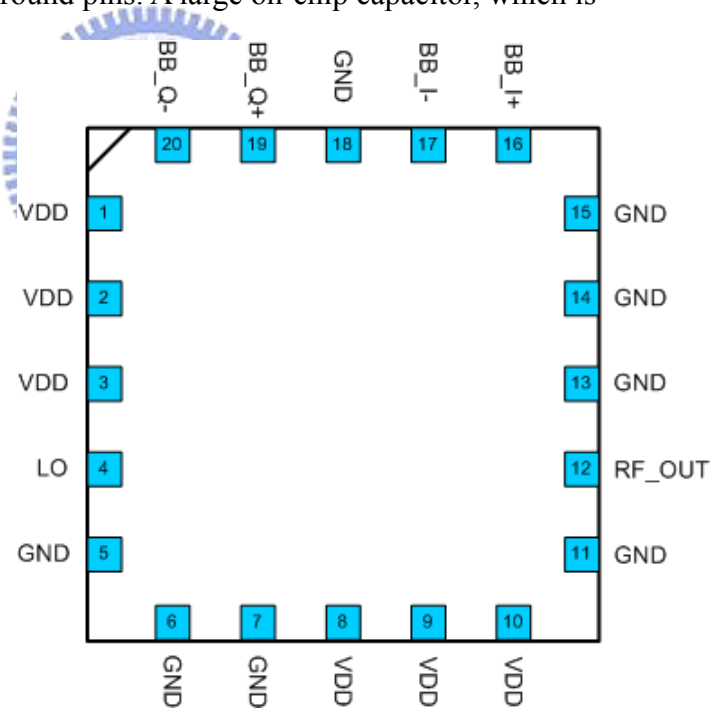


Fig. 4.3 Pin definition

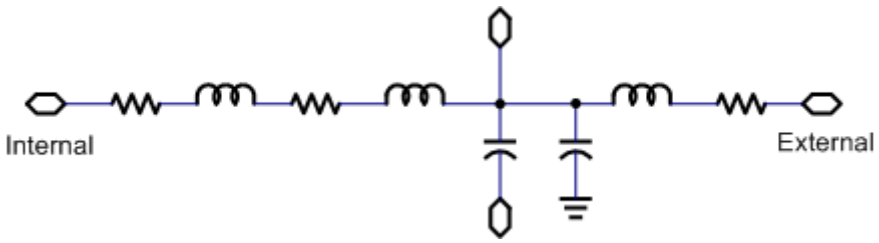


Fig. 4.4 Package model for each pin

Electrostatic discharge (ESD) may result in CMOS devices permanent damage without protection circuits. Fig. 4.5 shows the most popular ESD protection circuits in commercial using. The diode chains clamp the external discharge to ground or V_{DD}, and a large gate ground NMOS will break down once enormous potential across V_{DD} and ground. The ESD protection circuits provided by UMC ensure 3.6KV in human body mode (HBM) test but induce about 40fF capacitances in each pin. The ESD parasitic capacitances and the bond-wire inductors must be considered together during simulation.

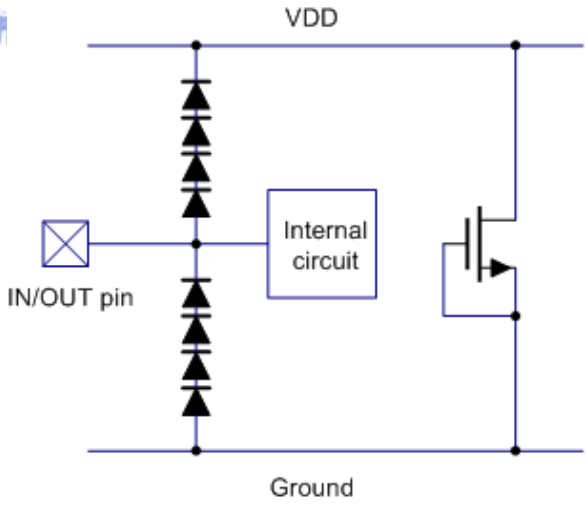


Fig. 4.5 ESD protection circuit

4.3 PCB layout considerations

The transmitter chip is mounted on the PCB board as shown in Fig. 4.6. The layer stack-up structure of a PCB is illustrated in Fig. 4.7. The loss tangent (δ= 0.0021) and dielectric constant stability for RO4003 material is superior to FR-4, so that RO4003 severs as the dielectric material (ε_r= 3.38) between layer 1 and layer 2. As mentioned above, the microstrip characteristic impedance could be obtained by CAD tools (APPCAD 3.0, Agilent), as shown in Fig. 4.8. We obtain the width of transmission line equals 17 mil. Layer 2 and layer 3 provide large and low impedance power planes. The area of the power planes near the chip look like a good, high frequency capacitor and help with decoupling.

The design rules of PCB layout are similar to the chip layout. The RF output port should be put away from the LO port. For differential paths, equal length and symmetric layout is essential. In order to reduce transmission loss, mitering corners on microstrip traces are formed and the microstrip length is as short as possible.

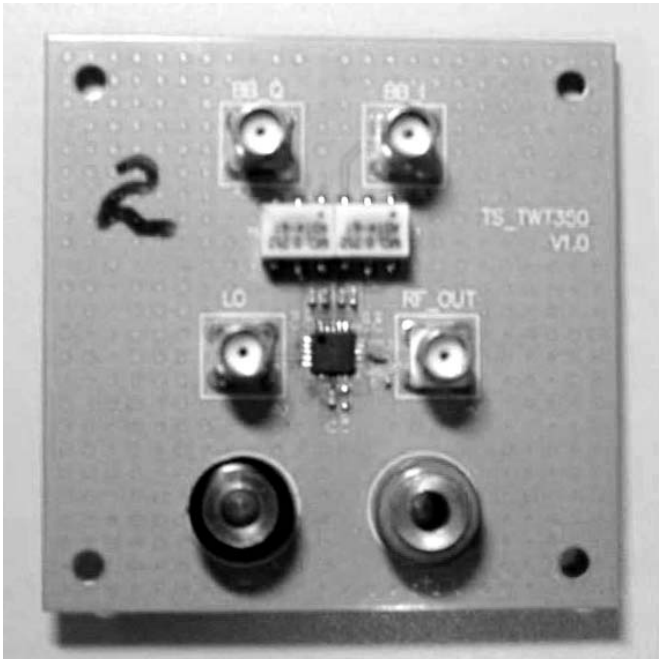


Fig. 4.6 PCB board

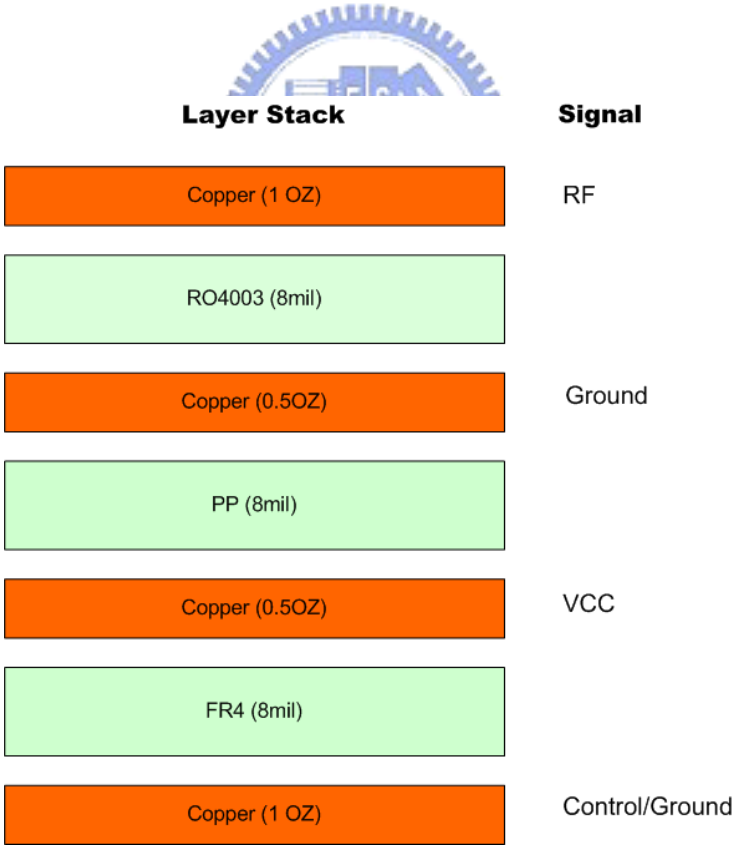


Fig. 4.7 Layer stack-up of PCB

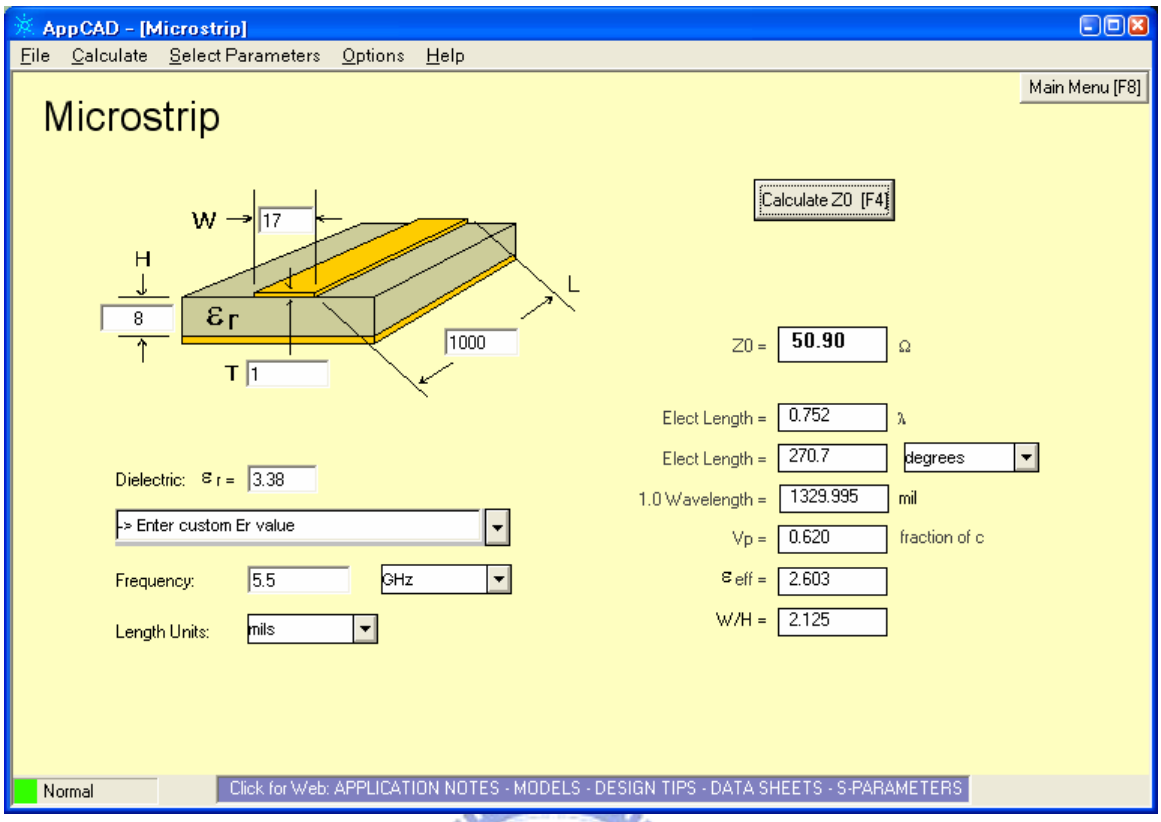


Fig. 4.8 Calculation of a microstrip characteristic impedance

Chap 5.

Measurement

Fig.5.1 shows the essential instruments which characters are listed as follows:

Spectrum analyzer (PSA, Agilent E4446A) 3Hz ~44GHz ×1

Signal generator (ESG, Agilent E4438C) 250K~6.0GHz ×2

Signal generator (ESG, Agilent E4432B) 250K~3.0GHz ×2

Power supply (Agilent E3610A) 0~8V 3A, 0~15V 2A ×1

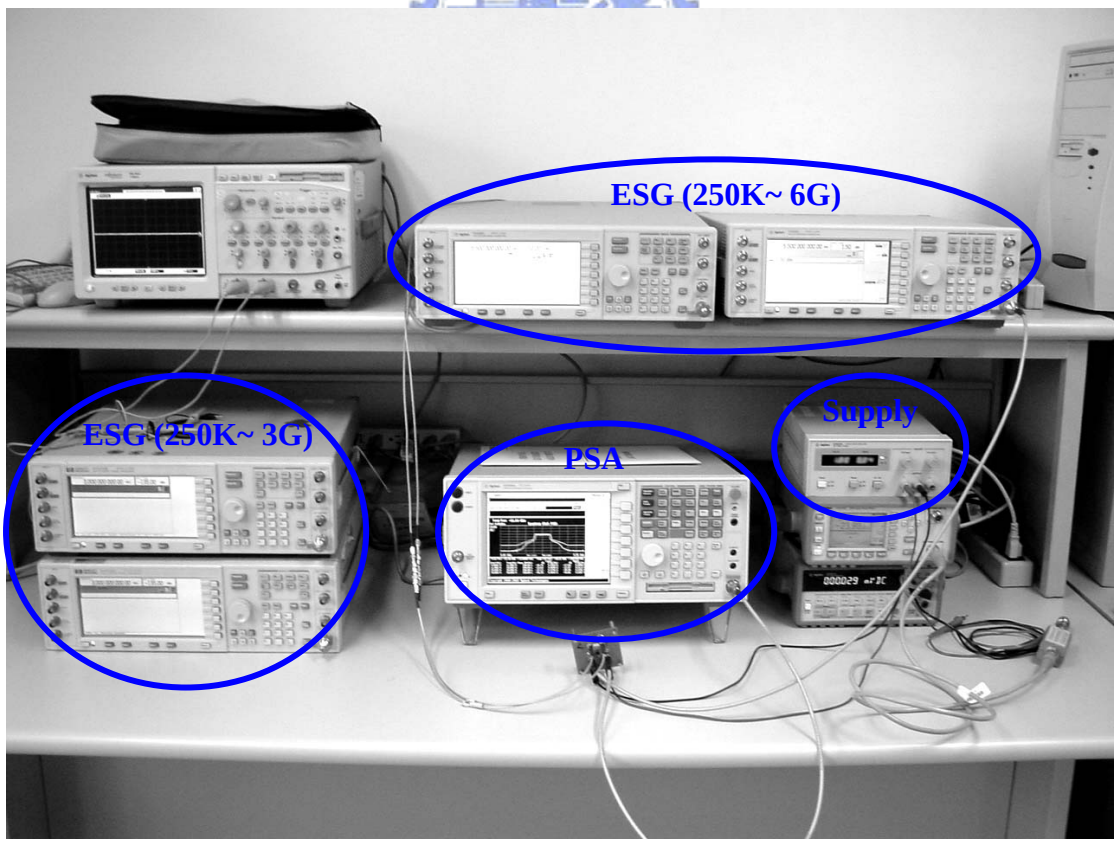


Fig. 5.1 Instrument overview

5.1 Harmonic test

5.1.1 Instrument setup

The equipments are connected as shown in the Fig. 5.2, and use the following procedure to set up those instruments for measuring the harmonics of the transmitter IC. Note that the 10MREF_OUT terminal of ESG1 must be connected to the 10MREF_IN of ESG2.

1. Set up the Spectrum analyzer parameters as follows: **Center frequency** = 5.5 GHz, **Span** = 100MHz, **Amplitude** = 10dBm, **RBW** = 300 KHz.
2. Set up the ESG1/ESG2 parameters: **Frequency** = 10MHz, **Level** = -7dBm.
3. Because the I and Q channel signals have 90^o phase difference, it is necessary to calibrate the phase before the measurement. Using the following steps (4~5) to do that.
4. Adjust the ESG2 **Phase** until the lower and upper sideband harmonics are equal, as shown in Fig. 5.3. Recode the phase θ_1.
5. Assign the ESG2 **Phase** $\theta_2=\theta_1-90^o$.
6. For the ESG3, set up the parameter as follows: **Frequency** = 5.5GHz, **Level** = 1.5dBm.

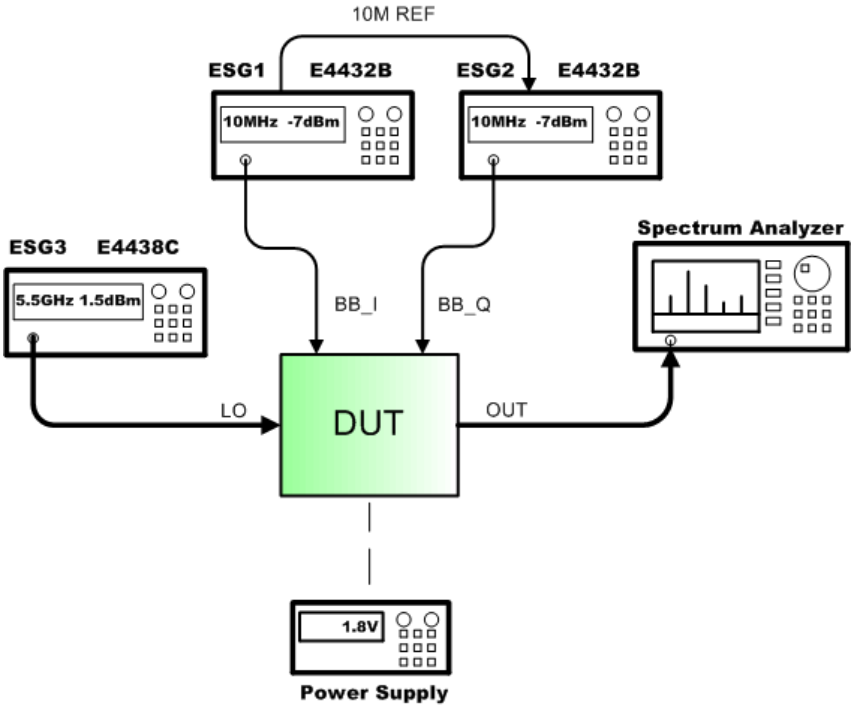


Fig. 5.2 Instrument configuration for harmonic test

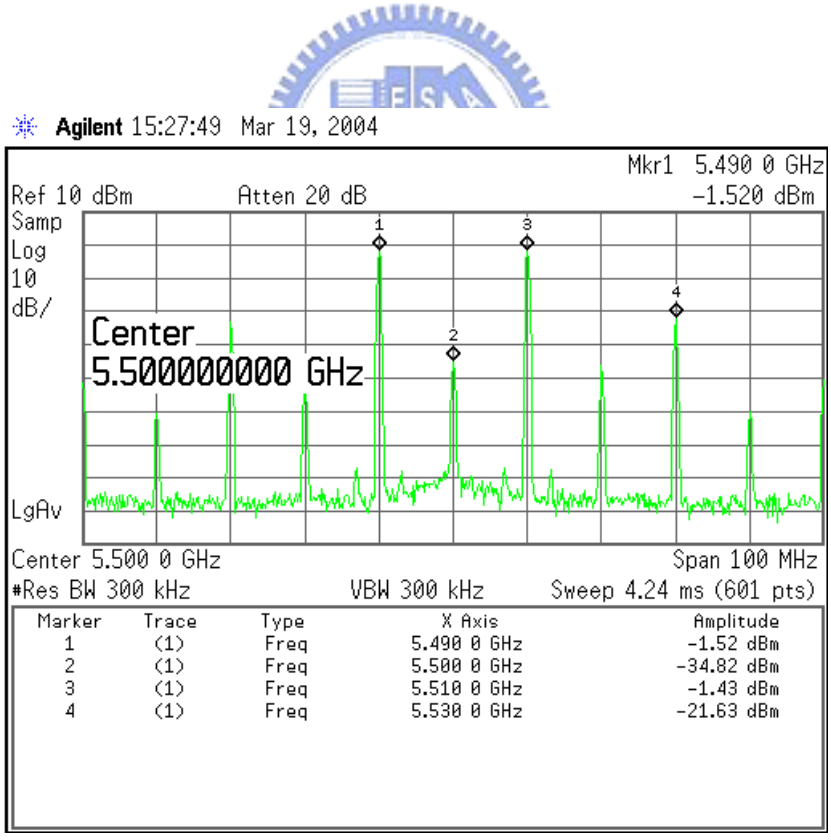


Fig. 5.3 Phase calibration

5.1.2 Results

Fig 5.4 exhausts the measured transmitter in-band spectrum when the 10MHz quadrature signals are applied to the input terminals of the BB_I and BBQ. Fig. 5.4 shows that it archives a sideband rejection of 34.3dB, a carrier rejection of 32.4dB and a third-order harmonic rejection of 31.1dB.

The out-of-band spectrum is illustrated in Fig.5.5, and it tells that the out-of-band rejection equal 51.8dB.

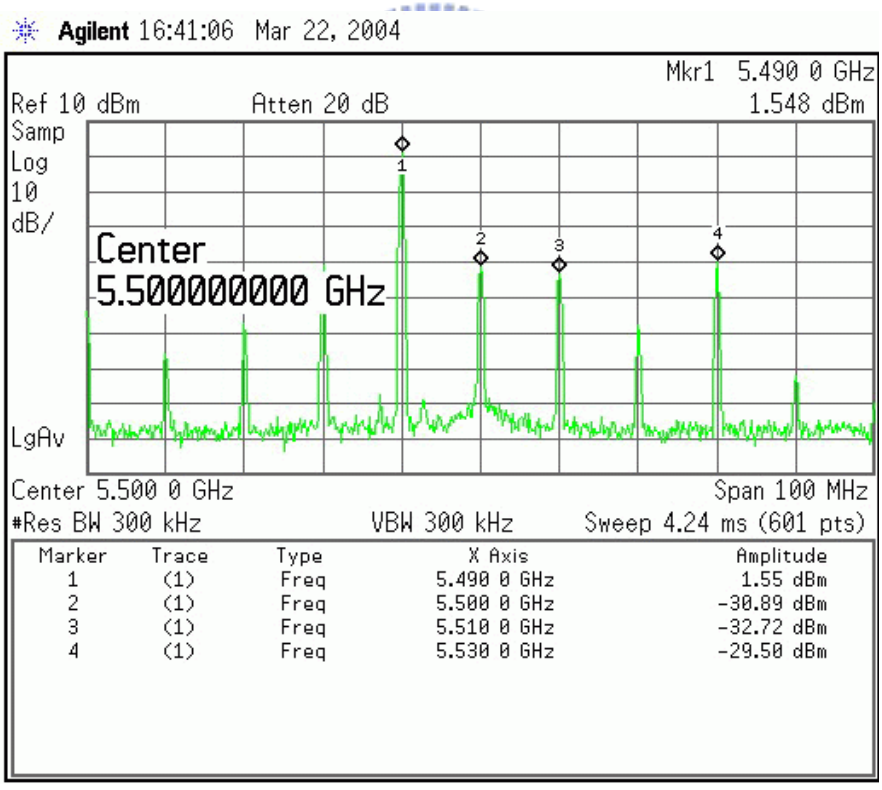


Fig. 5.4 In-band spectrum

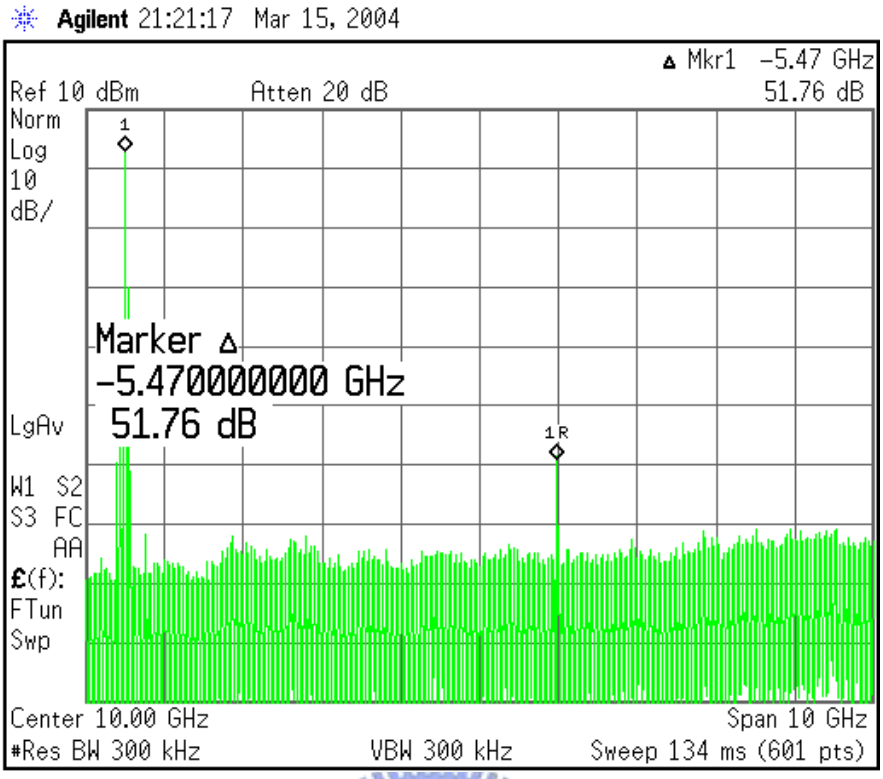


Fig. 5.5 Out-of-band spectrum

5.2 Frequency response test

5.2.1 Instrument setup

Connect the equipments as shown in the Fig.5.2, and use the following procedure to set up these instruments for measuring the frequency response.

1. Set up the spectrum analyzer parameters as follows: **Center frequency** = 5.5 GHz, **Span** = 1.5GHz, **Amplitude** =10dBm, **RBW** = 300KHz, **Trace> Maxhold** mode.
2. Set up the ESG1/ESG2 following parameters: **Frequency** = 10MHz, **Level** = -7dBm, and the phase difference = 90^{o} between the ESG1 and

ESG2

3. For the ESG3, set the **Level** = 1.5dBm and sweep **Frequency** from 5GHz to 6GHz.

5.2.2 Results

The frequency response of the output power is displayed in Fig. 5.6. The flatness remains below 4.1 dB over the entire band. The frequency response of the conversion gain is obtained by a MATLAB program for calculation and plotting as shown in Fig. 5.7. The conversion gain equals 10.5 dB at 5.5GHz. It must be noted that the cable loss (about 1.5dB) must be considered during the calculation.

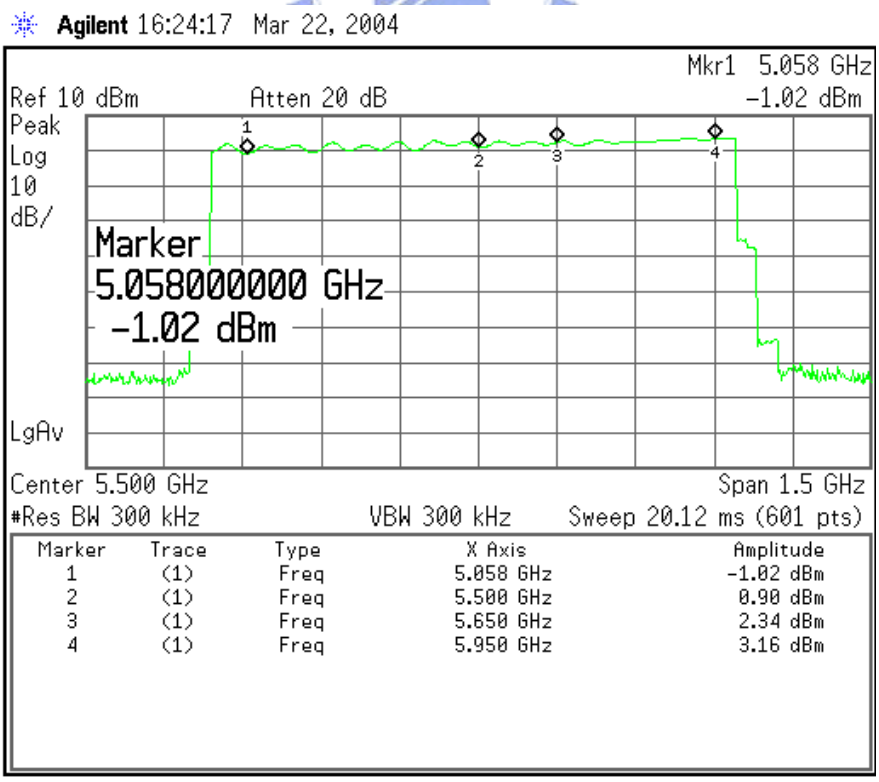


Fig. 5.6 Frequency response of output power

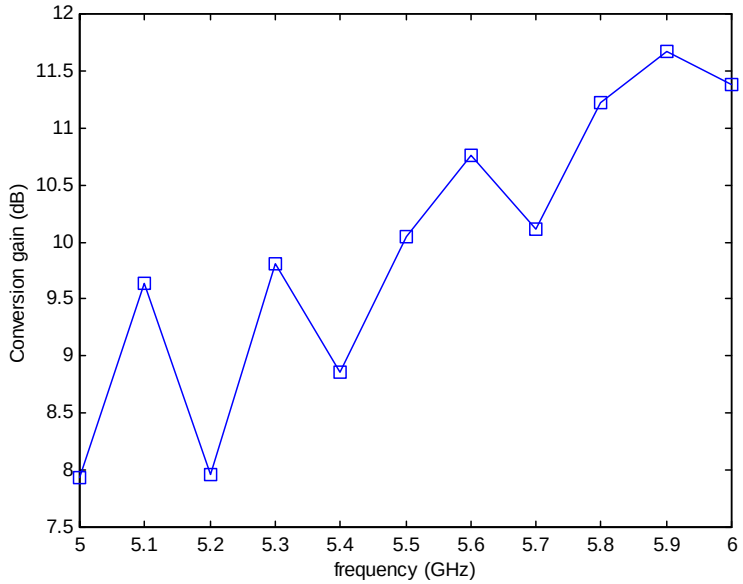


Fig. 5.7 Frequency response of conversion gain

5.3 Output P1-dB test

5.3.1 Instrument setup

Connect the equipment as shown in the Fig. 5.2, and use the following procedure to set up those instruments for measuring output 1-dB compression point.

1. Set up the spectrum analyzer parameters as follows: **Center frequency** = 5.5 GHz, **Span** = 100MHz, **RBW** = 300 KHz, **Amplitude** = 10dBm
2. Set up the ESG1/ESG2 following parameters: **Frequency** = 10MHz, **Level** = -7dBm and the phase difference = 90^{o} between the ESG1 and ESG2.
3. For the ESG3, set the **Frequency** = 5.5GHz and sweep **Level** from -20 to 0dBm.

5.3.2 Results

The measured data are recorded and plotted by MATLAB as shown in Fig.5.8. It indicates that the output 1-dBompressioin point occurs at 3.8dBm when the BB_power of -5dBm is applied.

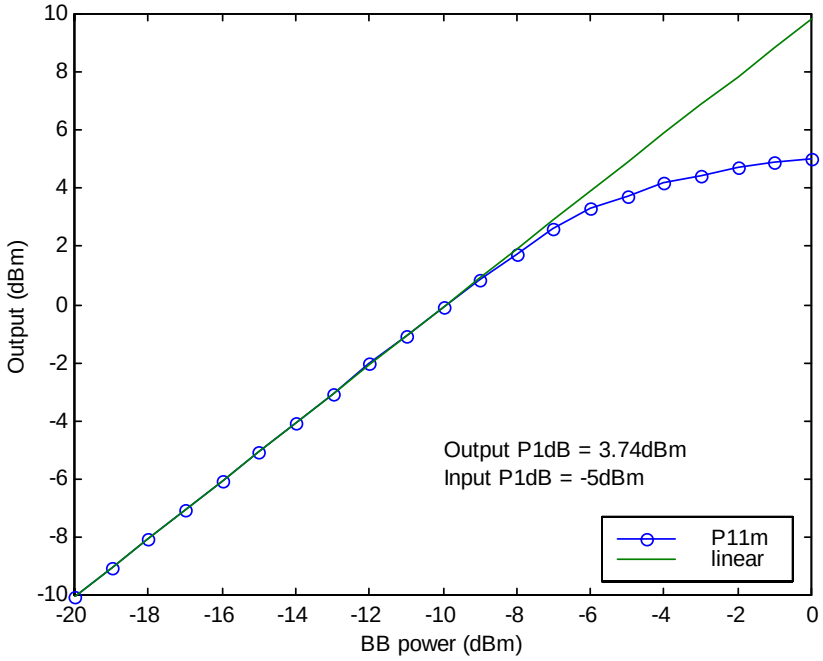


Fig. 5.8 OP-1dB compression point

5.4 IIP3 and OIP3 test

5.4.1 Instrument setup

The equipments are connected as shown in the Fig.5.2, and use the following procedure to set up those instruments for measuring IIP3 and OPI3.

1. Set up the spectrum analyzer parameters as follows: **Center frequency** =

5.5 GHz, **Span** = 100MHz, **RBW** = 300 KHz, **Amplitude** = 10dBm

2. Set up the ESG1/ESG2 parameters: **Frequency** = 10MHz, **Level** = -7dBm and the phase difference = 0^{o} between the ESG1 and ESG2.

3. For the ESG3, set the **Frequency** = 5.5GHz and sweep **Level** from -20 to 0dBm.

5.4.2 Results

The IIP3 and OIP3 point can be found by a simple MATLAB program. The measured data are recorded and plotted as shown in Fig.5.9. As the figure indicates, the IIP3 and the OIP3 is about 8dBm, 13.4dBm, respectively.

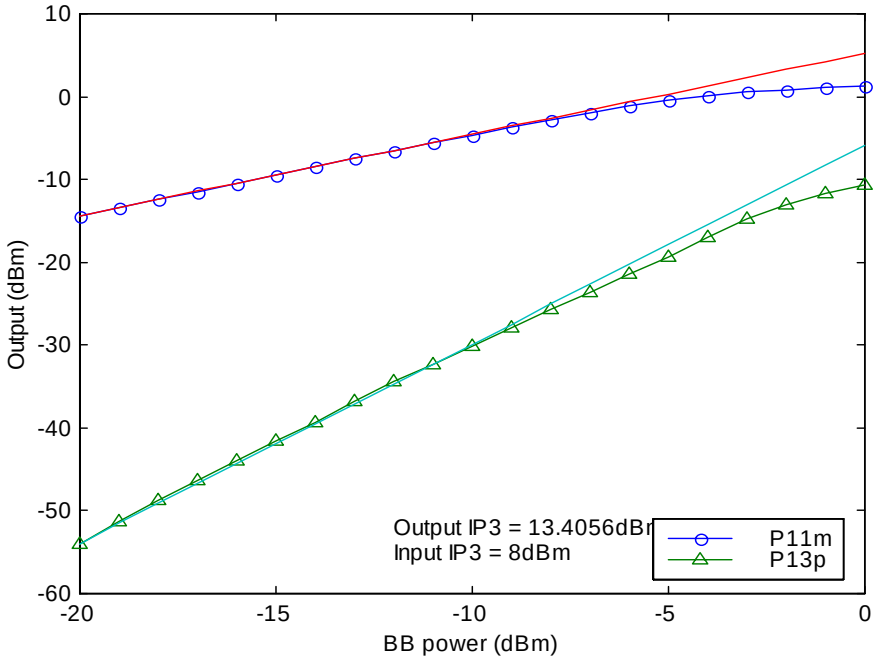


Fig. 5.9 IIP3 and OP3

5.5 Transmit spectrum mask test

5.5.1 Instrument setup

Connect the equipments as shown in the Fig.5.10. The BB_I/BB_Q port is connected to the I /Q _output connector of ESG1. In order to control the ESG1 for creating an 802.11a OFDM waveform, Agilent Signal Studio software is launched. The Agilent Signal Studio configuration is illustrated in Fig. 5.11. After downloading the 802.11 OFDM signal to the ESG1 by the LAN or GPIB interface, use the following procedure to set up the spectrum analyzer (PSA) parameters for measuring the spectrum mask.

1. Press **MODE** > **Spectrum analysis**.
2. Press **Frequency Channel** > 5.5 GHz
3. Press **Mode Setup** > **Radio Std** > **More 1 of 3** > **More 2 of 3** > **802.11a**, **Measure** > **More 1 of 2** > **Spectrum Emission Mask**, and **Meas Setup** > **Optimize Ref Level**.

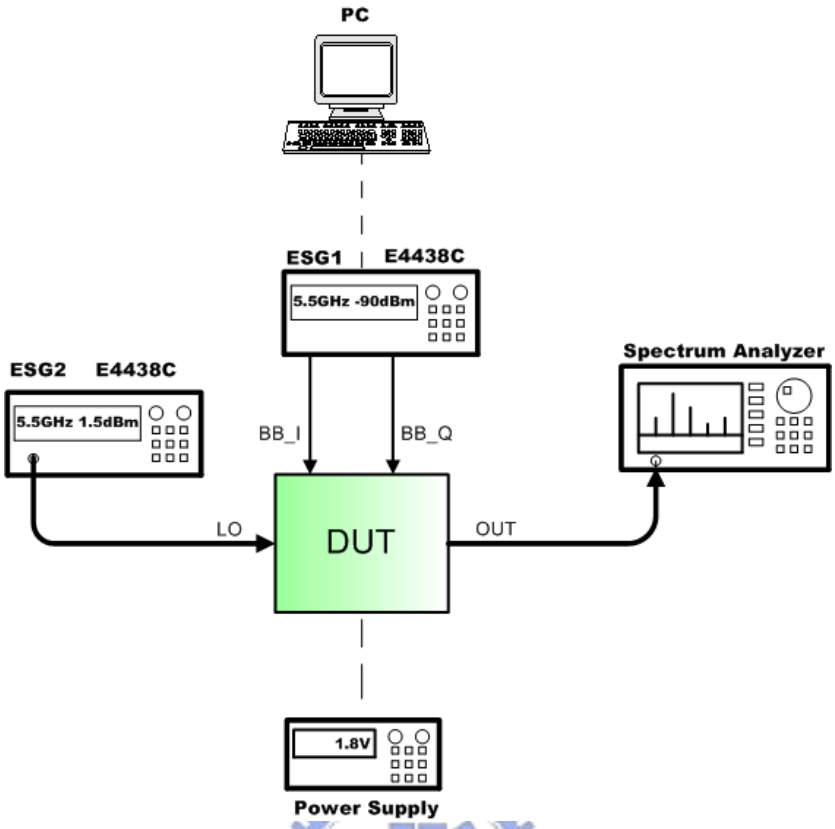


Fig. 5.10 Instrument configuration for spectrum mask test

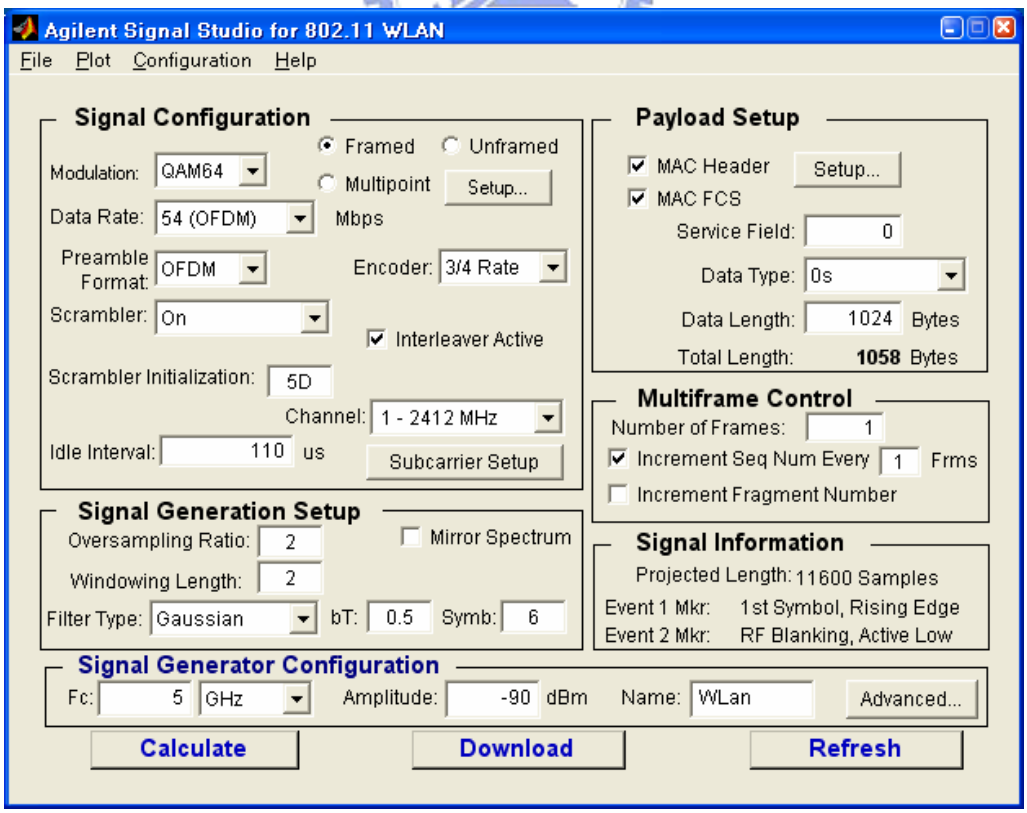


Fig. 5.11 Signal studio setup

5.5.2 Results

Fig. 5.12 displays the measured transmitter output spectrum while transmitting a -7.22dBm 54Mb/s QAM64 modulated signal. Because the PSA power measurement is averaging the power of the bursted transmission, the actual power can be calculated using the following equation

$$Power = Displayed\ Total\ Pwr + 10 \times \log(duty\ cycle) + \text{cable loss} \qquad (5.1)$$

The actual output power is about -4.7dBm, if the duty cycle is 80 %.

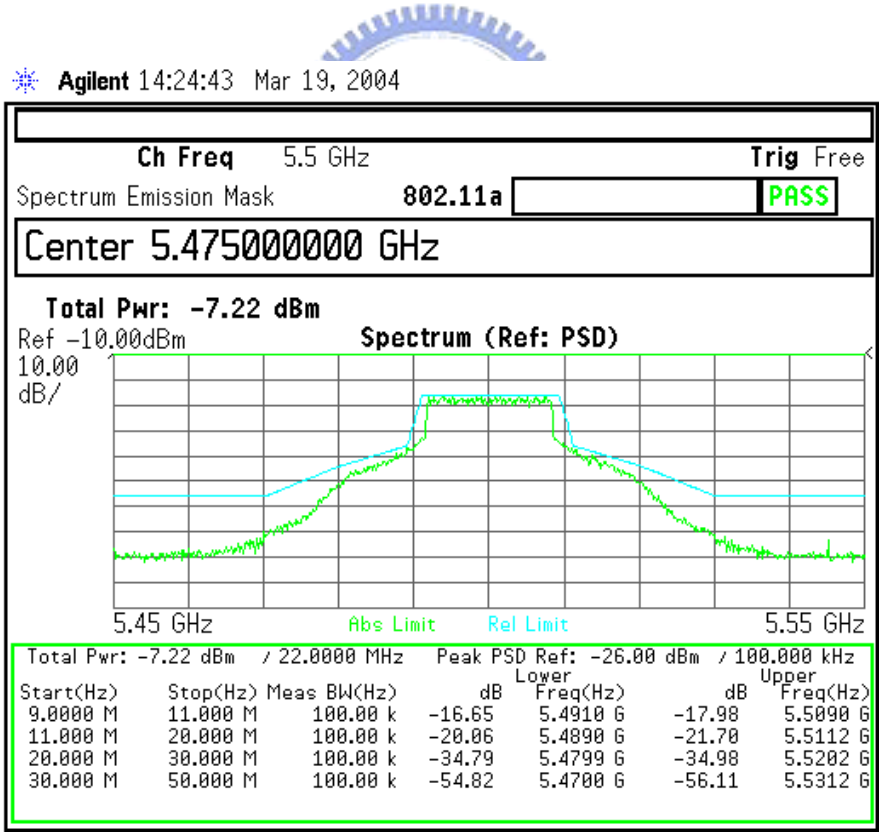


Fig. 5.12 IEEE 802.11a standard spectrum

5.6 System test

5.6.1 Instrument setup

The MIMO (multiple input multiple output) system can transmit or receive simultaneously two or more path signals by multiple antennas to overcome multi-path phenomenon. The transmitter chips are verified in the MIMO system as shown in Fig. 5.13. The diagram only shows the connection of path one signal, another path signal is directly connected by a cable. The data rate of entire system is about 40 Kb/s, which is limited by the DSP (base-band processor) performance.

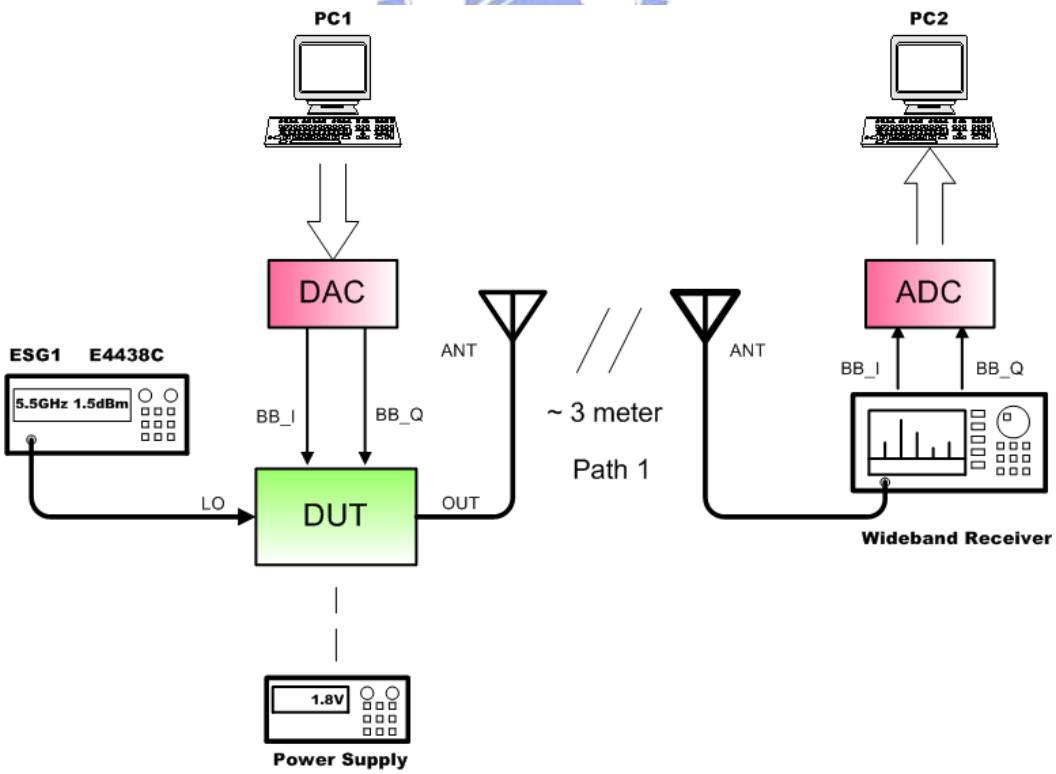


Fig. 5.13 Instrument configuration for system test

5.6.2 Results

Fig. 5.11 displays the transmitted/received images in the MIMO system. We compare the difference between the transmitted and received images. The antenna 1 images show the path1 signal, which is transmitted by this chip. The antenna 2 images are transmitted in a direct connection. The diagram tells us that the transmitted image differs slightly the received image, and the bit error rate is 2.27×10^{-3}.

Fig. 5.14 Result of the system test

5.7 Summary

The specifications, simulations and measurements are summarized in Table 5.1. According to Table 5.1, we can find that the major difference between simulations and measurements is OP 1-dB compression point. We will analyze the reasons of the errors as follows. First, the imperfect chip and PCB layout result in the performance degradation. Second, the circuit model (e.g. NMOS, ESD and package) not accuracy enough, especially operating in large signal swing. It is a great challenge to prove and meliorate that. This chip compares the performance with papers proposed as shown in Table 5.2[15][8] and Table 5.3[10][11][12].

Table 5.1 Performance of summary

Parameters	Specifications	Simulations	Measurements
Power Consumption	N/A	54 mW	63 mW
Frequency	5~6 GHz	5~6 GHz	5~6 GHz
Conversion Gain	10 dB	13.8 dB	10.5 dB
OIP3	14 dBm	15 dBm	13.4 dBm
Output P1dB	4 dBm	10.5 dBm	3.8 dBm
Flatness	N/A	2.7 dB	4.1 dB
Sideband rejection	>30 dB	38.7 dB	34.3 dB
Carrier rejection	>30 dB	33.4 dB	32.4 dB

Table 5.2 Performance of comparison

Parameters	This work	Po-Niang Lin (2003)	Ting-Ping Liu(2000)
IC process	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.25μm
Die size	6.25m^2	6.25m^2	2.7m^2
Power Consumption	63 mW	47 mW	120 mW
Frequency	5~6 GHz	5.15~5.35GHz	NA
Conversion Gain	10.5 dB	-14.5 dB	NA
OIP3	13.4 dBm	NA	NA
Output P1dB	3.8 dBm	-6.6 dBm	-2.5 dBm
Flatness	4.1 dB	NA	NA
Sideband rejection	34.3 dB	26 dB	33.4 dB
Carrier rejection	32.4 dB	18 dB	22.4 dB

Table 5.3 Performance of comparison

Parameters	Zargari(2002)	Zhang(2002)	Behzad(2003)
IC process	CMOS 0.25μm	CMOS 0.18μm	CMOS 0.18μm
Die size	22m^2(Tx/Rx)	22m^2(Tx/Rx)	11.7m^2(Tx/Rx)
Power Consumption	790 mW	135mW	380mW
Frequency	5.16~5.34GHz	5.15~5.35GHz	5.15~5.35GHz
Conversion Gain	NA	NA	NA
OIP3	NA	15dBm	NA
Output P1dB	17.8dBm	5dBm	19 dBm
Flatness	NA	NA	NA
Sideband rejection	51 dB	50 dB	NA
Carrier rejection	29 dB	38 dB	NA

Chap 6.

Conclusions

A 5GHz transmitter front-end chip for IEEE 802.11a is implemented and measured. The transmitter IC is fabricated in UMC 0.18-μm 1P6M CMOS technology and packaged in SPIL QFN20. The die occupied 2.5×2.5 mm^2. This chip achieves an output 1-dB compression of 3.8dBm at 5.5GHz with 10.5dB conversion gain and 34.3dB sideband rejection. Although imperfect layout and inaccurate device model causes the degradation of RF performance, it still can work well on system test verification.

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