國立交通大學

電機學院 電子與光電學程

碩 士 論 文

5.5GHz 低功耗射頻 CMOS 混頻器設計與研製

5.5GHz Low Power RF CMOS Mixer Design and Chip Fabrication

研 究 生：盧笙豐

指導教授：郭治群 博士

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摘　要

本篇論文介紹低功率消耗之無線區域網路之射頻吉伯特混波(Gilbert mixer)之電路設計。對於單晶片(SoC)手持式無線網路之產品應用，低功率消耗之電子式產品，以蔚為新的潮流及趨勢。本論文是以 TSMC 0.18μm 1P6M CMOS model 模擬電路及實現低功率電路。主要電路是以吉伯特混波器(Gilbert mixer)為主，電源供應系利用 LC 並聯諧振電路當作 RF-MOS 級 LO MOS 電源供應。吉伯特混波器基本架構圖以 multi-gate 電路放大器，其主要功能有二：第一為增加 Gm 值，以增加其增益轉換值(S_{21})；第二增加其線性度，利用不同之輸入閘級電壓，將非線性的部分做部分的互相抵銷，使其線性度增加。在閘級輸入電壓串聯一電感目的為使輸入信號的能量集中在閘及輸入端作為阻抗匹配，使其有最大的能量轉換。並適當的嘗試改變基本電路架構於射頻輸出端與 LO 間加入一電感，可得到更大的轉換增益(Conversion Gain)。我們亦嘗試在 IF 輸出端並聯一被動元件-電容，以增加其線性度。本合成器在實際封裝量測中，輸出 P-1dB 點為 2.5 dBm，IIP3 為 11dBm 即轉換增益為 7.46 dB，消耗功率為 9.5 mW。

5.5GHz Low Power RF CMOS Mixer Design and Chip Fabrication

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ABSTRACT

This thesis proposes a low-power mixer circuit design for wireless communication applications. For systems-on-a-chip (SoC) in portable wireless networks, low power requirement is increasingly important. In this study, TSMC 0.18μm 1P6M CMOS process and model are employed for circuit implementation and simulation to achieve low power. Gilbert cell mixer circuit is adopted and some new ideas are proposed to reduce power consumption. The proposed new ideas cover a parallel resonator realized by LC-tanks and multi-stage parallel RC networks for linearity improvement. Also, multi-gated structure is applied in the RF input as a transconductance amplifier to improve conversion gain and linearity . The higher conversion gain (S21) is due to larger Gm. The better linearity of higher IIP3 is attributed to third-order nonlinear term cancellation realized by gate bias tuning on the multi-gated structure. An on-chip inductor is added in RF input for impedance matching. For LO input impedance matching,

off-chip inductor is employed. For RF output a pair of on-chip inductors were used to increase conversion gain. The parallel R-C networks add to IF output terminal can improver linearity with higher IIP3. Measured performance in terms of linearity is P-1dB at 2.5 dBm and IIP3 at 11 dBm The conversion gain can be achieved at 7.46 dB, and power consumption can be maintained as low as 9.5 mW.

誌　謝

轉眼間，碩士在職專班生涯已過了三年半，前兩年以修課為主，後期即以論文研究為主。在此，感謝很多人的支持和幫忙，讓我的學業及論文得以完成。特別感謝我的指導教授 郭治群老師不辭辛勞的教誨及指導，並提供一個新的思考方向，讓我在研究過程中得以解決重重困難且得到更多的寶貴經驗。

感謝 ED635 實驗室同學宏霖、益民、致廷、登陽、姵瑩的幫忙，讓我們新的實驗室有更多的資源及提供我們一個更好的研究環境. 再此也感謝鼎勳實驗室所有同之幫忙。感寫我週遭關心我的好朋友，感謝您們的幫助及給我的鼓勵加油，感謝國科會國家晶片中心(CIC)提供先進的半導體製程技術，讓晶片的的以順利完成。

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Chapter 1

Introduction

1.1 Motivation

The advancement of semiconductor technology has driven the growth of wireless communication. Furthermore, the deep submicron CMOS technology has attracted much interest and effort to penetrate into wireless communication application due to advantage of lower cost and higher integration. Due to the fact, RF CMOS becomes a hot topic in academic research and technology development. Higher frequency and wider bandwidth can increase data rate and lower supply voltage is desired to achieve low power. However, the RF CMOS circuit design is traded off with many challenges like high frequency model accuracy, impedance matching, linearity, noise, and power consumption. Each factor influences circuit performance and its consideration increases the difficulty of RF circuit design. For RF MOSFET model, the major challenges include the parasitic resistance, inductance, and capacitance effects and accuracy in gate capacitance model, noise model, and subthreshold region models. As for passive device models, a broadband and scalable model for on-Si—chip inductors become a major challenge for RF integrated circuit simulation and design.

In this thesis, a single band 5.5 GHz down-converter mixer is designed for application in the 802.11a standard. The major features for this new mixer design include low-power-consumption, high-performance, high linearity and high conversion gain. Figure 1.1 shows the 802.11a function block. The fundamental wireless communication architecture includes a switch, a power amplifier (PA), a low-noise amplifier (LNA), an up-converter mixer, a down-converter mixer, a synthesizer, and a filter.

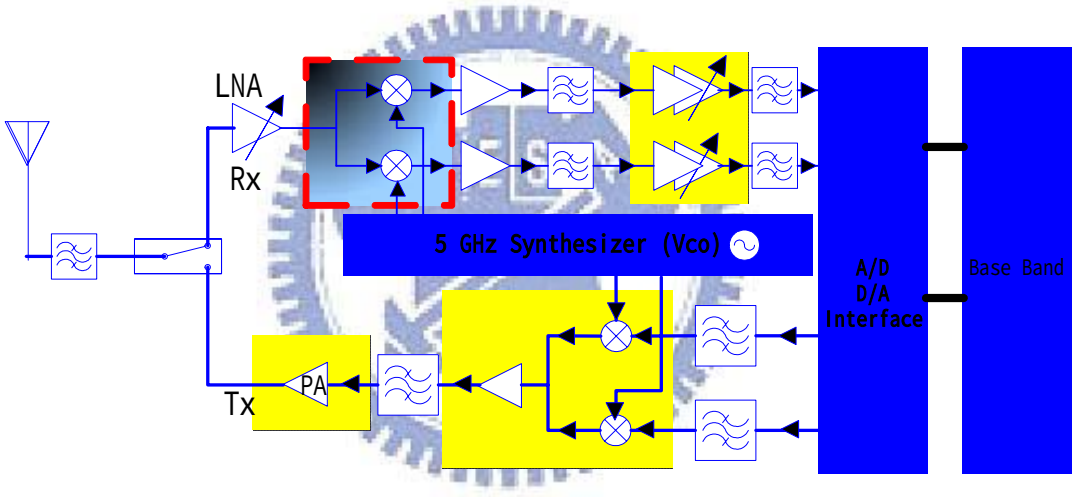


Fig. 1.1 Receiver mixer function block

1.2 IEEE 802.11a Standard

An IEEE 802.11a standard system has a total bandwidth of 300 MHz and a 20MHz bandwidth for each channel. The IEEE 802.11a standard applies the 5GHz unlicensed national information infrastructure (U-NII) bands, as shown in Fig. 1.2 [1]. The bandwidths available for 802.11a cover the lower band frequency from 5.15 GHz to 5.25 GHz, and the middle band frequency from 5.25GHz to 5.35GHz. Both bands

provide eight channels. Each band bandwidth is 200 MHz and outmost channel side band is 30 MHz. The upper band frequency 5.715GHz to 5.825GHz U-NII band accommodates four channels in the final 100 MHz of the bandwidth, and the outmost channel sideband is at 20 MHz.

This bandwidth is associated with an orthogonal frequency division multiplexing (OFDM) modulated signal, comprising 52 subcarriers, each of which has a bandwidth of 300KHz for each channel. Each subcarrier can be modulated by binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16-QPSK or 64 QQPSK modulation. The RF signal can rise to a fast data rate of 54 Mbps in 20 MHz for each channel.

For performance evaluation of the IEEE 802.11a, an error vector magnitude (EVM) is generally used to represent the quality of a digitally modulated signal. The EVM can indicate a disfigurement, such as an amplitude mismatch, a phase error, phase noise, nonlinearity and others. The modulation parameters depend on the data rate and are set as shown in Table 1.

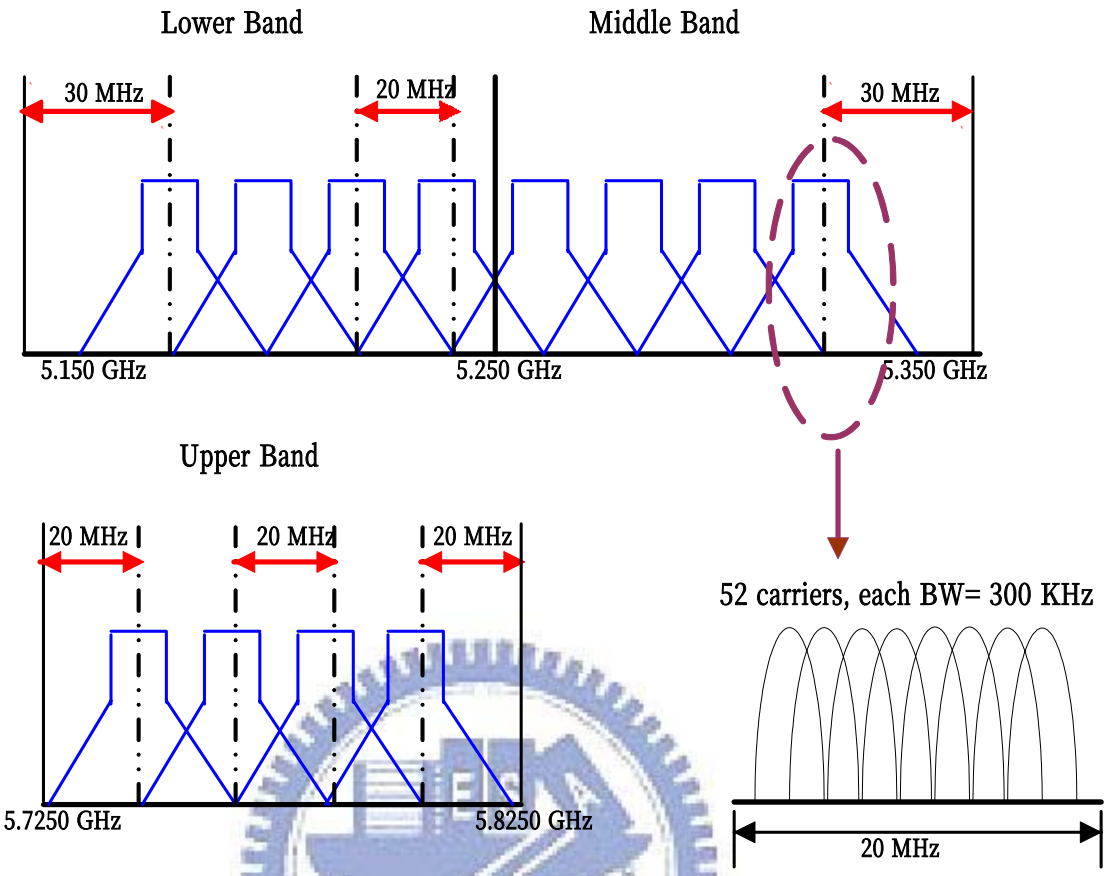


Fig. 1.2 IEEE 802.11a Channel Location for 5GHz U-NII Bands

Table 1.1 IEEE 802.11a modulation scheme and EVM requirement

Data Rate (Mbits/s)	Modulation	Coding Rate	EVM (dB)	Minimum sensitivity (dBm)
6	BPSK	1/2	-5	-82
9	BPSK	2/3	-8	-81
12	QPSK	1/2	-10	-79
18	QPSK	3/4	-13	-77
24	16-QAM	1/2	-16	-74
36	16-QAM	3/4	-19	-70
48	64-QAM	1/2	-22	-66
54	64-QAM	3/4	-25	-65

Inevitability, an adjacent channel interferes with the signal emitted from a

channel. IEEE 802.11a regulations define the maximum power level and the transmission spectrum mask. The maximum emission power is determined by FCC regulations, as indicated in Table 1.2.

Table 1.2 IEEE 802.11a transmit maximum power levels

Frequency band (GHz)	Maximum output power with up to 6dBi antenna gain (mW)
5.15~5.25	40 (2.5 mW/MHz)
5.25~5.35	200 (12.5mW/MHz)
5.725~5.825	800 (50 mW/MHz)

The transmitted spectrum density must have a 0 dBr bandwidth of not more than 18 MHz, –20 dBr at an 11 MHz frequency offset, –28 dBr at a 20 MHz frequency offset and –40 dBr at a 30 MHz frequency offset and above. The transmitted spectral density of the transmitted signal must fall within the spectral mask, as shown in Fig. 1.3.

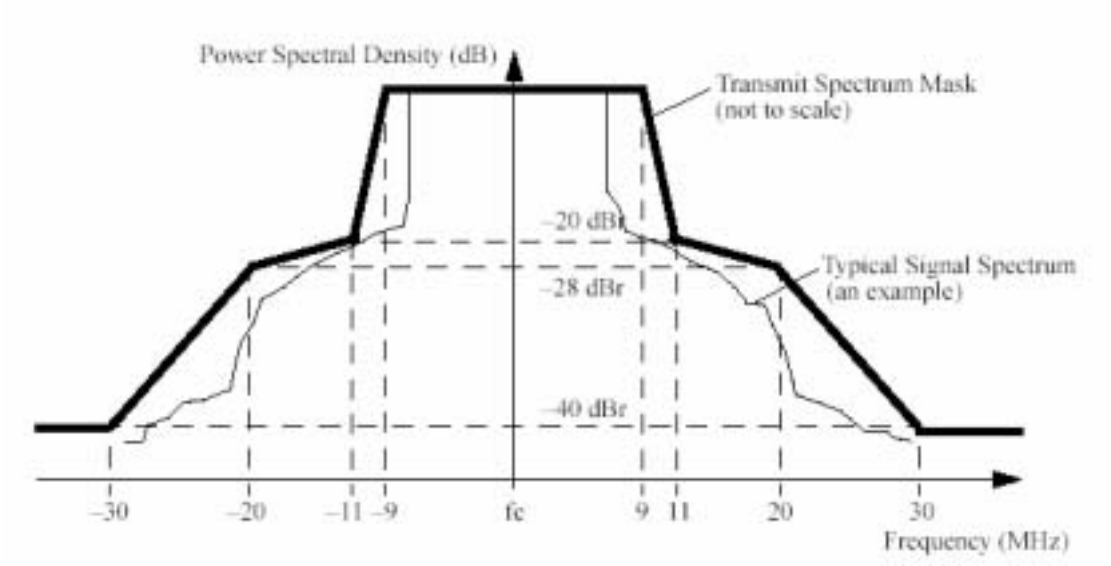


Fig . 1.3 IEEE 802.11a Transmitted Spectral

1.3 Thesis Organization

In this thesis, a down-converter mixer is designed and fabricated by 0.18 RF

CMOS technology to achieve advantage of low power consumption, high linearity and high conversion gain. The method to realize the mentioned advantages will be described in the following chapters.

Chapter 2

Receiver Architecture

Recently, commercial RF and wireless communication products have become more prevalent. The RF wireless communication carrier frequency has increased to 12 GHz and related fabrication processes have shrunk to the nanometer scale. Numerous RF and wireless products, such as mobile ‘phones, RFID, GPS, Bluetooth products and wireless networks, are now affecting daily life.

This chapter introduces several architectures, including an active mixer and a passive mixer. The architectures of heterodyne receivers and homodyne receivers are also discussed [2-3].

2.1 Introduction to RF Receivers

A wireless communication system transmits carrier information over a limited bandwidth, such as 30 kHz in IS-54, 200 KHz in GSM and 20 MHz in WLNA.

The narrow bandwidth of the system affects the design of an RF section. The transmitter must employ narrowband amplification and filter to prevent interference from an adjacent channel, as displayed in Fig. 2.1. The receiver must process a weak signal and reject strong interference from nearby antennae and bandpass filter signals, as presented in Fig. 2.2.

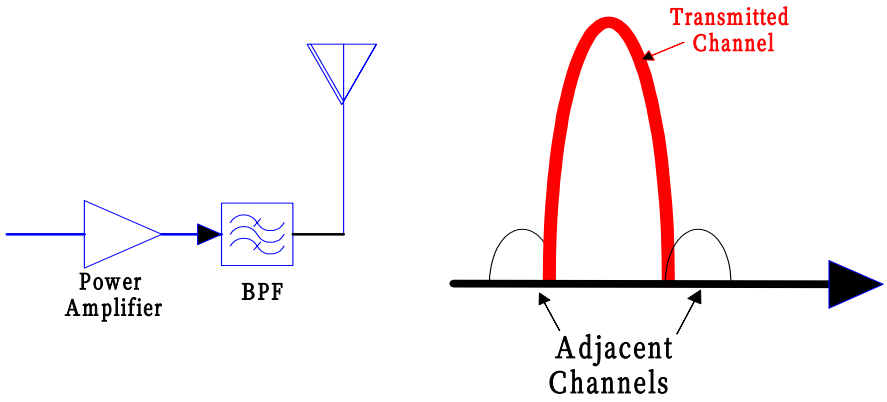


Fig. 2.1 Transmitter front end of a wireless transceiver

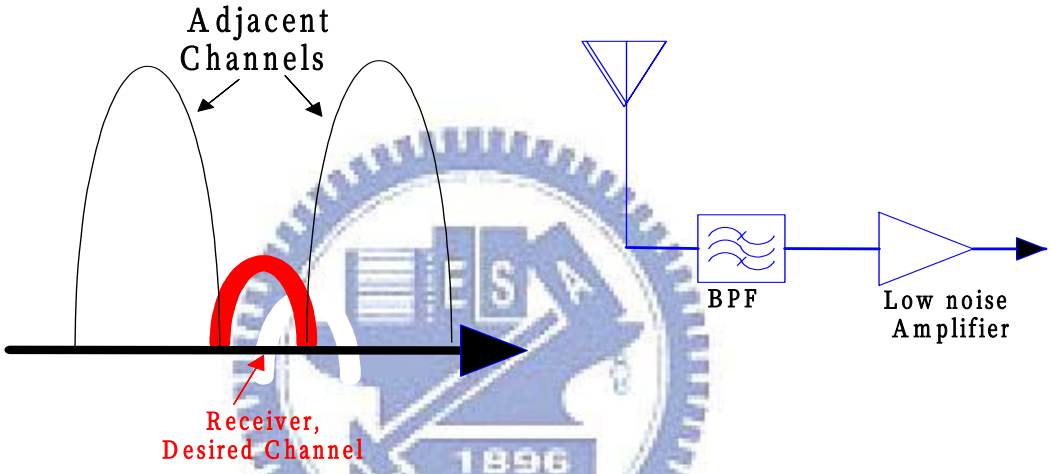


Fig. 2.2 Receiver front end of a wireless transceiver

In this section, we will describe the heterodyne, homodyne and image rejection architectures for the receiver design.

2.1.1 Heterodyne Receivers

The heterodyne receiver transforms a signal from carrier radio frequency (RF) to intermediate frequency (IF), base-band frequency. Heterodyne receivers are of two types - (I) simple heterodyne receiver and (II) multiple heterodyne receivers. As described above, the receiver front end signal suffers large interference and distortion

of the original signal and requires prohibitively high Q values.

2.1.1.1 Simple-Stage Heterodyne Receivers

The single stage heterodyne receiver in one stage converts radio frequency to intermediate frequency. It utilizes only one mixer. As shown in Fig 2.3, the radio frequency is received from the antenna, passed through an RF filter to suppress interference; sent to a low-noise amplifier (LNA) and then to the mixer, and eventually delivered to base-band chip. The simple heterodyne design must take into account the choice of IF and so depends on trade-offs among three parameters - (I) image reject filter loss, (II) image noise, and (III) spacing between image and desired band. Item III is of particular importance since designing a narrow band filter is very difficult.

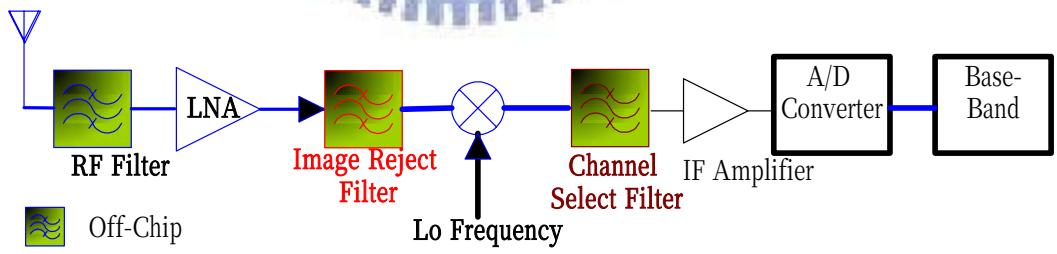


Fig. 2.3 (a) Simple heterodyne receiver

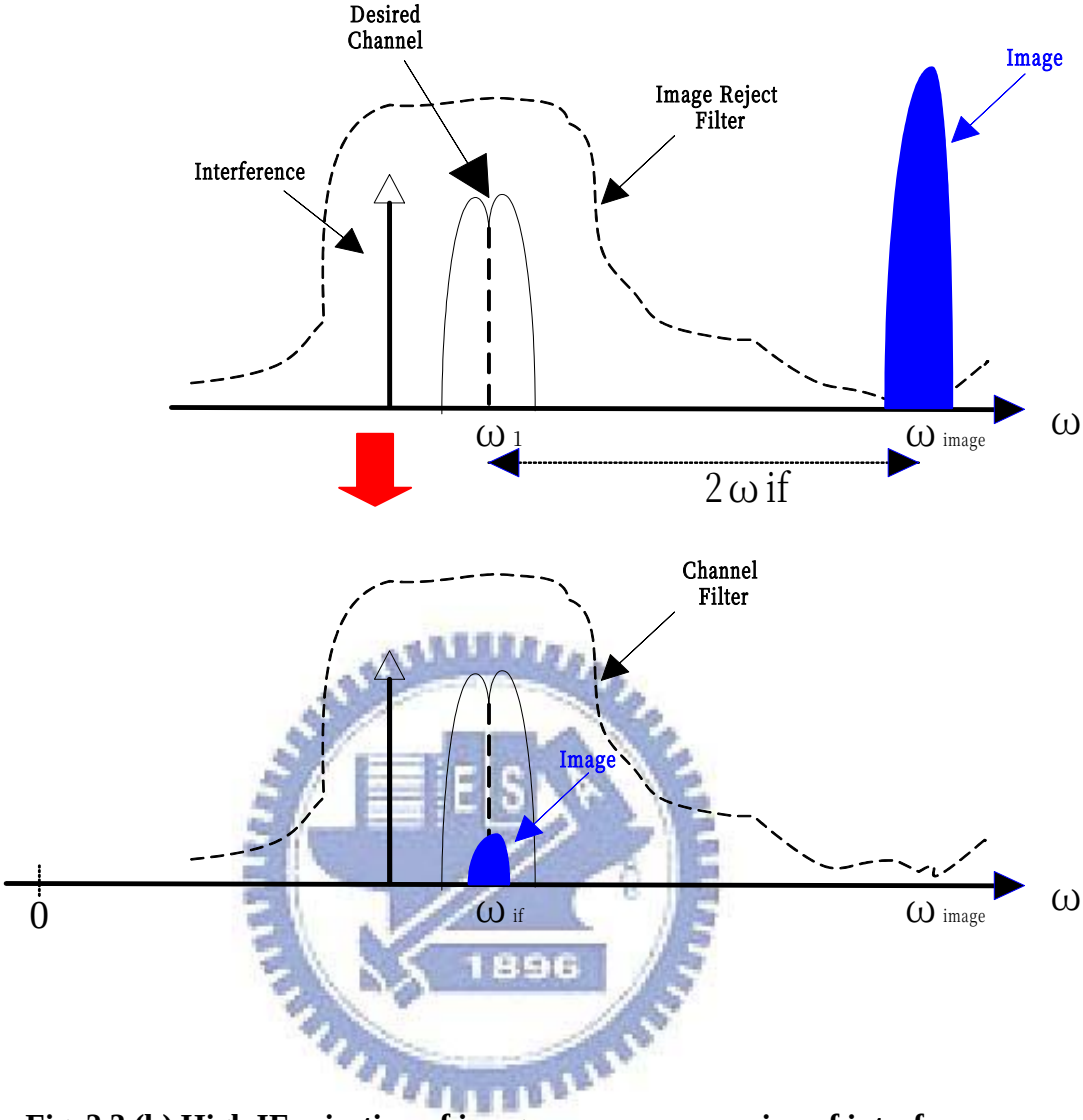


Fig. 2.3 (b) High IF rejection of image versus suppression of interferers

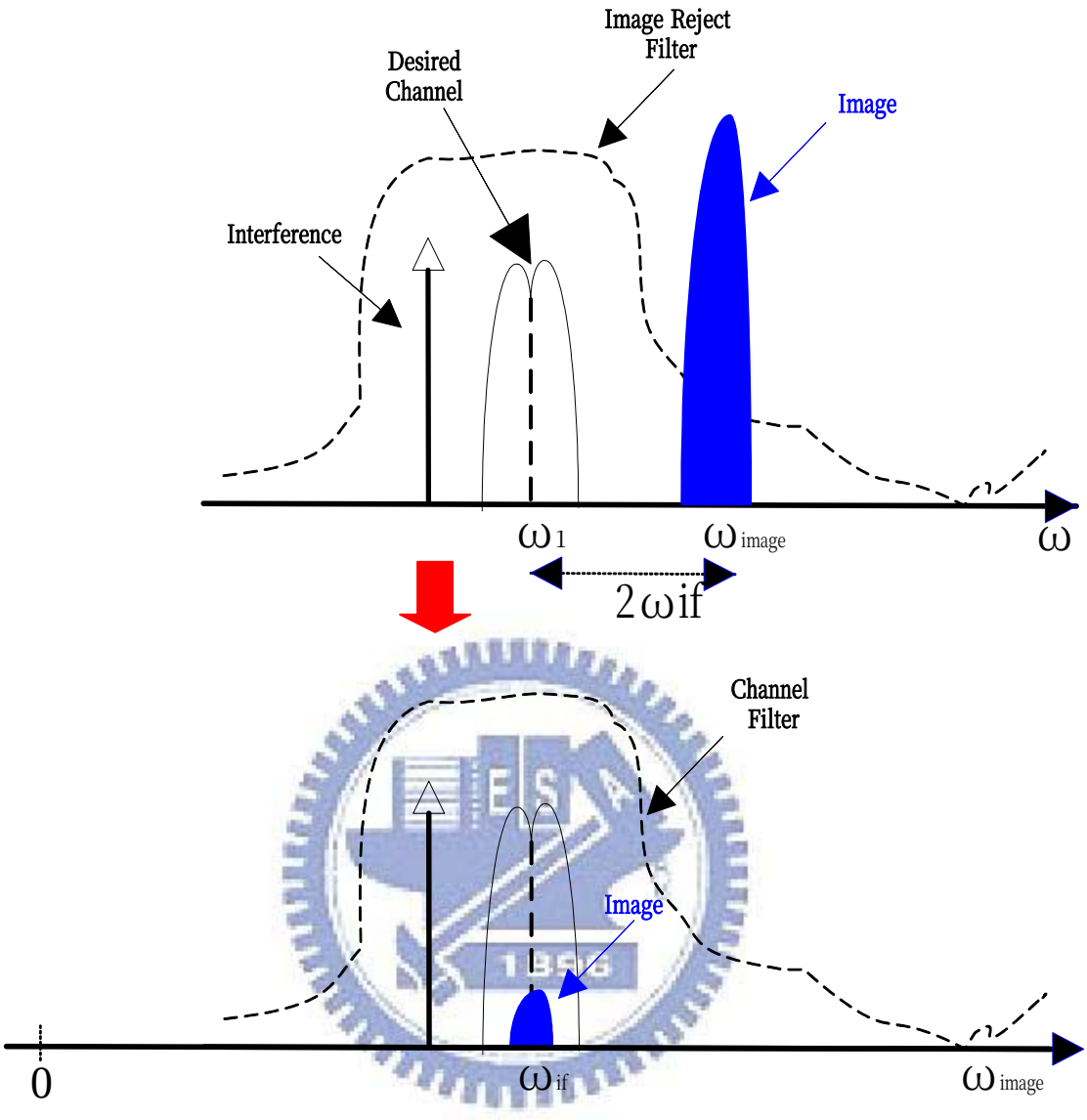


Fig. 2.3 (c) Low IF rejection of image versus suppression of interferers

If the radio frequency $\omega_{rf} = \omega_{lo} + \omega_{if}$, then the mirror image may happen at frequency $\omega_{rf} = \omega_{lo} - \omega_{if}$. The mixer and local oscillator frequencies make it difficult in the determination of the overlap frequency on the IF port. Accordingly, an image rejection filter (IR Filter) must be added before the mixer. The IR filter typically requires a high-Q filter, but the integration circuit (IC) does not allow the simple implementation of a high-Q solution. Therefore, the integration of the system is

complicated.

This simple heterodyne raises a series problems associated with mirror image rejection frequency interference. The image frequency degrades the sensitivity and signal-to-noise ratio (SNR). The image frequency is defined as $\omega_{image} \equiv \omega_{rf} - 2\omega_{if}$; the frequency of the down-conversion to IF is defined $\omega_{if} \equiv \omega_{rf} - \omega_{lo}$; RF is ω_{rf}, and the local oscillator frequency is ω_{lo}. The down-converter mixer process must be modeled mathematically to solve the image problem. The RF and LO input equations are defined as $V_{rf} = A_{rf} \cos\omega_{rf} t$ and $V_{lo} = A_{lo} \cos\omega_{lo} t$. and $A_{lo} = A_{rf} = A$ is assumed. Hence,

$$V_{if}(t) = A \cos\omega_{rf} t \cdot A \cos\omega_{lo} t \tag{2.1}$$

$$= \frac{1}{2} A^2 [\cos(\omega_{rf} + \omega_{lo})t + \cos(\omega_{rf} - \omega_{lo})t] \tag{2.2}$$

$$= \frac{1}{2} A^2 [\cos(\omega_{rf} + \omega_{lo})t + \cos\omega_{if} t] \tag{2.3}$$

The second term is the intermediate frequency (IF) of interest.

$\omega_{if} \equiv \omega_{rf} - \omega_{lo}$ and $\omega_{image} \equiv \omega_{rf} - 2\omega_{if}$ are used to rewrite the assumed image frequency equation $\omega_{image} = \omega_{lo} - \omega_{if}$.

$$V_{if}(t) = A_{inage} \cos\omega_{image} t \cdot A_{lo} \cos\omega_{lo} t \tag{2.4}$$

$$= \frac{1}{2} A^2 [\cos(\omega_{lo} - \omega_{if} + \omega_{lo})t + \cos(\omega_{lo} - \omega_{if} - \omega_{lo})t] \tag{2.5}$$

$$= \frac{1}{2} A^2 [\cos(2\omega_{lo} + \omega_{if})t + \cos\omega_{if} t] \tag{2.6}$$

Therefore, strong interference at the image frequency affects the IF signal, then the IF will strongly interfere with the desired signal, degrading the system (SNR). For the simple heterodyne receiver, an accurate IF frequency must be chosen. The frequency declines to IF from RF and the local frequency only once. A high IF is chosen. Accordingly, a high Q filter must be employed. The high-Q filter is not simple to implement with SoC and high-speed A/D converter design is very challenging. If a lower IF is chosen, the image frequency will not be eliminated and the high image frequency noise on IF will be excessive. Figures 2.3(b) and 2.3(c) reveal that if the IF is high, then the image can be suppressed but complete channel selection is very difficult. Therefore, the simple heterodyne has sensitivity and selectivity problems.

A simple heterodyne receiver application must take into account sensitivity and selectively, and the problem of integration for a SoC system.

2.1.1.2 Multiple Heterodyne Receiver

To solve the problem described in the preceding section, the concept of the simple heterodyne can be expanded to multiple heterodyne down-converter mixers. The multiple heterodyne has at least two frequency levels from the RF frequency down to IF, to eliminate the filter Q value requirement. Partial channel selection can be conducted and the image rejected in two stages, as shown in Fig. 2.4 (a).

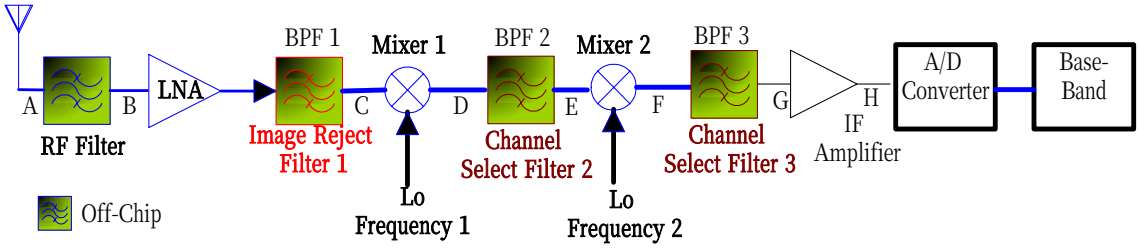


Fig. 2.4 (a) Dual-IF heterodyne receiver

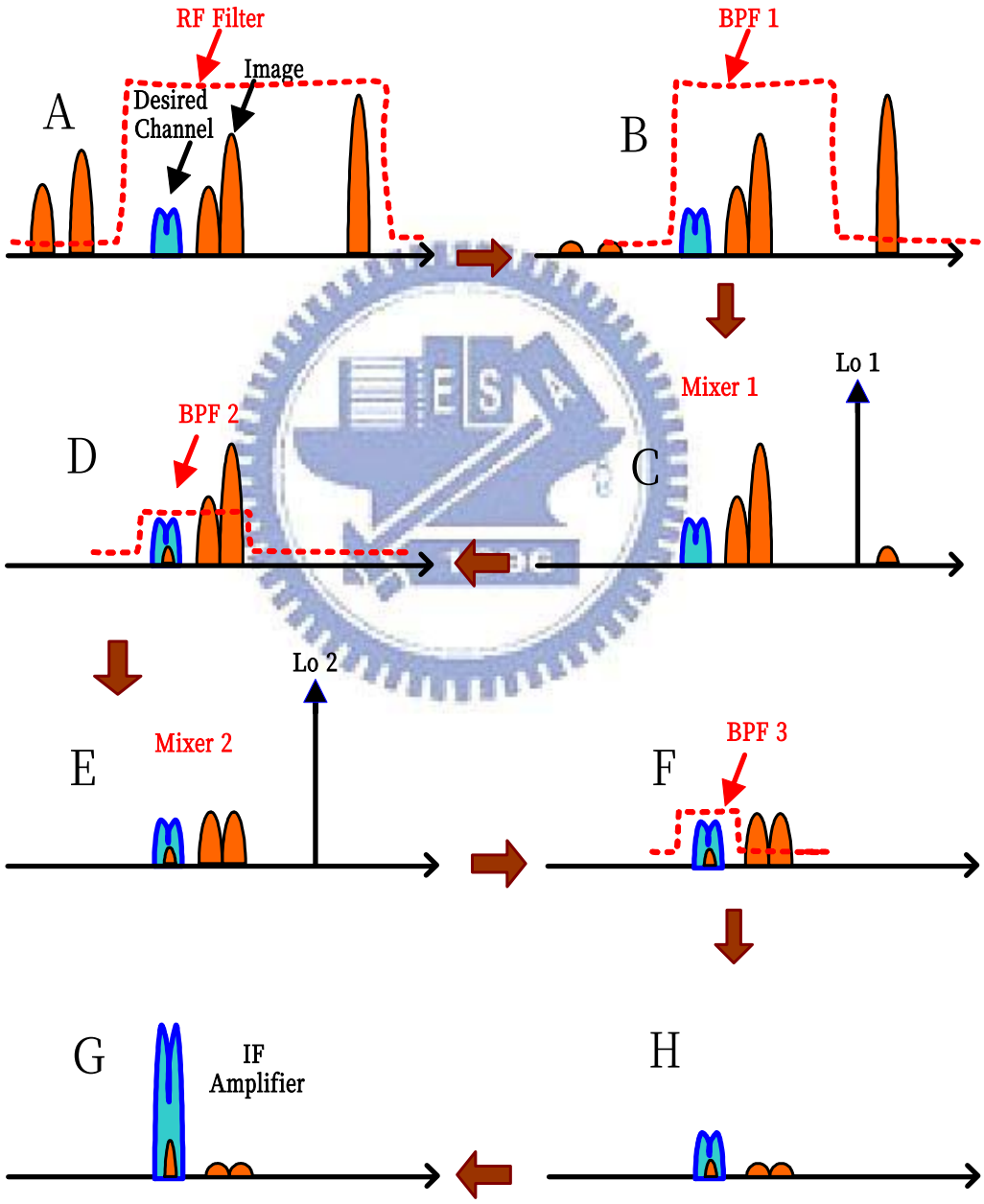
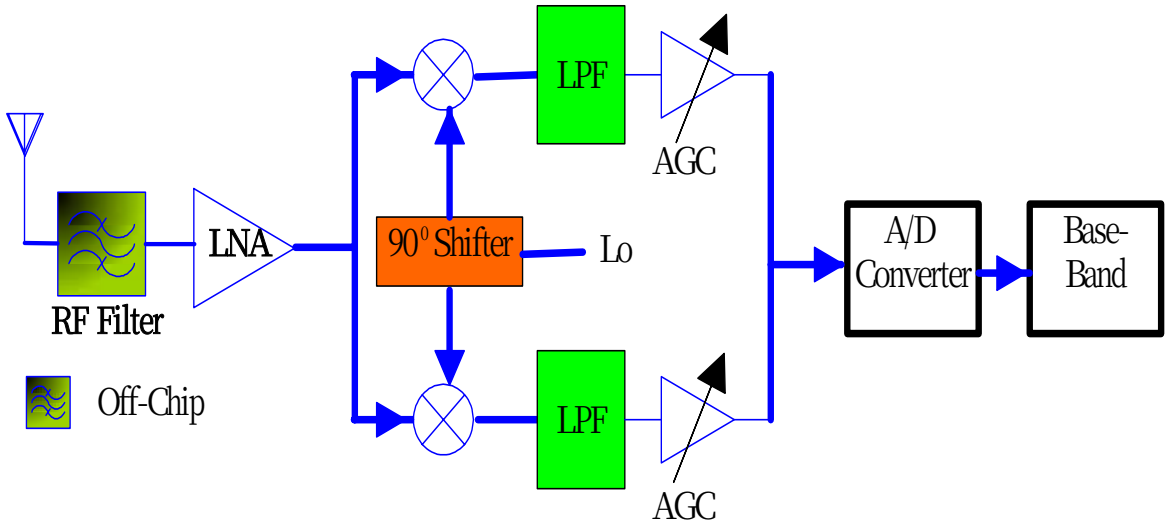


Fig. 2.4 (b) Dual-IF heterodyne receiver frequency conversion.

Despite the fact that the multiple heterodyne receiver does not require high Q,

integrating an SoC system will require that the band pass filter has a very large IC. Figures 2.4(a) and 2.4(b) show spectra at various points in the dual-IF receiver. The frond-end RF band selection filter suppresses image rejection and the spectra at point as shown figures Fig. 2.4(b) A and B. Following LNA and image reject filter, a spectrum from point as shown figures Fig. 2.4(b) B to C can be obtained. Then, the desired channel and the adjacent interference must be translated the spectrum at point C. The adjacent interference is slightly suppressed by BPF-2. Similarly, the second mixer provides reasonable linearity and signal translates to the second IF as shown figures Fig. 2.4(b) spectra D and E. After The BPF-3 channel filter absolutely suppresses the adjacent interference signal, as shown in Fig. 2.4(b), in spectra F to H. Finally, the IF signal is amplified.

The second down-conversion mixer typically generates both in-phase (I) and quadrature (Q) which components of the signal are used to translate the spectrum to zero frequency, yielding the block diagram in Fig. 2.5



. **Fig. 2.5 Quadrature down-conversion zero IF receiver.**

Despite the addition of the extra complexity component of the RF and IR filter and the increased size on SoC, heterodyne receivers are conventionally used as the most reliable.

2.1.2 Homodyne Receivers

Figure 2.6 shows a fundamental architecture of a homodyne receiver. The Lo frequency equals the RF input carrier frequency; such receivers are called “zero-IF” or “direct-conversion”. The homodyne receiver is designed as a low-pass filter instead of a channel select function.

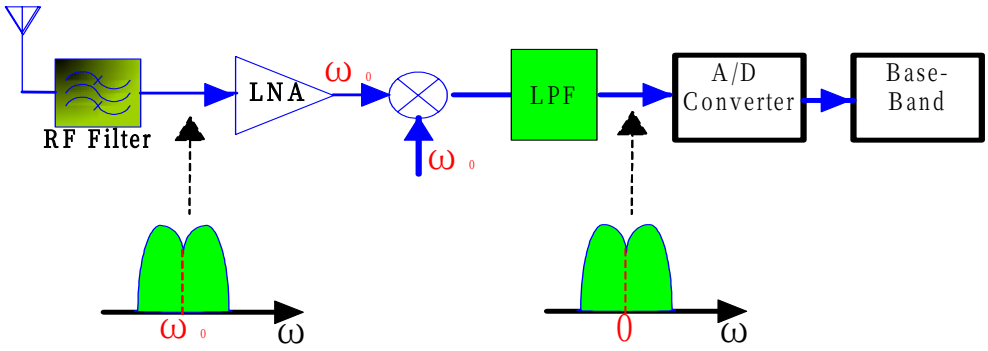


Fig. 2.6 Simple homodyne receiver.

The homodyne receiver architecture has evident relative characteristic without image reject signals. Since the homodyne receiver's RF receiver signal is through RF filter, LNA, mixer, and to LPF, which can remove image frequency by itself, the homodyne architecture does not require an image reject filter. Consequently, the homodyne requires no external connected component module, and can be integrated as a single entity.

A direct down-conversion receiver with a spectrum translated to zero frequency suffers from such issue such as DC offset, I/Q mismatch, even-order distortion, flicker noise and LO leakage problem, as described below.

(a). DC Offset

Since the local oscillator frequency equals RF, the isolation between the LO port and the LNA input or mixer input is finite. The strong extraneous signal is fed through from the LO port to the LNA input and the mixer input, as shown in Fig. 2.7 (a). Similarly, if a large leakage from the LNA to mixer input interferes through to LO port, it is possible multiplied by itself signal as shown in Fig, 2.7 (b), then, LO port signal and mixer input signal couple signal can corrupt or distort the original signal of the LAN or mixer input. The signal coupling issue then involves partial DC offset and may cause A/D converter saturation, after causing a demodulation error. This effect arises from the substrate or capacitance coupling.

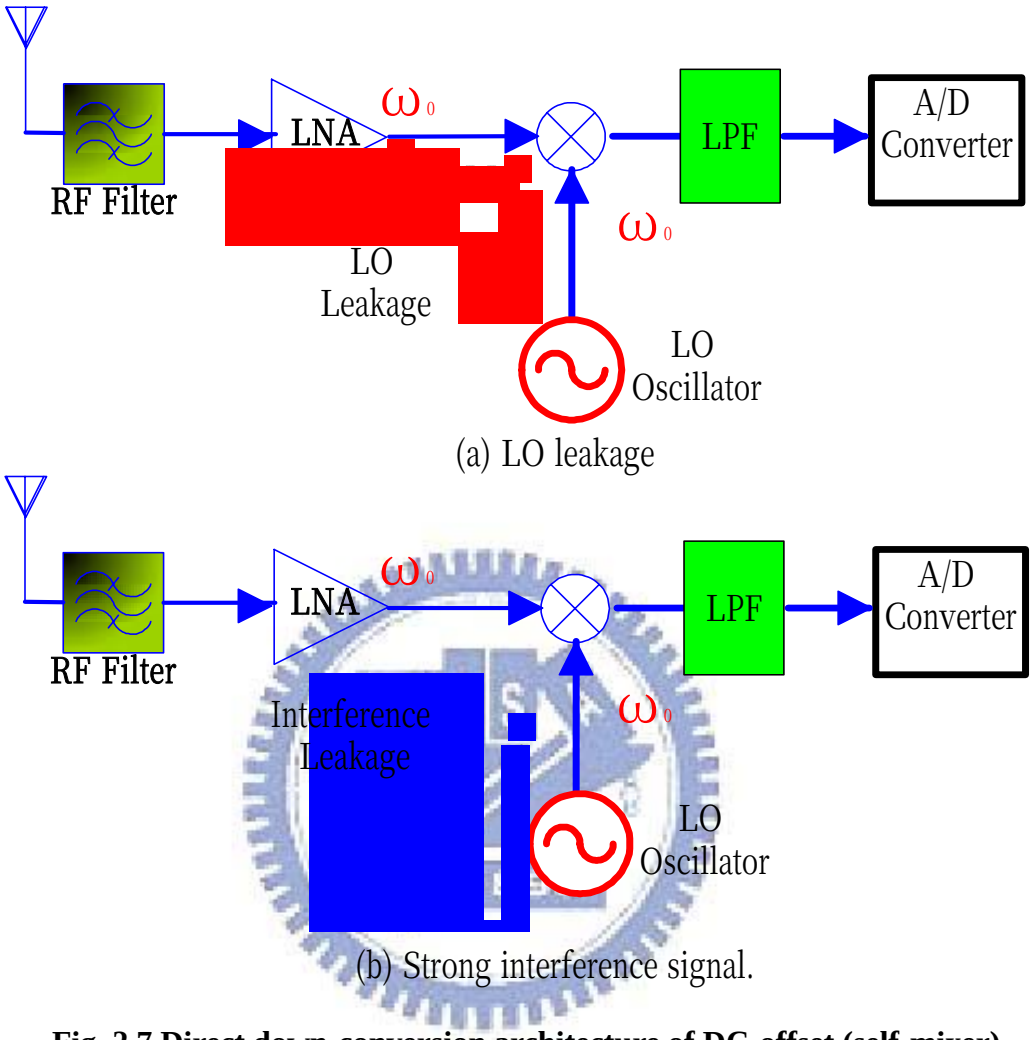
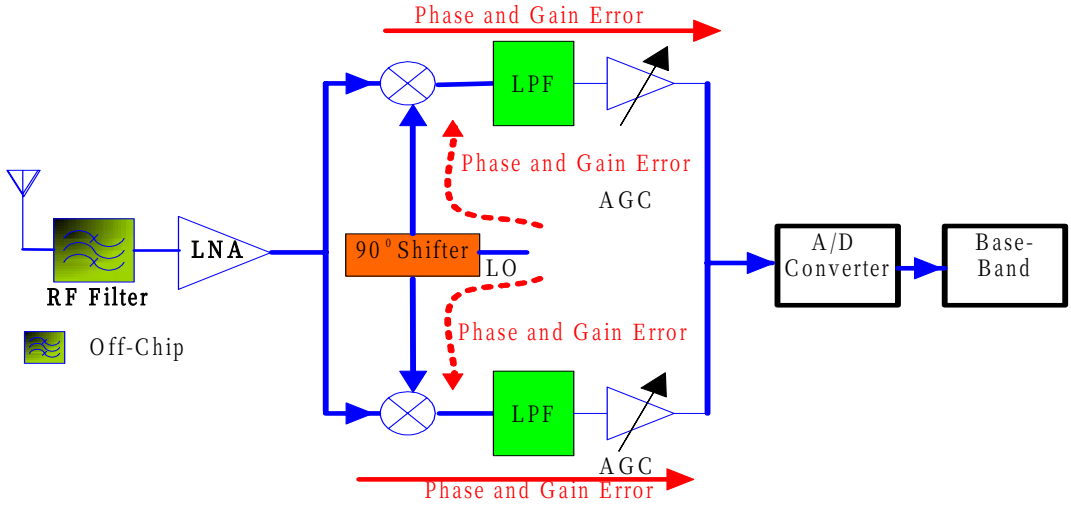


Fig. 2.7 Direct down-conversion architecture of DC-offset (self-mixer).

(b). I/Q Mismatch

The mixer is input LNA RF signal and LO port signal. IF both signals phase mismatch condition, causing down-converters signal constellation distortion, increasing the bit error rate. Figure 2.8 displays the mixer input from LNA RF input signal and local signal input contributions of gain, phase error, and above makes I/Q mismatch QPSK signal constellation.



(a) I/Q mismatch contributions by several stages

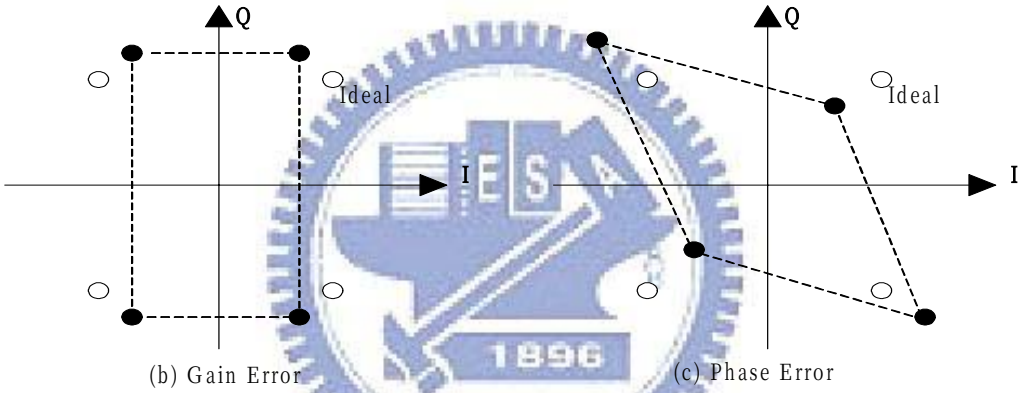


Fig. 2.8 I/Q mismatch contributions for difference stage and on QPSK signal constellation.

(c). Even-Order Distortion

The low noise amplifier (LNA) may cause even-order distortion interference adjacent to the IF channel, as shown in Fig. 2.9. The second term harmonic interferes with the zero-IF signal.

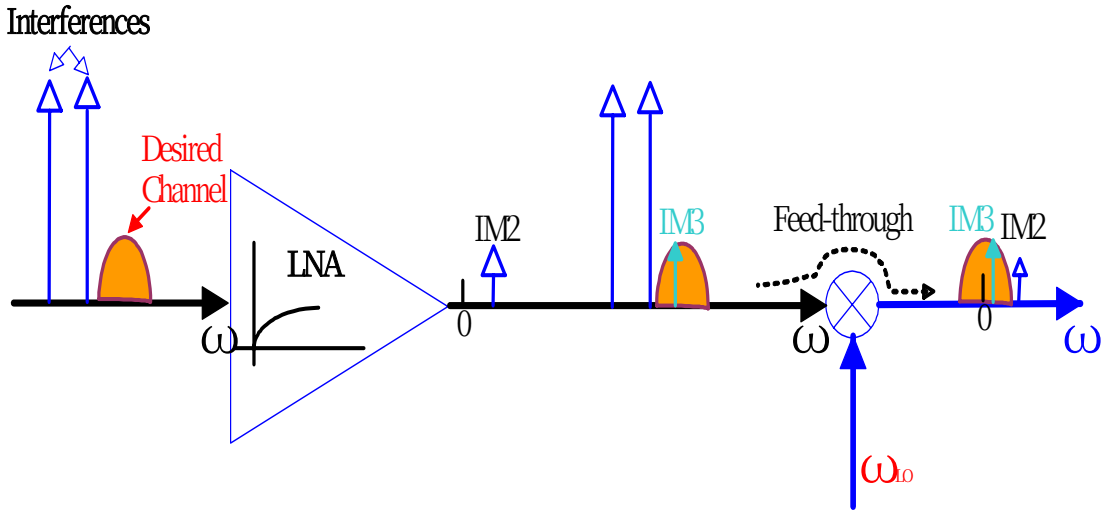


Fig. 2.9 Even-order distortion on interferes.

(d). Flicker Noise

The homodyne down-conversion spectrum is extended to zero frequency. Hence, in the homodyne architecture, low-frequency noise of the device generally approaches a function proportional to 1/f and named as flicker noise. The flick noise dominates in low frequency region and degrades the signal-to-noise ratio (SNR).

2.1.3 Comparison of the receiver architectures

Table 2 lists the key features for a receiver and makes comparison between heterodyne and homodyne receiver architectures.

Table 2.1 Comparison of Heterodyne and homodyne receivers architecture

Receiver Architecture / Comparison Item	Heterodyne receiver	Homodyne Receiver
Frequency conversions	Twice or More	Once
Channel Filter	IF	Base-Band
Required Discrete Filter	RF, Noise, IF	RF
Required High Q filter	Yes	No
Monolithic integration base-band to signal chip (SoC)	Very Difficult (More passive component)	Suitable
IF Selection	Base on system design specification.	Zero IF
Mainstream	Implement to commercial product.	Researching…

2.2 Design Parameters and Non-ideality

For a down-conversion mixer design, the key performance parameters, such as linearity by gain compression (P-1dB) and third-order intercept (IP3), sensitivity, noise figure, dynamics range, and conversion gain, will be considered and discussed in the following sections.

2.2.1 Linearity

Most of systems approximated as linear systems under sufficiently low power actually reveal nonlinear characteristics in higher power region. The small signals models used for RF and analog circuits, based on linear approximation are no longer valid under increasing power. The primary effect of nonlinearity is the frequency interference from adjacent channel frequency, which corrupts the desired signal. A strong signal driven RF amplifier or mixer will go into nonlinear region and the nonlinear signal generates an interference frequency, which may influence the desired signal. Therefore, the linearity of the receiver determines the maximum allowable input signal level.

For simplicity, these nonlinear systems are assumed to be memory-less and time-invariant. Taylor's series are used to analyze the nonlinearity.

$$y(t) = \alpha_0 + \alpha_1 x_i(t) + \alpha_2 x_i^2(t) + \alpha_2 x_i^3(t) + \cdots = \sum_{n=0}^{\infty} \alpha_n x_i^n(t) \qquad (2.7)$$

$$\text{Where} \qquad \alpha_n = \frac{1}{n!}\left(\frac{d^n y(t)}{dx_i^n}\right)\Big|_{x_i=0}$$

Here $x_i(t)$ is the input signal and $y(t)$ is the output signal. Equation (2.7) describes the output DC offset coefficient α_0, $\alpha_1 x_i(t)$ as the first-order term, $\alpha_2 x_i^2(t)$ as the second-order term, and so on. Here, the coefficient α_n is assumed to be independent of frequency and the receiver system can be approxminated as a linear

system provided that the coefficient $|\alpha_{i-1}| > |\alpha_i|$.

Generally, the analytic linearity problem involves a sinusoidal input in Eq. (2.7). Thus, we employ input signal as follows :

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{2.8}$$

Substituting equation (2.8) into (2.7).

$$\begin{aligned} y(t) = {} & \alpha_0 + \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 + \\ & \alpha_3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 + \cdots\cdots\cdots \end{aligned} \tag{2.9}$$

$$\begin{aligned} = {} & \alpha_0 + \alpha_1 (A_1 \cos \omega_1 t + \alpha_1 A_2 \cos \omega_2 t) + \\ & \alpha_2 A_1^2 \frac{1+\cos 2\omega_1 t}{2} + \alpha_2 A_2^2 \frac{1+\cos 2\omega_2 t}{2} + \alpha_2 A_1 A_2 \left[\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t\right] + \\ & \alpha_3 A_1^3 \left(\frac{\cos 3\omega_1 t + 3\cos \omega_1 t}{4} \right) + \alpha_3 A_2^3 \left(\frac{\cos 3\omega_2 t + 3\cos \omega_2 t}{4} \right) + \\ & 3\alpha_3 A_1^2 A_2 \left(\frac{1+\cos 2\omega_1 t}{2} \right) \cos \omega_2 t + 3\alpha_3 A_1 A_2^2 \cos \omega_1 t \left(\frac{1+\cos 2\omega_2 t}{2} \right) + \cdots\cdots\cdots \end{aligned}$$

Listing the fundamental and harmonic second-order and third-order terms gives the following.

The first-order terms with fundamental frequency is expresses by (2.10) and (2.11):

ω_1:

$$\begin{aligned} & \alpha_1 A_1 \cos \omega_1 t + \alpha_3 A_1^3 \left(\frac{3\cos \omega_1 t}{4} \right) + \left(\frac{3}{2} \right) \alpha_3 A_1 A_2^2 \cos \omega_1 t \\ = {} & \left(\alpha_1 A_1 + \frac{3}{4} \alpha_3 A_1^3 + \left(\frac{3}{2} \right) \alpha_3 A_1 A_2^2 \right) \cos \omega_1 t \end{aligned} \tag{2.10}$$

ω_2 :

$$\begin{aligned}&\alpha_1 A_2 \cos\omega_2 t + \alpha_3 A_2^3\left(\frac{3\cos\omega_2 t}{4}\right) + \left(\frac{3}{2}\right)\alpha_3 A_1^2 A_2 \cos\omega_2 t \\ &= \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \left(\frac{3}{2}\right)\alpha_3 A_1^2 A_2\right)\cos\omega_2 t\end{aligned} \tag{2.11}$$

Second-order terms:

$2\omega_1$: $\frac{1}{2}\alpha_2 A_1^2 \cos 2\omega_1 t$ (2.12)

$2\omega_2$: $\frac{1}{2}\alpha_2 A_2^2 \cos 2\omega_2 t$ (2.13)

$\omega_1 \pm \omega_1$: $\alpha_2 A_1 A_2 \left[\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t\right]$ (2.14)

Third-order terms:

$3\omega_1$: $\frac{1}{4}\alpha_3 A_1^3 \cos 3\omega_1 t$ (2.15)

$3\omega_2$: $\frac{1}{4}\alpha_3 A_2^3 \cos 3\omega_2 t$ (2.16)

$2\omega_1 \pm \omega_2$:

$$\begin{aligned}&\frac{3}{2}\alpha_3 A_1^2 A_2 \cos 2\omega_1 t \cos\omega_2 t \\ &= \frac{3}{4}\alpha_3 A_1^2 A_2 \left[\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t\right]\end{aligned} \tag{2.17}$$

$\omega_1 \pm 2\omega_2$:

$$\begin{aligned}&\frac{3}{2}\alpha_3 A_1 A_2^2 \cos\omega_1 t \cos 2\omega_2 t \\ &= \frac{3}{4}\alpha_3 A_1 A_2^2 \left[\cos(\omega_1 + 2\omega_2)t + \cos(\omega_1 - 2\omega_2)t\right]\end{aligned} \tag{2.18}$$

Through the Fourier transformation from time domain to frequency domain, $Y(\omega)$ yields the inter-modulation output spectrum in the frequency domain, as shown in Fig. 2.10.

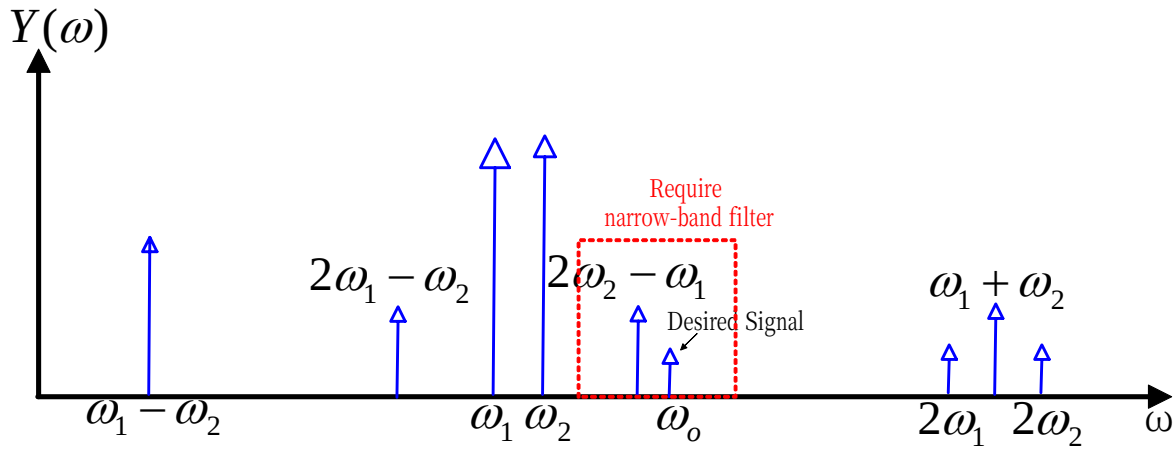


Fig. 2.10 Inter-modulation output spectrum in the frequency domain.

Generally, in RF linear systems, the saturation of conversion gain follows an increase in the input signal, accelerating conversion gain saturation. Equations (2.10) and (2.11) indicate that the amplitude of the desired signal is

$$\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \left(\frac{3}{2}\right)\alpha_3 A_1 A_2^2 \tag{2.19}$$

For $A_1 << A_2$ the gain of the desired signal equals to

$$\alpha_1 + \left(\frac{3}{2}\right)\alpha_3 A_2^2 \tag{2.20}$$

Assume that $\alpha_3 < 0$ (e.g., $\alpha_1 = -\alpha_3$) and that A_2 is sufficiently large, the output conversion gain in Eq. (2.20) can be dropped to zero. Accordingly, the third-order signal corrupts the gain as the input signal amplification increases.

2.2.1.1 P-1dB Gain Compression

As mentioned above, when the strength of the input signal to the amplifier drives the amplifier into saturation, the output signal from the amplifiers will be clamped. As a result, the linearity of a system determines the maximum range allowed

for the input signals to the amplifiers. This amplifier working range is defined by the input signal level at which the small-signal gain drop by 1 dB. This is called the 1dB compression point (P-1dB), as shown in Fig. 2.11.

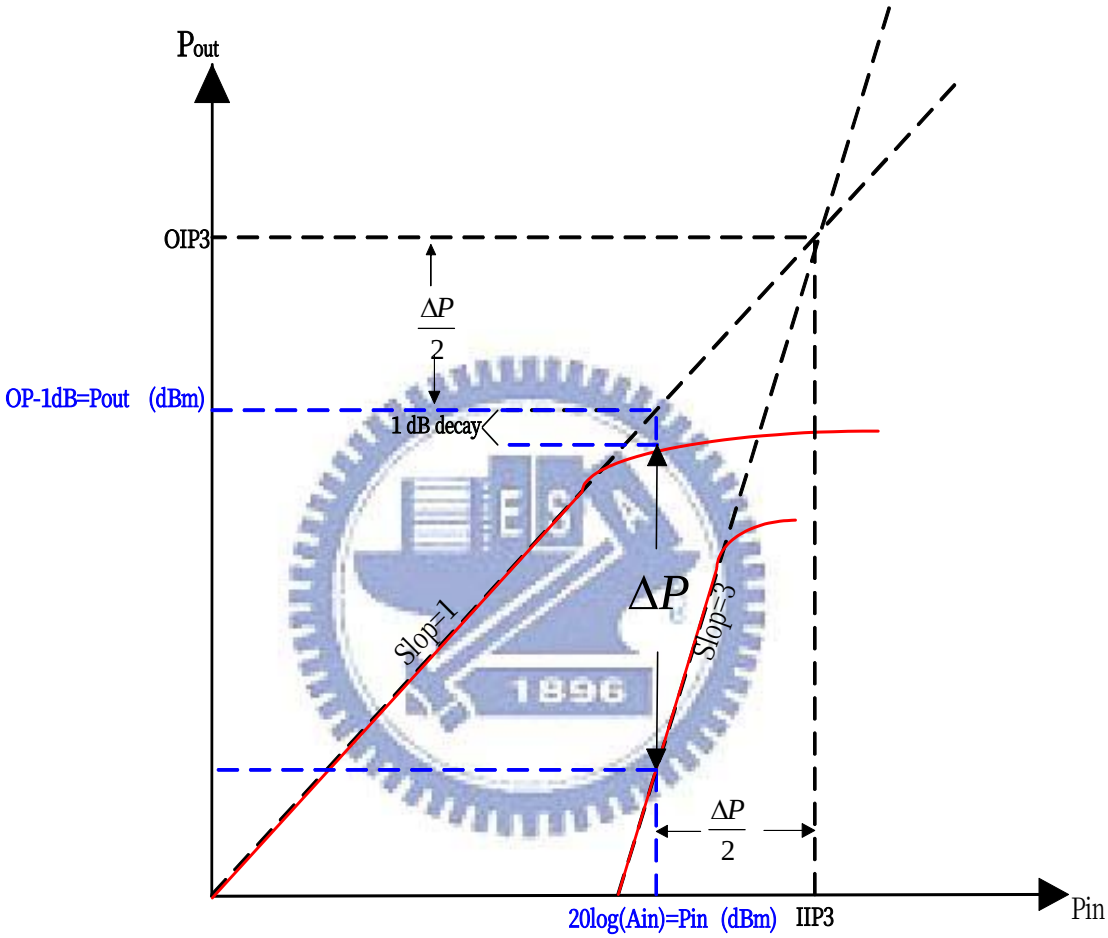


Fig. 2.11 P-1dB compression gain point

To determine 1dB gain compression point, a single tone excitation is carried out. A single input signal is assumed and given by $A_2=0$ in Eq. (2.8). In this case $\alpha_3<0$ (negative) and the second term degrades the gain.

$$\left(\alpha_1 A_1+\frac{3}{4}\alpha_3 A_1^3\right)\cos\omega_1 t=\left(\alpha_1+\frac{3}{4}\alpha_3 A_1^2\right)A_1\cos\omega_1 t \qquad (2.21)$$

The 1dB compression point is define as the input power level at which the

output power drops by 1 dB.

$$\alpha_1\big|_{dB} - 1dB = \alpha_1 + \frac{3}{4}\alpha_3 A_{1dB}^2$$

$$\Rightarrow 20\log\alpha_1 - 20\log 10^{1/20} = 20\log\left(\alpha_1 + \frac{3}{4}\alpha_3 A_{1dB}^2\right)$$

$$\Rightarrow \frac{\alpha_1}{1.122} = \alpha_1 + \frac{3}{4}\alpha_3 A_{1dB}^2 \Rightarrow -0.10873\,\alpha_1 \approx \frac{3}{4}\alpha_3 A_{1dB}^2$$

$$\Rightarrow A_{1dB} = \sqrt{0.1449\frac{|\alpha_1|}{|\alpha_3|}} \qquad (dBV) \qquad (2.22)$$

Equation (2.22) does not take into account the high-order harmonic terms. Due to the fact, the actual P-1dB compression point value is generally below what expected from Eq. (2.22).

Most of the measured P-1dB are expressed in dBm. dBm is an absolute unit of RF power. Therefore, dBV is converted to dBm. dBm is defined as a power dissipation of 1 mW at a characteristic impedance of 50 Ω in a system.

Hence,

$$\Rightarrow dBm = 10\log\left(\frac{Power}{1mW}\right) = 10\log\left(\frac{V_{rms}^2/50\Omega}{1mW}\right) = 10\log\left(\frac{V_{rms}}{\sqrt{0.001\cdot 50}}\right)^2$$

$$= 20\log(V_{rma}) - 20\log(0.05)^{1/2} = dBV + 13.01 \qquad (dBm) \qquad (2.23)$$

2.2.1.2 Third–order Intercept Point (IP3)

A receiver cannot remove two adjacent interfering signals using a filter, as

presented in Fig. 2.10. The narrow band filter design is not simple. Signal interference produces an inter-modulation of signals, affecting the RF system. The inter-modulation signal degrades system performance, and the bit error increases after demodulation.

The third-order intercept point is determined by a two-tone test, as shown in Fig. 2.12. The two-tone test is generally employed to identify adjacent channel frequency interferences, caused by the signal reciprocal effects of internal components. Two sinusoidal waves with frequencies of ω_1 and ω_2 are applied to an amplifier. Equation (2.8) is substituted into Eq. (2.6). The third-order terms are given by Eqs. (2.17) and (2.18) and the third-order intercept is plotted in Fig.2.11.

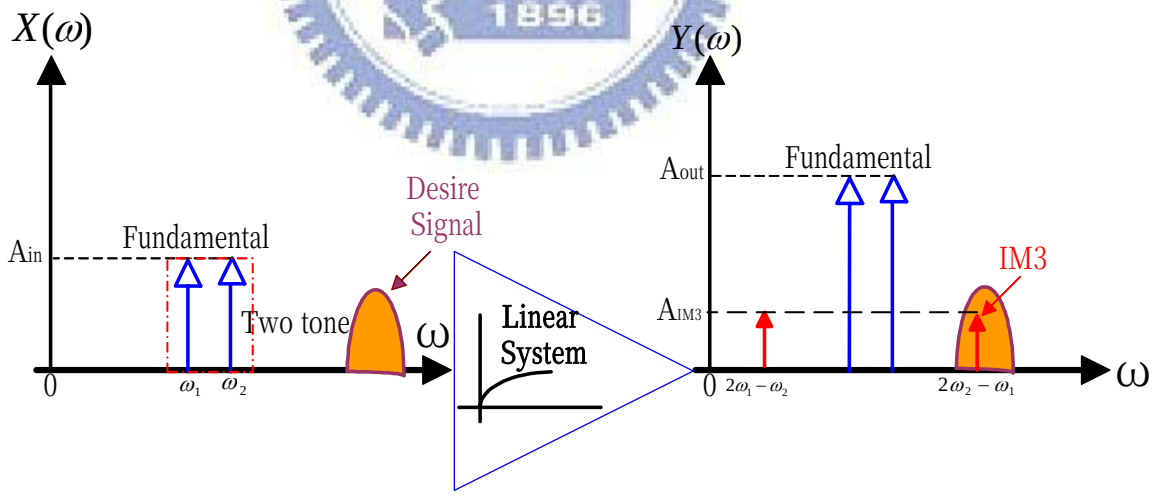


Fig. 2.12 Third-order inter-modulation between two tone interferences.

As shown in Fig. 2.11, the third-order intercept point terms are set across equal to the first-order point terms. Setting $A_1=A_2=A$ in Eq. (2.17), and equating the coefficient $\alpha_1 A_1$ to $\alpha_1 A_{IIP3}$, yields,

$$\alpha_1 A_{IIP3} = \frac{3}{4}\alpha_3 A_{IIP3}^3 \tag{2.24}$$

$$\Rightarrow A_{IIP3} = \sqrt{\frac{4}{3}\frac{|\alpha_1|}{|\alpha_3|}} \qquad (dBV) \tag{2.25}$$

Comparing Eq. (2.22) with Eq. (2.25) yields

$$\frac{A_{IIP3}}{A_{1dB}} = \frac{\sqrt{\frac{4}{3}\frac{|\alpha_1|}{|\alpha_3|}}}{\sqrt{0.1449\frac{|\alpha_1|}{|\alpha_3|}}} = \sqrt{\frac{\frac{4}{3}\frac{|\alpha_1|}{|\alpha_3|}}{0.1449\frac{|\alpha_1|}{|\alpha_3|}}} = 9.201 \tag{2.26}$$

$$\Rightarrow 20\log(A_{IIP3}) - 20\log(A_{1dB}) = 20\log(9.201) \cong 9.64 \quad (dB)$$

Hence, IIP3 is related to P-1dB by the equation as follows,

IIP3 = 1dB compression point + 9.64 dB (2.27)

The graphic shown in Fig. 2.11 can be used to calculate the input and output third-order intercept points given by (2.28) and (2.29) for IIP3 and OPI3, respectively.

$$IIP_3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm} \tag{2.28}$$

$$OIP_3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{out}\big|_{dBm} \tag{2.29}$$

2.2.1.3 Sensitivity

The sensitivity of an RF receiver system is determined by the minimum signal level that the receiver system can detect under an acceptable signal-to-noise ratio. Mathematically, the noise figure (NF) is defined as

$$NF \equiv \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{SNR_{out}} = \frac{S_{in}N_{out}}{S_{out}N_{in}} \tag{2.30}$$

where S_{in} and N_{in} represent the input power and the source resistance noises per unit

bandwidth. $S_{out} = G \cdot S_{in}$ and G is the power gain. The channel bandwidth (BW) is across the overall signal.

Therefore, the input signal power across the channel bandwidth is obtained by rewriting Eq. (2.30) as,

$$S_{in} = SNR_{out} \cdot N_{in} \cdot NF \cdot BW \tag{2.31}$$

Taking logarithms gives,

$$S_{in,\min}\big|_{dBm} = SNR_{\min}\big|_{dB} + N_{in}\Big|_{dBm/Hz} + NF\big|_{dB} + 10\log(BW) \tag{2.32}$$

Equation (2.32) predicts the sensitivity performance from the output SNR. The receiver input system is assumed to exhibit conjugate matching at the input; N_{in} is obtained as the thermal noise power :

$$N_{in} = \frac{4kTR_s}{4} \cdot \frac{1}{R_{in}} = kT = -174 \quad dBm/Hz \tag{2.33}$$

where T is the absolute room temperature (^{o}K) and N_{in} at 300^{o}K is equal to –174 dBm/Hz .

Thus, the minimum input power $S_{in,min}$ is derived as

$$S_{in,\min} = -174 \quad dBm/Hz + NF + 10\log(BW) + SNR_{\min} \tag{2.34}$$

In Eq. (2.34), the sum of the first three terms is sometimes called the “ noise floor ”, which is generally employed to define the dynamic ranges, such as SFDR and BDR in the following section. Since $SNR_{\min}$ is a function of the bandwidth, the noise floor is determined by setting $SNR_{\min}$ in Eq. (2.34) to zero.

2.2.1.4 Dynamic Range

The dynamic range (DR) is defined as the ratio of the maximum allowed input signal level to the minimum input signal level at which the signal quality is maintained [2], [3]. Two definitions of dynamic range are adopted to evaluate the dynamic performance, as shown in Fig. 2.13. These are called spurious-free dynamic range (SFDR) and blocking dynamic range (BDR). For both definitions of dynamic range, the minimum boundary is defined as the noise floor plus $SNR_{\min}$. The spurious-free dynamic range (SFDR) and blocking dynamic range (BDR) are interpreted as follows.

(a). Spurious-free dynamic range (SFDR).

The upper bound of SFDR is defined as an input two-tone test signal at which the third-order inter-modulation (IM3) distortion products do not exceed the noise floor, as displayed in Fig. 2.14.

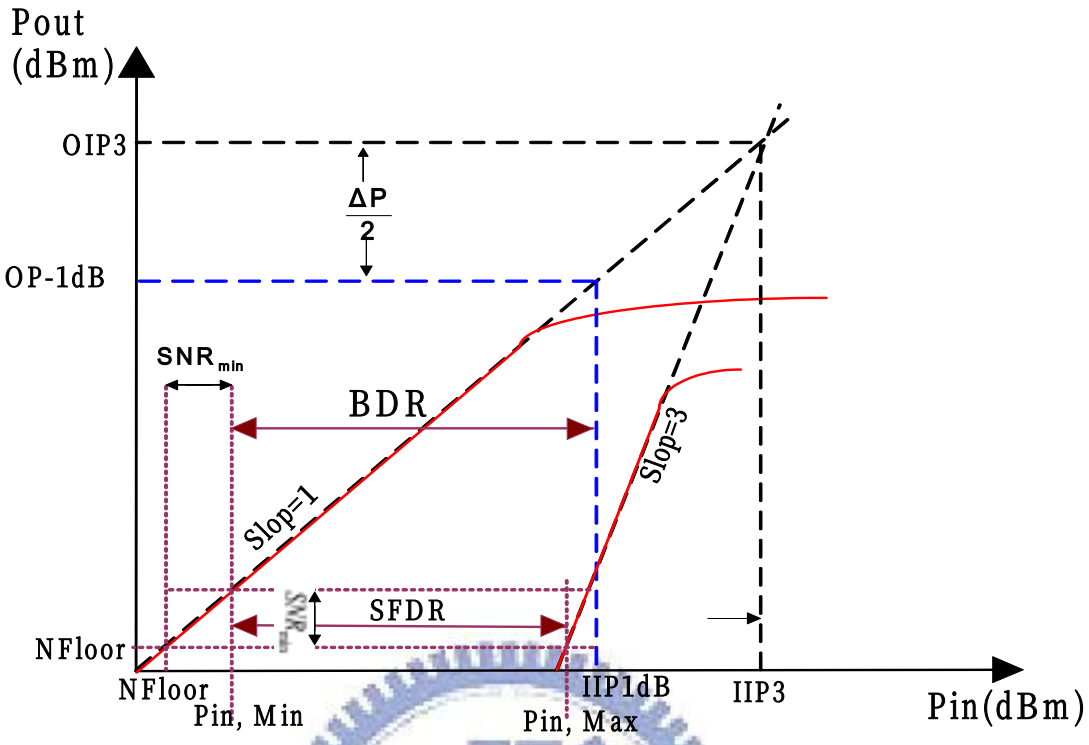


Fig. 2.13 SFDR and BDR defined by the noise floor and linearity parameters.

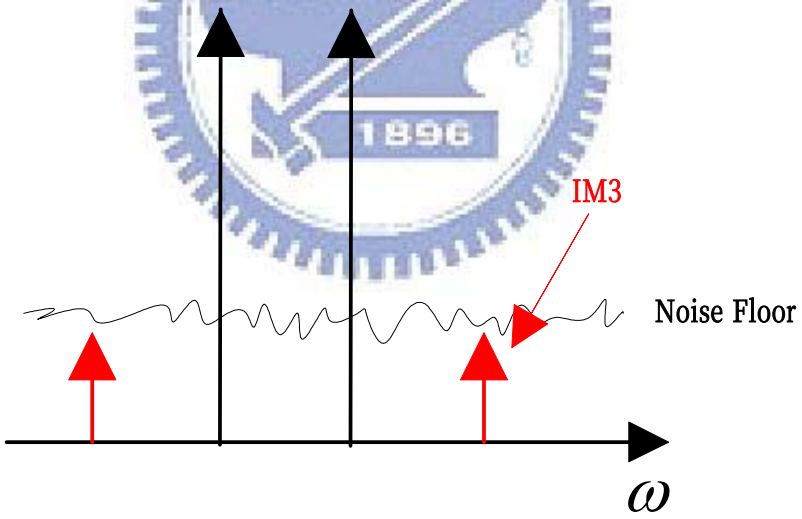


Fig. 2.14 Upper band of SFDR

From Eqs. (2.9) and (2.17), a quick calculation of IM3 is,

$$\frac{A_{\omega 1,\omega 2}}{A_{IM3}} \approx \frac{|\alpha_1| A_{in}}{3|\alpha_3| A_{in}^3 / 4} = \frac{4|\alpha_1|}{3|\alpha_3|} \frac{1}{A_{in}^2} \tag{2.35}$$

Substituting Eq. (2.25) into Eq. (2.35) and taking logarithms, yields,

$$\frac{4|\alpha_1|}{3|\alpha_3|}\frac{1}{A_{in}^2}=\frac{A_{IIP3}^2}{A_{in}^2} \tag{2.36}$$

where A_{in} is the input level at each frequency.

$$\begin{aligned} &20\log(A_{\omega 1,\omega 2})-20\log(A_{IM3})=20\log(A_{IIP3}^2)-20\log(A_{in}^2) \\ &\Rightarrow 20\log A_{IIP3}=\frac{1}{2}\left[20\log(A_{\omega 1,\omega 2})-20\log(A_{IM3})\right]+20\log(A_{in}) \end{aligned} \tag{2.37}$$

Thus,

$$IIP3=\frac{P_{out}-P_{IM,out}}{2}+P_{in} \tag{2.38}$$

$P_{IM,out}$ represents the power of the IM3 components at the output.

Since $P_{out}=P_{in}+G$ *and* $P_{IM,out}=P_{IM,in}+G$, where G is the circuit gain,

$$IIP3=\frac{3P_{in}-P_{IM,in}}{2} \tag{2.39}$$

The input level for the IM products should become equal to the noise floor.

Thus,

$$IIP3=\frac{3P_{in,\max}-P_{nf}}{2} \quad \Rightarrow \quad P_{in,\max}=\frac{P_{nf}+2\cdot IIP3}{3} \tag{2.40}$$

The relationship between SFDR and SNR_{min} is thus obtained.

$$\begin{aligned} &SFDR=\frac{2IIP3+P_{nf}}{3}-(P_{nf}+SNR_{\min}) \\ &\Rightarrow \quad =\frac{2(IIP3-P_{nf})}{3}-SNR_{\min} \end{aligned} \tag{2.41}$$

(b). Blocking dynamic range (SFDR)

The upper boundary of BDR is the P-1dB compression point, and the overall gain declines to zero since the small signal gain is attenuated by large interference. Figure 2.13 is used to obtain the equation for calculating BDR.

$$BDR = P_{-1dB} - P_{nF} - SNR_{\min} \tag{2.42}$$

Attempt to find out the relationship between SFDR and BDR.

Equations (2.26) and (2.41) are manipulated to yield, .

$$P_{-1dB} \cong IIP3 - 9.64dB \tag{2.43}$$

$$IIP3 = \frac{3}{2}(SFDR + SNR_{\min}) + P_{nf} \tag{2.44}$$

Thus,

$$\begin{aligned} & BDR = P_{1dB} - P_{nF} - SNR_{\min} \\ \Rightarrow \quad & = \frac{3}{2}SFDR + \frac{1}{2}SNR_{\min} - 9.64dB \end{aligned} \tag{2.45}$$

Both compression and blocking reduce the desired signal and then SNR is degraded.

Chapter 3.

Design of a 5.5 GHz CMOS Active Mixer

The accuracy of MOSFET model for simulating high frequency characteristic will have direct and dramatic impact on the RF circuit design and performance optimization. A compact CMOS model should cover both active and passive devices, such as MOS transistors, varactors, capacitors, inductors, and resistors. An accurate compact RF CMOS model can help facilitate RF circuit design with increased first-pass success. In this thesis, TSMC 0.18 μm mixed signal 1P6M silicide 1.8V/3.3V RF CMOS models are used in circuit simulation for the design of a new down-conversion mixer. This chapter discusses the trade-off of RF performance with the minimum noise figure (NF_{min}), conversion gain, and linearity.

A CMOS based RF amplifier or mixer circuit design can adopt common source and common gate for high-frequency applications. The common source exhibits a high conversion gain, and wide matching bandwidth in the deep-submicron process. The mixer design focuses on the trade-off between various performance parameters, such as the conversion gain, linearity, and flicker noise in the direct conversion receiver.

3.1 Mixer

In general, the basic mixer architectures can be classified as two major categories, one is the active mixer and another is the passiver mixer. The passive mixer has advantages over the active mixer, such as broadband and high speed due to much smaller junction capacitance, high linearity, dynamic range, and lower flicker noise. However, a passive mixer sometimes suffers disadvantages, such as unsuitability for integration in SoC, inherent conversion loss, poor port-to-port isolation, and high LO power requirement. In the following sections, mixers adopting various topologies will be introduced and discussed.

3.1.1 Passive Mixer

The passive mixer has advantages of high linearity, low noise, and low power. However, the major penalty suffered by the passive mixer is the worse loss in conversion gain.

A passive mixer can utilize MOS transistors or diodes as the basic devices in its circuit architecture. Most of passive diode mixers adopt Schottky diodes as shown in Fig. 3.1(a), mainly because the Schottky diodes represent majority carrier devices, and are faster than p-n junction diodes. MOS transistor is an essential element in active mixers and may be used in passive mixers, as shown in Fig. 3.1(b).

The passive mixer integration in SoC is very difficult since the Balun circuit is

almost passive or includes a center-tapped transformer, whose integration into SoC will occupy a large area on the chip. The passive mixer is generally popular for applications demanding high-linearity, low-noise, and low-power-consumption.

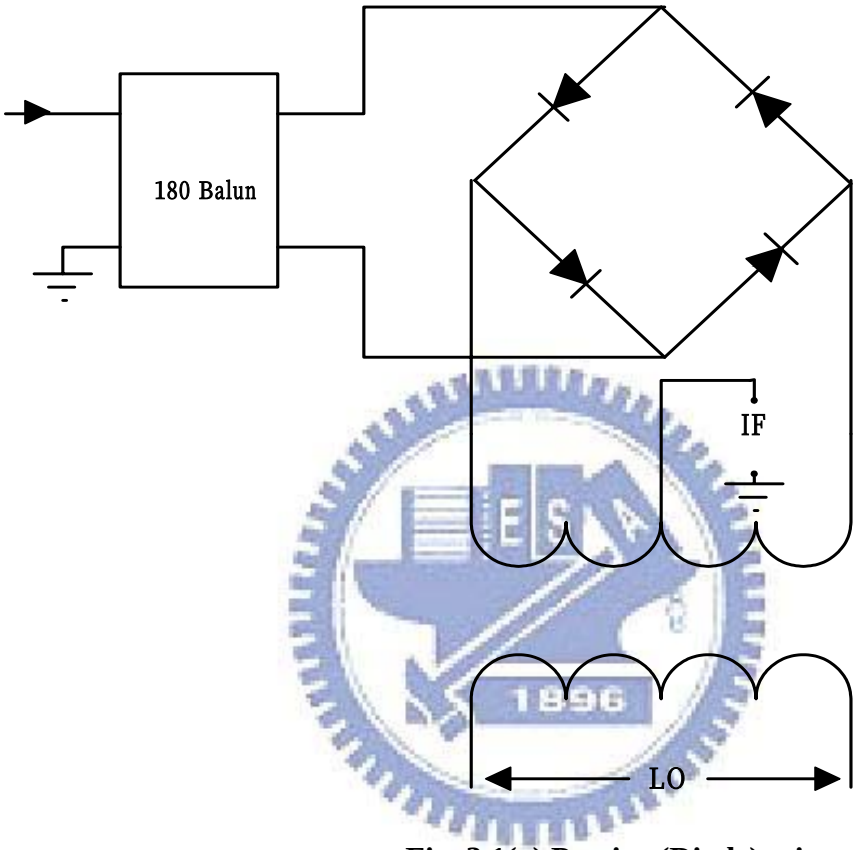


Fig. 3.1(a) Passive (Diode) mixer

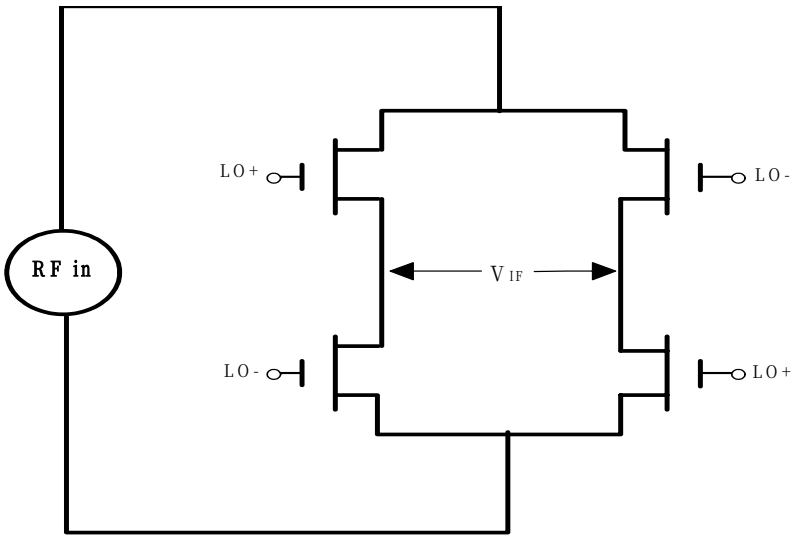


Fig. 3.1(b) Passive (MOS) mixer

3.1.2 Active Mixer

Gilbert cell is the most popular architecture adopted to build an active mixer and the resulted mixer is generally named as a Gilbert mixer. Figure 3.2(a) and (b) show the single and double balanced mixers, respectively. The noise figure of a typical Gilbert mixer circuit is between around 8~15 dB.

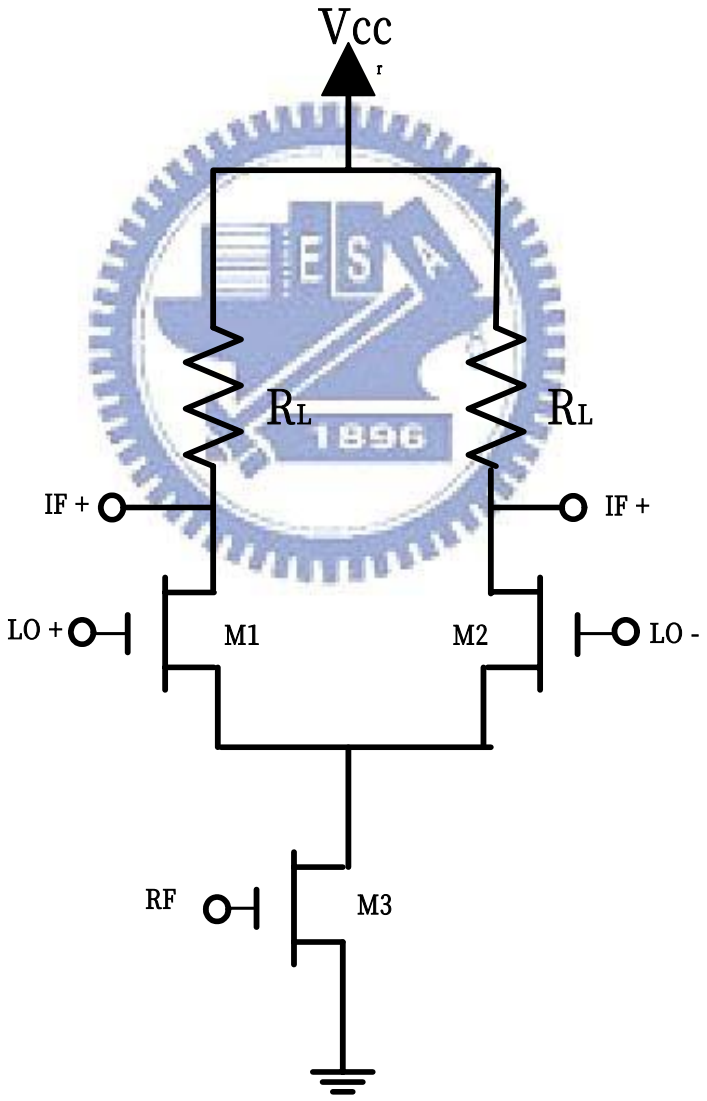


Fig. 3.2(a) Single Balanced Mixer

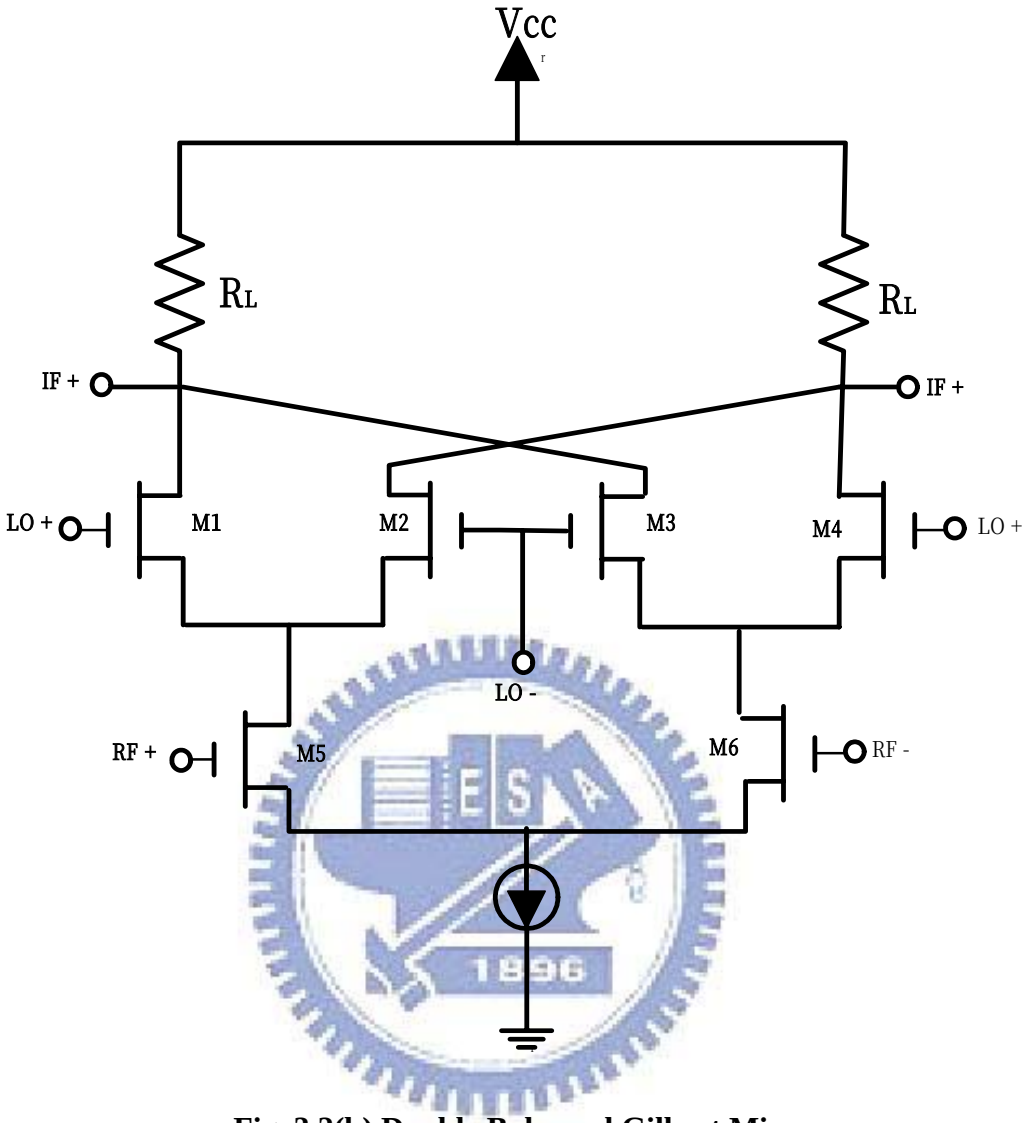


Fig. 3.2(b) Double Balanced Gilbert Mixer

3.2 Design of Low-Power-Consumption Circuit with LC-Tank

The basic circuit topology of a Gilbert mixer is a kind of cascade architectures incorporating RF stage and LO stage. Therefore, the supply voltages required for a Gilbert mixer have to include one set for LO and another one for RF, as shown in Fig. 3.3. A simplified circuit block in Fig. 3.3 illustrates the DC voltage and RF ground

signal through the full lines and dotted lines, respectively. The voltage (V_{cc}) applied to the drain-to-source of each MOS must be at least double the minimum threshold voltage (V_{th_min}), i.e. $V_{cc} > 2\ V_{th\_minthe}$ or minimum active component turn-on voltage (V_{on}), i.e. Vcc > 2 Von, to turn on all active components in normal operation. The standard Gilbert mixer requires a high voltage to maintain all MOS transistors in normal operating region. As a result, this kind of mixers generally suffer large power consumption. The voltage scaling limitation as identified in RF and LO explains the major bottleneck for low power design using the conventional Gilbert mixer. This work presents a low-voltage circuit design technology based on the LC tank for a down-conversion mixer, as show in Fig 3.4. A voltage is applied to turn on the active MOS transistors of the LO and RF circuits based on LC-tank resonance.

Fig. 3.4. shows a simplified circuit block diagram for the proposed low voltage mixer. The LC tank is designed with a target resonance frequency at 5.5 GHz for wireless applications, such as in 802.11a. The new topology can reduce the total supply voltage and keep LO or RF active elements in normal turn-on. Ideally, the passive components such as inductors (L) or capacitors (C) employed in a LC tank have no power consumption. In this way, the proposed circuit topology can help voltage scaling and achieve low power operation. For the circuit topology adopting a LC tank, there is headroom voltage in the DC equivalent circuit. The bypass capacitor

is used to couple the RF signal from the RF MOS transistor output to the LO MOS transistor input and isolate the DC bias between the LO and RF stages. The inductors and capacitors are assumed to be ideal and operate at the targetted RF frequency (ω_{RF}). When the LC-tank operates ideally with a parallel resonant frequency equal to ω_{RF} , its equivalent circuit is like an open circuit for an RF signal. Therefore, the minimum supply voltage can be reduced to a turn-on voltage (V_{on}) of a single transistor, supporting the circuit with a cascade architecture.

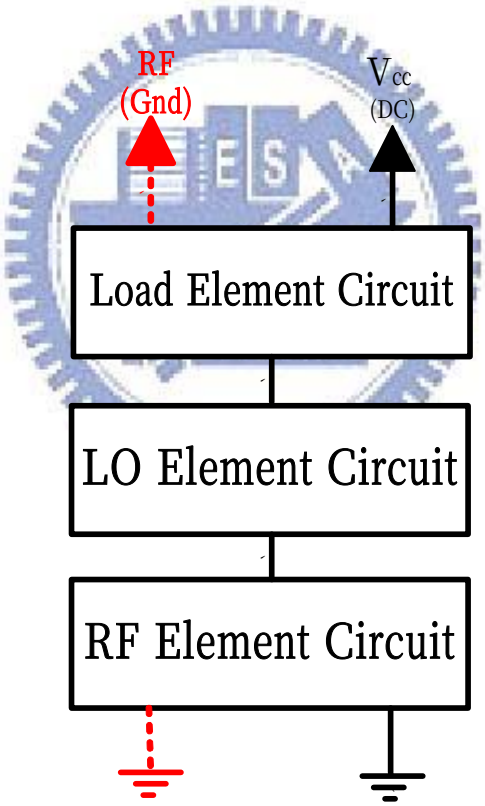


Fig. 3.3 A circuit block diagram for a typical Gilbert mixer with RF, LO, and load stages and the applied DC and RF ground (Gnd).

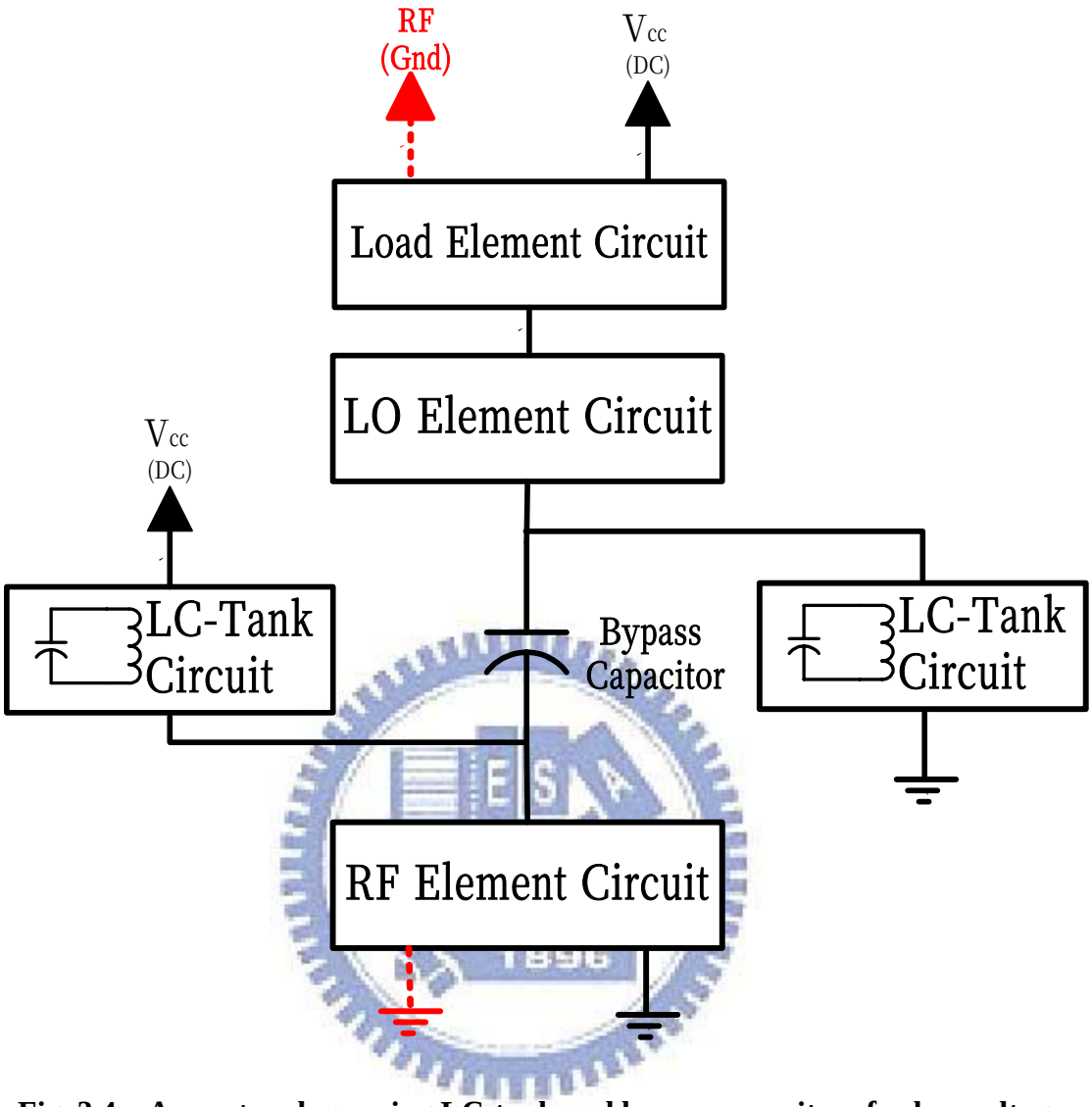


Fig. 3.4 A new topology using LC-tank and bypass capacitors for low voltage operation in a Gilbert mixer with applied DC, RF and RF Gnd.

3.3 5.5 GHz CMOS Down-Conversion Mixer

This section describes the combination of multiple gate MOS transistors at RF input, inductors at RF output, LC tanks at both RF and LO stages, bypass capacitors between RF and LO, and output loading capacitors. The low voltage design built on a CMOS Gilbert cell mixer has been described above. In the following section, the design for down-conversion mixing will be described and discussed.

3.3.1 5.5GHz Down-Conversion Mixer Circuit Block

The 5.5 GHz down-conversion mixer circuit design comprises eight circuit blocks, as shown in Figure 3.5. They are the multiple-gate RF amplifier, the parallel LC-Tank, the bypass capacitor, the local switch, the load circuit, the RF Balun, the LO Balun, and the measuring circuit. QFN package is used to integrate the on-chip and off-chip circuits together.

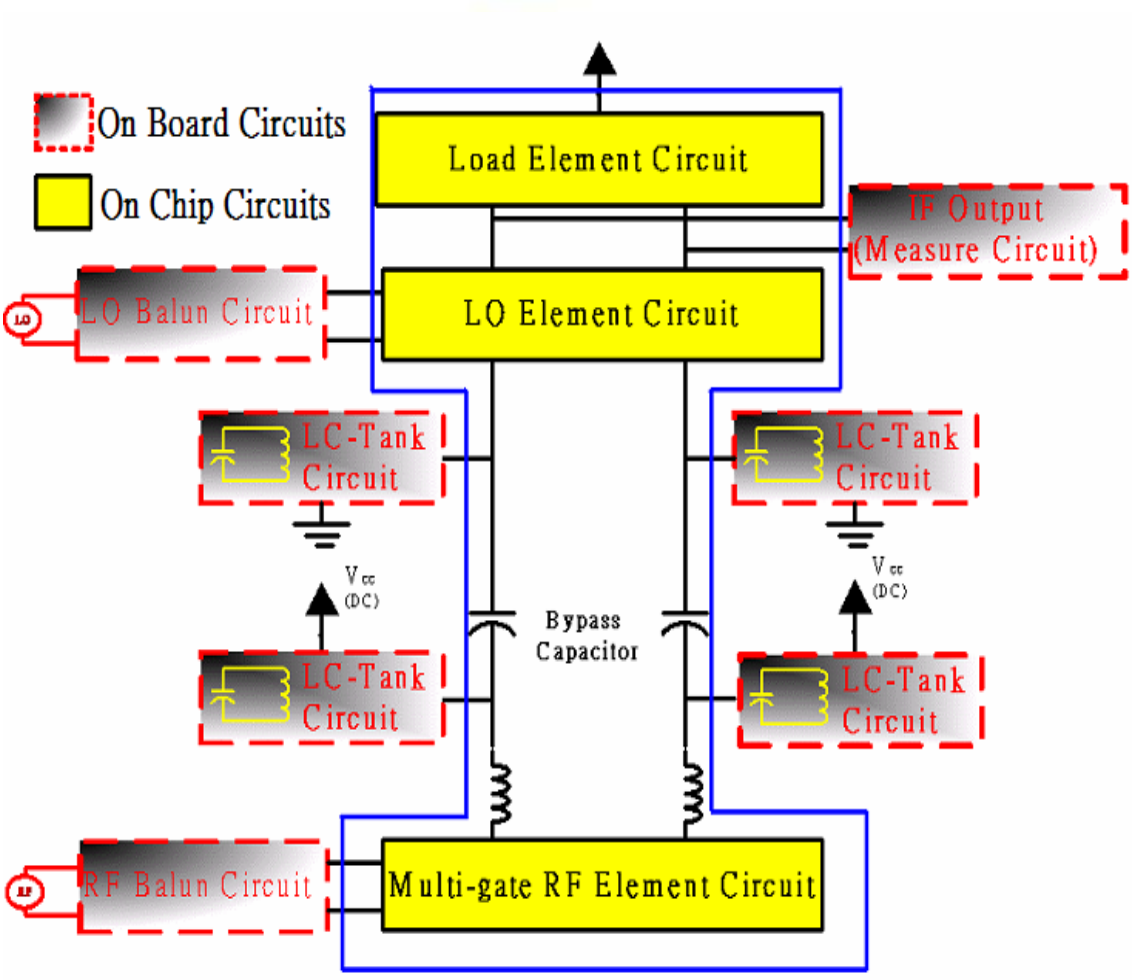


Fig. 3.5 The proposed CMOS RF mixer block

Figure 3.5 presents the on-chip circuit blocks by solid lines blocks and the

off-chip circuit blocks by dotted lines. The off-chip circuits occupy a much larger area than the on-chip circuits. Figure 3.6 displays the whole chip circuit design.

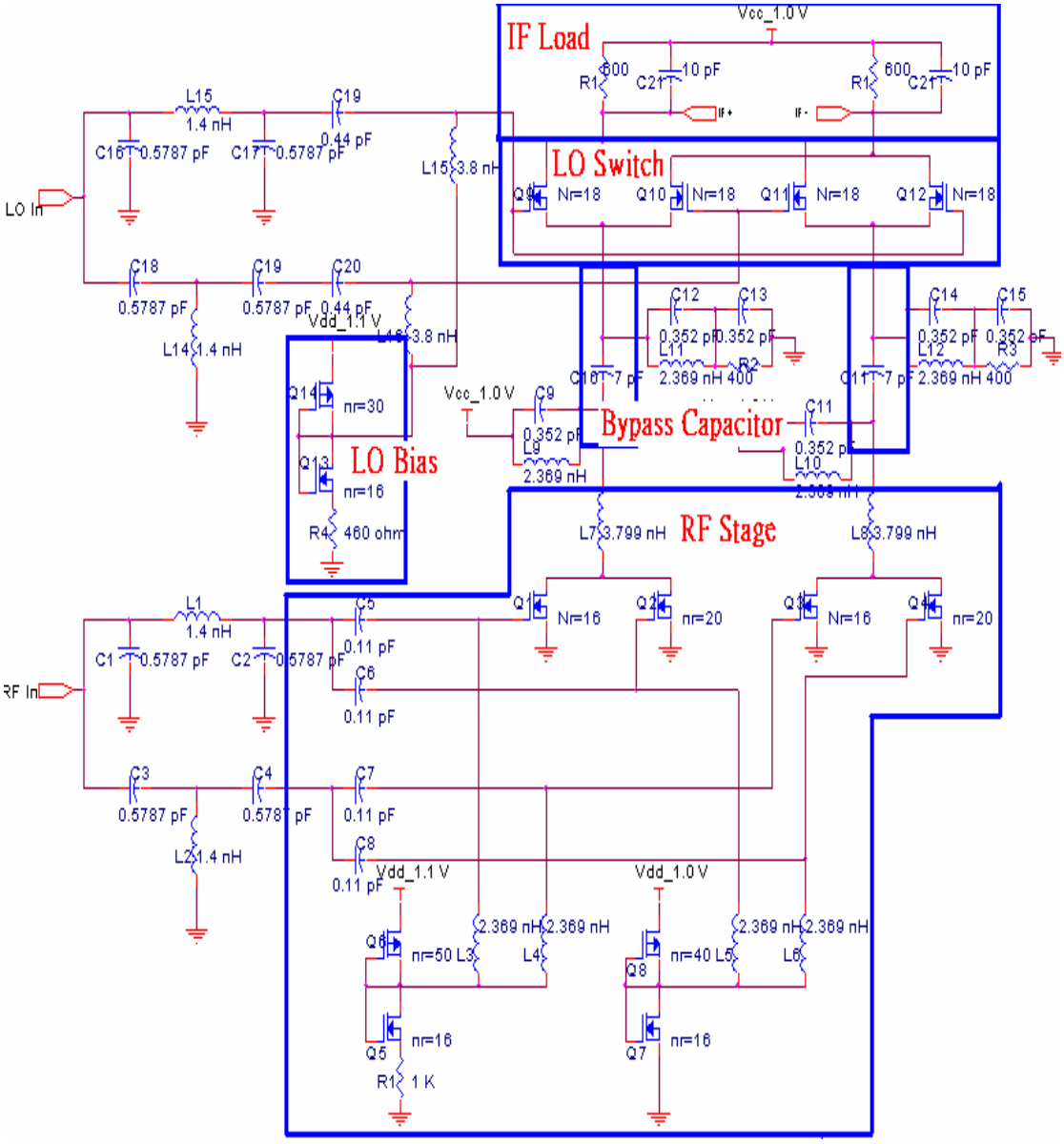


Fig. 3.6 The proposed double balanced RF mixer circuit tolopogies

The CMOS mixer is designed with the low-voltage topology described above. Figures 3.5 and 3.6 are used to represent each circuit block and its function in the proposed RF down-conversion mixer.

3.3.1.1 LC-Tanks

Manku first utilized LC-tanks for low-voltage design and reported the application in RF circuits [4]. In this work, LC tanks were designed with a target resonant frequency of 5.5 GHz, given by $f_o = \frac{1}{2 \cdot \pi \sqrt{L \cdot C}}$. A LC tank, at its resonance frequency, operates like an open circuit, as shown in Fig. 3.8. Therefore, LC-tank circuits may solve the problem generally suffered by the typical cascade circuit. The LC tanks required for this design were implemented by off-chip PCB layouts to meet the chip area constraint defined by CiC for test chip tape-out. For the LC tank design, the L value was determined from the calculated capacitance (C) value 0.352pF at a resonant frequency of 5.5 GHz. This thesis proposes RF output pull-up to supply the source low voltage, and LO pull-down to common ground [5].

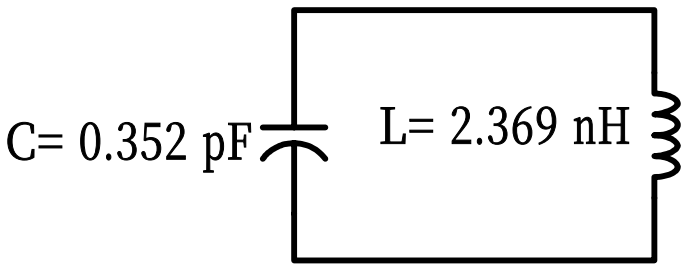


Fig. 3.7 LC-tanks circuits

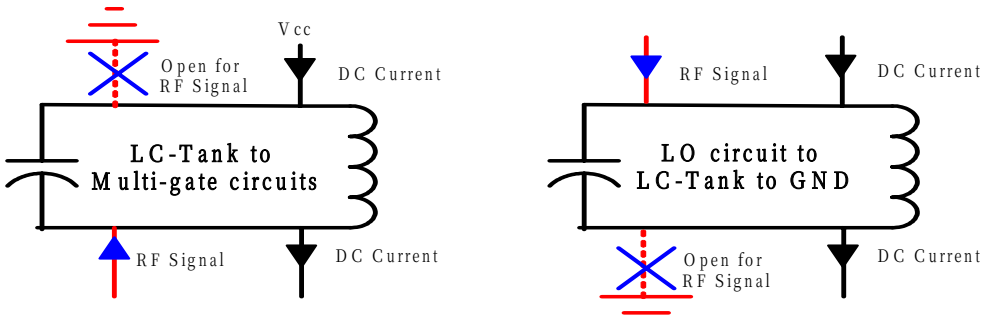


Fig. 3.8 Illustration the LC-tank circuit resonating frequency for RF signal and DC biasing status.

3.3.1.2 Multiple Gate MOS Transistors used in RF Input Stage

For an RF front end amplifier, such as used in LNA and mixer applications, high linearity at low power consumption is very important. Some possible solutions for low power design has been mentioned previously. Many approaches have been developed to compensate for non-linearity. For instance, MOSFET operation in a triode region has been used to improve the linearity of the main RF amplifier [5]. B. Kim proposed a new linearization method that is based on multiple gate transistors for the RF amplifier and the mixer in common source integrated circuits [7].

The linearity of LNA and mixer is generally related to the drain current i_{DS}, as plotted in Fig. 3.9. The linearity model is derived mathematically using Taylor series and Eq. 2.7 is applied to expand the i_{DS} harmonic terms. Eq. 2.7 is rewritten here and i_{DS}, g_m and v_{gs} used instead of $y(t)$, α and $x_i(t)$ [7].

Thus,

$$i_{DS} = \sum_{n=0}^{\infty} \frac{1}{n!} \left(\frac{d^n i_{DS}(t)}{dv_{gs}^n} \right) v_{gs}^n(t)$$

$$= I_{DC} + g_m v_{gs}(t) + \frac{g_m' v_{gs}^2(t)}{2!} + \frac{g_m'' v_{gs}^3(t)}{3!} + \cdots \quad (3.1)$$

The coefficient of v_{gs}^3 is well known to be important in the distortion of third-order inter-modulation (IM3) harmonics of an RF mixer.

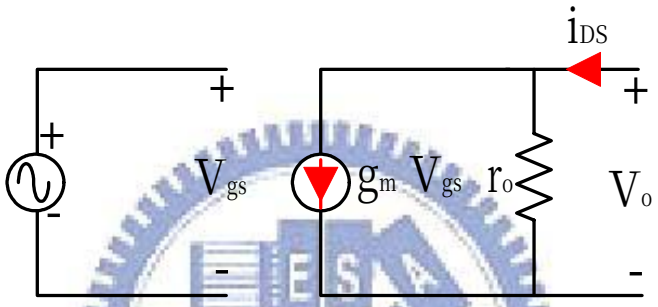


Fig. 3.9 MOSFET small signal model

Figure 3.10 (a) indicates the circuit schematics of a multiple gate topology for circuit simulation to verify its effect on linearity. Fig. 3.10 (b) presents the secondary derivative of transconductances (g_m") of Q1 and Q2, and Fig. 3.10(c) is the effective g_m" as a combination of Q1 and Q2. Sweeping the gate bias (V_{gs}) in the range of interest, the first transistor Q1 contributes negative transconductance $g_{m,Q1}''$ whereas the secondary transistor Q2 presents positive transconductance $g_{m,Q2}''$. Through appropriate tuning on V_{gs} applied to Q1 and Q2, g_m" can be nearly eliminated in a certain region of V_{gs} and the nonlinearity can be reduced. Simulation was carried out to investigate the differences between the single gate and multiple gate structures in

terms of linearity, conversion gain, and power consumption. The comparison results as shown in Fig.3.6 indicate that multiple gate structure can offer better linearity and conversion gain but suffers larger power consumption. A trade-off must be made between the power consumption and linearity. Table 3.1 makes comparison between single gate and multiple gate structures in terms of power consumption, P-1dB, IIP3, conversion gain, single side band noise (SSB), and double side band noise (DSB) predicted by simulation..

Table 3.1 Comparison between the single gate and multiple gate performance

Simulation Item (Without package model) freq=5500 MHz, LO freq=5490 MHZ	Simple Gate	Multiple Gate
Power Consumption	2.51 mW	2.81 mW
Linearity of P-1dB	3.689 dBm	6.188 dBm
Linearity of IIP3	8.2 dBm	12.2 dBm
Conversion Gain	13.318 dB	20.908 dB
Single Side Band Noise (LO=2.5 dBm)	26.571 dB	27.27 dB
Double Side Band Noise (LO=2.5 dBm)	21.748 dB	21.52 dB

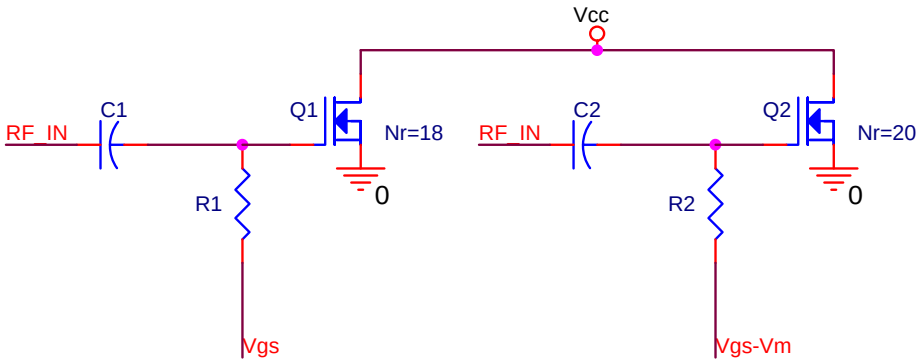
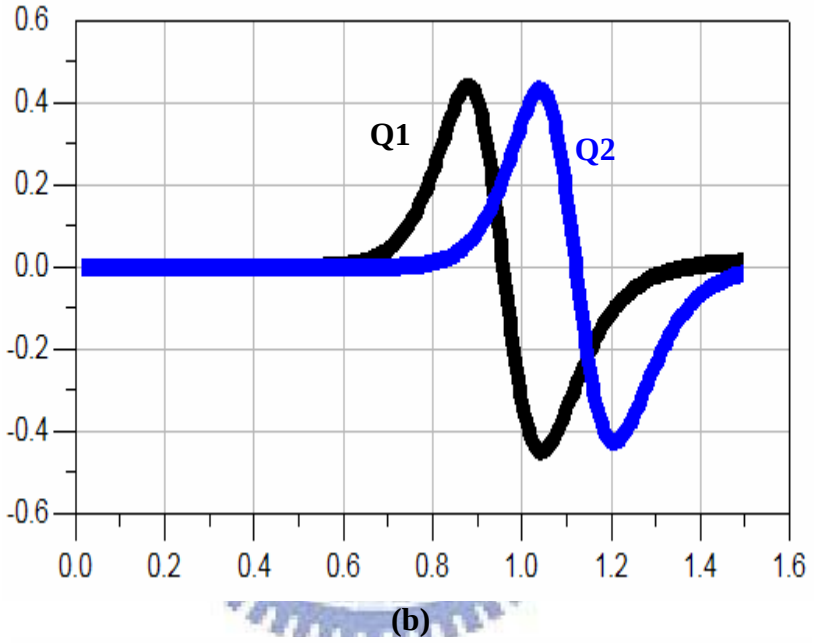
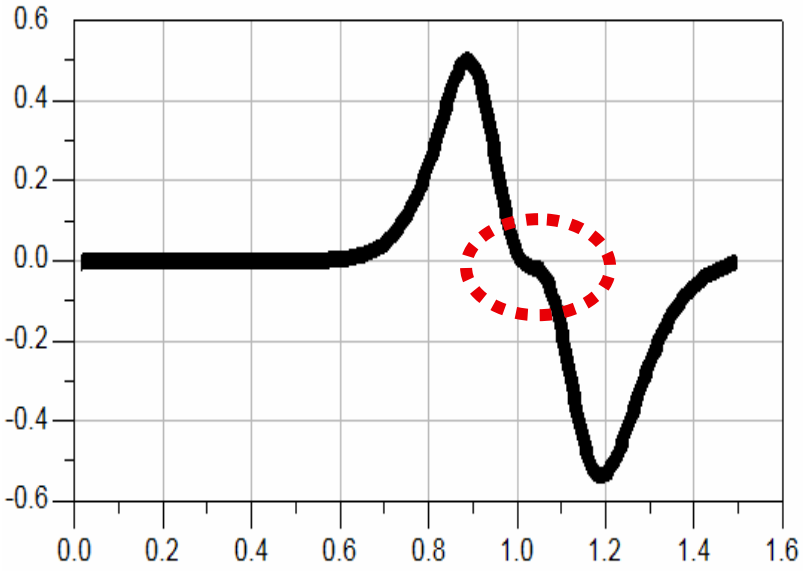


Fig. 3.10 (a) Multiple gated circuit topology.



(b)



(c)

Fig. 3.10 (b) g_m'' of Q1 and Q2 (c) the effective g_m'' resulted from combining Q1 and Q2 to increase linearity

3.3.1.3 RF Output Inductors

An inductor was in series with the RF output to increase the conversion gain available at mixer output [3]. The inductance of around 3.799 nH was adopted to optimize the output matching and improve the conversion gain. Then, the first phase design for RF stage is completed for the downconversion mixer as shown in Fig. 3.5. This circuit design improves the linearity by using multiple gate amplifier at transconductance stage and increases the conversion gain by using inductors at RF output. However, a large chip area consumed by the inductors for output matching becomes a major penalty in terms of cost and chip area utilization.

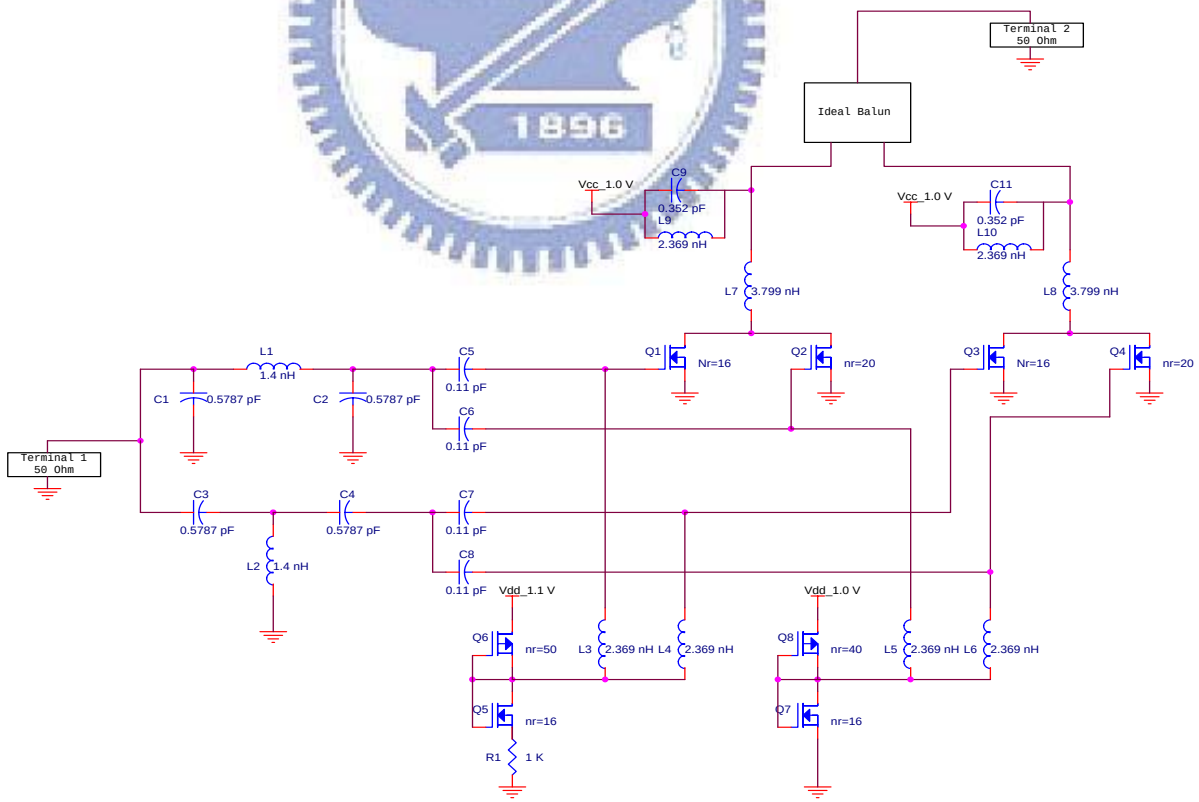


Fig. 3.11 Circuit schematics with RF amplifier, input and output Baluns for simulation and first phase design of the mixer

Figure 3.11 illustrates the circuit schematics for simulation. Fig. 3.12 indicates the input return loss S_{11} and conversion gain S_{21} simulated for the RF amplifier. In this design, the conversion gain S_{21} at 5.5 GHz achieve the maximum value of around 10, and S_{11} can be pushed to around –20 dB.

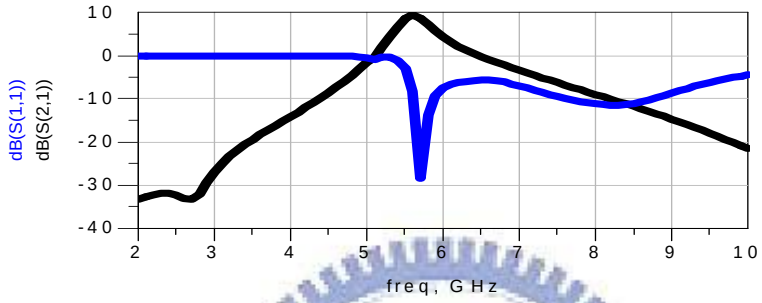


Fig. 3.12. RF amplifier S11, S21 calculated by circuit simulation

3.3.1.4 Balun Circuit Design [5]

Differential (balanced) inputs and outputs generally required for RF ICs can be realized by direct-coupled stages made up of pairs of transistors. These differential inputs and outputs must often be interfaced to single-ended (unbalanced) connections. The deep submicron CMOS process supports high-frequency active devices for RF applications, but the integration of high-quality passive components such as inductors, transformers, resistors and capacitors on a single chip is difficult because that passive devices generally occupy a large area. Although high-quality inductors and transformers have been accurately modeled and Balun applications have been reported [8], [9], the integrated inductor and transformer perform moderately because

of the resistive losses from trace metals and substrate loss associated with the underlying Silicon substrate.

In this section, a lumped element Balun was designed providing an effective solution to RFIC interfacing, which can achieve low cost and less PCB space than alternatives such as a transformer or transmission line Balun [8]. A comparative monolithic transformer with two coupled inductors has a greater quality factor (Q) than LC-Balun in differential circuits [10]. However, an accurate modeling and parameter extraction for monolithic transformers or inductors are more difficult and require more extensive effort and time to achieve accurate measurement and simulation [9].

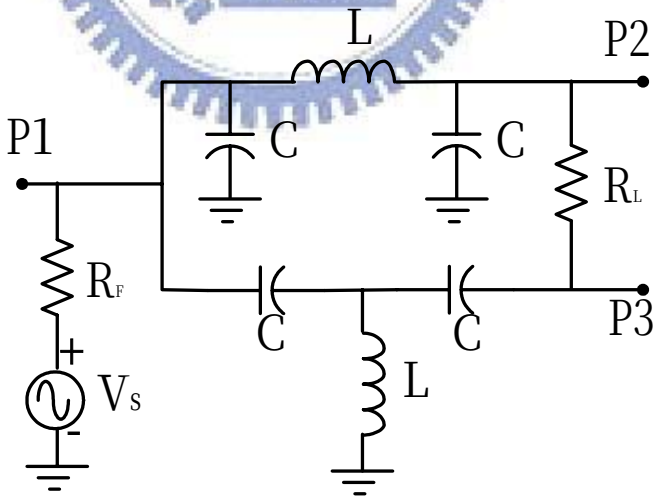


Fig 3.13 RF LC Balun Circuit.

Fig. 3.13 shows the LC Balun circuit applied to RF and LO inputs. It is easily

designed and can be fabricated on-chip or off-chip on PCB. In this thesis, it is implemented on PCB, i.e. an off-chip approach.

A circuit analysis was done on the LC Balun to determine the L and C values. The half-circuit theorem was applied to analyze the LC Balun circuit. In this way, the original LC circuit was partitioned to two identical half circuits, which are symmetric with respect to the source node.The circuit is therefore redrawn as shown in Fig. 3.14.

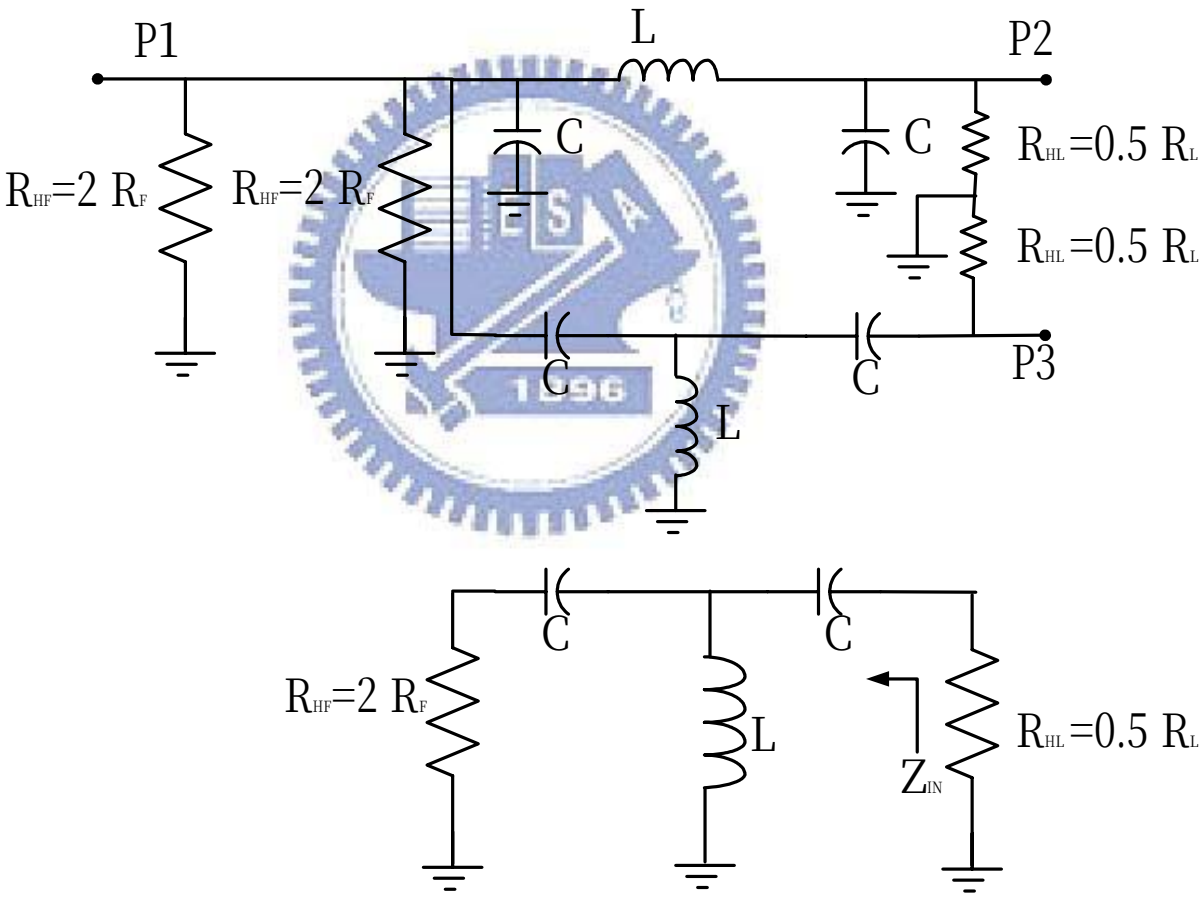


Fig. 3.14 Half-circuit equivalent circuit

Let $Z_{IN}=R_{HL}$ and $X_L = X_C$. Calculate Z_{IN} for the equivalent circuit, as shown in Fig. 3.14.

$$Z_{IN} = (R_{HF} - jX_C) // jX_L - jX_C$$

for $X_L = X_C$

$$(R_{HF} - jX_C) // jX_L - jX_C = \frac{X_L X_C}{R_{HF}}$$

and

$$Z_{IN} = R_{HL}$$

$$\therefore \quad \frac{X_L X_C}{R_{HF}} = R_{HL}$$

(3.2)

Thus,

$$X_C = \sqrt{R_{HF} \cdot R_{HL}} = \sqrt{R_F \cdot R_L} \tag{3.3}$$

The LC Balun circuit is designed for a band frequency of approximately 5.5GHz. Figure 3.15 plots the frequency response of LC-Balun , indicating that the amplitude mismatch is below 0.1 dB and the phase error between port 2 and port 3 is less than $1.5^{o.}$

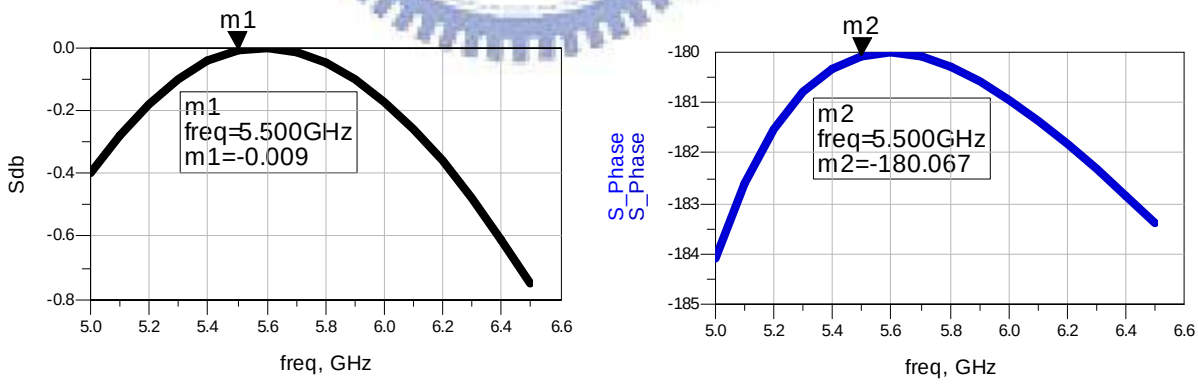


Fig. 3.15 Frequency response of LC-Balun in terms of magnitude error and phase error.

3.3.1.5 LO Switching

RF mixer is a kind of nonlinear circuit applied for wireless communication. The

mixer functions as a multiplication circuit that multiplies the input signal by the LO signal. Therefore, the IF harmonic equation $f_{IF} = mf_{LO} + nf_{RF}$, is obtained where m and n are integers. In this work, a double balanced mixer was adopted to gain better linearity. Gilbert cell mixer was selected as the basic structure to build the switching stage. In the following, an introduction and circuit analysis will be done for single balanced and double balanced mixers, respectively.

3.3.1.5.1 Single Balanced Mixers

A single balanced mixer accommodates a single-ended RF signal and a differential LO signal. The circuit schematics of a single balanced mixer shown in Fig. 3.2(a) is redrawn in Fig. 3.16. The RF signal passes through the M1 transconductor stage, providing an amplified signal that converts a voltage signal to a current signal, and the current signal passes through the current commutating stage M2 and M3 (i.e., switching stage), yielding down-conversion or up-conversion frequency at the IF terminal.

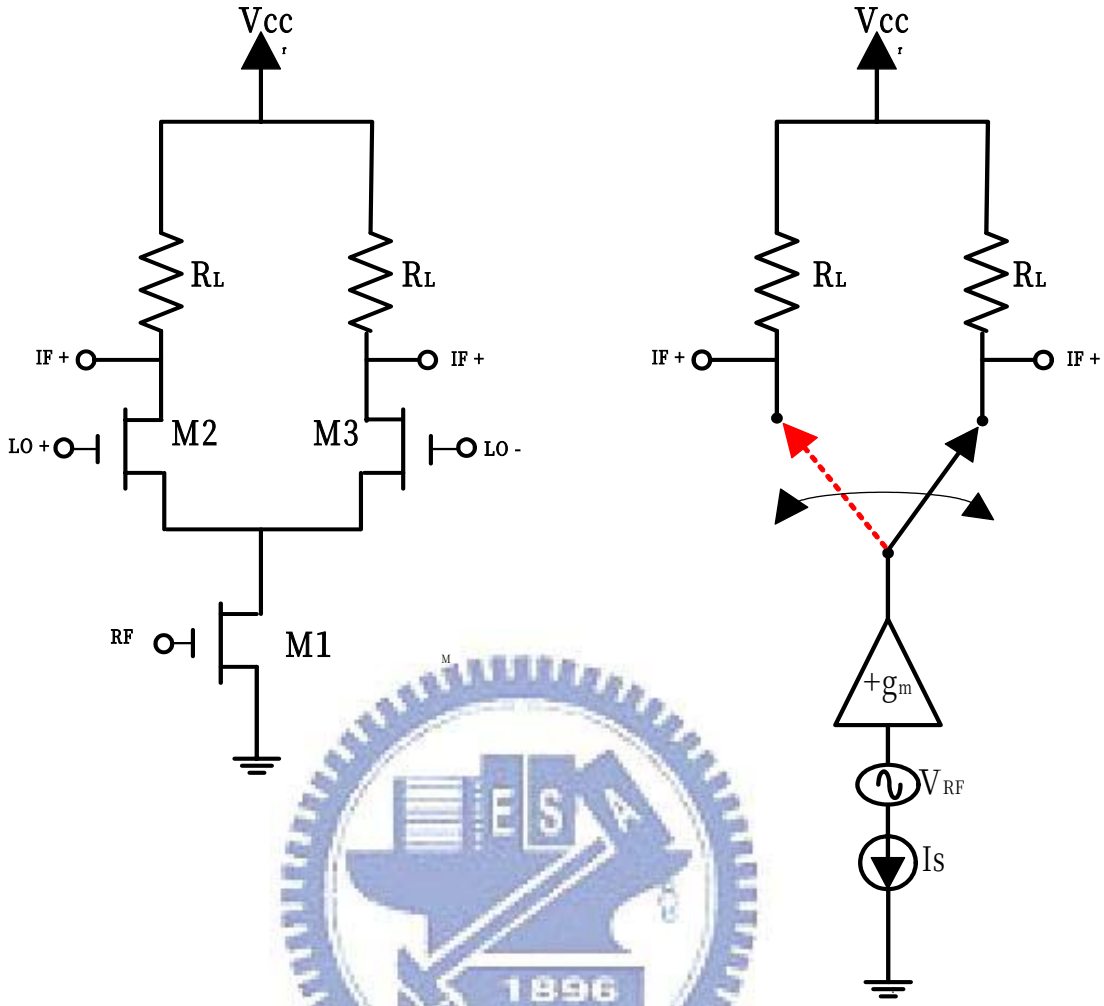


Fig 3.16 Circuit schematics of a single balanced mixer and the equivalent circuit of the LO switch.

The Fourier series is adopted herein to analyze the signal, as shown in Fig. 3.17.

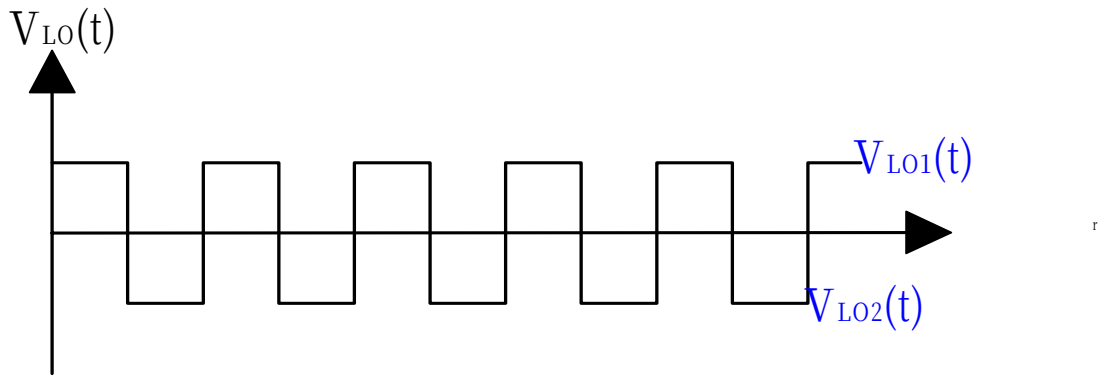


Fig. 3.17 LO switch waveform.

$$V_{LO}(t) = V_{LO1}(t) + V_{LO2}(t) \tag{3.4}$$

$$V_{LO1}(t) = \frac{1}{2} + \frac{2}{\pi}(\sin\omega_{LO}t + \frac{\sin 3\omega_{LO}t}{3} + \frac{\sin 5\omega_{LO}t}{5} + \cdots \quad) \tag{3.5}$$

$$V_{LO2}(t) = \frac{1}{2} + \frac{2}{\pi}(\sin\omega_{LO}t + \frac{\sin 3\omega_{LO}t}{3} + \frac{\sin 5\omega_{LO}t}{5} + \cdots \quad) \tag{3.6}$$

Let RF input signal $V_{RF}(t) = A_R \cos \omega_{RF} t$

Thus,

$$V_o(t) = \frac{4}{\pi} A_R \cos\omega_{RF}t \cdot (\sin\omega_{LO}t + \frac{\sin 3\omega_{LO}t}{3} + \frac{\sin 5\omega_{LO}t}{5} + \cdots \quad) \tag{3.7}$$

If A_R=1, then the single balance circuit has a voltage gain of around 6 dB.

3.3.1.5.2 Double Balance Mixer - Gilbert Cell Mixer

In contrast with the single balanced mixer, a double balanced mixer adopts differential signals at both RF and LO inputs. Fig. 3.18 presents the circuit schematics of a double balanced mixer, so called Gilbert mixer, and the equivalent circuit of the LO switch. The Gilbert cell mixer employs MOSFET differential pair serving as a transconductance amplifier and use four MOSFET realizing the LO switching function. Then, the LO inverse pair switches the down-grade/upgrade RF frequency to the IF terminal. The even-order harmonic frequency interference can be eliminated from the Gilbert cell mixer due to the feature of a differential pair balance architecture.

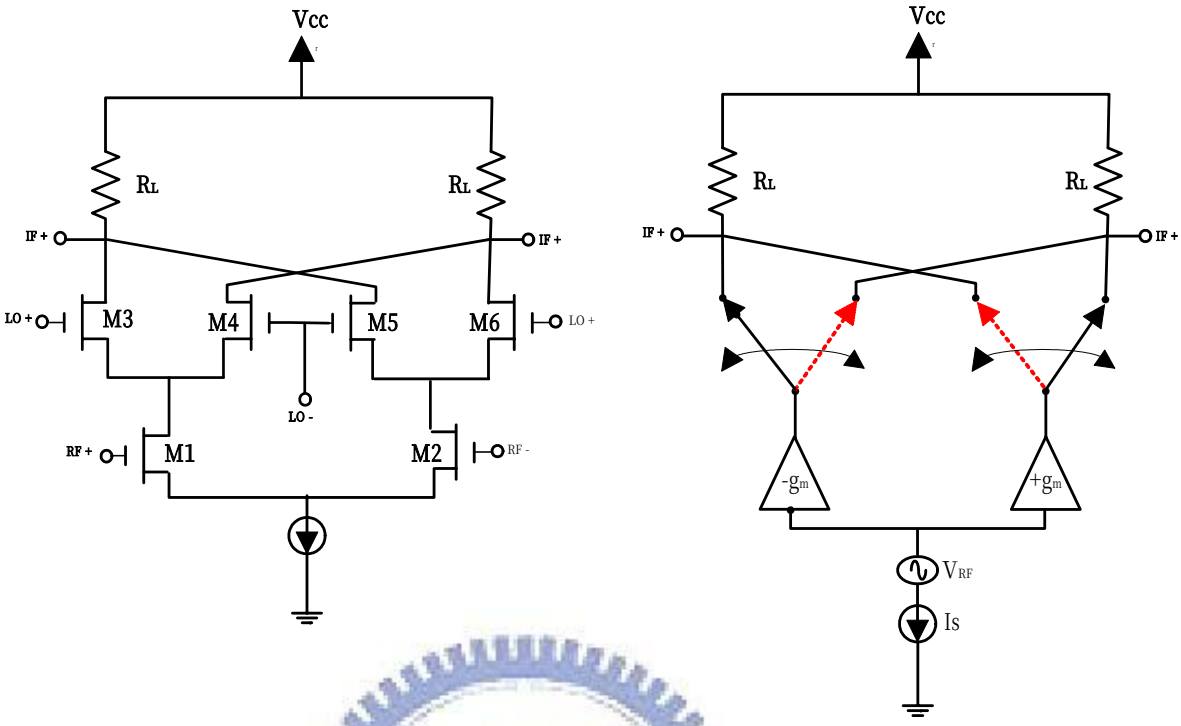


Fig. 3.18 Circuit schematics of a double balanced mixer and the equivalent circuit of the LO switch.

The ideal waveform of the LO switch is a square wave. Figure 3.18 shows the fundamental circuit architecture of an LO switch in a Gilbert cell mixer. All MOS transistors are assumed to work in the saturation region and all transistors to have the same characteristics. The substrate body effect and the output resistance are neglected [11]. The drain currents can be expressed as

$$i_{D1} = \frac{1}{2} k'_{n1} \frac{W_{n1}}{L_{n1}} (v_{GS1} - v_{th})^2 \quad (3.8)$$

$$i_{D2} = \frac{1}{2} k'_{n2} \frac{W_{n2}}{L_{n2}} (v_{GS2} - v_{th})^2 \quad (3.9)$$

$$I_s = i_{D1} + i_{D2} \quad (3.10)$$

here $k_n' = \mu_n C_{ox}$

Let $k_n = \frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}$ (3.11)

Equations (3.8), (3.9) and (3.11) can be rewritten

$$\sqrt{i_{D1}} = \sqrt{k_n}(v_{GS1} - v_{th}) \quad (3.12)$$

$$\sqrt{i_{D2}} = \sqrt{k_n}(v_{GS2} - v_{th}) \quad (3.13)$$

Subtracting Eq. (3.13) from Eq. (3.12) and substituting

$$v_{RF} = v_{GS1} - v_{GS2} = v_{gs1} - v_{gs2} \quad (3.14)$$

where v_{RF} is the RF differential input signal, yields

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{k_n}(v_{GS1} - v_{GS2}) \quad (3.15)$$

$$= \sqrt{k_n}(v_{gs1} - v_{gs2}) \quad (3.16)$$

$$= \sqrt{k_n}(v_{RF}) \quad (3.17)$$

Equations (3.10) and (3.17) are two equations in both i_{D1} *and* i_{D1}. They can be solved together to yield

$$i_{D1} = \frac{I_s}{2} + \sqrt{2k_n I_s}\left(\frac{v_{RF}}{2}\right)\sqrt{1 - \frac{(v_{RF}/2)^2}{(I_s/2k_n)}} \quad (3.18)$$

$$i_{D2} = \frac{I_s}{2} - \sqrt{2k_n I_s}\left(\frac{v_{RF}}{2}\right)\sqrt{1 - \frac{(v_{RF}/2)^2}{(I_s/2k_n)}} \quad (3.19)$$

Equations (3.18) and (3.19) are thus obtained. The limiting input RF signal magnitude can be calculated.

$$1-\frac{(v_{RF}/2)^2}{(I_s/2k_n)} \geq 0$$

$$\Rightarrow \frac{(v_{RF}/2)^2}{(I_s/2k_n)} \leq 1 \qquad \Rightarrow \qquad |v_{RF}| \leq \sqrt{2\frac{I_s}{k_n}} \tag{3.20}$$

At the bias point, $v_{RF} = 0$

$$i_{D1} = i_{D1} = \frac{I_S}{2} \tag{3.21}$$

Correspondingly,

$$v_{GS1} = v_{GS2} = v_{GS}$$

Thus,

$$\frac{I_S}{2} = k_n(v_{GS} - v_{th})^2 \tag{3.22}$$

The relationship can be used to rewrite Eqs. (3.18) and (3.19) in the form

$$i_{D1} = \frac{I_s}{2} + (\frac{I_s}{v_{GS} - v_{th}})(\frac{v_{RF}}{2})\sqrt{1-(\frac{v_{RF}/2}{v_{GS} - v_{th}})^2} \tag{3.23}$$

$$i_{D2} = \frac{I_s}{2} - (\frac{I_s}{v_{GS} - v_{th}})(\frac{v_{RF}}{2})\sqrt{1-(\frac{v_{RF}/2}{v_{GS} - v_{th}})^2} \tag{3.24}$$

For $(\frac{v_{RF}}{2}) << v_{GS} - v_{th}$

$$i_{D1} \cong \frac{I_s}{2} + (\frac{I_s}{v_{GS} - v_{th}})(\frac{v_{RF}}{2}) \tag{3.25}$$

$$i_{D2} \cong \frac{I_s}{2} - (\frac{I_s}{v_{GS} - v_{th}})(\frac{v_{RF}}{2}) \tag{3.26}$$

Given a long channel MOSFET operating in saturation region with a drain current at I_D , then the transconductance can be derived as $g_m = {2I_D}/{(v_{GS} - v_{th})}$,

Thus, $g_m = \frac{2(I_s/2)}{(v_{GS} - v_{th})} = \frac{I_s}{(v_{GS} - v_{th})}$ (3.27)

$$i_{D1} \cong \frac{I_s}{2} + g_m(\frac{v_{RF}}{2}) \quad (3.28)$$

$$i_{D2} \cong \frac{I_s}{2} - g_m(\frac{v_{RF}}{2}) \quad (3.29)$$

The IF output resistance is assumed to be RL, the input signal $v_{RF} = \sin \omega_{RF} t$, and LO transistors, M3-M6 exhibits ideal switching. Following (3.7), (3.28), and (3.29), the drain currents of LO transistors can be rewritten,

$$i_{D3}(t) = \frac{4}{\pi} g_m \frac{v_{RF}}{4} \cdot (\sin \omega_{LO} t + \frac{\sin 3\omega_{LO} t}{3} + \frac{\sin 5\omega_{LO} t}{5} + \cdots) \quad (3.30)$$

$$i_{D4}(t) = -\frac{4}{\pi} g_m \frac{v_{RF}}{4} \cdot (\sin \omega_{LO} t + \frac{\sin 3\omega_{LO} t}{3} + \frac{\sin 5\omega_{LO} t}{5} + \cdots) \quad (3.31)$$

$$i_{D5}(t) = \frac{4}{\pi} g_m \frac{v_{RF}}{4} \cdot (\sin \omega_{LO} t + \frac{\sin 3\omega_{LO} t}{3} + \frac{\sin 5\omega_{LO} t}{5} + \cdots) \quad (3.32)$$

$$i_{D6}(t) = -\frac{4}{\pi} g_m \frac{v_{RF}}{4} \cdot (\sin \omega_{LO} t + \frac{\sin 3\omega_{LO} t}{3} + \frac{\sin 5\omega_{LO} t}{5} + \cdots) \quad (3.33)$$

The IF output drain current equation is

$$i_{IF} = i_{D3} + i_{D5} - i_{D4} - i_{D6} \quad (3.34)$$

The negative represents a phase inversion of 180°

Substituting Eq. (3.30) to (3.33) into (3.34) yields relationship between the input and

the output signal.

$$v_{IF}(t) = i_{IF}(t) \cdot R_L$$

$$= g_m \cdot R_L \cdot v_{RF} \cdot \frac{4}{\pi} \cdot (\sin \omega_{LO} t + \frac{\sin 3\omega_{LO} t}{3} + \frac{\sin 5\omega_{LO} t}{5} + \cdots)$$

$$= g_m \cdot R_L \cdot \sin \omega_{RF} t \cdot \frac{4}{\pi} \cdot (\sin \omega_{LO} t + \frac{\sin 3\omega_{LO} t}{3} + \frac{\sin 5\omega_{LO} t}{5} + \cdots) \quad (3.35)$$

The first-order term in Eq. (3.35) is considered. The output signal is to be determined and the other terms represent the harmonic signals.

$$v_{IF}(t) = \frac{4}{\pi} \cdot g_m \cdot R_L \cdot \sin \omega_{RF} t \cdot \sin \omega_{LO} t$$

$$= \frac{4}{\pi} \cdot g_m \cdot R_L \cdot \frac{1}{2}[\cos(\omega_{RF} - \omega_{LO})t - \cos(\omega_{RF} + \omega_{LO})t$$

$$= \frac{2}{\pi} \cdot g_m \cdot R_L[\cos \omega_{IF} t - \cos(\omega_{RF} + \omega_{LO})t \quad (3.36)$$

Thus, the conversion gain fo a standard Gilbert mixer is given by

$$\text{Conversion Gain} = \frac{2}{\pi} \cdot g_m \cdot R_L \quad (3.37)$$

In practice, the LO signal is typically a sinusoidal wave rather than an ideal square wave. Assume the current-commutating stage be driven using a sinusoidal wave LO signal. The gain of the mixer can be expressed as [12].

$$\text{Conversion Gain} = \frac{2}{\pi} \cdot g_m \cdot R_L \left(1 - \frac{\sqrt{2}(V_{gs} - V_{th})}{\pi \cdot V_{Lo}}\right) \quad (3.38)$$

where $(V_{gs} - V_{th})$ is defined as the turn-on overdrive voltage of the LO transistors (M3~M6) and V_{LO} is the amplitude of the LO signal. Applying (3.38) to multiple gate

structures in a Gilbert cell mixer, the conversion gain can be expressed as

$$\text{Multiple Gated Conversion Gain} = \frac{2}{\pi} \cdot R_L (g_{m1} + g_{m2}) \left(1 - \frac{\sqrt{2}(V_{gs} - V_{th})}{\pi V_{Lo}} \right) \qquad (3.39)$$

The matching of all the transistors involved in the differential pairs must be optimized to improve the linearity of the mixer. Accordingly, the channel lengths of the transistors, such as M3~M6 in Fig. 3.18 were chosen longer than the minimum rule wherever possible.

3.3.1.6 IF Output – Parallel RC Network for Linearity Improvement

As for the IF stage, the output can be sensed as either a differential or a single-ended signal. In this design, a differential output is adopted to take advantage of higher conversion gain and better RF-to-IF isolation [12]. The use of multi-stage parallel RC networks at output was proposed for high linearity and low power CMOS mixer design [5]. Our simulation results indicate that the accommodation of multi-stage parallel RC networks at output indeed can improve mixer linearity in terms of P-1dB and IIP3. In the following, the comparison in linearity will be carried out between the new design with and the conventional ones without parallel RC networks.

3.3.1.7 Package Topology

QFN 20-pin package was employed in this design and was offered by SPIL. Figure 3.19 defines the pin name for chip wire bonding. The most important problems

of major concern are are the parasitic inductance and resistance in series with the bond wires and the parasitic capacitance originated from the bonding pads. Figure 3.20 illustrates the bond-wire package model . The series inductance is approximately 1nH/mm with a length of bond-wire that generally exceeds that of the on-chip inductor. The bond wires have significant influence on the circuit performance. Due to the fact, the package model of bond-wire must be taken into account in the full circuit simulation measurement. Chapters 4 and 5 will describe the simulation and measurement results.

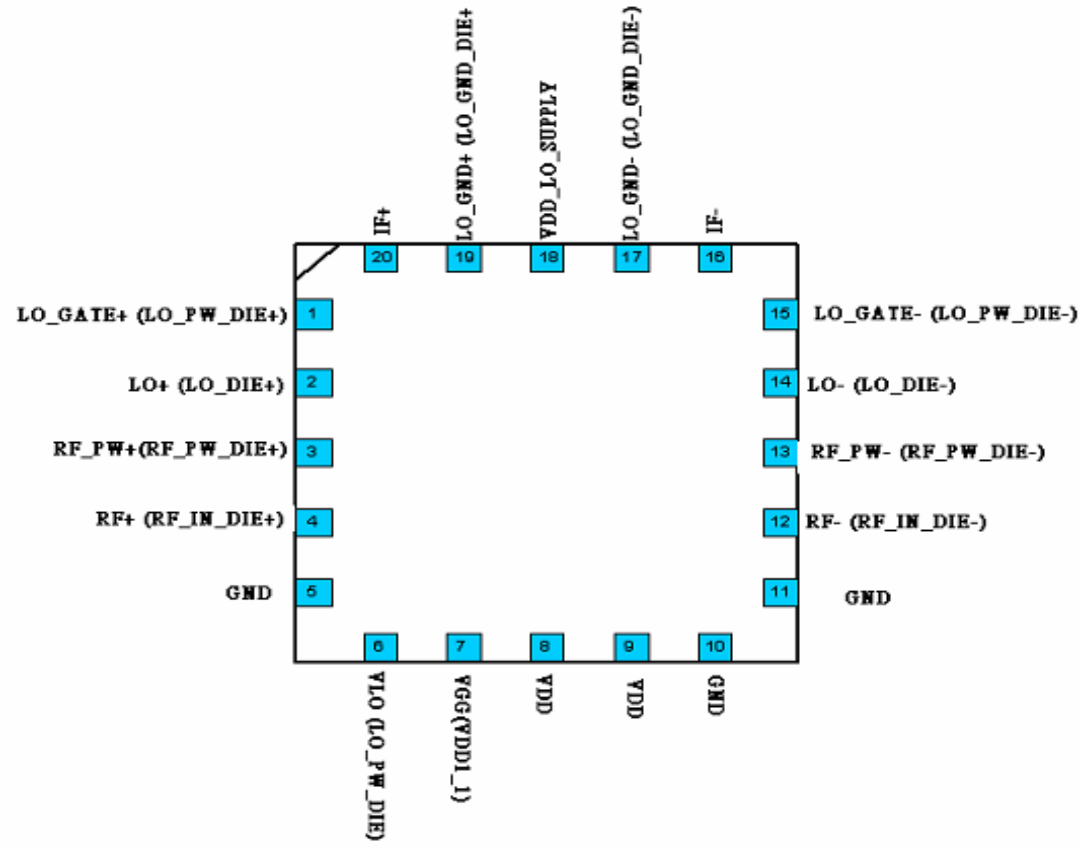


Fig. 3.19 Pin assignment for the bonding pads on board

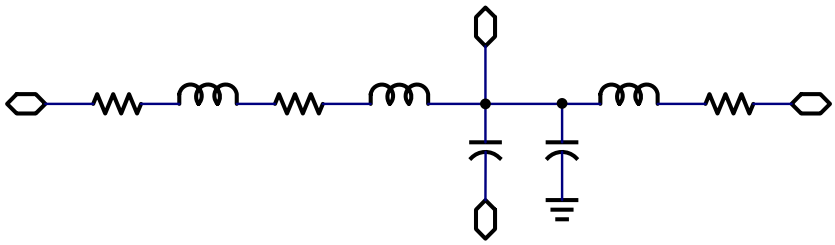


Fig. 3.20. Package model of the bonding pad and wires

3.4 Figure-of-Merit of RF CMOS Transistors

The RF CMOS transistor design is generally guided by the key performance parameters, such as the cut-off frequency (f_T), maximum oscillation frequency (f_{max}), minimum noise figure (NF_{min}), 1/f noise, and the third order harmonic intercept voltage (V_{IIP3}), etc. all the performance parameters are classified as figure-of-merit (FoM). The design challenges come from the trade-off between different performance parameters. In the following, the first-order equations for the RF FoM, such as f_T, f_{max}, NF_{min}, and V_{IIP3} are given below [13].

$$f_t = \frac{1}{2\pi}\frac{g_m}{C_{gg} + C_{par} + C_{gso} + C_{gd0}} \tag{3.40}$$

$$f_{\max} = \frac{1}{2}\frac{f_t}{(R_g + R_i)\cdot(g_{ds} + 2\cdot\pi\cdot f_t \cdot C_{gdo})} \tag{3.41}$$

$$NF_{\min} = 1 + K\frac{f}{f_t}\sqrt{g_m(R_g + R_i + R_s)} \tag{3.42}$$

$$V_{IP3} = \sqrt{\frac{24 \cdot g_m}{g_{m3}}} \tag{3.42}$$

where g_m is the transconductance; g_{m3} is the third-order derivative of the drain current versus gate bias, and V_{IIP3} is the extrapolated input voltage amplitude at which the first and third-order amplitudes are equal. The capacitances C_{gg}, C_{par}, C_{gso} and C_{gdo} are the intrinsic input capacitance, the parasitic gate-bulk capacitance, the gate-source capacitance and the date-drain overlap capacitance. R_g is the gate resistance and R_i is the real part of the input impedance due to nonquasistatic effects. Rs and g_{ds} are the source series resistance and output conductance.

Fig. 3.19 presents NFmin versus drain currents under varying frequencies, simulated for 0.18um N-MOSFET. Herein, TSMC 0.18 um mixed signal and RF CMOS model was employed for this simulation.

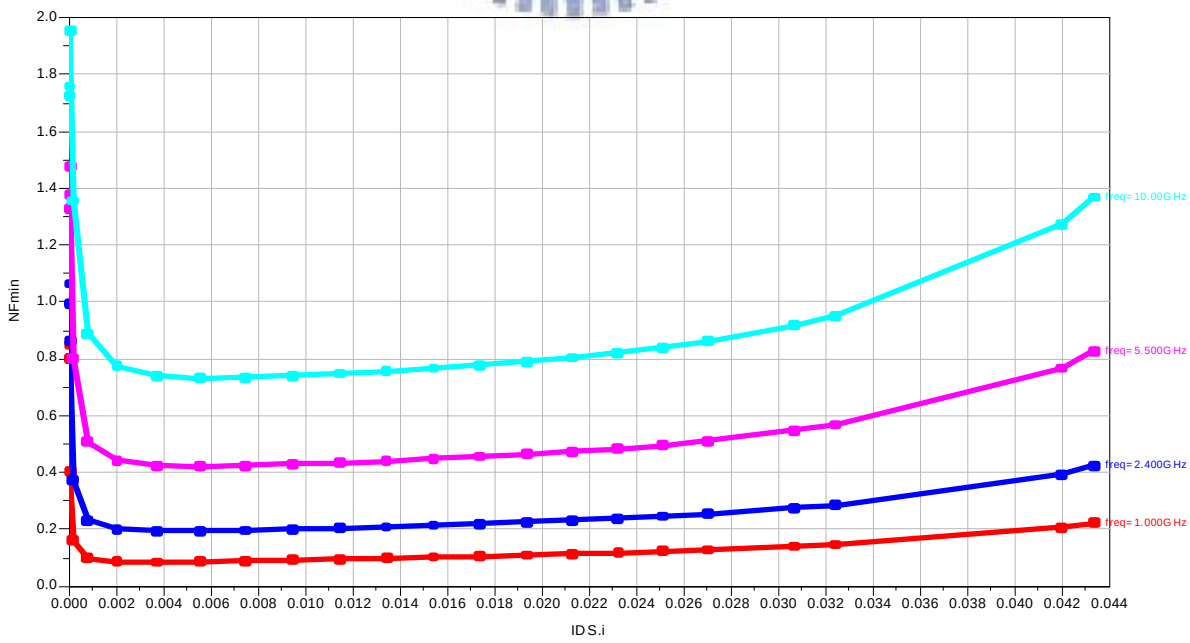


Fig. 3.21 0.18um N-MOSFET NF_{min} versus drain current under varying frequencies

3.5 Noise Analysis for RF Active Mixers

Basically, the noises appearing in the electronic devices can be classified as thermal noise, shot noise, flicker noise, and generation-recombination noise. For CMOS devices and circuits of our major focus, thermal noise and flicker noise are two dominant noise sources. As for an active CMOS mixer, the noise sources involve all transistors and resistors in this circuits, such as transconductance amplifier, switching pairs, and load stage. In the following, we will concentrate our discussion on thermal noise at high frequency and leave flicker noise as an uncovered topic.

3.5.1 Noise Analysis - Power Spectral Density (PSD) [14]

The noise characteristics of mixers is quite complicated, because of the features of nonlinearity and the time-variance. The output noise generated in a mixer generally exhibits a time-varying characteristics. Furthermore, an active mixer working with a periodic LO is in essense a nonlinear periodic system. The resulted response to an input noise is actually a time-varying process with a period of LO signal time constant ($T_{LO}=2\pi/\omega_{LO}$, ω_{LO} : LO signal frequency). As a result, the power spectral density (PSD) of the noise is time-varying with a time constant of T_{LO}. Assume a small signal equivalent circuit model incorporating mentioned noise sources and take into account of correlated and uncorrelated terms, PSD of output noise can be derived as follows for single balanced and double balanced mixers, respectively.

[1] Transconductance stage noise

Single balanced mixer

*M*1, *M*2 : switching pair

*M*3 : transconductance stage

$$S_{n3}(\omega) = S_{n3}^{c}(\omega) + S_{n3}^{u}(\omega)$$

$$= 4kTg_{m3}\left\{\gamma\left(\frac{\omega_{p3}^{\ 2}}{\omega_{z3}^{\ 2}}\right) + \left[g_{m3}R_{sG3}' + \gamma\left(1 - \frac{\omega_{p3}^{\ 2}}{\omega_{z3}^{\ 2}}\right)\right]\left(\frac{\omega_{p3}}{\omega_{LO}}\right)\tan^{-1}\left(\frac{\omega_{LO}}{\omega_{p3}}\right)\right\} \quad (3.43)$$

where

g_{m3} : the transconductance of M3

γ : channel thermal noise factor

$$R_{sG3} = \frac{R_G}{3} + R_S$$

$\frac{R_G}{3}$: distributed gate resistance

R_G : input source resistance

ω_{p3}, ω_{p3} : pole and zero of $S_{n3}(\omega)_{i_{ng}, i_{nd}}$

ω_{LO} : LO signal frequency

then the PSD of time-average process is given by

$$\overline{S_{n3}^{0}(\omega,t)} = \sum_{n=-\infty}^{n=\infty} |p_{1,n}|^2 S_{n3}(\omega - n\omega_{LO})$$

$$= S_{n3}(\omega)\sum_{n=-\infty}^{n=\infty} |p_{1,n}|^2 = \frac{S_{n3}(\omega)}{T_{LO}}\int_0^{T_{LO}} |p_1(t)|^2 dt \quad (3.44)$$

define

$$E_{p1} = \sum_{n=-\infty}^{n=\infty} |p_{1,n}|^2 = \frac{1}{T_{LO}}\int_0^{T_{LO}} |p_1(t)|^2 dt \quad (3.45)$$

For a double balanced mixer, e.g. Gilbert cell mixer

*M*1, *M*2 : switching pair

*M*3, *M*4 : switching pair

*M*5, *M*6 : transconductance stage

$$\overline{S_{n56}^{0}(\omega,t)} = E_{p1}S_{n56}(\omega) \quad (3.46)$$

[2] Switching pair noise

Single balance mixer

$$\overline{S_{n12}^{0}(\omega,t)} = 4kT\gamma\left(\frac{2I_{ss}}{\pi V_s}\right)\left\{\gamma\left(\frac{\omega_{p12}{}^2}{\omega_{z12}{}^2}\right)+\left[\left(\frac{1.16I_{ss}}{\pi V_s}\right)R_{SG12}{}'+\gamma\left(1-\frac{\omega_{p12}{}^2}{\omega_{z12}{}^2}\right)\right]\left(\frac{\omega_{p12}}{\omega_{LO}}\right)\tan^{-1}\left(\frac{\omega_{LO}}{\omega_{p12}}\right)\right\} \quad (3.47)$$

double balance mixer : assume symmetric for two pairs of switches

$$\overline{S_{n12}^{0}(\omega,t)} + \overline{S_{n34}^{0}(\omega,t)} = 2x\overline{S_{n12}^{0}(\omega,t)} \quad (3.48)$$

where

I_{SS} : tail current through transconductance amplifier
through M3 for a single balance mixer
through M5, M6 for a double balance mixer

[3] LO port noise

$$\overline{S_{nLO}^{0}(\omega)} = 4kT\left(R_{LO}+2R_{G1}\right)\left(\frac{2.32I_{ss}{}^2}{\pi V_o V_s}\right) \quad (3.49)$$

where

R_{LO} : equivalent noise resistance

R_{G1} : physical poly gate resistance

3.5.2 Noise Analysis – Noise Figure [14]

Based on the PSD of all noise sources, such as transconductance amplifier, switching pairs, and LO port, derived in 3.5.1, noise figure can be calculated. In the following expressions, single side band (SSB) noise were derived for single balanced and double balanced mixers, as given by (3.50) and (3.51), respectively. Regarding the double side band (DSB) noise, it is not considered in this study due to the fact that the image signal generally does not carry useful information in RF mixers.

$$NF_{SSB} = \frac{\overline{S_{n3}^{0}(\omega,t)} + \overline{S_{n12}^{0}(\omega,t)} + \overline{S_{nLO}^{0}(\omega,t)} + 4KT/R_L}{g_c^2}\cdot\frac{1}{4KTR_s} \text{ (Single-Balanced)} \quad (3.50)$$

$$NF_{SSB} = \frac{\overline{S^0_{n56}(\omega,t)} + 2\cdot\overline{S^0_{n12}(\omega,t)} + 2\cdot\overline{S^0_{nLO}(\omega,t)} + 4KT/R_L}{g_c^2} \cdot \frac{1}{4KTR_s} \text{ (Double-Balanced}$$

(3.51)

These equations represent a new analytical model for high-frequency noise in RF CMOS active mixers. Equations (3.50) and (3.51) indicate that the noise is generated by the parasitic and load resistances (R_S and R_L) and transconductance.

3.5.3 Noise Analysis – Mixer Noise Optimization [15]

Applying Eqs. (3.38) or (3.39) to the LO stage (current commutating stage), if the amplitude of the V_{LO} signal is increased but the gate over-drive (V_{gs}-V_{th}) is decreased, the gain of the mixer will be reduced, and vice versa. Based on Eq. (3.52) [15] , the relation between the LO signal and the noise figure of the mixer is considered. Increasing LO signal can improve the noise figure of the mixer. This phenomenon is consistent with our simulation and measurement results. However, the large LO signal exhibits stronger interference and worse LO-pulling problem in the integration system.

As mentioned above, the larger LO signal can reduce the noise of the mixer. The designer can increase the bias for the transconductance stage to improve linearity or conversion gain. However, the increase of conversion gain sometimes leads to larger noises contributed from the LO switching stage and output load resistance.

$$\overline{V_{o,n}^2} = 8kTR\left(1+\gamma\frac{2R_L I}{\pi V_{LO}}+\gamma\frac{R_L I_{ds}}{2(V_{gs}-V_{th})}\right) \tag{3.52}$$

Chapter 4.

Chip Circuit Design and Simulation

TSMC 0.18μm CMOS mixed signal and RF (MS/RF) models [15] was employed for this CMOS mixer circuit simulation and design. This RF CMOS model includes passive elements such as resistors, inductors, capacitors, and RF MOSFETs as the major active devices. Also, on-chip circuit layout will be introduced.

4.1 Models

In mixed signal and RF circuit design, an accurate and scalable model is strongly demanded to assure circuit simulation accuracy and facilitate success of circuit design. For active devices, the intrinsic MOSFET model suitable for logic circuit simulation is no longer valid for RF circuit design. Parasitic and coupling effects from interconnection, substrate, and pads should be considered and taken into the model. As for passive devices, such as inductors, capacitors, and resistors, substrate lossy and conductor loss become important effects required for accurate modeling. To solve the mentioned problems at high frequencies, lumped element equivalent circuit models are more practical than numerical due to the computation efficiency for circuit simulation.

4.1.1 RF MOS Model

TSMC 0.18μm 1P6M CMOS MS/RF process can support 1.8V/3.3V circuit design. Multiple finger MOSFETs with various gate lengths and finger widths are available for circuit design. For 1.8V core operation, the gate lengths range from 0.18 μm to 0.5 μm and the gate widths are in the scale of 1.5 μm to 8 μm. The biases applied to the gate and drain for 1.8/3.3V devices are summarized in Table 4.1. In this work for low power mixer design, 1.8V core N/P MOSFETs are adopted to achieve low voltage and low power operation. Fig 4.1 shows the equivalent circuit model of the RF NMOS transistors.

Table 4.1 Bias Conditions of RF MOSFETs

Bias Condition / Device	|Vgs|	|Vds|	|Vbs|
1.8V RF NMOS	0.5~1.8V	0.6~1.8V	0~1.8V
1.8V RF PMOS	0.5~1.8V	0.6~1.8V	0~1.8V
3.3V RF NMOS	0.8~3.3V	0.8~3.3V	0~3.3V
3.3V RF PMOS	0.8~3.3V	0.8~3.3V	0~3.3V

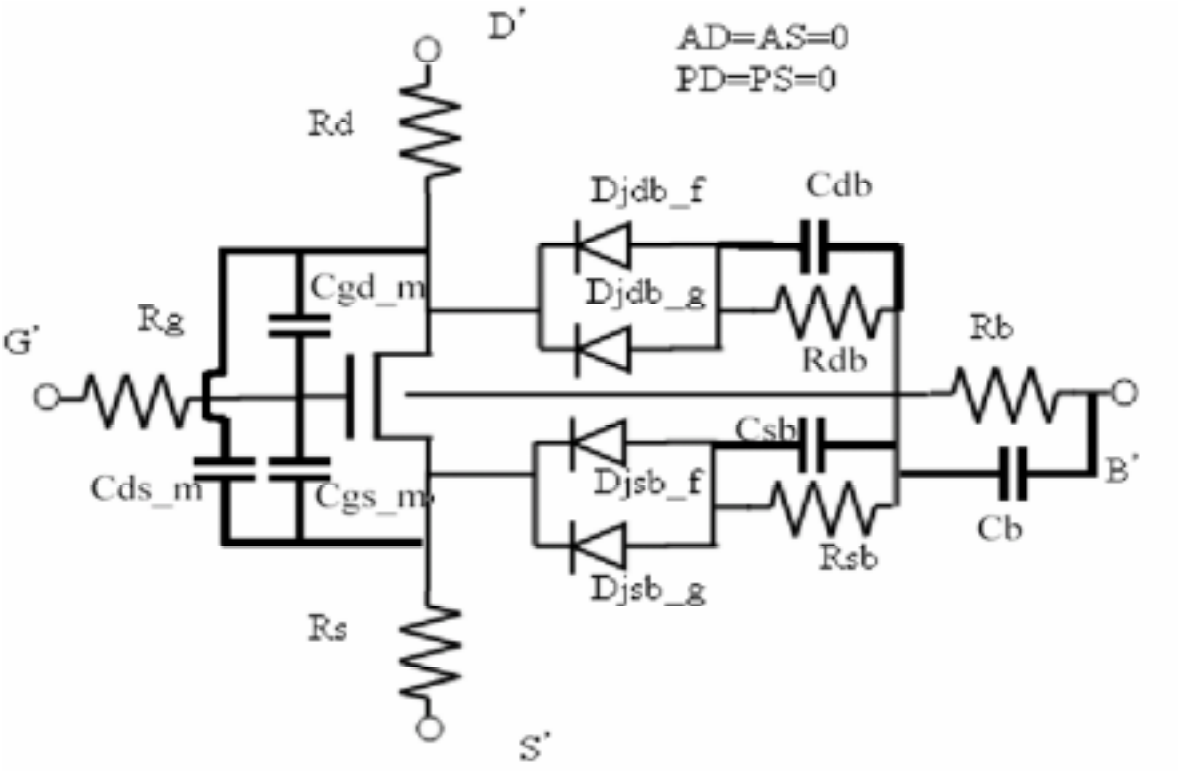


Fig. 4.1 Equivalent circuit model for RF MOS transistor.

where

a. Rsb, Rdb and Rb are the substrate resistance.

b. Csb, Cdb and Cb are the substrate capacitance.

c. Rg is the effective gate resistance.

d. Djdb_f, Djdb_g, Djsb_f and Djsb_g are the external drain to bulk junction diode.

e. Rd and Rs are the parasitic resistance of metal routing connected to the drain/source of the MOS transistors.

f. Cgs_m, Cgd_m and Cds_m parasitic capacitance from metal routing connection to the gate/drain/source of the MOS transistors.

4.1.2 Spiral Inductor Model

A rectangular spiral inductor employs a thick AlCu metal with a physical thickness at 2.0 μm. The spiral inductor is modeled as a two-port S-parameter to fit equivalent circuit model. The symmetric octagonal spiral equivalent circuit is introduced, and fabricated on top of a P-substrate in a metal-5 (bottom) and a metal-6 (top) layer, as shown in Fig. 4.2. The lump RLC equivalent circuit is adopted to model the rectangular spiral inductor, shown in Fig. 4.3.

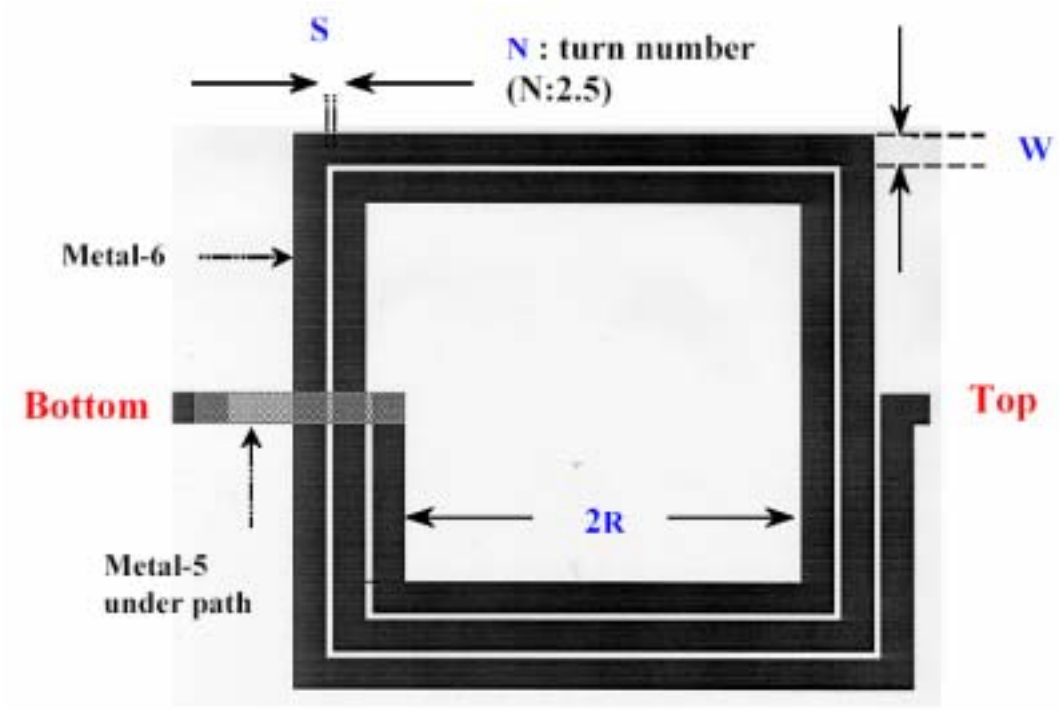


Fig. 4.2 Top view and physical dimension of rectangular spiral inductor.

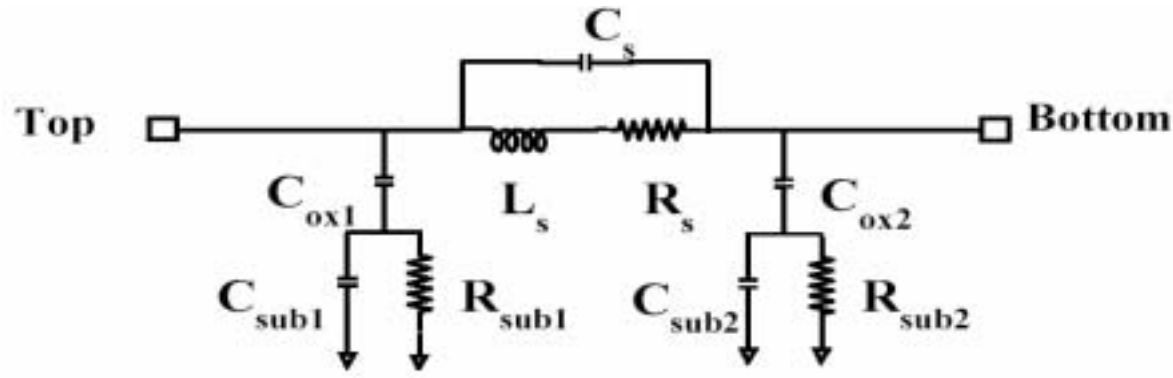


Fig. 4.3 Equivalent circuit of rectangular spiral inductor.

Parameters

Ls : Inductance

Rs: : Metal series resistance.

Cs: : Overlap (of OR in) capacitances of spiral and center tap underpass.

Cox (1 and 2) : Oxide capacitance between the spiral and substrate.

Rsub (1 and 2) : Silicon substrate resistance.

Csub ((1 and 2) : Silicon substrate capacitance.

4.1.3 MIM Capacitor Model

Figure 4.4 presents the layout of the MIM capacitor structure. The square MIM (metal-insulator-metal) capacitor is modeled as a two-port S-parameter fit.

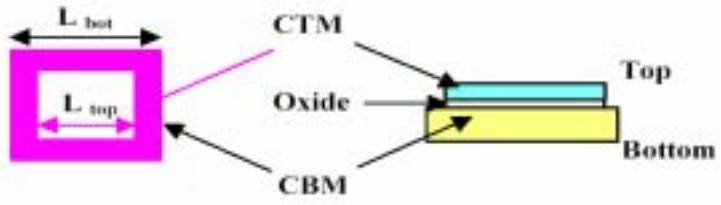


Fig. 4.4 (a) MIM capacitor layout.

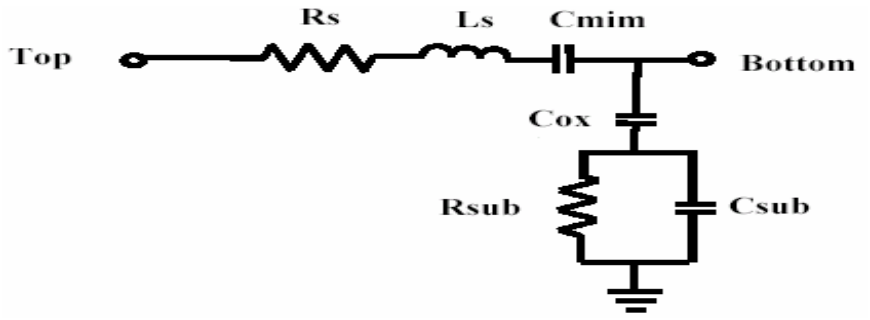


Fig. 4.4 (b) Equivalent circuit for MiM capacitors.

4.2 Simulation Results of Down-Conversion Mixer

Figure 3.6 displays the proposed low-voltage CMOS Gilbert mixer. Multiple gates are applied to increase the linearity of the mixer. Table 3.1 shows the simulation results. Following Chapter 3, the output load parallel capacitor can increase linearity. The simulation will show to compare the IF output to parallel with/without capacitor in terms of output linearity. Beyond the above simulation results, the simulation includes non-package circuit chip simulation. The results based on the QFN package model will be presented later. In this simulation, biases of 0.7V and 1.0V are applied, and both results are presented.

4.2.1 Improved Linearity using Parallel RC Networks Capacitor at IF Stage

The simulation revealed an interesting result that the adoption of parallel RC network at the output of IF stage can effectively improve the linearity [17]. To explain this effect, filtering of high-oder harmonics through the RC network is proposed as the possible primary mechanism. The minimum capacitance required to make the effective filtering is around 8 pF for this mixer. Therefore, multiple stage RC networks were implemented at the output of IF stage. Table 4.2 summarizes the simulation results and reveals better linearity in terms of higher P-1dB and IIP3 for IF with RC networks than that with simple resistor network. Fig. 4.5(a) and (b) present

the simulated conversion gain and P-1dB for mixers with and without capacitors at the output of IF stage. The simulation results prove the improved linearity realized by adoption of capacitors and the resulted parallel RC networks. Again, the improved linearity was demonstrated by increased IIP3 as shown in Fig. 4.5 (d) with RC networks in comparison with Fig. 4.5(c) with resistor network. Fig. 4.5(e) indicates the filtering effect on high order harmonics by parallel RC networks incorporating capacitors.

Table 4.2 Compared IF stage with capacitor and without capacitor by simulation

Power supply voltage / Simulation Item	1V (TT, 25°C) IF with RC networks	1V (TT, 25°C) IF with resistor networks
Power consumption	<3mW (2.81mW)	<3mW (2.81mW)
Conversion Gain	20.908 dB	20.833 dB
P-1dB (10MHz)	6.188 dBm	4.373 dBm
IIP3	12.2 dBm	-0.8 dBm
Single Side Band Noise	27.82 dB	27.029 dB
Double Side Band Noise	21.52 dB	20.508 dB
RF freq=5500MHz, LO freq=5499MHZ LO=2.5 dBm, IIP3 RFin =5.5 GHz		

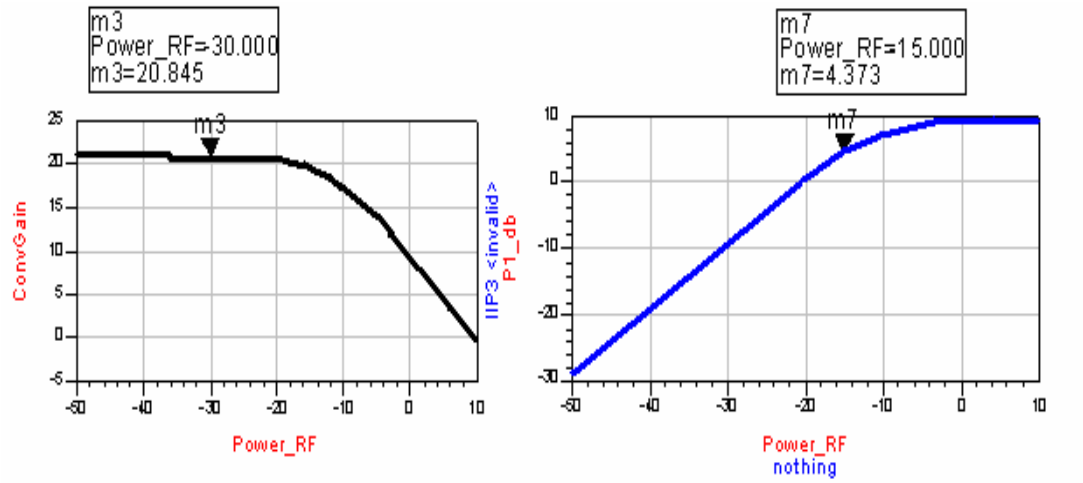


Fig. 4.5 (a) Conversion gain and P-1dB for IF stage with resistor networks (without capacitor).

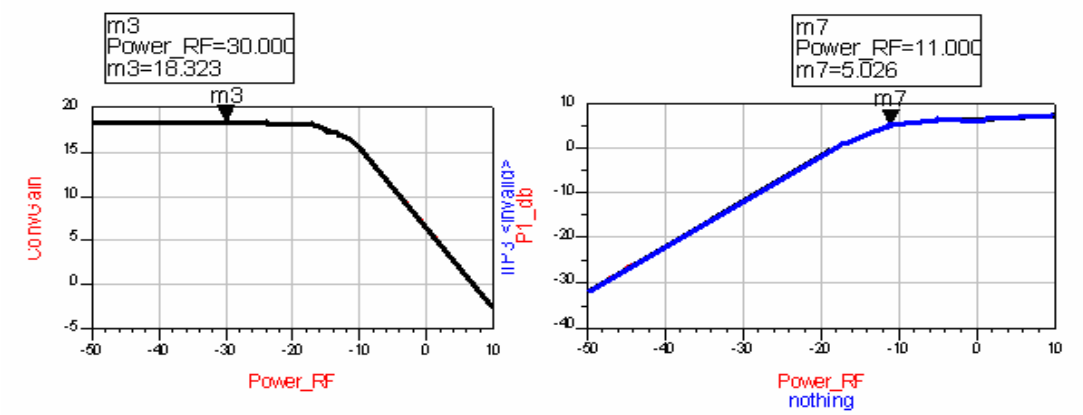


Fig. 4.5 (b) Conversion gain and P-1dB for IF stage with RC networks (with capacitors).

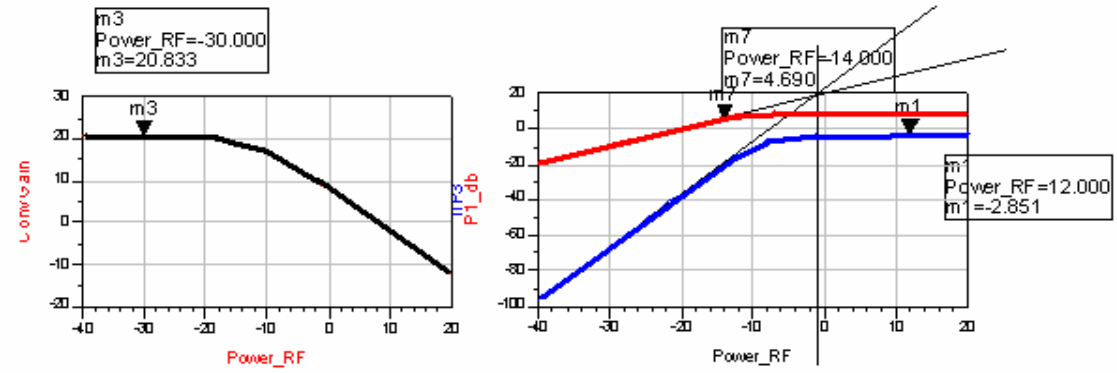


Fig. 4.5 (c) Conversion gain and IIP3 for IF stage with resistor networks (without capacitor).

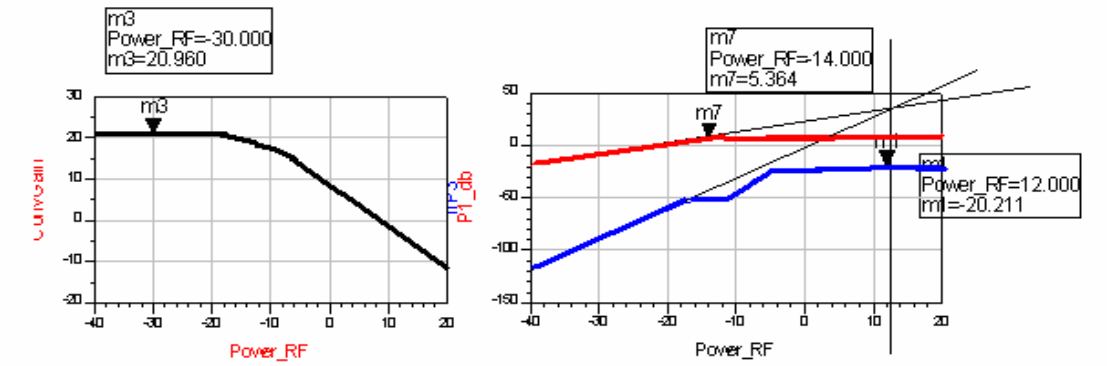
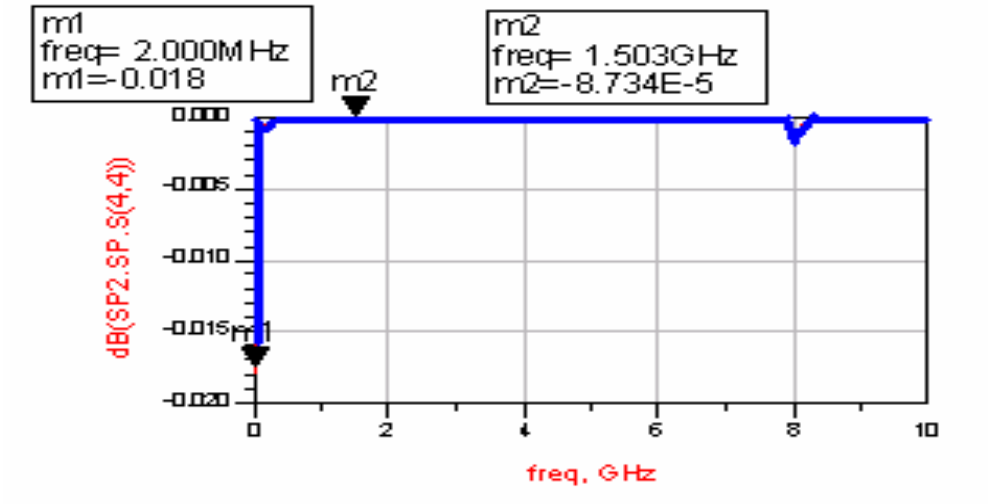
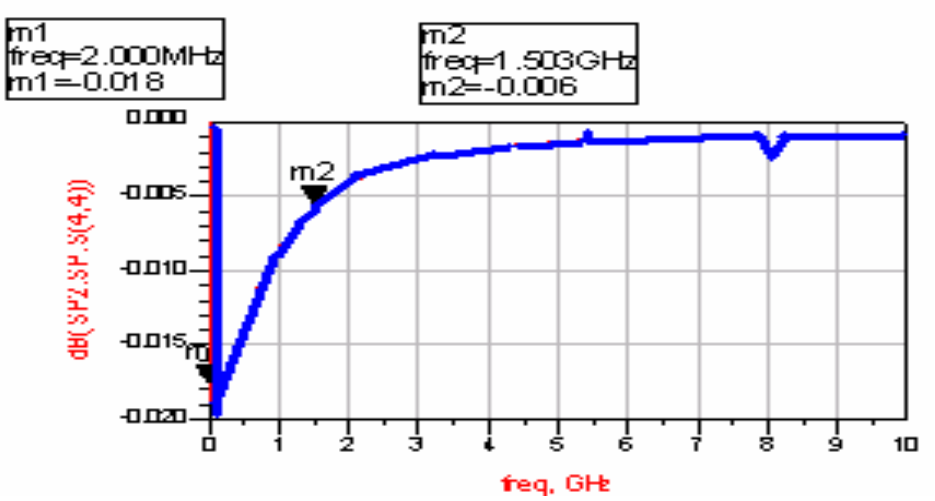


Fig. 4.5 (d) Conversion gain and IIP3 for IF stage with RC networks (with capacitors).



Resistor networks at IF stage (without capacitors)



Parallel RC networks at IF stage (with capacitors)

Fig. 4.5 (e) Filering effect on high frequency harmonic by adopting parallel RC networks to improve linearity

4.2.2 Relationship Between LO Signal for Linearity and Noise Figure

The noise analysis of the mixer is considerably more complex. The third-order inter-modulation intercept of a signal mixer is given by, [17]

$$V_{IP3} \approx 4 \cdot \sqrt{\frac{2}{3}} \cdot \left(v_{gs} - v_{th}\right)_{RFIn} \tag{4.1}$$

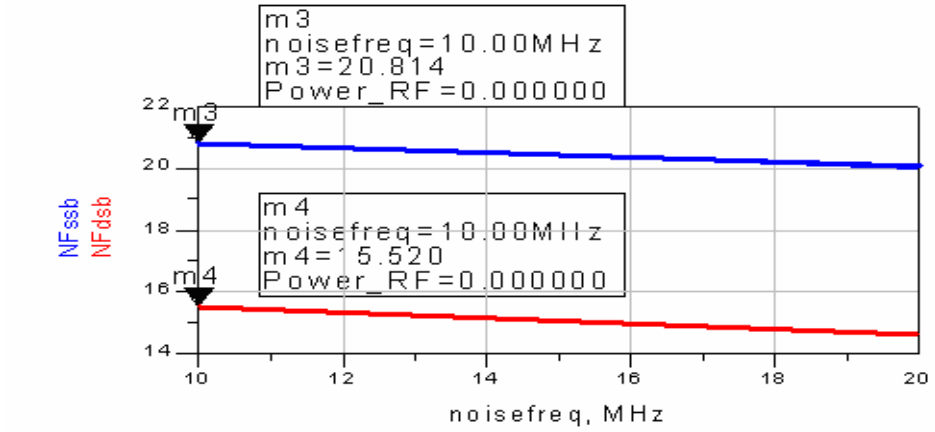
Equations (3.39), (3.45) and (4.1) demonstrate that the sine wave of the LO switches of gate driven voltage magnitude and input transconductance stage donates the noise quantity. This is a fundamental trade –off among linearity, conversion gain and noise in the active mixers.

Despite the fact that the large LO signal over-driver can enhance the linearity and the noise figure. However, the LO signal must maintain a moderate swing magnitude when the LO MOS is operated in the saturation region.

Table 4.3 and Fig. 4.6 presents the relation between the LO signal magnitude and the noise figure, the linearity and the conversion gain.

Table 4.3 Compared linearity and noise figure for LO signal magnitude

Power supply voltage / Simulation Item	1V (TT, 25°C, LO=2.5 dBm)	1V (TT, 25°C, LO= 10 dBm)
Power consumption	<3mW (2.81mW)	<3mW (2.81mW)
Conversion Gain	20.908 dB	10.325 dB
P-1dB (10MHz)	6.188 dBm	5.644 dBm
IIP3	12.2 dBm	17.60 dBm
Single Side Band Noise	27.82 dB	20.814 dB
Double Side Band Noise	21.52 dB	15.520 dB
RF freq=5500MHz, LO freq=5499MHZ LO=2.5 dBm, IIP3 RFin =5.5 GHz		



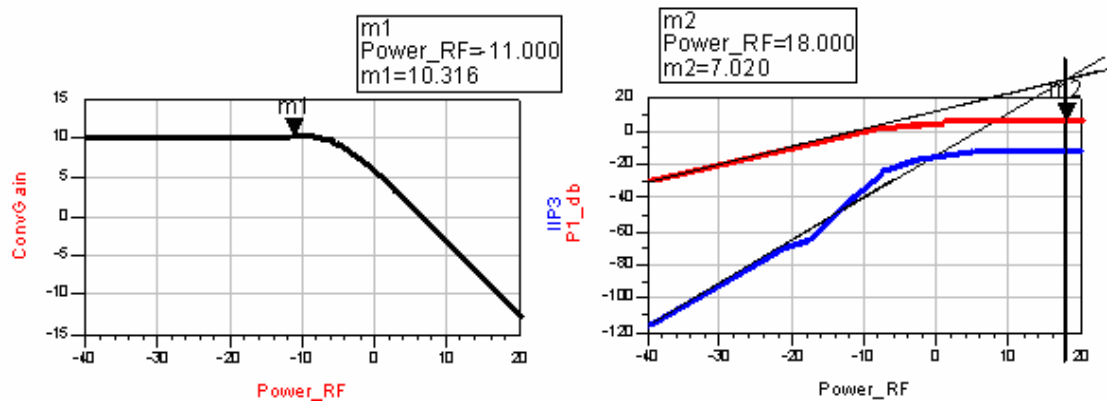


Fig. 4.6 (a) LO=10dBm (e.g. 0.71V) noise figure, conversion gain and IIP3 plot

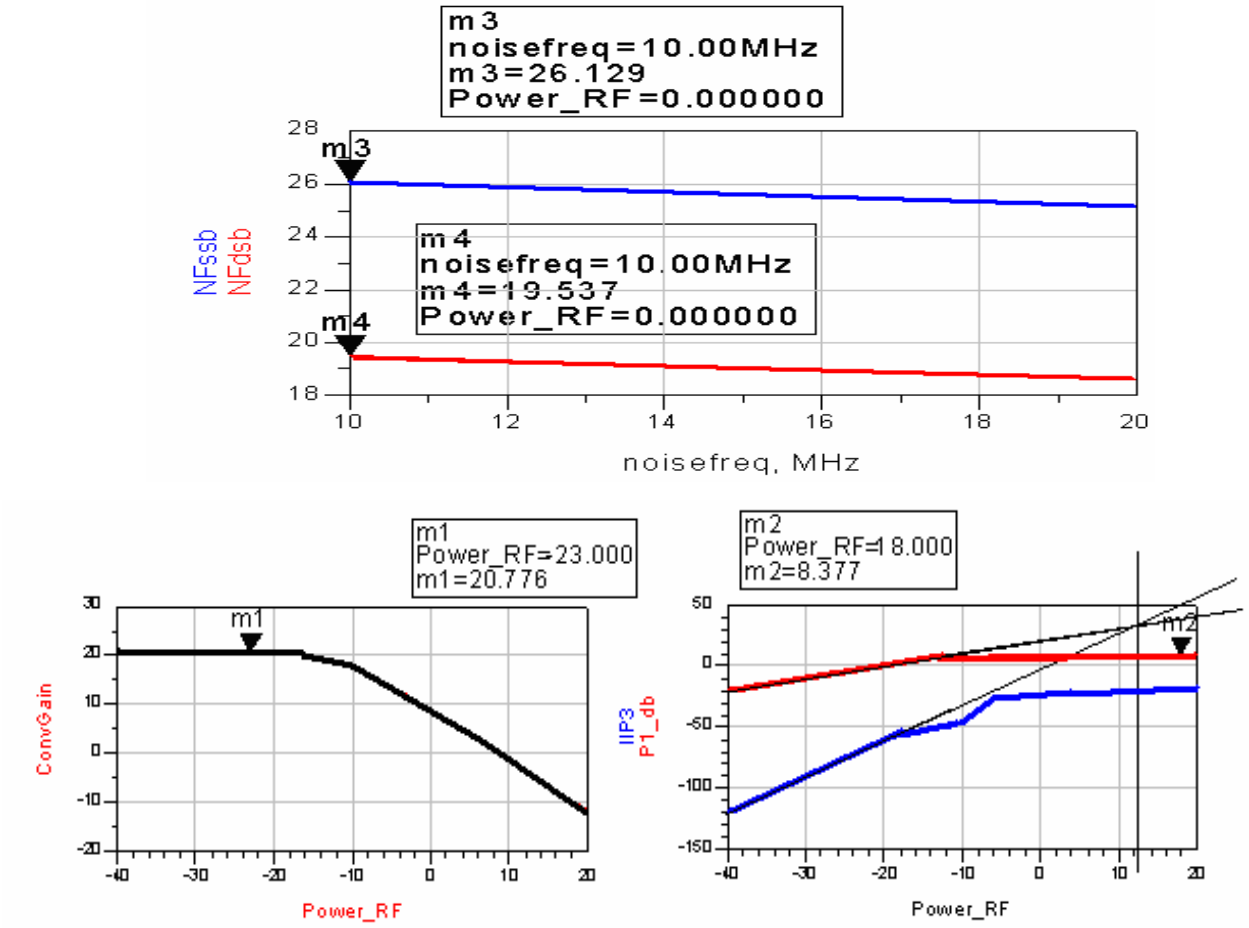


Fig. 4.6 (b) LO=2.5 dBm (0.31V) noise figure, conversion gain and IIP3 plot

4.2.3 On-Chip Circuit Simulation Results

(a) Simulation of 1V on-chip at 25°C

The simulation results below are based on the TSMC model instead of the off-chip circuit component, as shown in Figs 4.7 and 4.8. Tables 4.4 and 4.5 present the on-chip corner model simulation results for the mixer biased at 1.0V at 25°C and 75°C. They include conversion gain, noise figure, gain compression and IIP3.

Table 4.4 Corner model simulation results in biasing 1.0V and 25 °C

Power supply voltage / Simulation Item	1V, SS, 25°C	1V, TT, 25°C	1V, FF, 25°C
Power consumption	2.067 mW	2.81 mW	3.8 mW
Conversion Gain	18.857 dB	20.908 dB	18.003 dB
P-1dB (10MHz)	6.58 dBm	6.188 dBm	5.127 dBm
IIP3	9.5 dBm	12.2 dBm	8.4 dBm
Single Side Band Noise	26.766 dB	27.82 dB	26.474 dB
Double Side Band Noise	20.586dB	21.52 dB	20.828 dB
RF freq=5500MHz, LO freq=5499MHZ LO=2.5 dBm, IIP3 RFin =5.5 GHz			

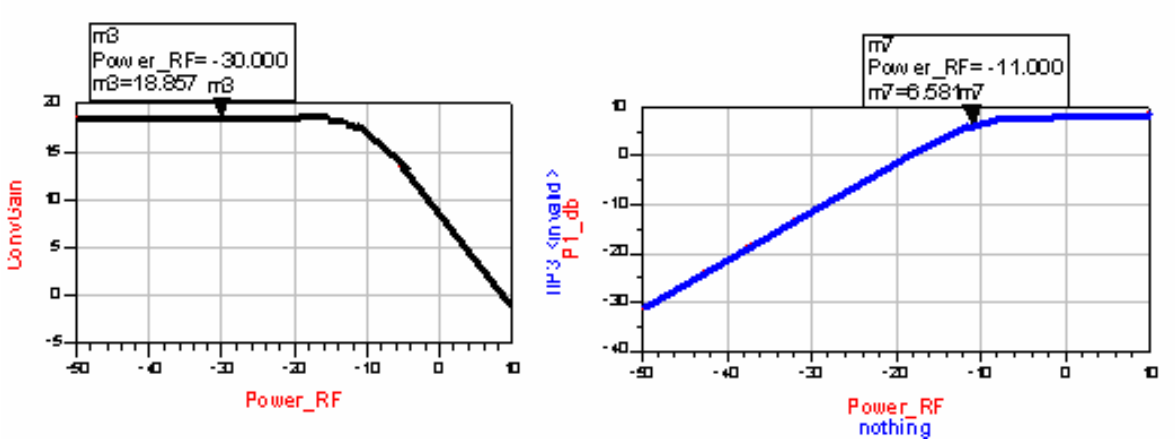


Fig. 4.7 (a) 25°C@1.0V SS of corner model simulation plots for conversion gain and P-1dB

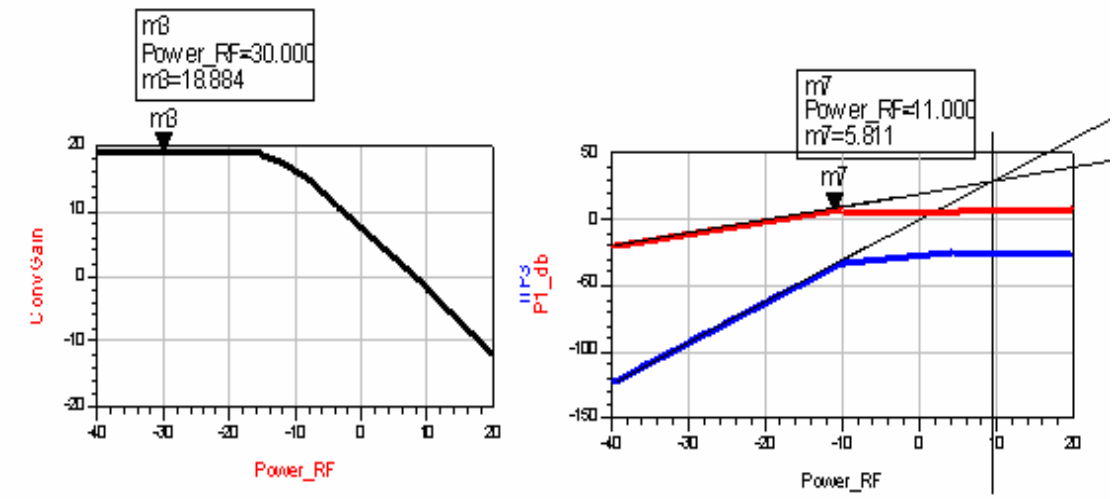


Fig. 4.7 (b) 25°C SS of corner model simulation plots for conversion gain and IIP3

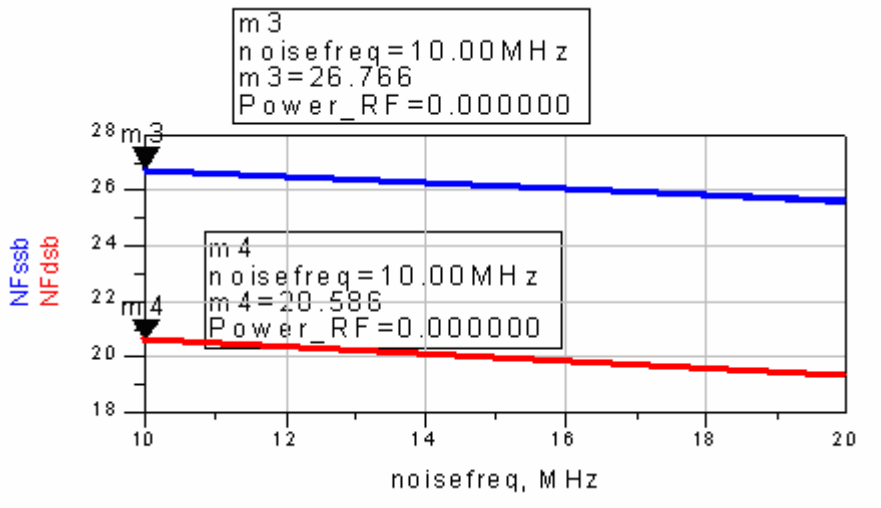


Fig. 4.7 (c) 25°C@1.0V SS of corner model simulation plots for noise figure for SSB and DSB

(b) 1V on chip 75°C simulation

Table 4.5 Corner model simulation results in biasing 1.0V and 75 °C

Power supply voltage / Simulation Item	1V, SS, 75°C	1V, TT, 75°C	1V, FF, 75°C
Power consumption	3.168 mW	4.23 mW	5.68 mW
Conversion Gain	20.238 dB	24.267 dB	19.248 dB
P-1dB (10MHz)	5.647 dBm	4.161 dBm	4.177 dBm
IIP3	8.2 dBm	8.2 dBm	8.10 dBm
Single Side Band Noise	26.978 dB	26.549 dB	26.899 dB
Double Side Band Noise	20.923 dB	20.210 dB	21.589 dB
RF freq=5500MHz, LO freq=5499MHZ LO=2.5 dBm, IIP3 RFin =5.5 GHz			

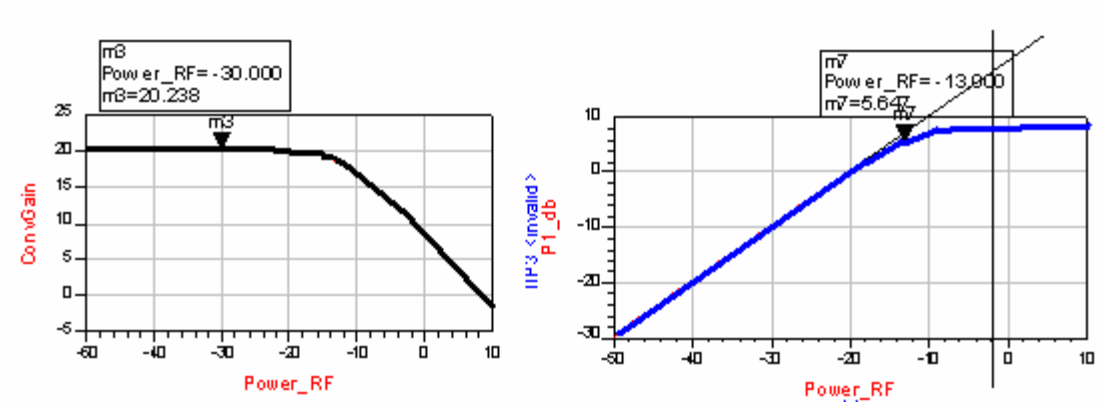


Fig. 4.8 (a) 75°C@1.0V SS of corner model simulation plots for conversion gain and P-1dB

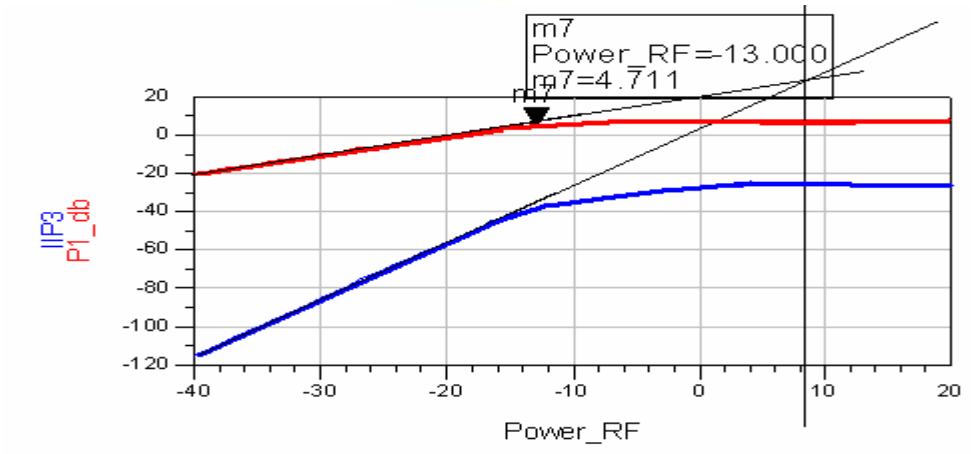


Fig. 4.8 (b) 75°C@1.0V SS of corner model simulation plots for IIP3

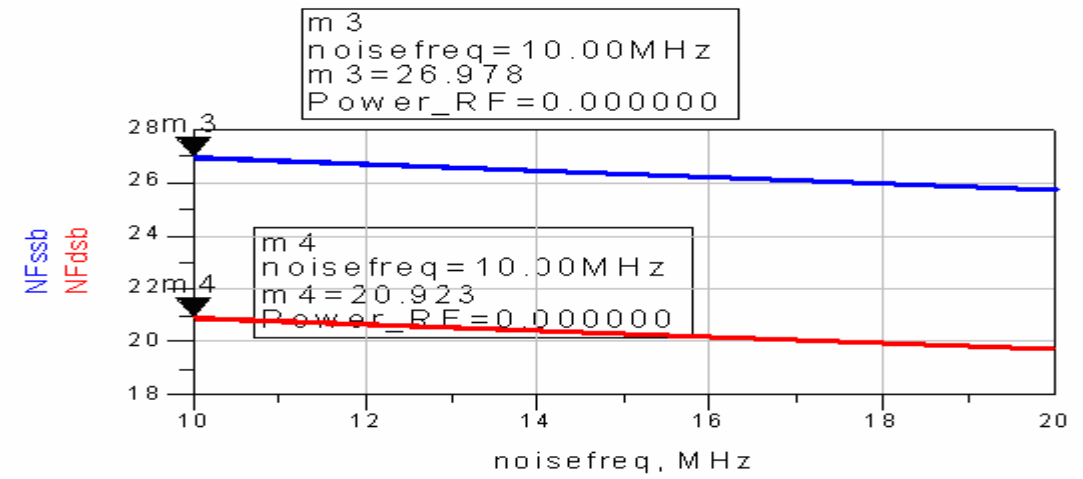


Fig. 4.8 (c) 75°C@1.0V SS of corner model simulation plots for noise figure for SSB and DSB

4.2.4 On-board Circuit Simulation Results - QFN Package

(a) Simulation of 1V on QFN chip at 25°C

In this simulation, the SPIL QFN package model is employed. The TSMC model rather than the off-chip component model is used. Figures 4.9 and 4.10 and Tables 4.6 and 4.7 present results of the simulation of the package on QFN using the corner model for the mixer biased at 1.0V at 25°C and 75°C . They include conversion gain, noise figure, gain compression and IIP3.

Table 4.6 Corner model simulation results on QFN chip in biasing 1.0V and 25 °C

Power supply voltage / Simulation Item	1V, SS, 25°C	1V, TT, 25°C	1V, FF, 25°C
Power consumption	2.031 mW	2.744 mW	3.7124 mW
Conversion Gain	18.753 dB	24.291 dB	19.857 dB
P-1dB (10MHz)	7.467 dBm	5.798 dBm	4.891 dBm
IIP3	15.5 dBm	10 dBm	8.2 dBm
Single Side Band Noise	26.652 dB	27.250 dB	29.035 dB
Double Side Band Noise	19.501 dB	20.696 dB	21.888 dB
RF freq=5500MHz, LO freq=5499MHZ LO=2.5 dBm, IIP3 RFin =5.5 GHz			

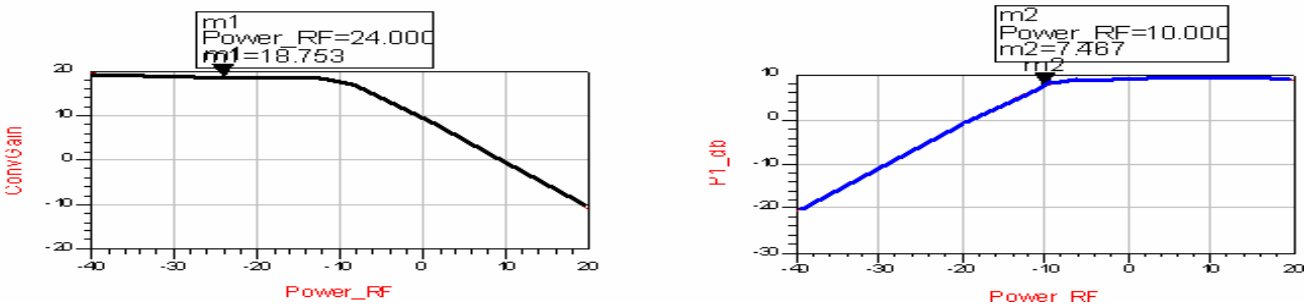


Fig. 4.9 (a) 25°C@1.0V SS of corner model simulation plots for conversion gain and P-1dB

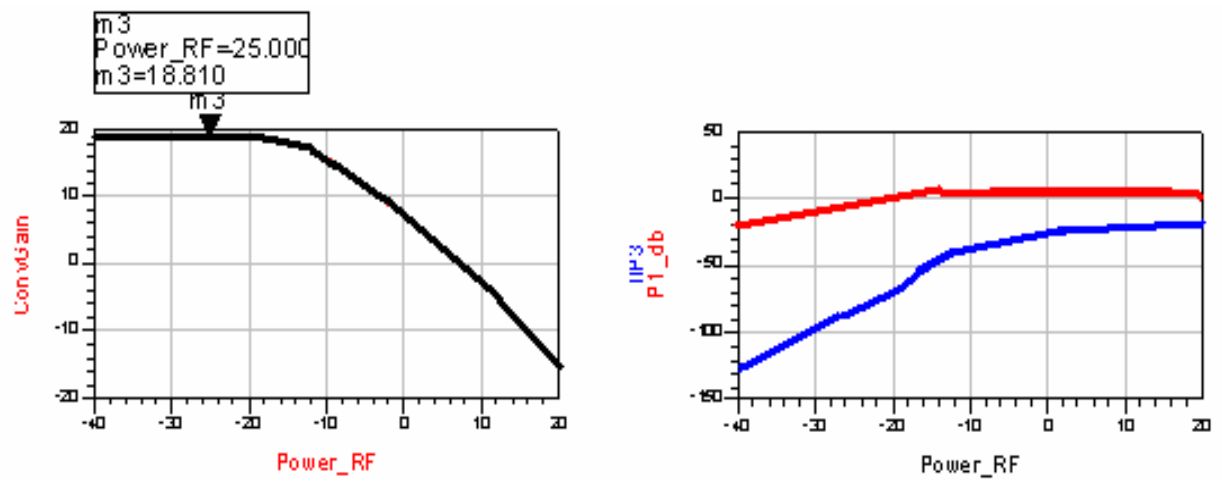


Fig. 4.9 (b) 25°C SS of corner model simulation plots on QFN chip for conversion gain and IIP3

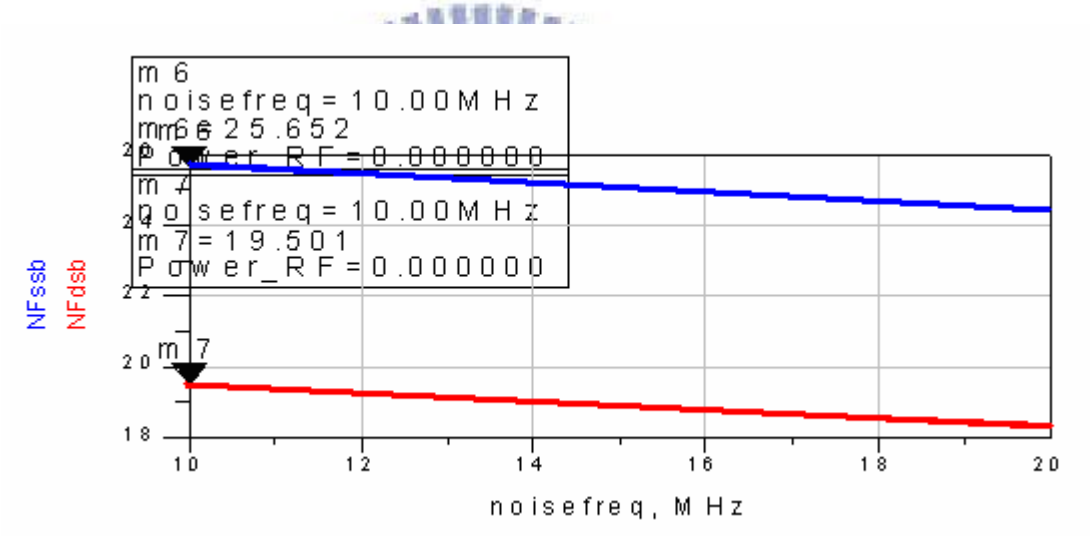


Fig. 4.9 (c) 25°C@1.0V SS of corner model simulation plots for noise figure for and DSB

(a) Simulation at 1V on QFN chip at 75°C

Table 4.7 Corner model simulation results on QFN chip in biasing 1.0V and 75 °C

Power supply voltage / Simulation Item	1V, SS, 75°C	1V, TT, 75°C	1V, FF, 75°C
Power consumption	3.148 mW	4.19 mW	5.601 mW
Conversion Gain	19.855 dB	27.971 dB	21.681
P-1dB (10MHz)	4.786 dBm	3.971 dBm	4.061 dB
IIP3	10.2 dBm	6.6 dBm	6.4 dBm
Single Side Band Noise	25.386 dB	26.643 dB	28.106 dB
Double Side Band Noise	29.506 dB	20.281 dB	21.256 dB
RF freq=5500MHz, LO freq=5499MHZ LO=2.5 dBm, IIP3 RFin =5.5 GHz			

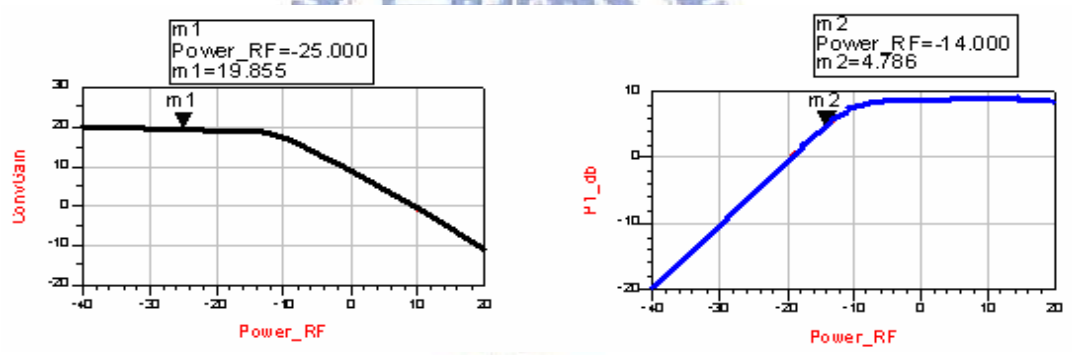


Fig. 4.10 (a) 75°C@1.0V SS of corner model simulation plots for conversion gain and P-1dB

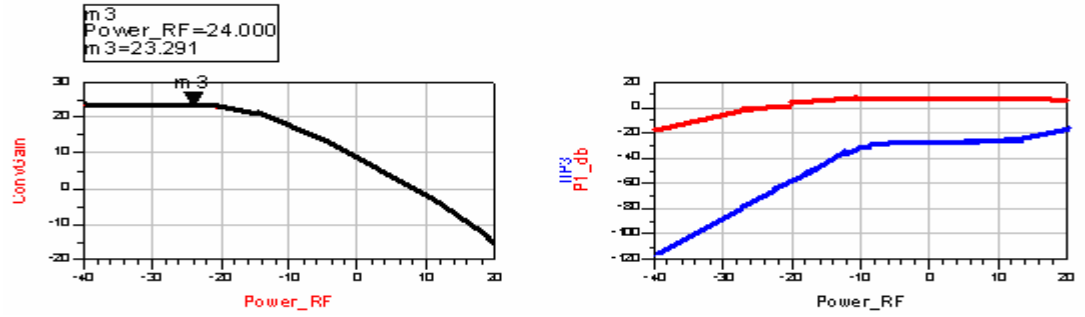


Fig. 4.10 (b) 75°C SS of corner model simulation plots on QFN chip for conversion gain and IIP3

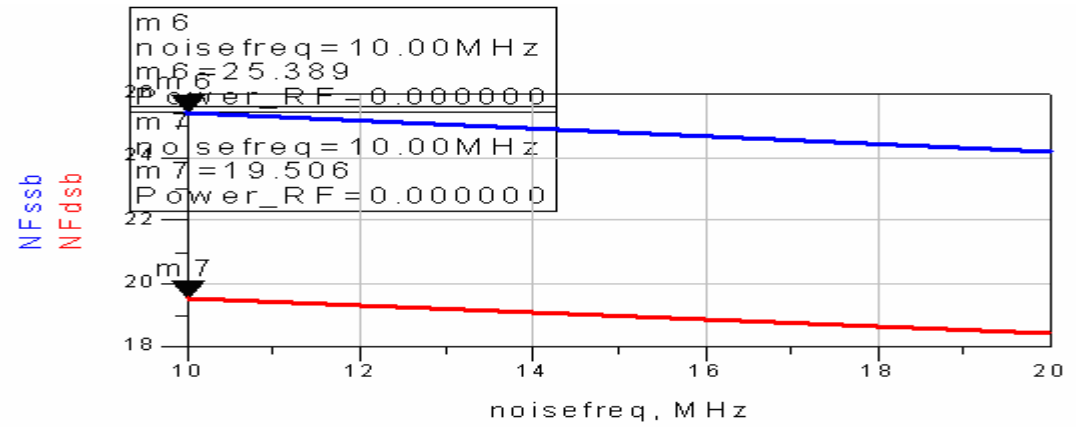


Fig. 4.10 (c) 75°C@1.0V SS of corner model simulation plots for noise figure for SSB and DSB

4.3 Chip Circuit Layout

Implementing analog and RF circuits is very difficult. Since the analog and RF of the layout will determine the analog and RF circuit performance. Even when all model parameters of the design are the same, changing he layout can totally change the performance of the circuit. Therefore, the circuit layout is an important topic, especially when the desired frequency is high.

Figure 4.11 shows a circuit layout with symmetric differential pair architecture. The symmetric layout and differential circuit architecture can improve the circuit and help overcome parasitic mismatch. Perpendicular turns of the medal must be avoided: for example, the in Fig. 4.12(b) is better than that in Fig. 4.12(a).

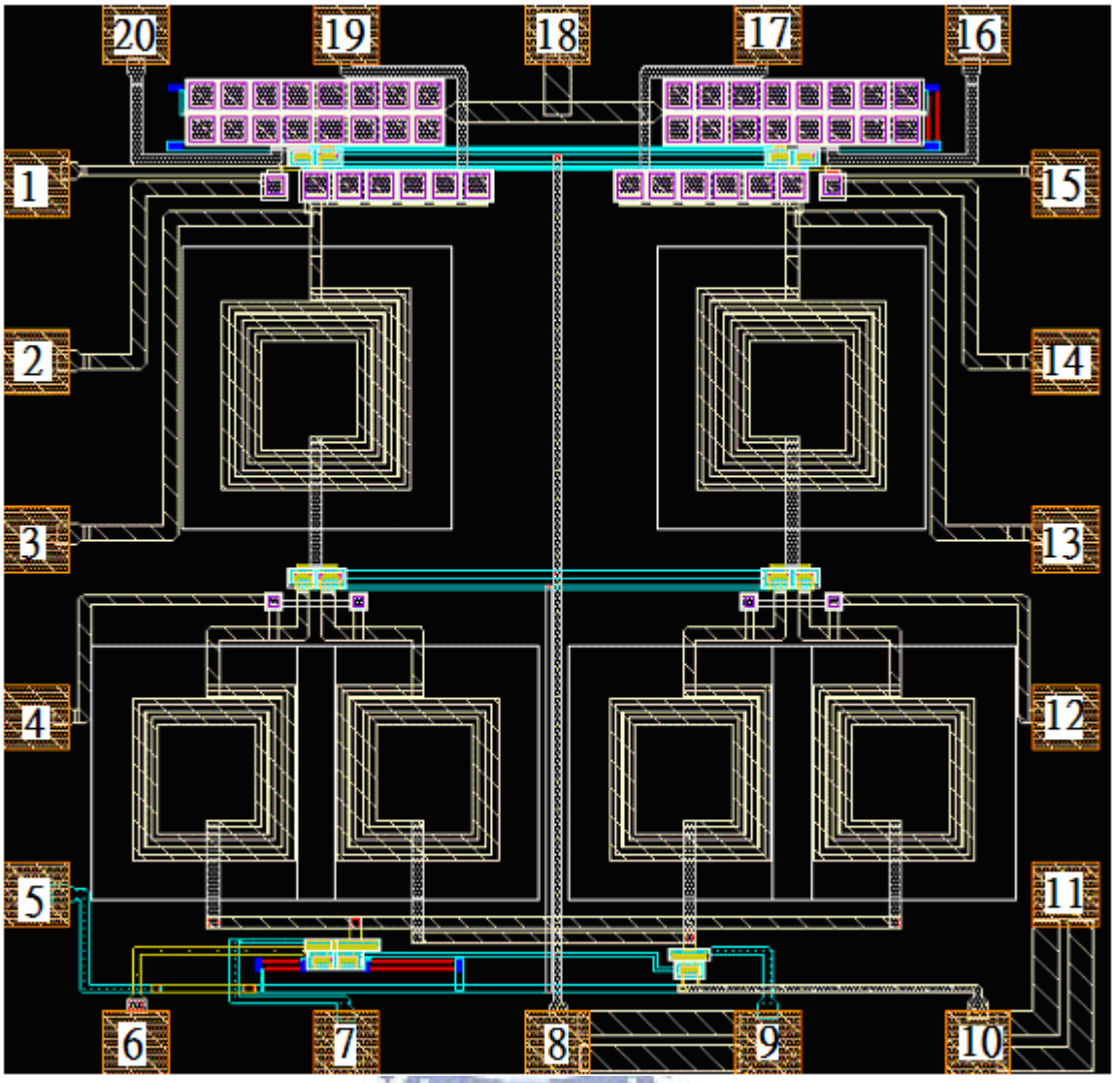
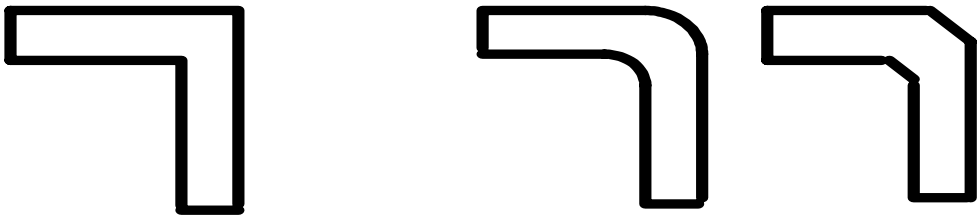


Fig. 4.11. On-wafer chip layout of mixer for symmetric layout



(a) (b)

Fig. 4.12 Turning in layout of perpendicular

Chapter 5.

Measurement

The circuit must be designed to support measurement. For RF measurement, suitable instruments and testing are very important. The following section presents the mixer measurement results in the below.

5.1 Measurement Setup

In this circuit design is measure down-conversion mixer performance. The measurement function includes conversion gain, linearity, noise figure and power consumption. Figure 5.1 shows a testing circuit board for an off-chip circuit for IF performance measurement.

Fig. 5.1 Off-chip circuit and IF test board

5.1.1 Measurement Configuration

Three signal generators from 250kHz to 40 GHz are required for two-tone testing (IIP3). An Agilent E8257D ESG is employedto support signal generation. The Agilent 8563E spectrum analyzer or Agilent Infinium oscilloscope is utilized to detect the IF output signal. The power combiner is the 2way-0° from Mini-Circuits. OPA-695 is applied for single-end output signal measurement from IF signal output. The IF output uses a high impedance to produce reasonable voltage gain. However, the standard impedance of the spectrum analysis is 50 Ω, which does not statisfy the high impedance requirement. Two methods exist to solve this problem; (a) active probe (Agilent 85024A AT Probe). (b) oscilloscope impedance set to 1MΩ. Figure 5.2 shows the setup for down-conversion mixer performance measurement.

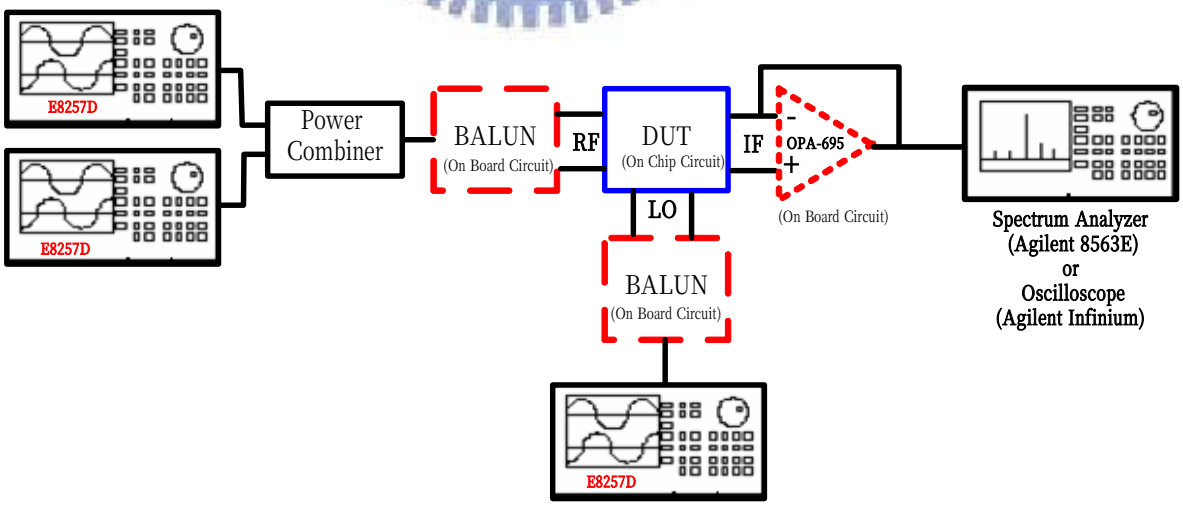


Fig. 5.2 Down-conversion mixer measurement setup diagram

5.1.2 Noise Measurement

Figure 5.3 displays the noise figure measurement setup. The noise figure is measured using the Agilent N8975A Noise Figure Analyzer with a noise source. The RF port is connected to the noise source, whose frequency is set to that of the mixer output signal to be measured, while ESG E8257D provides an LO signal to execute down-conversion..

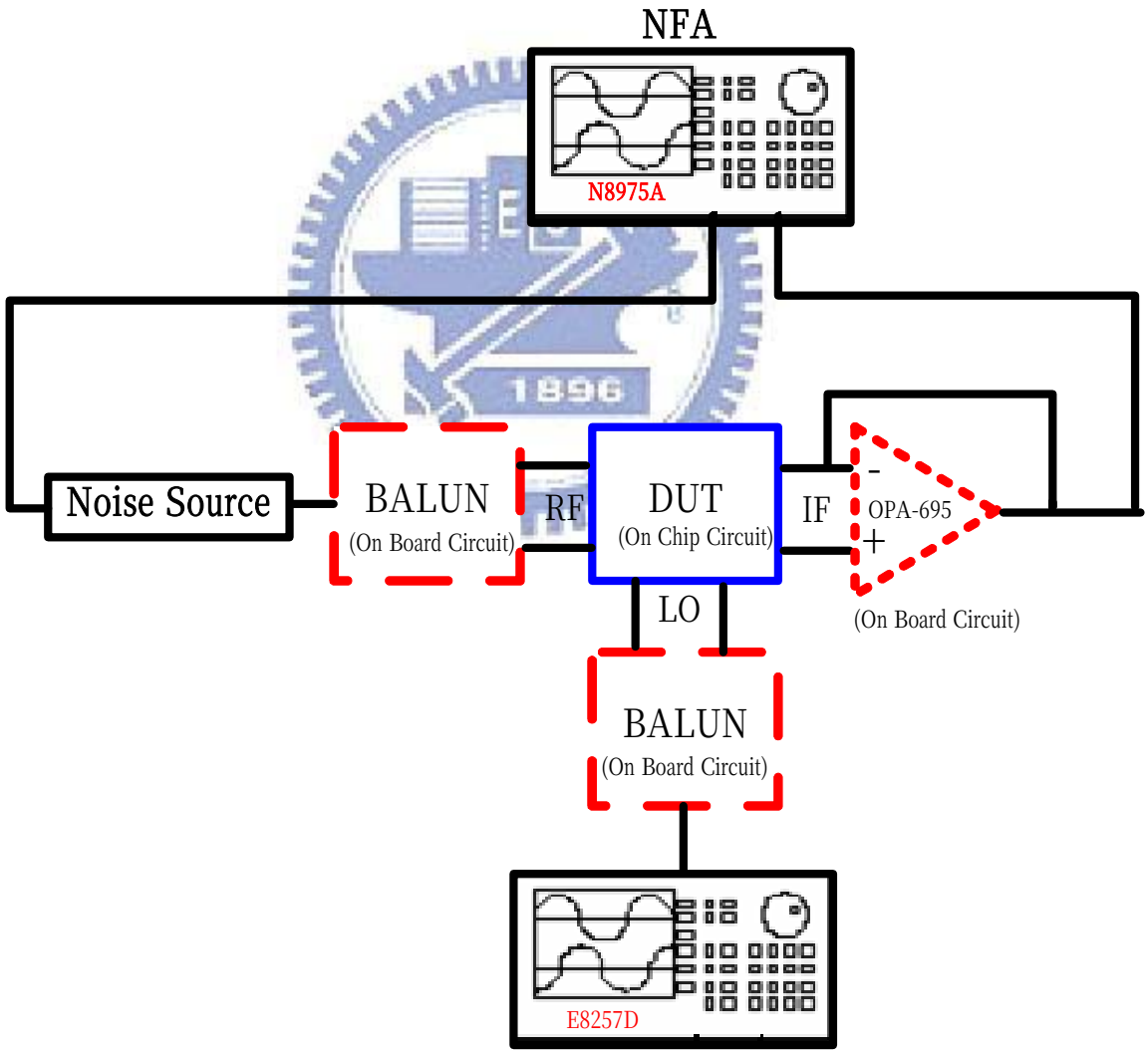


Fig. 5.3 Noise Measurement Setup

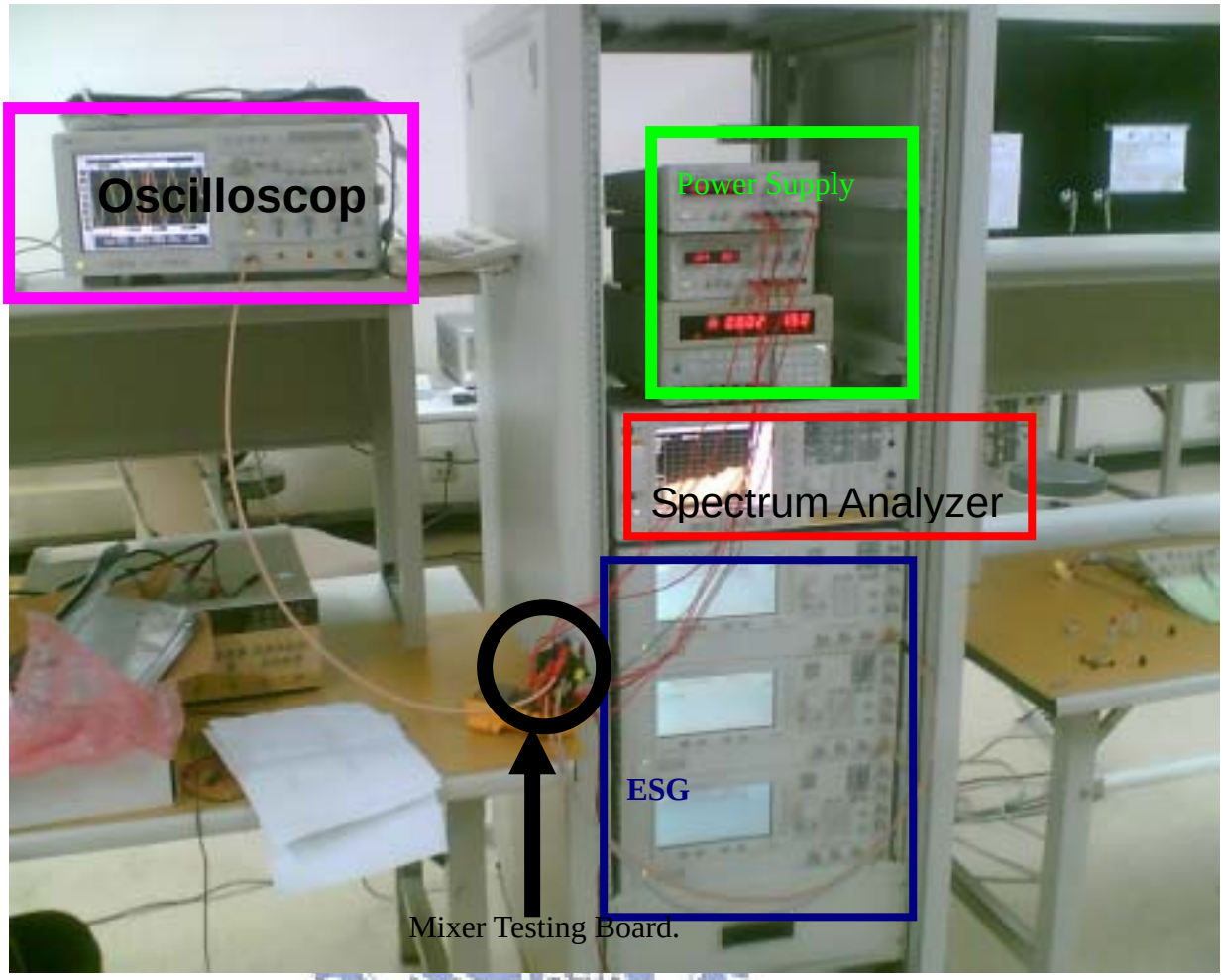


Fig. 5.4 Instruments overview in RF measured laboratory

5.2 Measurement Results

This section presents the measurement results, including conversion gain, linearity of P-1dB, IIP3, power consumption and noise figure.

5.2.1 Conversion Gain Measurement

Figure 5.5 presents measured gain vs. input power. The measured result decays to around 13 dB. This root cause is PCB, and on board SMD components characteristic not match simulation parameters, such as LC tanks, Balun circuit.

Figure 5.6 plots the conversion gain performance vs. radio frequency.

the conversion gain v.s radio frequency sweeping.

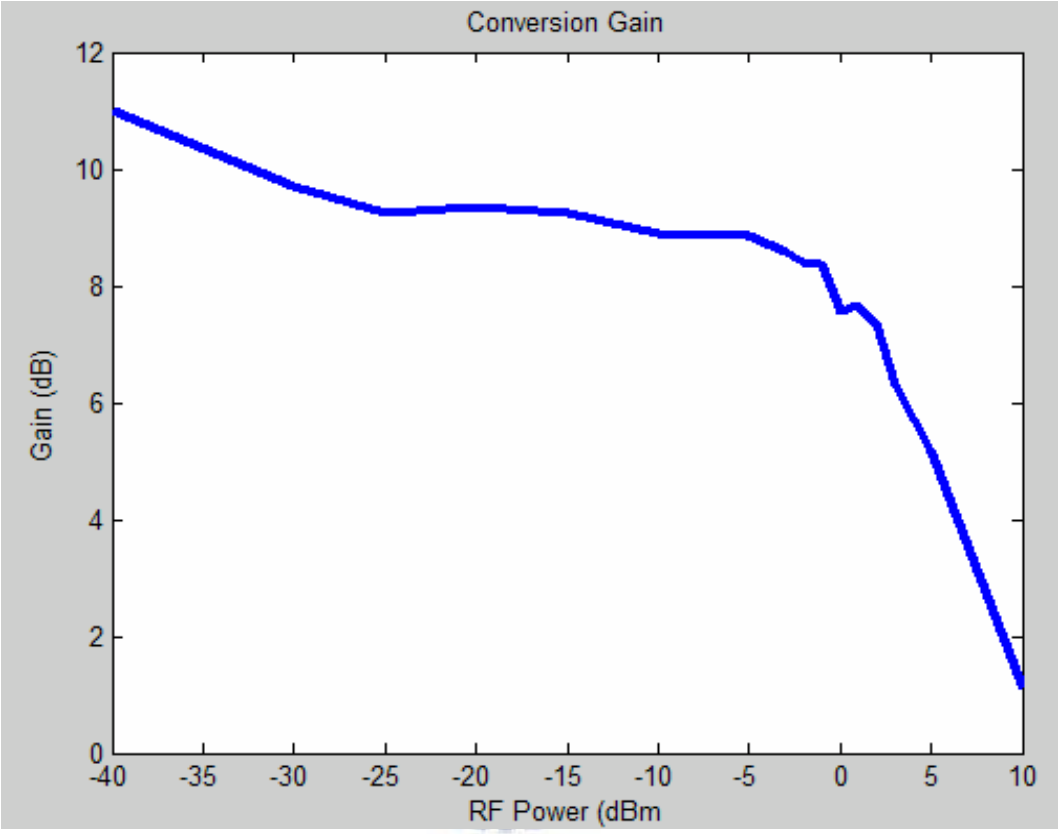


Fig. 5.5 Measured gain v.s RF Power input (RF=5.501 GHz, LO=5.500 GHz@ LO=2.5

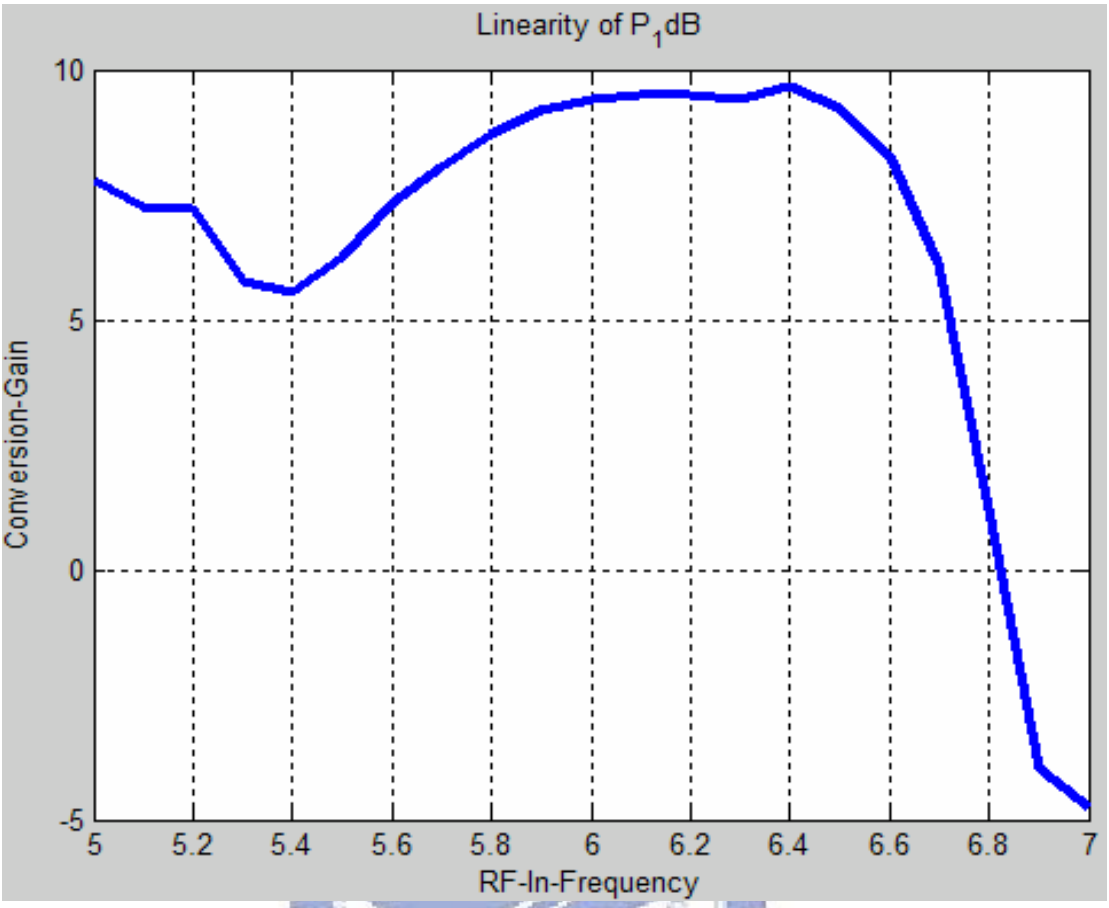


Fig. 5.6 Measured gain v.s RF input frequency (RF=0 dBm, LO=2.5 dBm, IF output is constant 1MHz)

5.2.2 P-1dB/IIP3 Measurement

P-1dB is said 1-tone tested too. The authors' laboratory has no AT probe with a spectrum analyzer. Since the simulated IF output is measured with a resistance of 1MΩ , the spectrum analyzer impedance is 50Ω. Therefore, the oscillator is employed to measure the conversion gain and P-1dB and IIP3, when the impedance is set to 1MΩ. To measure IIP3, the oscillator function FFT is adopted to obtained the output signal spectrum. Figure 5.7 plots the measured IF output magnitude. Figure 5.8 plots the measured P-1dB. The linearity of P-1dB is approximately 2.5 dBm.

The IIP3 is said that 2-tone tested too. Figure 5.9 shows the two-tone tested spectrum from the oscillator, and the RF spectrum. Figure 5.10 shows the linearity of IIP3, as displayed to Fig. 5.10. The linearity of IIP3 is approximately11 dBm.

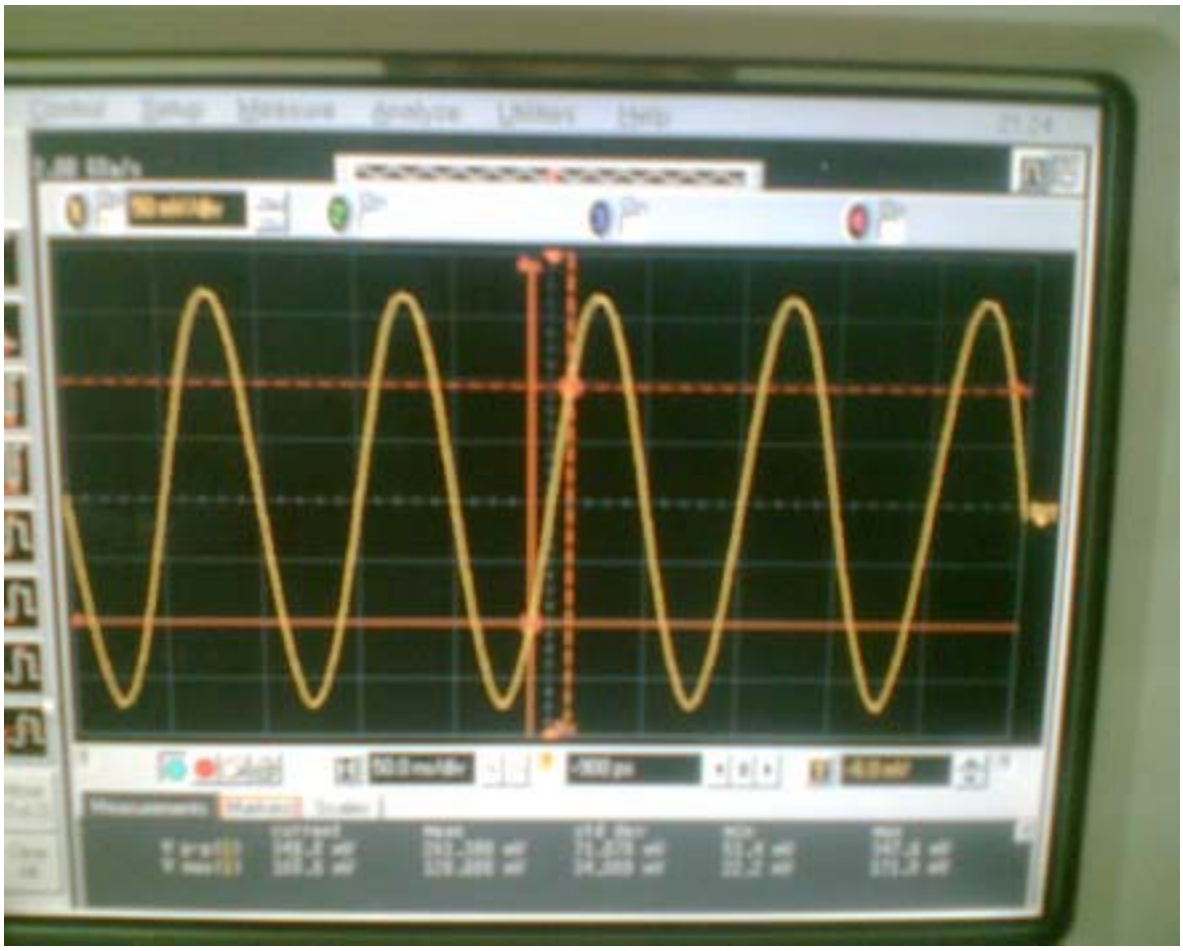


Fig. 5.7 Measured IF output magnitude

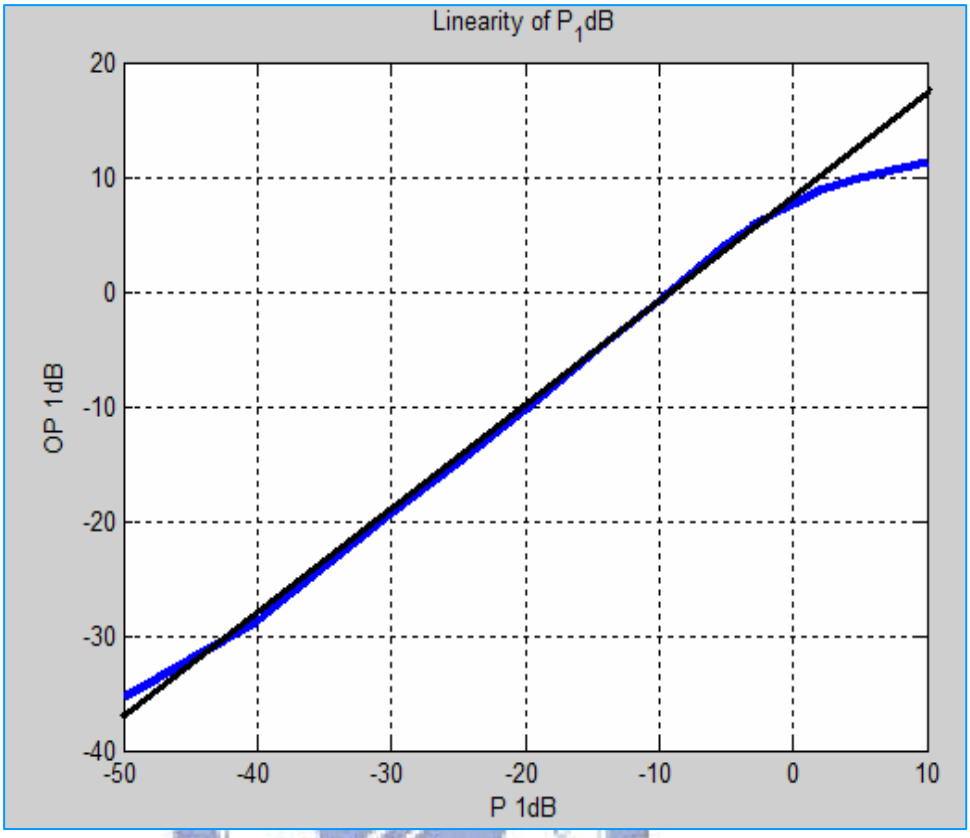


Fig. 5.8 Measured P-1dB linearity curve.

Fig. 5.9 (a) Oscillator measured 2-tone test result. .

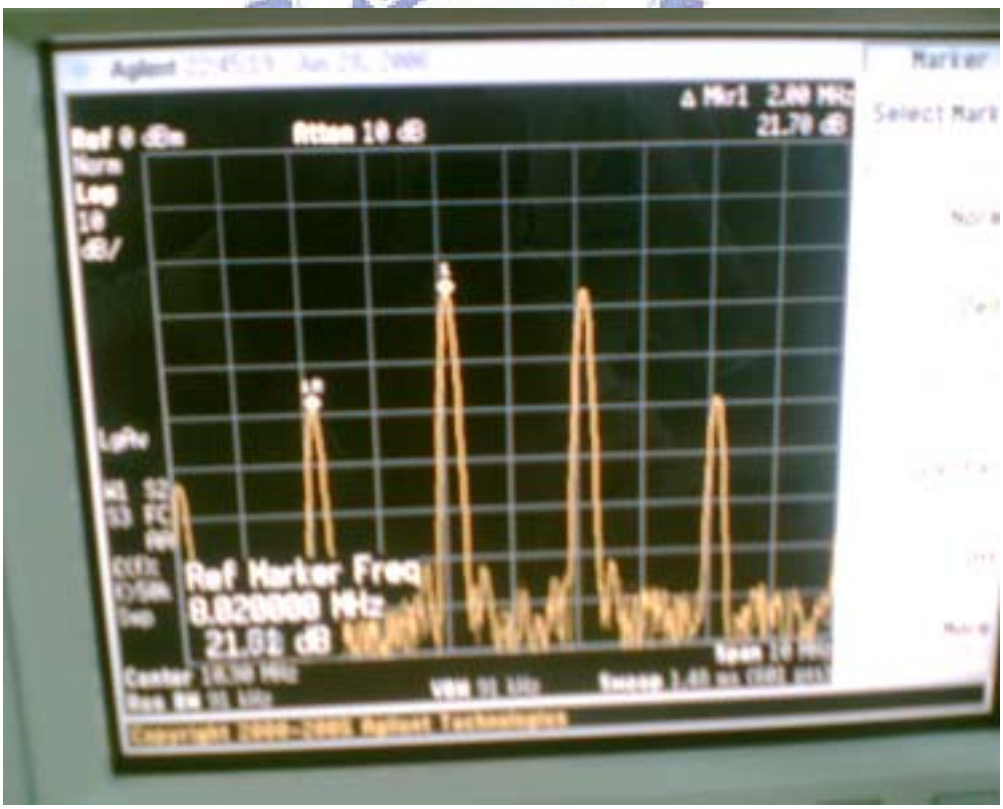


Fig. 5.9 (b) Agilent spectrum analyzer measured 2-tone test result.

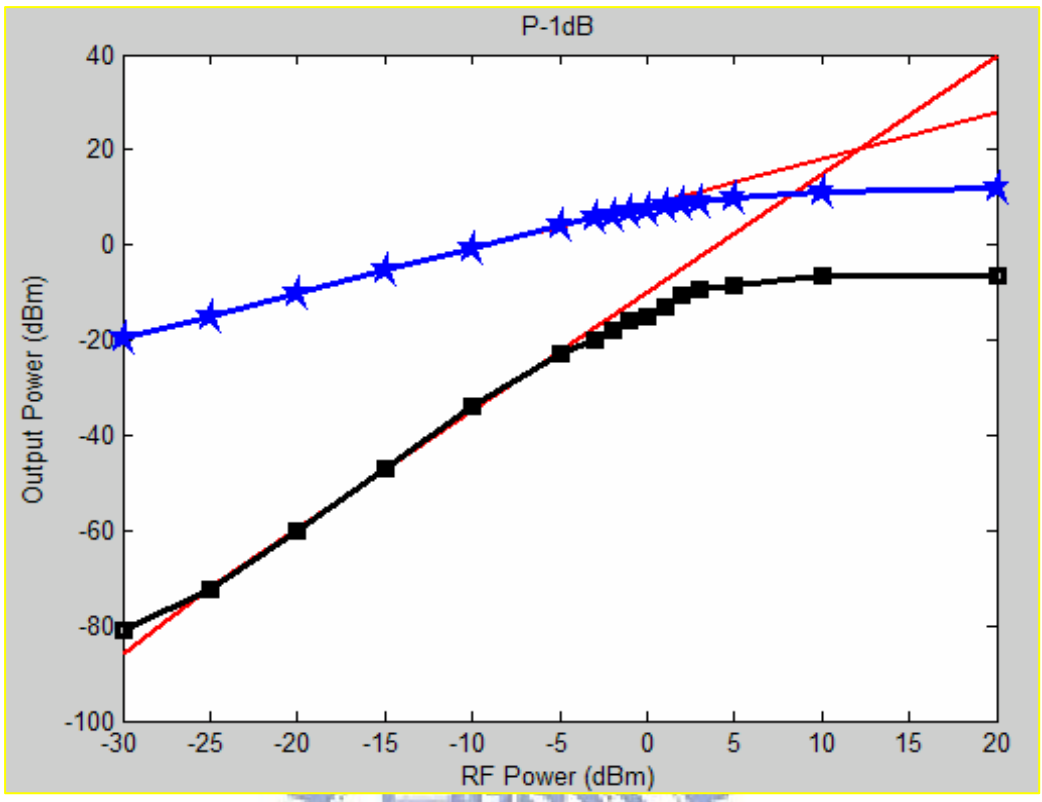


Fig. 5.10 Measured IIP3 linearity curve by 2-tone test.

5.2.3 Noise Figure Measurement

The simulation and measurement of the noise figure of RF mixer circuit is very difficult. First, since the magnitude of the noise figure of the mixer is a function of the LO signal magnitude, this magnitude is the inverse of the output noise figure magnitude. Hence, the obtaining an accurate noise figure is very difficult. Second, the noise figure analyzer provides only a single-ended measurement solution. Third, the NFA provides a loading impedance of 50 Ω instead of high impedance, with inconsistence trouble. The limited frequency range of NFA is 10M~26.5GHz. Figure 5.10 presents the mixer noise figure obtained using NFA.

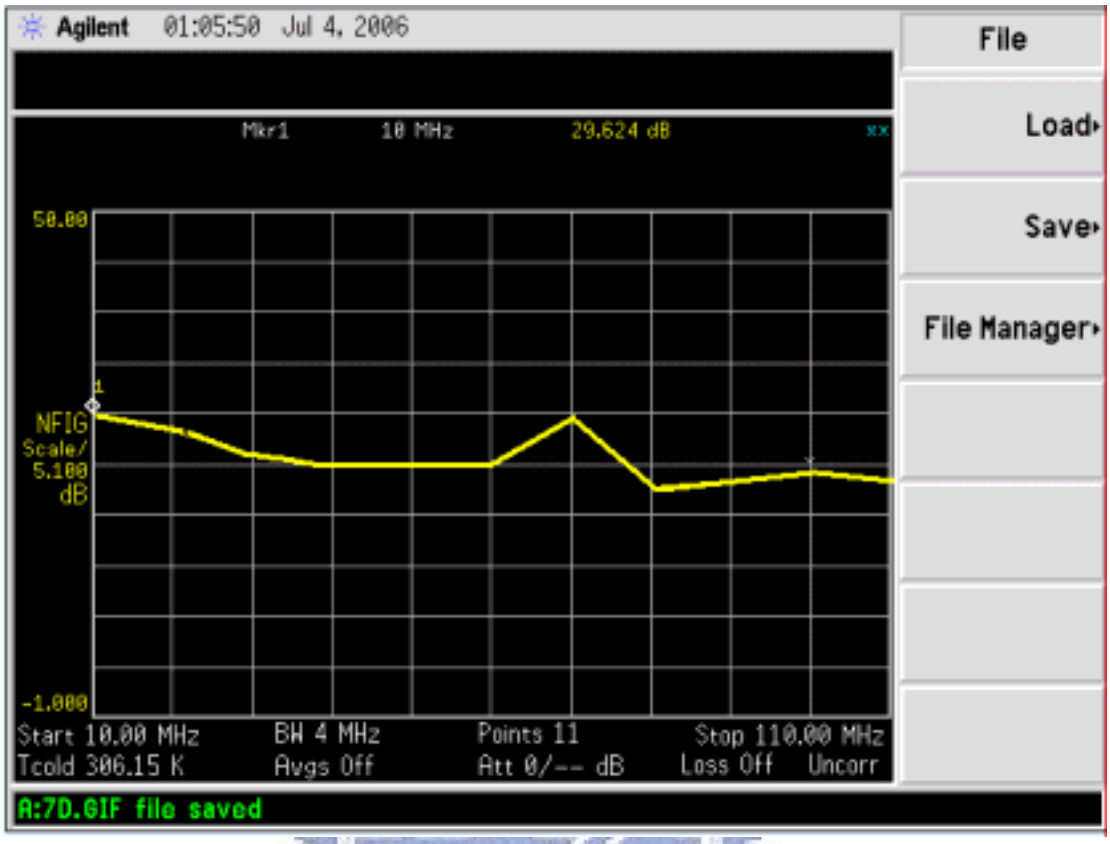


Fig. 5.11 Measured noise figure by NFA.

5.3 Summary

Table 5.1 presents the measurement results.

Table 5.1 Comparison between simulation and measurement results

Item	Simulation Result	Measurement
Power Consumption	8.1 mW	9.5 mW
Conversion Gain	8.16 dB, RF_ in@ 0dBm 25.088 dB, RF in@	7.56 dB @ 0dBm 9.40 dB @ -20
P1dB (1MHz)	5.6 dBm	2.5 dBm
IIP3	0.5 dBm	11 dBm
Single Side Band	26.55 dB	29.624 dB
RF_In =5.501 GHz, LO_In=5.5 GHz @2.5 dBm.		

Chapter 6.

Conclusion and Future Work

6.1 Conclusion

A 5.5 GHz receiver front-end mixer for IEEE WLNA 802.11a has been fabricated by 0.18 um RF CMOS technology. The measured performance of the mixer demonstrated a gain of 7.56 dB; IIP3 at 11 dBm, and the noise figure at 29.624 dB. The simulation can predict that the parallel RC circuits applied in the IF output can improve mixer linearity in terms of IIP3 and P-1dB. This circuit can be working from 5GHz to 6.8 GHz.

The deviation suffered by the measurement compare with simulation such as lower conversion gain and higher noise figure is caused by the process shift, off-chip component mismatch and the model weakness in term of QFN package inductor and resistor equivalent circuit.

6.2 Future Work

The major challenge remained with this work is the deviation between simulation and chip measurement result. It is because that simulation accuracy is acceptable for on chip Balun and LC tank design; however, there is no qualified

simulation tool for Balun and LC tank design on PCB by the method SMD. One more problem is that the resistance due to process deviation will cause shift in power consumption.

The PCB layout can be improved by considering the characteristic wavelength of microstrip line. Regarding Balun circuits design, the replacement of conventional design using passive components by active components [19], [20] can improve this circuit performance, and reduce the size of the on-wafer chip circuit layout .

In Taiwan, there are many IC design houses with strong capability in digital circuit design. Therefore, base-band circuit is generally not a big problem for most of design houses. However, competitiveness in the wireless market depends on the single chip integration with base-band, VCO, PA, LNA, mixer and a filter. The end customers want a total solution from design house in terms of a complete design flow covering from system spec definition through chip design and then to total integration.

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