New Ballasting Layout Schemes to Improve ESD Robustness of I/O Buffers in Fully Silicided CMOS Process

Ming-Dou Ker, *Fellow, IEEE*, Wen-Yi Chen, *Student Member, IEEE*, Wuu-Trong Shieh, and I-Ju Wei

***Abstract*—Silicidation has been reported to result in substantial negative impact on the electrostatic discharge (ESD) robustness of MOS field-effect transistors. Although silicide blocking (SB) is a useful method to alleviate ESD degradation from silicidation, it requires additional mask and process steps to somehow increase the fabrication cost. In this paper, two new ballasting layout schemes to effectively improve the ESD robustness of input/output (I/O) buffers with fully silicided NMOS and PMOS transistors have been proposed. Ballasting technique in layout is a cost-effective method to enhance the ESD robustness of fully silicided devices. Experimental results from real IC products have confirmed that the new ballasting layout schemes can successfully increase the HBM ESD robustness of fully silicided I/O buffers from the original 1.5 kV to over 6 kV without using the additional SB mask.**

***Index Terms*—Ballast resistance, electrostatic discharge (ESD), ESD protection, input/output (I/O) buffer, silicidation.**

I. Introduction

TO INCREASE the driving capability and maximum operating frequencies of MOS field-effect transistors (MOSFETs), silicidation has been widely adopted in chip fabrications since deep-submicrometer CMOS era. In the fully silicided CMOS technologies, the silicidation is typically carried out through metallurgical reaction between silicon and predeposited silicide metals (titanium, cobalt, or nickel) [1]–[3]. With proper annealing steps, refractory metal silicides are formed to provide a low resistivity for the diffusions and polysilicon gates of MOSFETs.

Although the low resistivity from silicides is advantageous to the driving capability and operating frequencies of MOSFETs, it has been reported that silicidation induces electrostatic discharge (ESD) degradation due to the current crowding within the shallow surface [4]–[6]. Moreover, the bend-down of silicidation located near the shallow trench isolation (STI) corner leads to the deterioration of the ESD robustness of fully silicided devices [7]. Owing to these effects during ESD stresses, silicidation has been confirmed to result in precipitous degradation on the ESD protection levels of CMOS ICs in advanced CMOS technologies.

To recover the silicidation-induced degradation on ESD robustness, CMOS processes with additional silicide blocking (SB) have been proposed [8]–[14]. Because the temperature for silicon dioxide (SiO_2) to form metallurgical silicides is higher than that for silicon, SB can be achieved by depositing sacrificial oxide on the selected regions before the deposition of silicide metal. The sacrificial oxide therefore separates the contact between silicon and the silicide metal, preventing these selected regions from silicidation during the subsequent annealing processes. By using the SB on ESD protection devices, the ESD robustness of CMOS ICs can be restored without affecting the operating speed of internal circuits. However, to deposit the sacrificial oxide and to define the selected regions for SB, additional mask and process steps are required. As a result, introducing SB into the CMOS manufacturing processes will increase the fabrication cost. To compromise with the fabrication cost, or owing to the inaccessibility of SB in some given process technologies, some cost-effective ballasting techniques have been proposed to improve the ESD robustness of fully silicided MOSFETs [15]–[28].

In this paper, the mechanism and previous works of ballasting techniques on fully silicided MOSFETs are briefly reviewed. Two new ballasting layout schemes are proposed to effectively improve the ESD robustness of input/output (I/O) buffers with fully silicided NMOS and PMOS transistors. Experimental results from real IC products fabricated in a 0.35-μm fully silicided CMOS process have confirmed that the new ballasting layout schemes can successfully increase the human body model (HBM) ESD robustness of fully silicided I/O buffers from the original 1.5 kV to over 6 kV without using the additional SB mask. Moreover, by using the new proposed ballasting layout schemes, no additional layout area of I/O buffers is required, compared to that drawn with the traditional SB technique [17].

II. Review on Ballasting Techniques for Fully Silicided I/O Buffers

Due to the huge discharging current in ESD events, current crowding has been known to cause serious impact on ESD

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M.-D. Ker is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan, and also with the Department of Electronic Engineering, I-Shou University, Kaohsiung County 84001, Taiwan (e-mail: mdker@ieee.org).

W.-Y. Chen is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan.

W.-T. Shieh and I-J. Wei are with ELAN Microelectronics Corporation, Hsinchu 30076, Taiwan.

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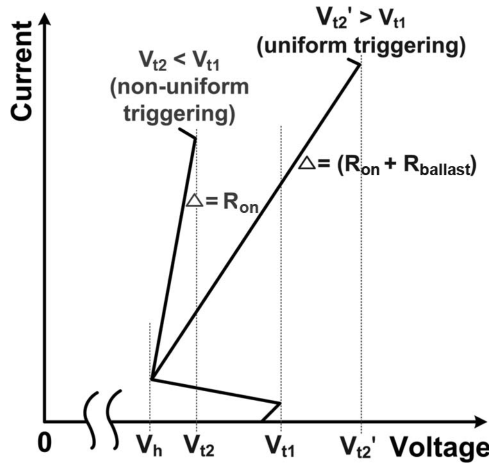

Fig. 1. Current–voltage (I–V) characteristics of gate-grounded NMOS for ESD protection, indicating the relation between V_{t2} and V_{t1} values to the uniform or nonuniform triggering.

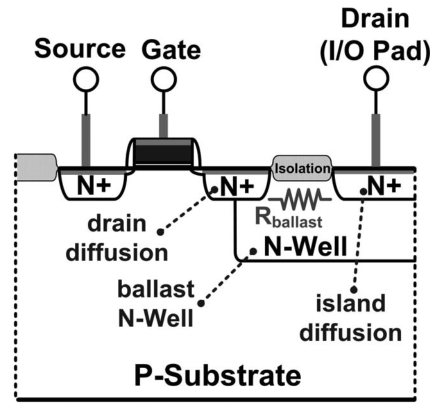

Fig. 2. Ballast N-well to increase the ballast resistance of NMOS. The separated diffusion region that connects to I/O pad is labeled as island diffusion, and the diffusion region that is closer to the gate is labeled as drain diffusion in this paper.

protection devices. By increasing the ballast resistance in the ESD protection MOSFETs, ESD current path can be spread deeper into the substrate of large volume, which, in turn, improves ESD robustness [6]. Moreover, sufficient ballast resistance can improve the turn-on uniformity of ESD protection NMOS with multifingers in layout.

In a multifinger NMOS, different distances from the drain region of each finger to the grounded guard ring result in asymmetry of substrate resistance, which causes the central fingers of NMOS to be more easily triggered on under ESD stresses [29]. After the triggering of the multifinger NMOS under ESD stresses, the ESD overstress voltage is clamped to its holding voltage (V_h) plus the product of ESD current (I_{ESD}) and the turn-on resistance (R_{on}). The typical I–V curve of gate-grounded NMOS under ESD stress is shown in Fig. 1. Without sufficient ballast resistance, $(I_{\text{ESD}} \times R_{\text{on}})$ is not large enough to make the secondary breakdown voltage (V_{t2}) higher than the trigger voltage (V_{t1}). As a result, ESD current is concentrated in some earlier turned-on area to cause local damages but the rest area cannot be triggered on in time to discharge the ESD current. Such nonuniform turn-on behavior among the multiple fingers of NMOS limits its ESD robustness, even if the NMOS was drawn with a large device dimension. By introducing the ballast resistance R_{ballast}, the turn-on resistance of the multifinger NMOS can be increased from R_{on} to $(R_{\text{on}} + R_{\text{ballast}})$. As long as the V'_{t2} can be increased greater than V_{t1}, the multifinger NMOS can be uniformly triggered on during ESD stresses [30]. As a result, sufficient ballast resistance can force ESD current being conducted into the deeper substrate and also increase the ESD robustness due to the improvement of turn-on uniformity among the multiple fingers of gate-grounded NMOS.

To realize the ballast resistance in fully silicided NMOS, one of the layout methods is to use the high sheet resistance from N-well. Fig. 2 shows the device cross-sectional view of an NMOS with the N-well ballasting technique. The ballast N-well electrically shorts the separated diffusions and contributes the desired R_{ballast} to the overall turn-on resistance of NMOS [15]–[17]. The holding voltage and the trigger voltage of NMOS may be also increased due to the insertion of ballast N-well. For the facility of description, the separated diffusion that connects to the I/O pad is labeled as the island diffusion in this paper. The other separated diffusion, which is closer to the gate of MOSFET, is labeled as the drain diffusion. The isolation in the drawing of figures in this paper represents either field oxide (FOX) or STI.

Although the ballast N-well is useful to increase the ESD robustness of fully silicided NMOS, it makes the layout area to expand due to the process ability of defining the minimum spacing between two adjacent diffusion regions. Generally, technology nodes with isolation of local oxidation of silicon (LOCOS) ask for larger spacing for two adjacent diffusion regions than those with STI isolation because of the bird's beak encroachment during wet oxidation [31]. With the finest process controllability over the gate length in CMOS technologies, replacing the separation between island and drain diffusions from FOX (or STI) to dummy polygate minimizes the spacing between two adjacent diffusion regions [18], [19]. Although the N-well ballasting technique is useful and easy to be utilized on fully silicided NMOS, it cannot be applied to fully silicided PMOS which is implemented in the N-well.

In CMOS technologies, the resistance from a single contact, via, or interconnects keeps increasing due to the constant shrinkage on either horizontal or vertical dimensions [32]. As a result, some ballasting techniques with back-end elements were used to build up the ballast resistance without increasing the process complexity [20]–[24]. By stacking as many metal layers as possible to construct a vertically meandering ESD current path, the back-end-ballast (BEB) technique is simple to increase the ballast resistance in the ESD protection MOSFETs. Poly-BEB and contact ballasting techniques further segment the current conduction path into several parallel branches and insert polysilicon or diffusion resistors in series with every back-end segmentation to facilitate the ballast of BEB technique [20]–[23]. When a local segment starts to suffer current crowding, the poly or diffusion resistor on the segment induces current defocus feedback, which forces the ESD current to redistribute, and hence improves the turn-on uniformity during ESD stresses [20], [24].

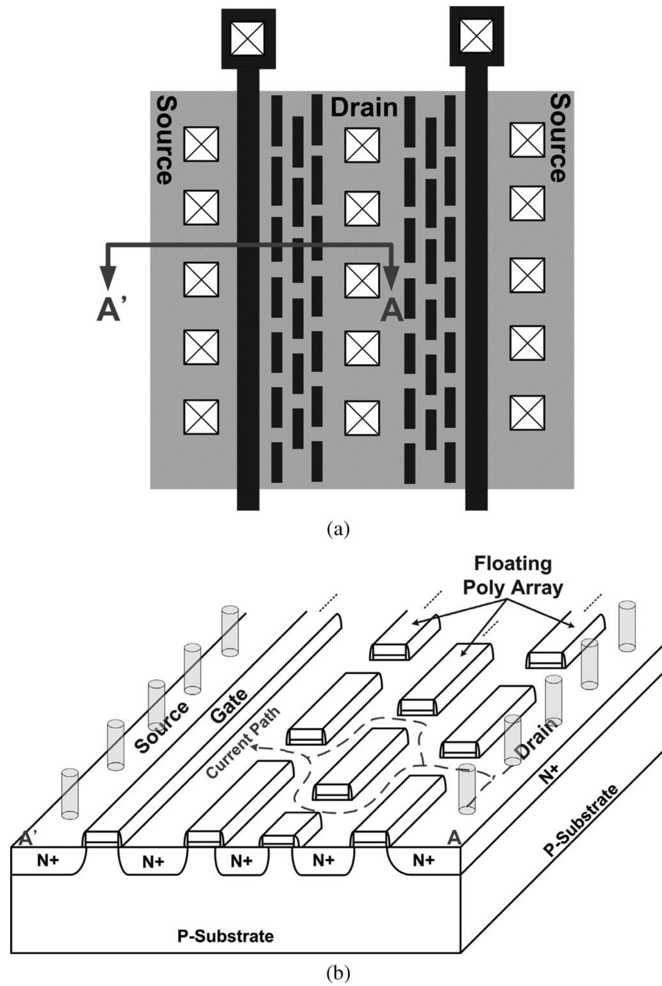

Fig. 3. (a) Layout top view and (b) device cross-sectional view along A–A' line of the fully silicided NMOS with FPA technique [27].

To further shrink the layout area of the fully silicided MOSFETs due to the additional polysilicon resistor in the poly-BEB technique, the active-area-segmentation (AAS) technique has been proposed [24]. In the AAS technique, source or drain regions are segmented to diffusion stripes to ballasts the MOSFET for ESD protection with current defocus feedback. Moreover, the AAS technique holds the potential of featuring extremely compact layout area. The bulk coupling effect therefore alleviates the nonuniform triggering and increases the ESD robustness of MOSFETs [33]. The effectiveness of the bulk coupling effect has been confirmed by floating the body of NMOS under ESD stresses [34].

Moreover, some ballasting methods manage to increase the ballast resistance by creating a horizontally meandering current path on diffusion regions, such as the staggered diffusion technique [26] and the floating polyarray (FPA) technique [27]. As the layout top view of FPA technique shown in Fig. 3(a), the interlaced FPA intervenes in the straightforward current path along A–A'. The current flow path is therefore forced to wind within the FPA, as shown in Fig. 3(b), which increases the equivalent ballast resistance to improve ESD robustness.

From the previous works, sufficient ballast resistance drives ESD current deeper into the substrate to gain better heat dissipation. The ballast resistance contributes to the overall turn-on resistance, which fulfills the $(V_{t2} > V_{t1})$ condition to enhance the turn-on uniformity of NMOS under ESD stresses. Even in the condition of $(V_{t2} < V_{t1})$, current defocus feedback and bulk coupling effect can still prevent MOSFETs from being easily filamented during ESD events.

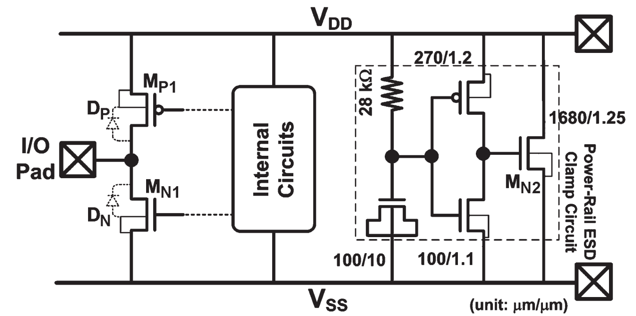

Fig. 4. Whole-chip ESD protection scheme and the corresponding device dimensions of the power-rail ESD clamp circuit used in this paper.

III. Fully Silicided I/O Buffers Under ESD Stresses

Because electrostatic charges may be either positive or negative, there are four ESD test modes at I/O pins with respect to the grounded V_{DD} or V_{SS} pins. The four ESD test modes are positive-to-V_{SS} (PS), positive-to-V_{DD} (PD), negative-to-V_{SS} (NS), and negative-to-V_{DD} (ND) modes [35], [36]. Due to the variety of test combinations, both the NMOS and PMOS in an I/O buffer are susceptible to ESD failure. For example, the PS-mode ESD tests can lead to breakdown of the driver NMOS, whereas the ND-mode ESD tests can lead to breakdown of the driver PMOS. Although the whole-chip ESD protection scheme equipped with power-rail ESD clamp circuit is effective to discharge ESD energy by avoiding junction breakdown of I/O buffers [36], an overshooting or undershooting voltage is still harmful to the I/O buffer, particularly under the conditions with high ESD stress voltage.

In this section, the effectiveness of the N-well ballasting technique to the whole-chip ESD robustness of fully silicided I/O buffers is investigated. Chips are fabricated in a 0.35-μm 5-V fully silicided CMOS process with LOCOS isolation. SB is not available in this process due to the consideration of cost reduction. Because the N-well ballasting technique cannot be applied to PMOS, the driver PMOS in I/O buffer discussed in this section was left unballasted. All I/O buffers in this paper are self-protected, which have no additional ESD protection device connected to the I/O pad. The whole-chip ESD protection scheme with the corresponding device dimensions is shown in Fig. 4. The operating frequency specification of the I/O buffers in this paper is 20 MHz. The main ESD protection NMOS (M_{N2}) in the active power-rail ESD clamp circuit has a total device dimension (W/L) of as large as 1680 μm/1.25 μm. For fully silicided I/O buffers without ballasting, no ballasting technique was applied to M_{N2} of the power-rail ESD clamp circuit. With the proposed layout schemes in this paper, the N-well ballasting technique was also applied to M_{N2} of the

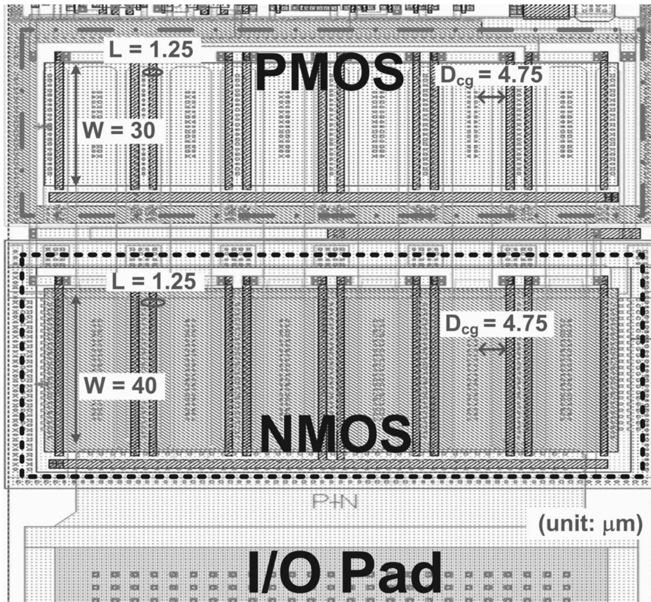

Fig. 5. Layout top view of the self-protecting fully silicided I/O buffer in a CMOS IC product.

power-rail ESD clamp circuit when such N-well ballasting technique was applied in the I/O buffers.

The target for ESD robustness of those IC products requested by customers is to pass a 6-kV HBM ESD test [35]. To verify the ESD robustness, the starting voltage of HBM ESD test is 0.5 kV, and the step voltage during ESD tests is 0.5 kV. Each pin is stressed three times with the specified HBM ESD level, and the failure criterion is I–V curve shifted over 20% as compared to the original I–V curve before ESD stress. The test will stop when ESD failure happens on one or more I/O (including power) pin(s).

A. Fully Silicided I/O Buffer Without Ballasting

In nowadays CMOS ICs, to minimize the required layout area for I/O buffers, self-protecting I/O design (I/O buffer without additional ESD protection devices) is usually adopted. The layout of the self-protecting I/O buffers in a CMOS IC product is shown in Fig. 5. Gate length in the I/O buffer is increased to avoid the reverse channel length dependence [37]. The device dimension for driver NMOS (M_{N1}) is 480 μm/1.25 μm with each finger width of 40 μm, and the device dimension for driver PMOS (M_{P1}) is 360 μm/1.25 μm with each finger width of 30 μm. The spacing for drain contact to polygate edge (D_{cg}) is 4.75 μm for both driver NMOS and PMOS, which is originally drawn for SB rules. However, to reduce the fabrication cost, no SB is adopted in the given CMOS process for IC production. The main ESD protection NMOS in the active power-rail ESD clamp circuit has the same layout style as that of the driver NMOS in I/O buffer.

The ESD test results in Table I show that the fully silicided I/O buffers without ballasting failed to pass the essential ESD specification of 2-kV HBM ESD stresses. Among the ESD measurements of the unballasted I/O buffers, PS-mode ESD test shows the lowest ESD protection level. Under the PS-mode ESD stresses, the ESD current is first discharged to V_{DD} through the forward diode D_P inherent in M_{P1} and to the grounded V_{SS} through the power-rail ESD clamp circuit. In spite of the gate-driven technique to enhance the turn-on speed of the power-rail ESD clamp circuit during ESD stresses [38], [39], the overshooting voltage on the I/O pad cannot be completely suppressed due to the inevitable turn-on resistance of devices and interconnects. Consequently, due to the lack of proper ballasting design, when the overshooting voltage on the I/O pad induces breakdown on the fully silicided driver NMOS, it is easily filamented due to severe current crowding and nonuniform triggering. A scanning electron microscope (SEM) image of the unballasted I/O buffer after 2-kV PS-mode ESD stress is shown in Fig. 6, where the trace of current filamentation is found on the driver NMOS. The failure analysis (FA) result has verified that the driver NMOS is driven into breakdown during the 2-kV PS-mode ESD test. Nonuniform triggering among the multiple fingers of the unballasted driver NMOS can be clearly observed in Fig. 6, since ESD failure only locates on one of the fingers. Moreover, the ESD failure is located on the central portion of the finger. The central portion of the finger is farther from the grounded guard ring, so that the larger equivalent substrate resistance makes the parasitic bipolar junction transistor (BJT) inherent in the central portion easier to be triggered. The burned-out trace from drain to the grounded source through silicon surface further indicates that insufficient ballast resistance makes the ESD current to crowd on the surface with limited shallow depths. Accordingly, a D_{cg} spacing of 4.75 μm in a fully silicided NMOS is insufficient to provide adequate ballast resistance due to the small sheet resistance from silicides.

B. I/O Buffer With N-Well Ballasting Technique on Driver NMOS

To enhance the PS-mode ESD robustness, the N-well ballasting technique was applied to the driver NMOS of I/O buffer [15]. The main ESD protection NMOS (M_{N2}) in the active power-rail ESD clamp circuit was also implemented with N-well ballasting. The driver PMOS was still left unballasted in this test. Fig. 7 shows the diagram of the I/O buffer with a sketch of its metal connection to the I/O pad. To keep the same cell width of I/O buffers in IC chips, both D_{cg} spacing and gate length are kept the same as those in the I/O buffers without ballasting. Spacing for island diffusion and drain diffusion is 1.75 μm in layout. In the I/O buffers with N-well ballasting, each finger width of driver NMOS is 30 μm, and each finger width of driver PMOS is 25 μm. The total device dimension (W/L) of NMOS (PMOS) in I/O buffer is 360 μm/1.25 μm (300 μm/1.25 μm). The driver NMOS with ballast N-well in this test was laid out with truncation to the island diffusions to prevent ESD damage from the tips of N+ island diffusions to the P+ guard ring. With a foundry-provided N-well sheet resistance of 800 $\Omega/\Box$, the overall resistance imposed on NMOS (with 12 fingers in parallel) due to the ballast N-well is 800 $\Omega \times (1.75\ \mu\mathrm{m}/30\mu\mathrm{m}) \div 12 = 3.88\ \Omega$. With the operating frequency specification of 20 MHz in this paper, the driving capability can be effectively compensated by suitable transistor sizing to meet the desired specification

TABLE I
ESD ROBUSTNESS AMONG THE I/O BUFFERS STUDIED IN THIS PAPER

	HBM ESD Robustness (unit: kV)				
	PS-mode	PD-mode	NS-mode	ND-mode	V_{DD}-to-V_{SS}
Fully-Silicided I/O Buffer without Ballasting	1.5	2.5	> 8	4.5	> 8
I/O Buffer with N-Well Ballasting Technique on NMOS	7	> 8	> 8	4	> 8
I/O Buffer with the New Proposed Type-A Layout Scheme	6	6	> 8	> 8	> 8
I/O Buffer with the New Proposed Type-B Layout Scheme	7	> 8	> 8	> 8	> 8

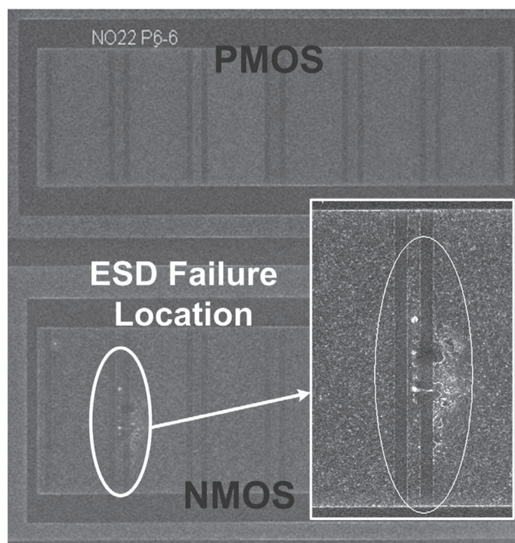

Fig. 6. SEM image of the fully silicided I/O buffer without ballasting after 2-kV PS-mode ESD stress. ESD failure is found on only one finger of the driver NMOS. Current filamentation is also observed on the surface of the driver NMOS without ballasting.

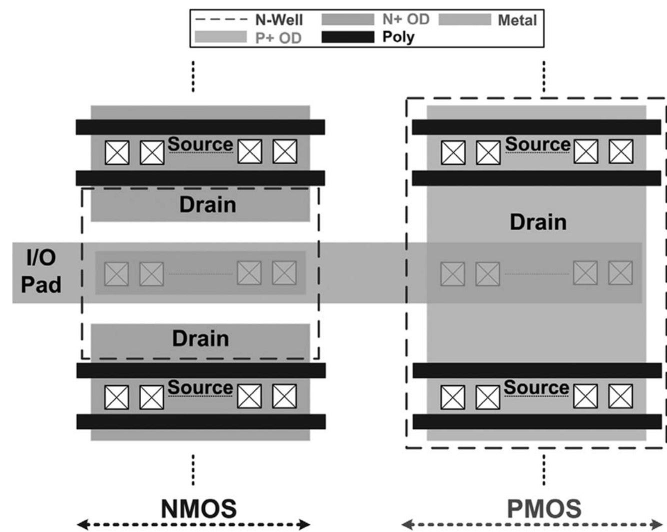

Fig. 7. Diagram to show the metal connection to the I/O pad for the driver NMOS with ballast N-well but the driver PMOS without ballasting.

of I/O applications. For example, the output resistance of a driver NMOS with 12-mA driving specification is $0.4\ \text{V} \div 12\ \text{mA} = 33.33\ \Omega$, which is much higher than the 3.88-Ω parasitic resistance from ballast N-well.

Moreover, the parasitic junction capacitance (C_j) and sidewall capacitance (C_{jsw}) of N-well/P-substrate junction are $1.08 \times 10^{-4}\ \text{pF}/\mu\text{m}^2$ and $7.32 \times 10^{-4}\ \text{pF}/\mu\text{m}$, respectively. The C_j and C_{jsw} of N+/P-substrate junction are $6.19 \times 10^{-4}\ \text{pF}/\mu\text{m}^2$ and $2.58 \times 10^{-4}\ \text{pF}/\mu\text{m}$, respectively. Although the C_{jsw} value for N-well is higher than the C_{jsw} value for N+ diffusion, the C_j value for N-well is much lower than the C_j value for N+ diffusion due to the larger depletion width of N-well/P-substrate junction. For self-protecting driver NMOS, due to the large device width and the increased drain contact to polygate spacing, the C_j value will take a major portion in the overall junction capacitance. As a result, the added capacitance due to ballast N-well can be still small without affecting the I/O operating frequency specification of 20 MHz in this paper.

The ESD measurement results for the I/O buffers with N-well ballasting technique are shown in Table I. Although the N-well ballasting technique substantially increases PS-mode ESD robustness to 7 kV, the 4-kV ND-mode ESD test result has become the bottleneck for the I/O buffers to attain the performance target of 6-kV HBM ESD robustness.

During the ND-mode ESD tests, ESD current is discharged through the power-rail ESD clamp circuit and the forward diode D_N inherent in the driver NMOS. As a result, the voltage across the V_{DD} and I/O pad is

$$\Delta V_{\text{ND}} = [I_{\text{ESD}} \times (R_{\text{on,Power-Rail}} + R_{\text{VSS}} + R_{\text{on,DN}}) + V_{t,\text{DN}}] \quad (1)$$

where the $R_{\text{on,Power-Rail}}$ and $R_{\text{on,DN}}$ denote the turn-on resistance of power-rail ESD clamp circuit and the diode D_N during ESD stresses, R_{VSS} denotes the effective resistance of the V_{SS} interconnection, and $V_{t,\text{DN}}$ denotes the cut-in voltage of the diode D_N. At high I_{ESD} level, i.e., high ESD stress voltage, the ΔV_{ND} can exceed V_{t1} of the driver PMOS, which, in turn, induces the parasitic p-n-p BJT in the PMOS to be turned on. As a result, part of the ESD current is discharged through the driver PMOS under high ESD current conditions. Due to the lack of proper ballasting, the ESD current discharged through the driver PMOS is crowded within the shallow surface,

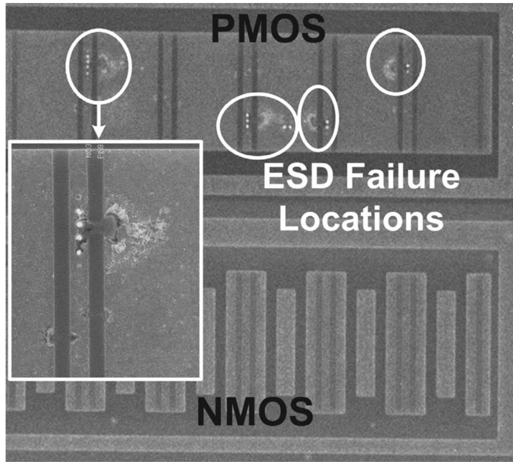

Fig. 8. SEM image of the fully silicided I/O buffer with N-well ballasting technique on the driver NMOS after 4.5-kV ND-mode ESD stress. Failure locations are found on the driver PMOS due to the triggering of p-n-p BJT inherent in PMOS.

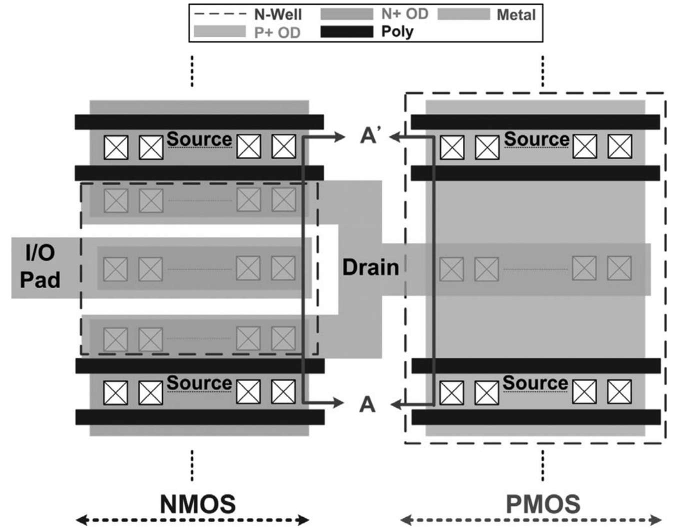

Fig. 9. Diagram to show the metal connection to the I/O pad for the driver NMOS realized with type-A layout scheme.

which further deteriorates the ESD robustness of driver PMOS. For I/O buffers with N-well ballasting technique on the driver NMOS, the PMOS has smaller device width than that in the fully silicided I/O buffers in this paper. Accordingly, although the driver PMOSs in the two structures are both fully silicided without ballasting, I/O buffer with N-well ballasting technique on driver NMOS has lower ND-mode ESD robustness (4 kV) compared to the ND-mode ESD robustness of fully silicided I/O buffer without ballasting (4.5 kV).

The SEM image of the I/O buffer after 4.5-kV ND-mode ESD stress is shown in Fig. 8. Current traces from the source of driver PMOS toward its drain regions are observed, which confirms that the breakdown of the unballasted driver PMOS is the limitation to the ESD robustness of I/O buffer with N-well ballasting technique. Failure spots are found within more than one of the PMOS fingers, because PMOS devices barely exhibit snapback phenomenon in deep-submicrometer CMOS technologies [6].

IV. New Layout Schemes to Improve the ESD Robustness of Fully Silicided I/O Buffers

Although the N-well ballasting technique prevents PS-mode ESD failure on the driver NMOS and increases the whole-chip ESD protection level from 1.5 to 4 kV, it still cannot achieve the adequate performance target of 6-kV HBM ESD robustness. From the ESD measurement and FA results, ballasting technique on the driver PMOS is vital to the improvement of ESD robustness on fully silicided I/O buffers. As a result, two new layout schemes are proposed to ballast both NMOS and PMOS devices in the I/O buffer. The new proposed designs have been verified in some IC products fabricated in the same 0.35-μm 5-V fully silicided CMOS process and have been confirmed with substantial improvement on the whole-chip ESD protection level.

A. I/O Buffer With the New Proposed Layout Scheme (Type A)

To provide efficient ballast on the driver PMOS, Fig. 9 shows the diagram of type-A layout scheme. The driver NMOS in the type-A layout scheme is drawn with N-well ballasting. However, the drain of the driver PMOS is not connected directly to the I/O pad. Instead, the drain of PMOS is connected to the drain diffusion of driver NMOS, which is electrically connected to the I/O pad by means of the ballast N-well. The driver NMOS and PMOS in the type-A layout scheme have the same device dimensions as those in the I/O buffers with N-well ballasting technique on driver NMOS. The main ESD protection NMOS (M_{N2}) of the power-rail ESD clamp circuit in this scheme is N-well ballasted. Device cross-sectional view along the A–A' line of the I/O buffer with the type-A layout scheme in Fig. 9 is shown in Fig. 10. It can be understood from Fig. 10 that only the island diffusion of driver NMOS is directly connected to the I/O pad. Through such a layout arrangement, PMOS current is forced to flow through the N-well ballast resistor in the driver NMOS, making the N-well to ballast for both driver NMOS and PMOS during ESD stresses.

In type-A layout scheme, the ESD current under PS-mode ESD tests first flows to the floating $V_{\rm DD}$ through the N-well ballast resistor and the D_P diode. Then, the ESD current is discharged to the grounded $V_{\rm SS}$ through the power-rail ESD clamp circuit. Under the PD-mode ESD tests, the ESD current is first discharged to the grounded $V_{\rm DD}$ through the N-well ballast resistor and the D_P diode. Therefore, voltages across the stressed I/O pad and ground under the PS- and PD-mode ESD tests are

$$\Delta V_{\rm PS} = [I_{\rm ESD} \times (R_{\rm ballast} + R_{\rm on,DP} + R_{\rm VDD} + R_{\rm on,Power-Rail}) + V_{t,\rm DP}] \tag{2}$$

$$\Delta V_{\rm PD} = [I_{\rm ESD} \times (R_{\rm ballast} + R_{\rm on,DP} + R_{\rm VDD}) + V_{t,\rm DP}]. \tag{3}$$

With the ESD current being forced to flow through the N-well under PS- and PD-mode conditions, it has been reported that the N-well resistor under high current level exhibits high resistance characteristic due to drift velocity saturation [17]. As the TLP measurement results shown in Fig. 11, under

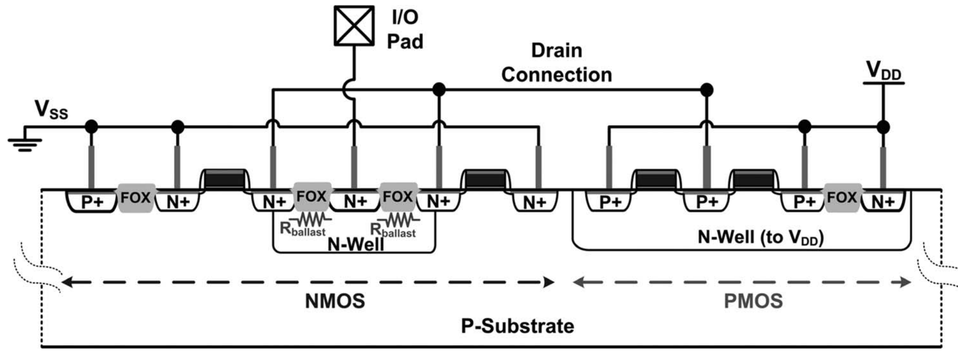

Fig. 10. Cross-sectional view along the A–A' line of the fully silicided I/O buffer realized with type-A layout scheme.

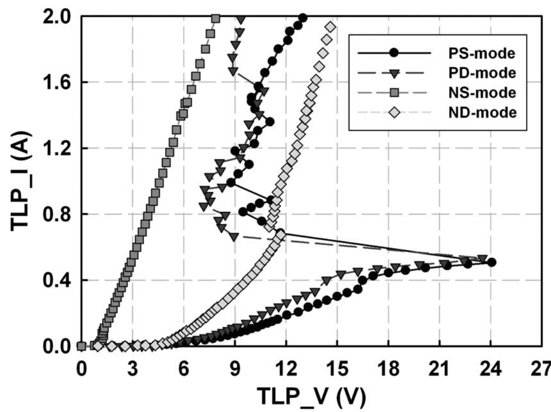

Fig. 11. TLP-measured I–V curves for the I/O buffer with type-A layout scheme. The tests were manually stopped at 2 A without causing failure to the I/O buffer.

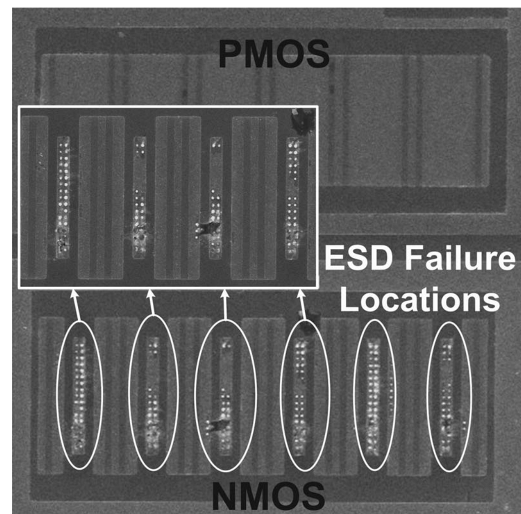

Fig. 12. SEM image of the fully silicided I/O buffer realized with type-A layout scheme after 6.5-kV PS-mode ESD stress. Uniformly distributed N+-to-N-well ESD damages are found on the driver NMOS.

PS-mode (positive TLP stress on I/O pad with $V_{\rm SS}$ relatively grounded) and PD-mode (positive TLP stress on I/O pad with $V_{\rm DD}$ relatively grounded) TLP measurements, the drift velocity saturation results in the 24-V voltage at an $I_{\rm ESD}$ of 0.5 A. The applied voltage is mainly dropped within the N-well region. At the same time, electron-hole pairs are generated to support the increased current, and electric field is built up toward the N+ island diffusion/N-well junction. The electric field buildup eventually results in avalanche breakdown to happen at the N+/N-well junction, which results in the snapback as shown in Fig. 11. With the avalanche breakdown at N+/N-well junction, the hole concentration can exceed the background doping of N-well, which results in conductivity modulation and lowers the turn-on resistance of N-well [40], [41]. For NS-mode (positive TLP stress on $V_{\rm SS}$ pin with I/O pin relatively grounded) and ND-mode (positive TLP stress on $V_{\rm DD}$ pin with I/O pin relatively grounded) TLP measurements, ESD currents are discharged through the D_N diode and power-rail ESD clamp circuit (in ND-mode test) without flowing through the ballast N-well. Therefore, the high resistance characteristic from N-well is not observed in the ND- and NS-mode TLP I–V curves in Fig. 11.

The HBM ESD measurement results in Table I show that the fully silicided I/O buffers with type-A layout scheme have the PS- and PD-mode ESD protection level as high as 6 kV. Under the ND-mode ESD tests, although the $\Delta V_{\rm ND}$ can exceed V_{t1} of the driver PMOS under high ESD stress voltage, the N-well

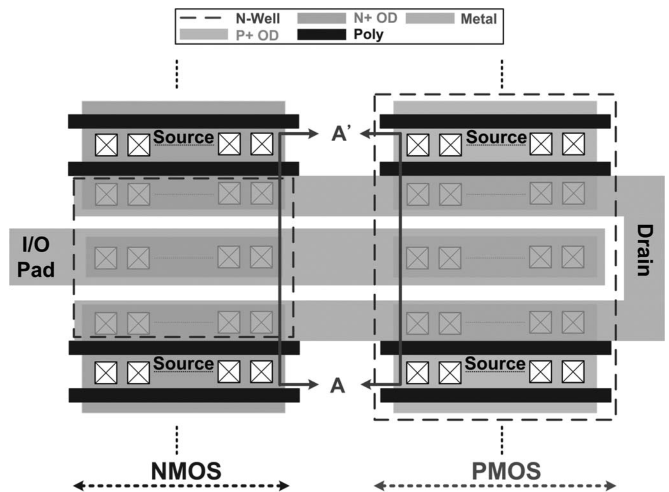

Fig. 13. Diagram to show the metal connection to the I/O pad for driver NMOS and PMOS in the type-B layout scheme.

ballast resistor suppresses the ESD current discharged through the PMOS. Accordingly, fully silicided I/O buffers with type-A layout scheme have an ND-mode HBM ESD robustness of over 8 kV. By using the type-A layout scheme, ND-mode ESD failure on the driver PMOS has been successfully overcome, and the 6-kV performance target has been achieved.

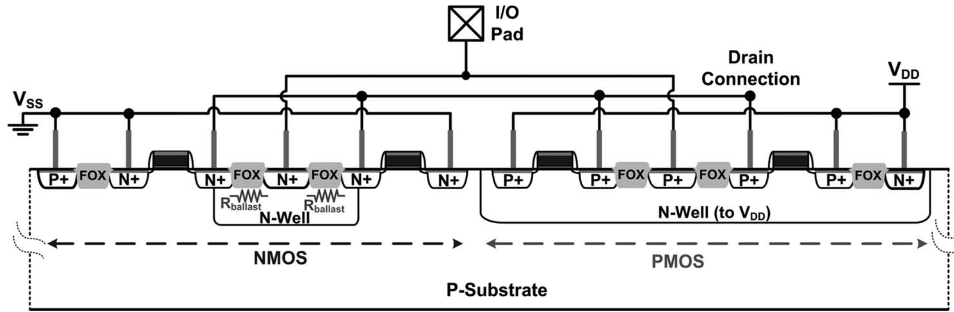

Fig. 14. Cross-sectional view along the A–A' line of the fully silicided I/O buffer realized with type-B layout scheme.

Among the four ESD test modes on I/O buffers, ESD current under PS- and PD-mode ESD tests has to flow through the ballast N-well. The N+/N-well junction breakdown is expected to result in large power dissipation over the ballast N-well, which results in the melting of contacts on the island diffusions of the driver NMOS. With the ESD current flowing from island diffusion through the ballast N-well to the drain diffusion of driver NMOS, melted metal contacts can result in short from island diffusion to the drain diffusion of driver NMOS, which results in substantial shift of I–V curve compared to the original I–V curve before ESD stress. The I/O buffer is then judged as a failure because the short of island and drain diffusions results in I–V shift over 20% compared to the original I–V curve before ESD stress. The melted metal contacts may also result in short from island diffusion to the P-substrate, which can also cause sharp I–V shift after ESD stress. Consequently, the N+-to-N-well ESD failure has become the limitation to the type-A layout scheme. As the SEM image shown in Fig. 12, the I/O buffer after 6.5-kV PS-mode ESD stress shows N+-to-N-well failure on the driver NMOS. From the uniformly distributed ESD failure locations in Fig. 13, the effectiveness of the type-A layout scheme to ballast the I/O buffer for ESD protection has been verified.

B. I/O Buffer With the New Proposed Layout Scheme (Type B)

In the type-A layout scheme, although the ballast N-well leads to significant improvement on ESD robustness, it also introduces the $(I_{\mathrm{ESD}} \times R_{\mathrm{ballast}})$ voltage drop to ΔV_{PS} and ΔV_{PD}. The R_{ballast} of N-well resistor becomes large under high current conditions. The increased $(I_{\mathrm{ESD}} \times R_{\mathrm{ballast}})$ voltage drop pinches the ESD protection window and makes internal circuits more susceptible to ESD failure. Even though the internal ESD failure is not observed in this paper, eliminating the R_{ballast} term in ΔV_{PS} and ΔV_{PD} is still beneficial to the PS- and PD-mode ESD tests. Since the main ESD protection device in a power-rail ESD clamp circuit generally has been drawn with large device dimension, it usually stands much higher ESD stress levels than the NMOS or PMOS in I/O buffers. Furthermore, averting the PS- and PD-mode ESD currents from being discharged through the R_{ballast} can further avoid the N+-to-N-well ESD failure shown in Fig. 12.

To modify the type-A layout scheme and to eliminate the R_{ballast} term under PS- and PD-mode ESD tests, type-B layout scheme is proposed. A diagram is shown in Fig. 13 to illustrate the type-B layout scheme, where the N-well ballast resistor

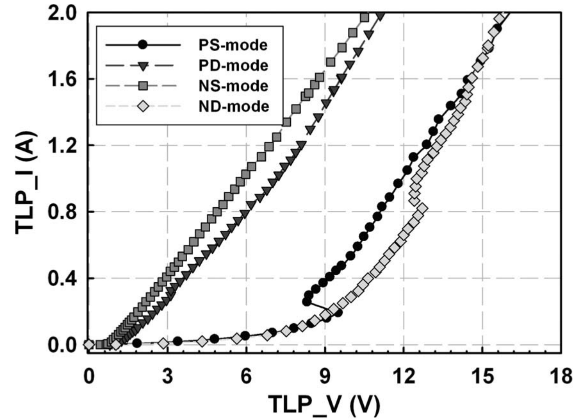

Fig. 15. TLP-measured I–V curves for the I/O buffer with type-B layout scheme. The tests were manually stopped at 2 A without causing failure to the I/O buffer.

is applied to both driver NMOS and PMOS. The drain of the driver PMOS is separated into drain diffusion and island diffusion by FOX, as shown in Fig. 13. The drain diffusions of driver PMOS and NMOS are connected to each other, and the island diffusions of both driver PMOS and NMOS are directly connected to the I/O pad. With such a distinct metal routing in the type-B layout scheme, the P+ island diffusion provides an efficient discharging path for PS- and PD-mode ESD tests, where ESD current can be discharged directly through the D_P diode without flowing through the ballast N-well in NMOS. The cross-sectional view along A–A' line in Fig. 13 is shown in Fig. 14. Under the normal circuit operating conditions, with the shorted drain diffusions of driver NMOS and PMOS, PMOS can pull high the I/O pad through the ballast N-well in the driver NMOS. Device dimensions for driver NMOS and PMOS in type-B layout scheme are the same to those in type-A layout scheme, and I/O buffers with either type-A or type-B layout scheme can meet the operating frequency specification of 20 MHz.

By avoiding the ESD current to flow through the ballast N-well under PS- and PD-mode ESD stresses, the ESD currents are mainly discharged through the diode D_{P1} and power-rail ESD clamp circuit (in PS-mode). As the PS- and PD-mode TLP-measured I–V curves shown in Fig. 15, high resistance characteristic from the ballast N-well in type-A layout scheme is avoided in type-B layout scheme. Therefore, ΔV_{PS} and ΔV_{PD} in type-B layout scheme are much smaller compared to those in type-A layout scheme. Under ND- and NS-mode

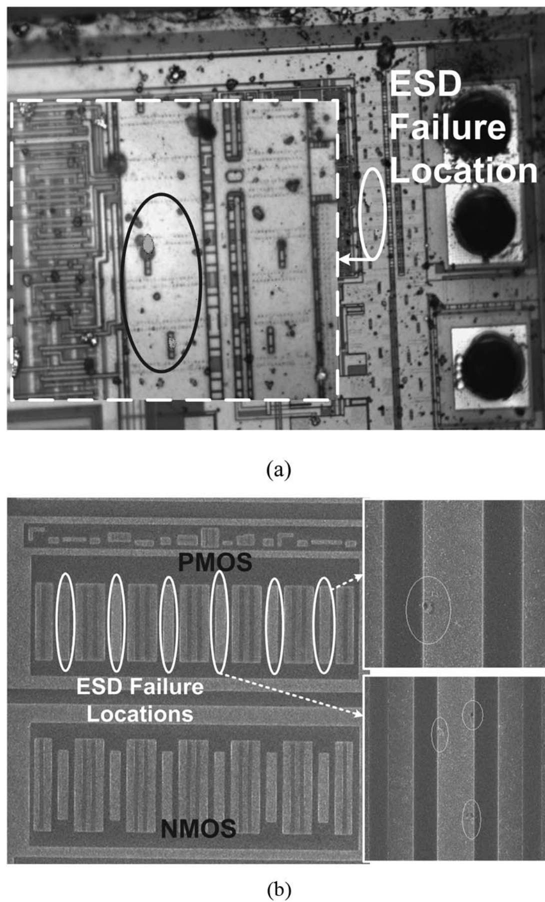

Fig. 16. (a) EMMI and (b) SEM images of the fully silicided I/O buffer realized with type-B layout scheme after 7.5-kV PS-mode ESD stress.

conditions, the D_N diode and power-rail ESD clamp circuit are effective in discharging ESD currents, as shown in Fig. 15.

Because the ESD current can be discharged without flowing through the ballast N-well in the driver NMOS, the N+-to-N-well ESD failure on driver NMOS is avoided in type-B layout scheme. Moreover, the N-well can ballast the driver NMOS when $\Delta V_{\rm PS}$ or $\Delta V_{\rm PS}$ is higher than $V_{t1,\rm MN1}$. The PS-mode HBM ESD robustness of the I/O buffer has therefore been increased to 7 kV, and the PD-mode HBM ESD robustness has been increased to over 8 kV, as shown in Table I. The emission microscope (EMMI) analysis in Fig. 16(a) shows that the failure of the I/O buffer with type-B layout scheme after 7.5-kV PS-mode ESD stress locates on the driver PMOS. The corresponding SEM image of the failure on driver PMOS in Fig. 16(a) is shown in Fig. 16(b). Without the ESD damage on source but silicide meltdown on island diffusions, the SEM image reveals the PS-mode ESD failure on the P+/N-well diode (D_P) of driver PMOS, which has further confirmed that the type-B layout scheme has taken advantage of the highest whole-chip ESD protection capability from the I/O buffers.

V. Conclusion

Silicidation used in CMOS processes has been reported to cause substantial degradation on the ESD robustness of CMOS devices. To mitigate the negative impact on ESD robustness from silicidation, two new ballasting layout schemes for fully silicided I/O buffers have been proposed in this paper. The new proposed ballasting layout schemes have been verified on a real IC product fabricated in a 0.35-μm 5-V fully silicided CMOS process. Without adequate ballasting technique in the original layout, the fully silicided I/O buffer has a very poor ESD level of 1.5 kV in HBM ESD tests. Ballast N-well on the driver NMOS is useful to avoid PS-mode ESD failure on NMOS, but the ND-mode ESD failure over the unballasted driver PMOS still limits the ESD robustness to only 4 kV. With the proposed type-A layout scheme, the whole-chip ESD protection level has been improved to the performance target of 6-kV HBM ESD robustness. The proposed type-B layout scheme further increases the whole-chip ESD robustness up to 7 kV in a 0.35-μm fully silicided CMOS process. No additional mask or process step are required to fulfill either one of the new proposed layout schemes. The new proposed ballasting layout schemes are process portable to different CMOS technologies. Moreover, the type-B layout scheme ballasts I/O buffers without imposing the ballast resistance on the ESD protection window. With the new proposed ballasting layout schemes, the additional mask and process steps for SB can be saved to reduce the fabrication cost without sacrificing the ESD robustness of IC products.

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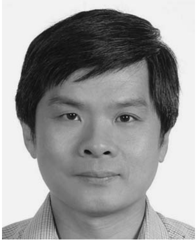
Ming-Dou Ker (S'92–M'94–SM'97–F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 1993.

He was the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute, Hsinchu. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao Tung University. From 2006 to 2008, he served as the Director of the Master Degree Program with the College of Electrical Engineering and Computer Science, National Chiao Tung University; as well as the Associate Executive Director of the National Science and Technology Program on System-on-Chip in Taiwan. Since 2008, he has been the Chair Professor and the Vice President with I-Shou University, Kaohsiung County, Taiwan. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 370 technical papers in international journals and conferences. He has proposed many inventions to improve the reliability and quality of integrated circuits, which have been granted with 150 U.S. and 145 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences. He was the Associate Editor for the IEEE TRANSACTIONS ON VLSI SYSTEMS. He was a Distinguished Lecturer in the IEEE Circuits and Systems Society (in 2006–2007) and in the IEEE Electron Devices Society (in 2008–2009). He was the President of Foundation in the Taiwan ESD Association. In 2008, he has been elevated as an IEEE fellow "for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI microsystems." In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan and one of the top hundred Distinguished Inventors in China.

Wen-Yi Chen (S'08) received the B.S. degree from the Department of Electronics Engineering and the M.S. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 2003 and 2005, respectively. He is currently working toward the Ph.D. degree in the Institute of Electronics, National Chiao Tung University.

After military service, he joined the Circuit Design Department, SoC Technology Center, Industrial Technology Research Institute, Hsinchu, as a Circuit Design Engineer. In 2006, he was with the Amazing Microelectronic Corporation, where he worked with system-level ESD protection design. His current research interests include reliability of high voltage CMOS devices and ESD protection design in mixed-voltage I/O circuits.



Wuu-Trong Shieh received the B.S. degree from the Department of Electronics Engineering and the M.S. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 1986 and 1988, respectively.

From 1990 to 1994, he was a Circuit Design Engineer with the Product Development Division, Hualon Microelectronics Corporation, Hsinchu. In 1995, he joined ELAN Microelectronics Corporation, Hsinchu, which is an IC design house focusing on R&D and marketing of consumer ASIC and MCU, where he is currently the Director of ELAN Product Development Division and in charge of supervising the development of IC products. His technical area of expertise is major with the designs of digital integrated circuits and on-chip ESD protection for consumer ICs.

I-Ju Wei received the B.S. degree from the Department of Electronics Engineering, Minghsin University of Science and Technology, Hsinchu, Taiwan, in 1989.

She was an Engineer with the Electronics and Optoelectronics Research Laboratories, Industrial Technology Research Institute, Hsinchu. She is currently with ELAN Microelectronics Corporation, Hsinchu, as the Department Manager of Layout Division for product development. Her technical expertise is major with chip layout for consumer IC products, including the area-efficient I/O cell layout with high ESD robustness.