國立交通大學

電機資訊學院 電子與光電學程

碩 士 論 文

低電壓５-GHz 互補式金氧半電晶體
直接降頻式射頻前端接收器

DESIGN OF LOW VOLTAGE 5-GHz
CMOS DIRECT-CONVERSION FRONT-END RECEIVER

研 究 生：丁 彥

指導教授：吳重雨 教授

中 華 民 國 九 十 三 年 七 月

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研 究 生：丁　彥　　Student：Yen Ding

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國 立 交 通 大 學

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碩 士 論 文

A Thesis

Submitted to Degree Program of Electrical Engineering Computer Science

College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronics and Electro-Optical Engineering

July 2004

Hsinchu, Taiwan, Republic of China

中華民國九十三年七月

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摘　　要

低耗電與高資料傳輸特性使得無線區域網路的發展日漸蓬勃，在無線區域網路 802.11a 規格頻譜中，特別將 52 個次頻道中，保留編號 0 的次頻道不予發送，這對於選用架構簡單的直接移頻接收器十分有利，並且也增加了單晶片整合的機會。本論文使用互補式金氧半電晶體製作一個直接移頻接收器，透過國家晶片系統設計中心，以臺灣積體電路製造股份有限公司提供的 0.18 μm 製程技術實現。論文最大的重點在於處理直接移頻架構的自我混波問題，提出一個新的準位偏移補償電路，並當作混波器的負載，直接消除因自我混波所產生的直流準位偏移電壓。射頻接收器所含電路有低雜訊放大器、正交壓控振盪器及降頻器。

量測結果顯示，所設計的射頻前端接收器可於 1.1 V 電源下正常運作。射頻接收器在規範的頻寬中均有 – 15 dB 輸入反射因數、17.8 dB 電壓增益、14.9 dB 雜訊指數、 – 23 dBm 之 1 dB 增益壓縮點，當接收器輸入端灌入一組與振盪器同頻且強度為-50 dBm 的信號時，其自我混波後的直流準位偏移電壓為 1 ~ 3 mV。此外，接收器消耗功率為 37.56 mW，晶片面積為 2.09 mm^2。

DESIGN OF LOW VOLTAGE 5-GHz CMOS DIRECT-CONVERSION FRONT-END RECEIVER

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ABSTRACT

Wireless local network is a fast growing market that enables lower power dissipation and higher data rates. The IEEE 802.11a standard which channel 0 is useless among 52 sub-carriers; this is favorable for direct-conversion architecture. This thesis proposes a CMOS direct-conversion receiver, and is realized by TSMC 0.18 μ m technology via Chip Implementation Center. The major issue in the direct-conversion architecture is self-mixing problem; a new offset compensation circuit is used as the mixer loads to alleviate the DC offset. The receiver comprises a low-noise-amplifier, a quadrature voltage-controlled oscillator and downconverter.

Measured results reveal that the designed receiver can operate well at 1.1 V power supply. It performs –15 dB input refection coefficient in interesting band, 17.8 dB conversion gain, 14.9 dB noise figure, -23 dBm 1 dB compression point. The DC offset voltage is 1 ~ 3 mV with input injected power of –50 dBm. It consumes 37.56 mW and die area is 2.09mm^2.

誌 謝

能夠順利畢業，要感謝的人實在很多。首先，要對我的指導教授吳重雨老師致上最誠摯的感謝。老師在這二年裡不論在硬體或是軟體上提供了我一個最佳的學習環境。在學習上老師也給予了適時的指導與啟發，使我不在錯誤當中打轉，更教導了我許多做事的方法與態度。

其次我要感謝實驗室的學長高宏鑫、鄭秋宏、廖以義、施育全、周忠昀、林俐如、黃冠勳、江政達、王文傑、虞繼堯、蘇烜毅、蔡俊良、李彥伯、黃柏獅、劉沂娟的努力，才使實驗室軟硬體設備一應俱全。在如此的環境下，我的論文才能順利完成。再來我要感謝實驗室的同學：吳瑞仁、蘇芳德、鄭建祥、張秦豪、許德賢、謝致遠、陳旻琁、陳勝豪、林韋霆、杜長慶、蘇紀豪、楊文嘉、李宗霖、邱偉茗、林大新、王騰毅、張家華、曾偉信、阿爛、黃如琳、郭秉捷、張瑋仁、林棋樺、李權哲、周政賢、蕭聖文、陳正瑞、陳政良、陳煒明……等，研究功課或外出遊玩，陪伴著我一起渡過了這二年的研究生涯。

還有我的同梯蔡裕文，由於他的鼓勵，我才會來攻讀碩士學位，做電路設計，衷心感謝。最後我要感謝我的家人，對我放棄工作來唸書的支持，使我在學習之餘無後顧之憂。

其他要感謝的人還有很多，無法一一列出，在此一併謝過。

丁 彥

國立交通大學

中華民國九十三年七月

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

As the vigorous development of wireless communication systems, many related application products have been promoted. The current trend of those products is towards integrated circuits on single chip and the RF IC played the leading role in the wireless communication systems. Besides supplying more functionality, any useful RF IC solution also orientates to more small, costless, and power saver. Performance, cost, and time to market are three critical factors influencing the choice of technologies in the competitive RF industry. CMOS technology has low cost and high fabrication turnaround time make it desirable to use a single mainstream digital CMOS process for all IC products [1]. Based on CMOS techniques contribute architectural innovations in the wireless systems may lead to revolutionary improvements. The RF section of new phones has experienced significant size reduction due to evolution of RF architecture [2]. Many of practical RF architectures have their significant characteristic, an optimum design method is considering the entire communication systems including both RF and baseband functionalities, choosing the proper sub-blocks. Wireless equipments with high performance depend on proper-designed circuit in accordance with specification defined, such as GSM and GPRS for mobile communication or Bluetooth and IEEE 802.11 family for wireless local area network. RF circuit is usually a main of bottlenecks, even if they occupy only a small part in the overall.

Mobility is at the heart of wireless communications. Many wireless communication

systems will emerge to serve special needs that are not met well by the existing system. Without the challenge of mobility, they are able to achieve higher spectrum efficiency and other economies relative to wireless systems that serve mobile subscribers [3].

It is difficult to grasp the analogy and high-frequency characters in the RF circuit design. Researcher should carefully investigate on material, lithography, parasitical elements, choosing architecture and other ways to overcome the existent obstacles. As plenty studies bring lots of efficient development, more and more wireless equipments have become commercial and popular products.

1.2 REVIEW ON CMOS RF FRONT-END RECEIVER

The transceiver is a quite major component in the wireless communication equipment that includes commonly receiver, transmitter and frequency synthesizer. RF front-end receiver generally consists of several main components: Low-noise amplifier (LNA), Downconverter and Filter. LNA amplifies RF signal received from antenna with low noise contribution. Downconverter mixes RF signal amplified by LNA with LO signal generated by VCO and outputs interested frequency signal to feed subsequent circuit stage. Filter suppresses undesired signal for baseband circuit receiving message of sufficiently low error rate. Fig 1 enumerates one of receiver architectures for example.

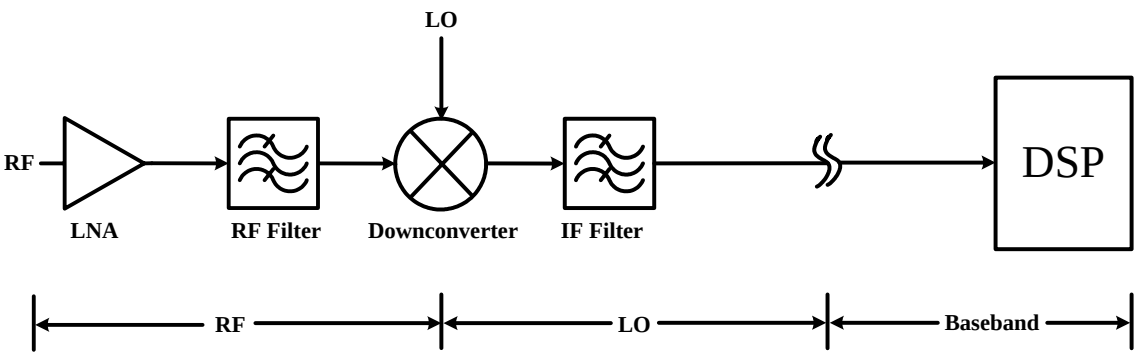


Fig. 1 A common receiver architecture

Wireless communication is a narrow-band system, which usually suffers from nonlinearity issues while signals of various frequencies are received simultaneously; intermodulation phenomenon corrupts the adjacent-channel signal [4]. It is hard to suppress the undesired intermodulated signal by any existent filter.

Complexity, cost, power dissipation, and number of external components have been the primary criteria in selecting receiver components. In the past, heterodyne is the architecture that is selected for the most of the cellular handsets due to its high performance [5], but a lot of its components is still needed to be discrete. There are special issues on different architectures that will be discussed in the following：

1.2.1 Receiver Architectures

As RF receiver is evolving continuously, several architectures in recent years can be generalized. The-well-know architectures are heterodyne receiver, homodyne receiver and low-IF/ image-reject receiver [4].

A. Heterodyne receiver

Heterodyne receiver downconverts the received RF signal to interested intermediate frequency (IF), which is usually much lower than the initially received frequency band. The heterodyne receiver is illustrated in Fig. 2.

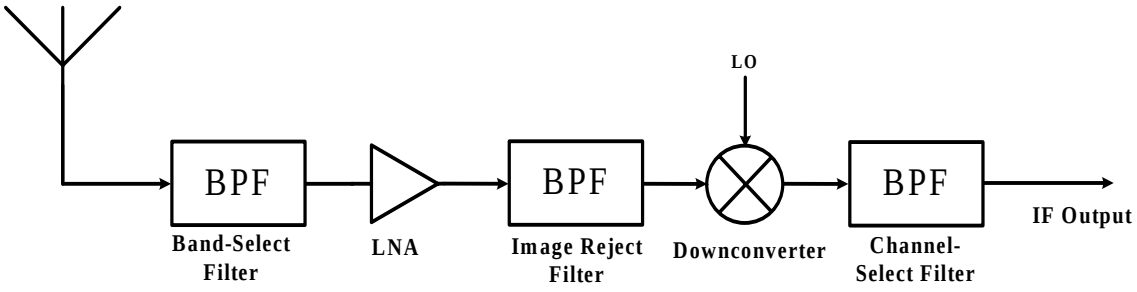


Fig. 2 Architecture of heterodyne receiver

This topology leads to the severe tradeoff between sensitivity and selectivity [4]. A high IF increases the difference frequency between image and desired signal and gets a better image-rejection performance, but this need a channel-selection filter with very high Q-factor. It is difficult to design a filter of sufficiently high Q-factor on chip. Even

if integrated image-reject filter is realized in practice [6]. This is not suitable for low power design. If the IF is low, the channel-selection filter has a more relaxed requirement, but proper image suppression becomes harder to achieve. To relax the trade-off, dual-IF topology is applied [7], but it has power-consumption issue due to more circuit stage for multi-downconversion procedure.

Compared to other topologies, heterodyne receiver can achieve better performance; but it is more complexity, difficult integration and not appropriate to different wireless standards and modes.

B. Homodyne receiver

The homodyne receiver also called zero-IF or direct-conversion which avoids the disadvantages of the heterodyne architecture by converting the RF signal directly to baseband. It translates the channel of interest directly to zero frequency in one step by mixing with an LO output of the same frequency. A low-pass filter that is used to suppress nearby interferers filters the resulting baseband signal. The homodyne receiver is illustrated in Fig. 3.

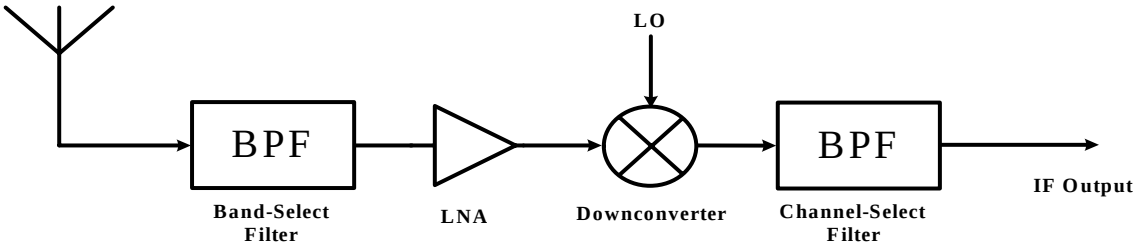


Fig. 3 Architecture of homodyne receiver

The main advantage of homodyne receiver is the high integration, simplicity of structure, cost and power reduction. It avoids the need for an off-chip IF filter and requires only one single frequency synthesizer. The problem of the image is minimized, as the incoming RF signal is down-converted directly to zero, if the quadrature down-converter is used [8]. As result, no image-reject filter is required. The possibility of changing the bandwidth of the integrated low-pass filters (and thus, changing the

receiver bandwidth) is the other advantage if multimode and multi-band applications are of concern [9]. The homodyne receiver also allow analog-to-digital converter (ADC) and digital signal processing (DSP) circuits to perform demodulation and other ancillary functions, relaxes the selectivity requirements if highly integrated, low-cost and low-power realization [5].

Homodyne receivers suffer impairment of DC offset, flicker noise, I/Q mismatch and even-order distortion. The effects of even-order distortions can generally be made sufficiently by negligible with good circuit techniques and I/Q mismatch is the biggest challenge in the implementation of CMOS frequency synthesizer. However, DC offset and flicker noise problems are generally considered much more serious and challenging to the designers.

C. Low-IF/Image-reject receiver

The low-IF topology starts from combined the advantages of both receiver types introduced above. The low-IF receiver is no DC offset problem but have image problems. The most common techniques to remove the image are to use IR architecture [10] or polyphase filter [11]. Furthermore, the signal bandwidth in low-IF conversion is twice that in direct conversion, therefore requires doubling the analog-to-digital conversion sampling rate, and results in higher power consumption. Finally, the double signal bandwidth in low-IF conversion mandates to double the baseband filter bandwidth, which further increases design complexity and power consumption [12].

One type of image-reject receiver is the Hartley architecture [13]. The main drawback of this architecture is that the receiver is very sensitive to mismatches due to phase and gain imbalance of the local oscillator signals, which causes incomplete image cancellation. Also, the loss and noise of the shift-by-90° stage and the linearity of the adder are critical parameters. Another type of image-reject receiver is the Weaver architecture [14]. Similar to the Hartley receiver, the image can no longer be cancelled

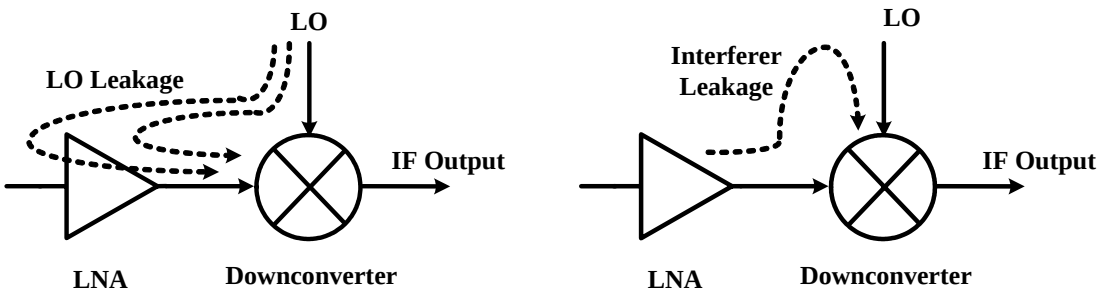
completely if the two local oscillator signals are not perfect 90°. However, the Weaver architecture is also sensitive to mismatches, but it avoids the use of RC-CR network, thereby achieving greater image rejection despite process and temperature variation [2].

1.2.2 Issues of Direction-Conversion

The direction-conversion receiver entails a number of issues that consulted previously need to conquer in favor of full integration.

A. DC offset

The major disadvantage is that severe DC offset can be generated at the output of the mixer. DC offset in a homodyne receiver are illustrated in Fig. 4. The DC offset can be generated by self-mixing of the LO leakage signal with the LO signal [Fig. 4 (a)] or self-mixing of a strong interferer due to leakage from the LNA [Fig. 4 (b)]. The LO and interferer leakage arise from capacitive and substrate coupling. If self-mixing varies with time, it leads DC offset issue to be exacerbated. Undesired DC offset corrupts the baseband signal and saturate the following gain stages. Also, DC offset in I/Q signal paths shifts the baseband signal constellation, causing potential signal saturation, as well as degrading the bit error rate (BER) performance [15]. Moreover, the transistor mismatch in the signal path and demodulation of large amplitude modulated signal via second-order nonlinearity of the mixer that also generates DC offset.



(a) (b)

Fig. 4 Self-mixing of LO leakage and interferer leakage

A solution for DC offset removal is to employ ac-coupling, i.e. high–pass filtering, in the down-converted signal path. Unfortunately, this solution removes the DC energy

of desire signal. It requires prohibitively large capacitors or resistors and accompanies unavoidable in-band loss. A low corner frequency in the HPF may lead to temporary loss of data in the presence of wrong initial conditions, and result in long transient settling during gain changes or Tx-to-Rx switching [16]. There is similar way to withstand DC offset by ac-coupling and unity gain amplifier, but it must face the linearity issue simultaneously [17].

The dc-coupled with feedback configuration, using negative feedback around the baseband amplifier, is another topology to suppress the DC offset. It circumvents the disadvantages in the ac-coupling method. However, the gain of baseband amplifier is large and has a number of stages. It makes the feedback path with very large capacitance or the extremely small transconductance. Additionally, It is also constraint on stability in the circuit design [18][19][20].

Also, in the multi-phase reduced frequency conversion receiver architecture, the VCO frequency is reduced and deviated from the carrier frequency and the DC offset can be drastically reduced [21]. But it brings about complexities and symmetrization on circuit design, consumes extra power due to using multi-phase mixer and VCO.

The architecture of balanced harmonic mixer can alleviate offset extremely, it uses second harmonic of the LO signal that takes part in the mixing process. As a result, the LO leakage generates no DC component but an output which is still situated at the LO frequency and can be easily filtered out [22][23]. The main issues of this architecture are its weakness on linearity and require higher LO strength due to use of second harmonic signal.

Dynamic calibration and DSP techniques are other popular techniques employed to minimize signal degradation [12][24]. It uses DACs and lookup table (LUT) to calibrate static dc periodically and compensate for temperate fading. However, this requires extra DACs and LUT circuit. The operation and algorithm are complicated, the calibration is

executed only in idle mode and no signal detected.

An offset cancellation mixer can cancel offset by dynamically varying the bias on the loads, which are designed to provide constant impedance independent of the load cancellation current [25]. Nevertheless, the circuit needs extra two digital filter (ex: IIR) to detect dynamic offset. It also requires DACs and common-mode feedback (CMFB) circuits. This would consume more power and pay more attention to circuit stability.

The comparison on DC offset removal methods are listed in Table 1-1. Generally, the offset cancellation circuit in a receiver should be simplification, power saving and erode performance few as far as it can.

Table 1-1 Comparison on DC offset removal methods

Reference	[17]	[19]	[21]	[23]	[12]	[25]
Large C or R	v	v				
Long settling time and in-band loss	v					
Constraint on stability		v				
Weakness on linearity				v		
Required CMFB						v
Sensitive to layout			v			
Architecture complexities			v		v	
Require DACs					v	v
Consume extra power	v	v	v	v	v	v

B. Flicker noise

The flicker noise, also knows as $1/f$ noise, is an intrinsic noise phenomenon found in semiconductor devices, especially in CMOS implementations. Flicker-noise property of a device is semiconductor dependent, and the corner frequency is typically in the vicinity of 1MHz for MOSFET devices [15]. Since the mixer output is down-converted

to a baseband signal, it is quite sensitive to noise and easily be corrupted by the large flicker noise of the mixer.

The flicker-noise effect can be minimized by proper selection of semiconductor processes with low corner frequency and providing adequate gain in the front end to improve relative signal-to-noise ratio (SNR) at the down-converter output. It also can incorporate very large device to minimize the magnitude of the flicker noise [4]. A two-stage mixer where the V/I converter and the switching quad biasing current can be independently optimized that achieves lower noise figure while maintaining the same conversion gain [26]. Since holes are less likely to be trapped, pMOSFETs have less flicker noise than nMOSFETS.

C. I/Q mismatch

I/Q mismatch, or phase and gain mismatch, introduced by the mixer is another critical issue for homodyne receiver topology. Gain error simply appears as a non-unity scale factor in the amplitude. Phase imbalance, on the other hand, corrupts each channel by a fraction of the data pulses in the other channel; in essence degrading the signal-noise ratio if the I and Q data streams are uncorrelated. Any mismatch distorts the constellation diagram of the baseband signal, resulting in an enhanced BER [4]. Tolerable gain and phase imbalance depends on modulations techniques employed in a system. For example, the use of 64-QAM modulations require a SNR of 30 dB, which is substantially greater than required by the FSK modulation in Bluetooth and the QPSK modulation in 802.11b. This high SNR translates to stringent phase noise requirements and tight I/Q matching constraints [27].

The problem of I/Q mismatches needs to conquer and to make it less sensitive to process variation and temperature. For instance, a self-calibrated circuit with ring oscillator [28] or an LC oscillator with a poly-phase filter [29] can get over it very well. However, they come up against large power consumption.

A quadrature LC-VCO can easily generates I/Q signals at the cost of twice power consumption and twice area [30]. An advantage of this architecture is its large signal swing that enables the VCO to drive mixer or prescaler directly. If LC-VCO is well designed, twice power consumption of two VCOs is not an obstacle compared to the power-consuming buffer or ring oscillator. There is still a problem that device variation can induce I/Q mismatch. It is possible to compensate the effect by self-calibrated the VCOs tail current [31].

D. Even-order distortion

Two high-frequency strong interferers close to the channel of interest experience a nonlinearity circuit, such as LNA, those interferers generate a low-frequency beat in the presence of even-order distortion. In the presence of mismatches and asymmetry of the RF path, except for odd-order intermodulation effects, even-order distortion can also becomes problematic in direct-conversion [4].

Even-order effect can be reduced by adopting differential circuits or by HPF filtering the beats. Differential LNAs and double-balanced mixers are less susceptible to distortion because of the inherent cancellation of even-order products. However, the phenomenon is critical for balanced topologies as well due to unavoidable asymmetry between the differential signal paths and cost twice of the single-sided half circuit [32].

1.2.3 Low-Voltage Receivers

There is a receiver realized for 5-GHz wireless application [33]. It use homodyne architecture, implement in 0.25- μ m CMOS technology and operated at 3-V. It comprising a differential LNA, an active mixer, a VCO buffer and a quadrature voltage-controlled oscillator exhibits low noise figure. But it consumes higher power dissipation and no DC offset cancellation design in the circuit.

The key for such a RF receiver design is how to reduce power consumption and cost. Circuit operation at reduced supply voltage is a common practice adopted to

reduce power consumption. However, the circuit performance degrades and one gets low circuit bandwidth and voltage swing at low voltage. Scaling down the threshold voltage of MOSFETs compensates for this performance loss to some degree, but this result in increased static power dissipation [34].

There are two receiver realized with low voltage supply for 5-GHz wireless application [35][36]. One comprising a differential LNA, an active mixer, and a quadrature voltage-controlled oscillator exhibits high linearity. The other comprising a differential LNA, a Gilbert mixer, integer-N frequency synthesizer, AGC loop, and low-pass channel-select filter performs low-power consumption.

1.3 MOTIVATION

In IEEE 802.11a, the center sub-channel is unused, providing an empty spectrum of +/- 156.25 kHz after translation to the baseband. It is very favorable for direct-conversion architecture. Base on this reason, the design of this thesis is to realize a 1-V 5-GHz direct-conversion front-end receiver based on IEEE 802.11a specification and integrated with LNA, quadrature VCO and downconverter for low-power wireless system applications by TSMC 0.18 μm technology. The standard specifies an operating frequency range 5.15 ~ 5.35 GHz with 8 channels of 20 MHz bandwidth per-channel.

This thesis is proposed a new offset compensation circuit with band-pass filter as the downconverter loads to suppress extraneous offset voltages corrupt the signal and saturate the following stages. Based on low-power consumption, this trend dictates that the RF front-end receiver will have to operation with low supply voltage.

The receiver adopts differential circuits to reduce the even-order distortion effect, selected PMOS and provided adequate gain to minimize the flicker noise. Quadrature LC-VCO architecture is to make it less sensitive to I/Q mismatches. Fig 5 shows the receiver architecture in this thesis.

1.4 THESIS ORGANIZATION

Chapter 2 proposes a downconverter comprising DC offset compensation circuit with design considerations, post-simulation results on downconverter. The down converter is also applied in a proposed RF receiver front-end. Chapter 3 illustrates IEEE 802.11a PHY standard and link budget of circuit block. The low-voltage RF receiver front-end comprises a differential LNA, two downconverters and a quadrature voltage-controlled oscillator. The implementation and post-simulation results is completed. Chapter 4 contains experimental results and discussions. Finally, conclusions and future works are described in Chapter 5.

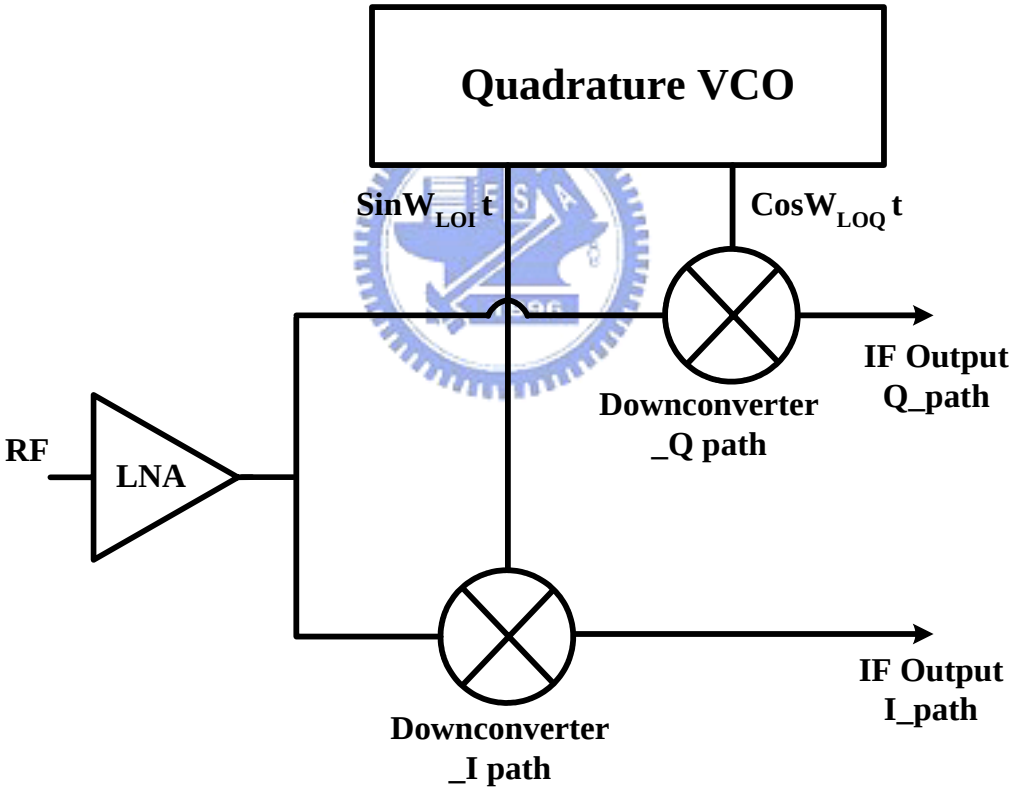


Fig. 5. Receiver architecture in this thesis

CHAPTER 2

DOWNCONVERTER WITH DC OFFSET COMPENSATION

In the radio frequency transceiver operated in the gigahertz range, the quadrature modulator/de-modulator is one of the key components, which has significant effects in the quality of converted signals. The direct-conversion quadrature downconverter can effectively reduce cost, power dissipation, and chip area compared to the heterodyne quadrature modulator. It also has good performance in image rejection and LO leakage.

2.1 OPERATIONAL PRINCIPLE

Downconverters are commonly used to multiply signals of different frequencies in an effort to achieve frequency translation. Clearly a linear system cannot achieve such a task, and it need to select a nonlinear device such as a diode, BJT, or FET that can generate multiple harmonics. Consider an N-MOS device operating in saturation region. The drain current is function of the gate and source voltages, ideally written as

$$\begin{aligned} i_D &= K\,[(v_G - v_S) - V_T]^2 \\ &= K\,[v_G^2 - 2v_G v_S + v_S^2 - 2(v_G - v_S) + V_T^2] \end{aligned} \quad (1)$$

, Where $K = \frac{1}{2}\mu_0 C_{OX}\frac{W}{L}$ and V_T are assumed to be constants. Suppose a basic cell is designed to have an input/output relation similar to (1), shown in Fig. 6. It depicts the basic system arrangement of a mixer connected to an RF signal, a_1, and local oscillator signal, b_1, which is also known as the pump signal. The function is supposed to be

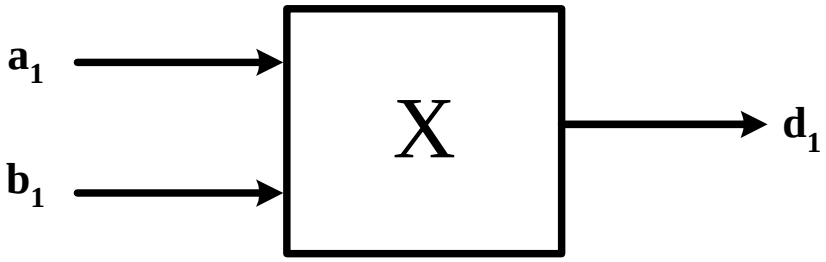


Fig. 6 Basic cell X

$d_1 = a_1^2 - 2 \cdot a_1 b_1 + b_1^2 - 2 \cdot (a_1 - b_1) \cdot C + C^2$, where C is a constant.

Next step, include another basic cell X to construct a differential-input one, basic cell Y, illustrated in Fig. 7.

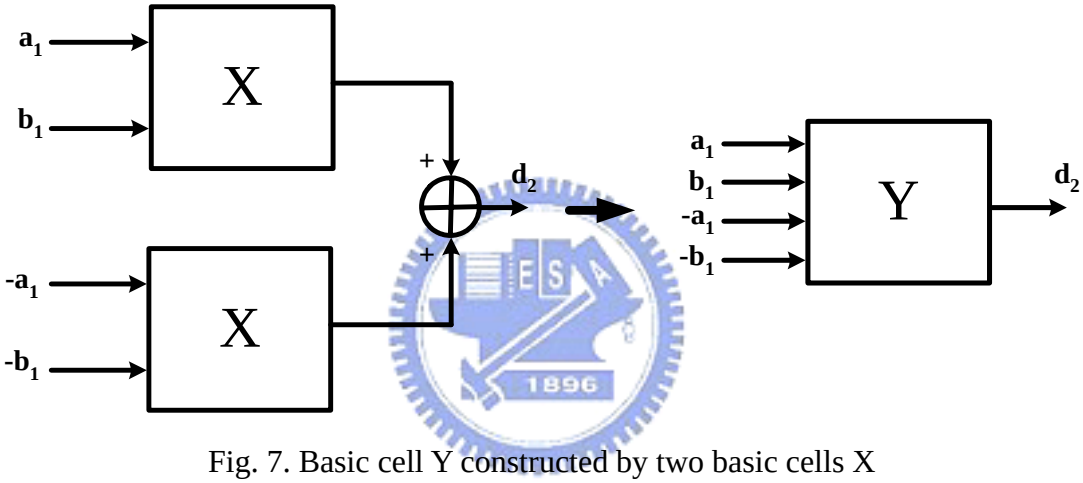


Fig. 7. Basic cell Y constructed by two basic cells X

The second basic cell X is fed by $-a_1$ and $-b_1$, then input/output relation of basic cell Y is $d_2 = 2 \cdot (a_1^2 + b_1^2) - 4 \cdot a_1 b_1 + 2 \cdot C^2$. Fig 8 presents a double-balanced structure for another function, where

$$d_3 = -\{[2 \cdot (a_1^2 + b_1^2) - 4 \cdot a_1 b_1 + 2 \cdot C^2] - [2 \cdot (a_1^2 + b_1^2) + 4 \cdot a_1 b_1 + 2 \cdot C^2]\} = 8 \cdot a_1 b_1 \qquad (2)$$

In this thesis, the downconverter is used the double-balanced structure and if substitution of parameters is introduced as

$$a_1 = \cos \omega_{RF} t \,, \quad b_1 = \cos \omega_{LO} t$$

, the input/output relation becomes

$$d_3 = 8 \cos \omega_{RF} \cdot t \times \cos \omega_{LO} \cdot t$$

The result can corresponds to the I-channel of quadrature IF output. By the same way,

the Q-channel IF output is obtained if

$$a_1 = \cos \omega_{RF} t\,, \quad b_1 = \sin \omega_{LO} t$$

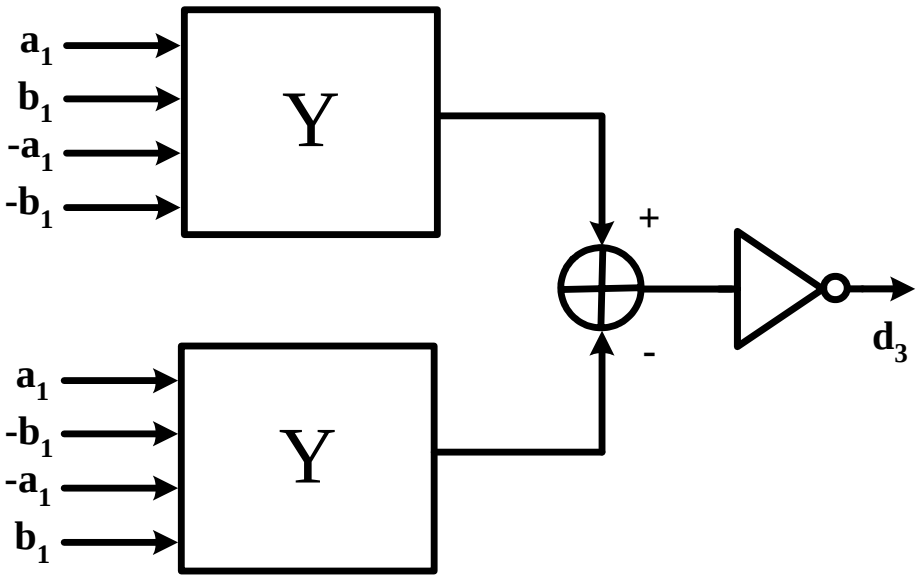


Fig. 8. Double-balanced structure

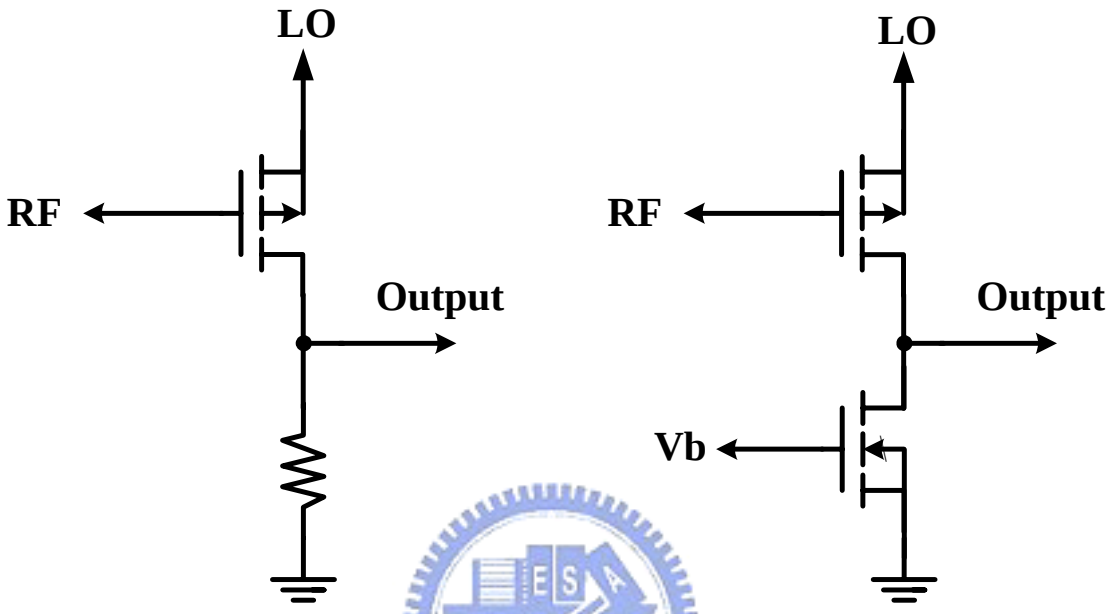
2.2 DESIGN CONSIDERATION

2.2.1 DC Offset Compensation

As previously chapter mention, the DC offset is generated by self-mixing effect. Generally, the total gain from the RF antenna to the ADC is typically around 100 dB so as to amplify the microvolt input signal to a level that can be digitized by a low cost, low power ADC. Of this gain, typically around 25 dB is contributed by the LNA/mixer combination and residue is provided by the automatic gain control (AGC). If an offset is obtained resulting from self-mixing and produces at the output of the downconverter is on the order of tens-milli volt. Thus, it directly amplified by the AGC; the offset voltage saturates the following circuit or downconverter itself, thereby prohibiting the amplification of the desired signal [15].

When the self-mixing is occurred, it may treat a current appearing at the output of the downconverter. These current flows into the downconverter load and bring an extra

voltage on the load. Fig. 9 shows a simple example for DC offset observation. Assuming the P-MOS acts as a downconverter and the RF signal and local oscillator signal have the same frequency, this plays similarly a self-mixing situation. Supposing the extra voltage at the output of downconverter is positive.



(a) (b)

Fig. 9. Simple example for dc offset observation

In the Fig. 9 (a), the RF signal and LO signal will downconvert to DC and a DC current flows into the resistor, therefore a extra voltage build on the output of initial bias point. Fig. 9 (b) is a P-MOS mixer with a constant biasing load, N-MOS. After mixing signal, an additional current appear and flow into N-MOS. If the N-MOS device is in saturation region and channel-length modulation is considered, the drain current is written as:

$$I_D = K(V_{GS} - V_t)^2 \cdot (1 + \lambda V_{DS}) \quad (3)$$

, where λ is channel-length modulation parameter. The V_{DS} voltage will vary with the I_D proportionally when the voltage of V_{GS} is constant. It means that the output voltage vary with the strength of injecting power. Larger injecting power for self-mixing process will produce more unwanted current to flow into the load, further DC offset

voltage appear on the output node of downconverter. It influences the downconverter itself and following stage severely.

Because of substrate coupling effects are always existent: coupling of the LO to the LNA and RF port of the downconverter cause static offset or LO couples to the antenna, radiates and then reflects off moving objects back to the antenna, a time varying offset is created. The undesired reaction won't disappear and need to handle appropriately.

A new method to compensate the DC offset is proposed in this thesis. As show in Fig. 10, the P-MOS also acts as the downconverter and the output voltage is feedback to bias the N-MOS load by a large feedback resistor, instead of the constant bias, Vb. When an additional current appear by self-mixing and flow into N-MOS, the V_{GS}=V_{DS} as the I_G is zero, the equation (3) can be re-written as:

$$I_D = K(V_{DS} - V_t)^2 \cdot (1 + \lambda V_{DS}) \tag{4}$$

With the same amount of offset current, the V_{DS} are suppressed in square degree. The tens-milli volt order of voltage mention previously by self-mixing at the output of the downconverter can be reduced to few milli volts. The offset suppressed ability of this circuit is proportional to the transconductance of the N-MOS load.

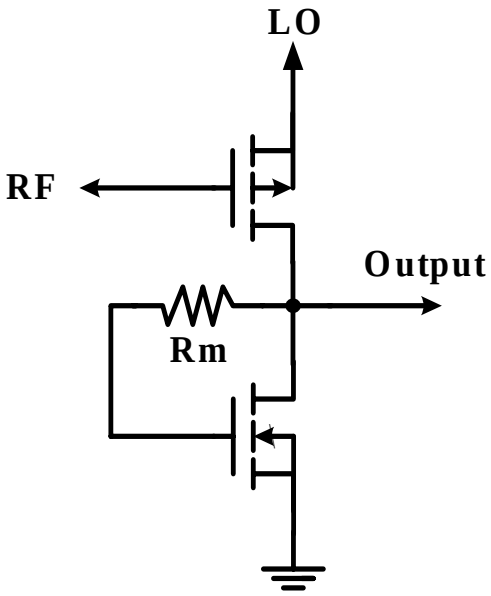


Fig. 10 DC offset compensation circuit

2.2.2 Band-Pass Filter

In the conventional receiver, the downconverter always connect to a channel select filter that can filter out the unwanted band, such as harmonic signal and any interferers outside the interesting band. Since offset removal circuit would entail channel select filter filtering the baseband signal, it is important to examine the consequences of such an operation for the modulation schemes of interest. In IEEE 802.11a specification, the center subcarrier is unused, providing an empty spectrum of ± 156.25 kHz after translation to the baseband. Thus, if the lower corner frequency of the band-pass filters, f_L, fall below this value, then the spectrum of the subcarriers carrying information remains intact. Consequently, a lower corner frequency of 150 kHz and bandwidth of 10 MHz band-pass filters are required.

A second-order LC high-pass filter with low corner frequency (about 150 kHz) is required a very high Q value, a value difficult to achieve. It is important to note that typical filters exhibit a trade-off between the loss and the Q value. In order to significantly relax the linearity and Q value requirement of the baseband stage, the front-end receiver chain further contains a band-pass filter to provide partial channel selection.

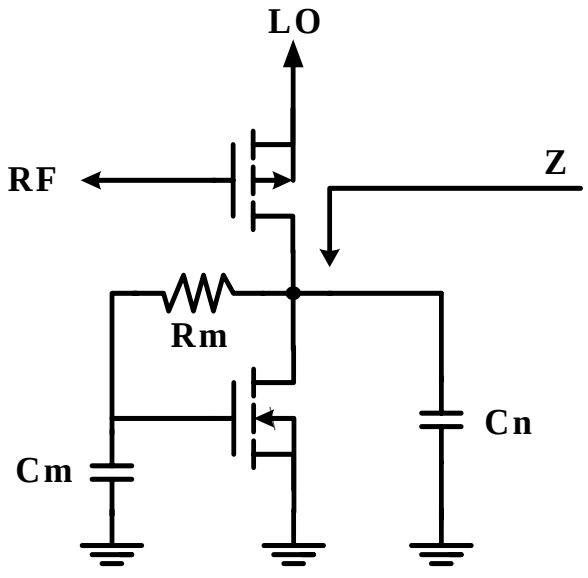


Fig. 11. A band-pass filter as downconverter load

The downconverter contains a band-pass filter showing in Fig. 11. The P-MOS also acts the downconverter and the Cm is connected at gate of the N-MOS to form a simple partial channel selection filter. Because of the N-MOS is worked in the saturation inevitably, using the small-signal model of the N-MOS device, hybrid-π model, and the output impedance looking from Z of Fig. 11 can be written as:

$$Z = \frac{1 + Rm \cdot (Cm + C_{gd}) \cdot S}{Cm \cdot C_{gd} \cdot Rm \cdot S^2 + (Cm + C_{gd} \cdot Rm \cdot g_m) \cdot S + g_m} \Big\| \frac{r_o}{1 + r_o \cdot Cn \cdot S} \tag{5}$$

$$= \frac{Rm \cdot (Cm + C_{gd}) \cdot S + 1}{Rm(CmCn + C_{gd}Cn + CmC_{gd}) \cdot S^2 + \left[Cn + Cm + C_{gd} g_m Rm + \frac{Rm(Cm + C_{gd})}{r_o} \right] \cdot S + \frac{1}{r_o} + g_m}$$

$$\cong \frac{1 + Rm \cdot Cm \cdot S}{Cm \cdot Cn \cdot Rm \cdot S^2 + (Cm + Cn) \cdot S + gm}$$

, where the C_{gs} is lumped with Cm. r_o is the MOS small-signal output resistance and gm is top-gate transconductance. From the equation (5), the output impedance Z very with frequency and it has two corner frequencies, f_L and f_H. The f_L is mainly decided by the Cm and Rm. The f_H is dominated by the Cn. Proper choosing the passive elements can get the required frequency spectrum as showing in Fig 12, if the output impedance of downconverter is greater than the load Z. Using this kind of impedance treat as downconverter load and the IF output is accomplished a simply channel selection.

A new DC offset compensation circuit with band-pass filter is proposed. Without DACs or complex multi-phase architecture, this circuit uses a few passive components to achieve offset compensation and filtering and it is effective in that it does not incur any in-band loss. The proposed circuit doesn't increase numerous power dissipations and a benefit for low-voltage and low-power design.

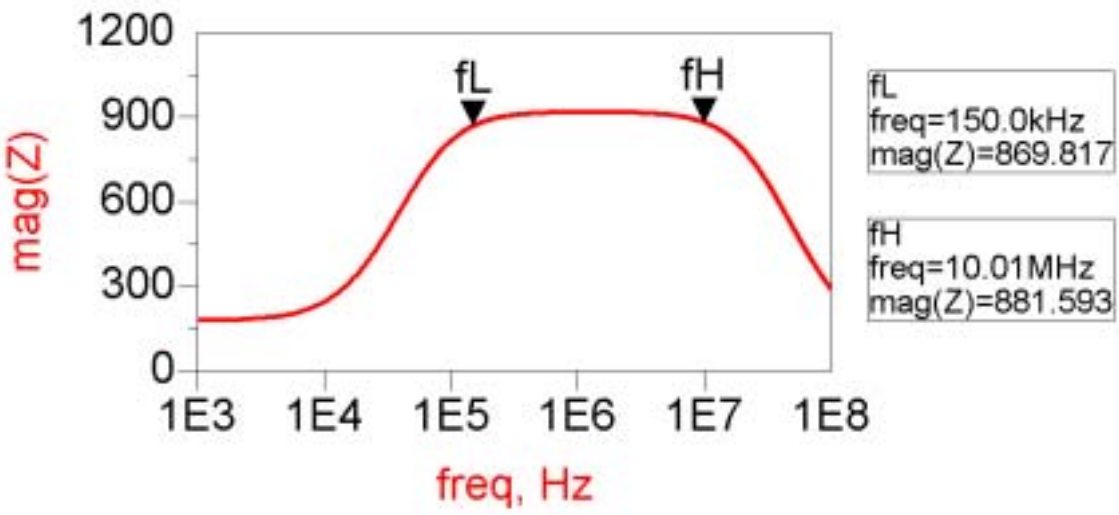


Fig. 12. Band-pass impedance frequency spectrum

2.2.3 Voltage Conversion

This subsection describes how circuit devices construct the function block and the voltage conversion in preceding discussion. Referring to Fig. 13, basic cell X in Fig. 6 is realized by a PMOS device. By the similar way, implementation of basic cell Y is presented in Fig. 14. To realize the output result in equation (2), Fig 14 is developed to Fig. 15. The equation (2) can be modified to equation (6), a more realistic function, by the circuit implementation in Fig. 15.

$$d_3 = 8Z_L K \cdot V_G \cdot V_S \tag{6}$$

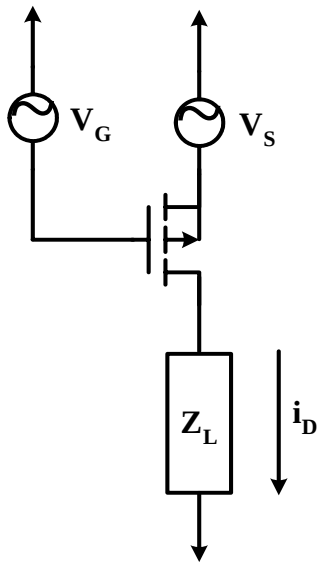


Fig. 13. Realizations of basic cell X

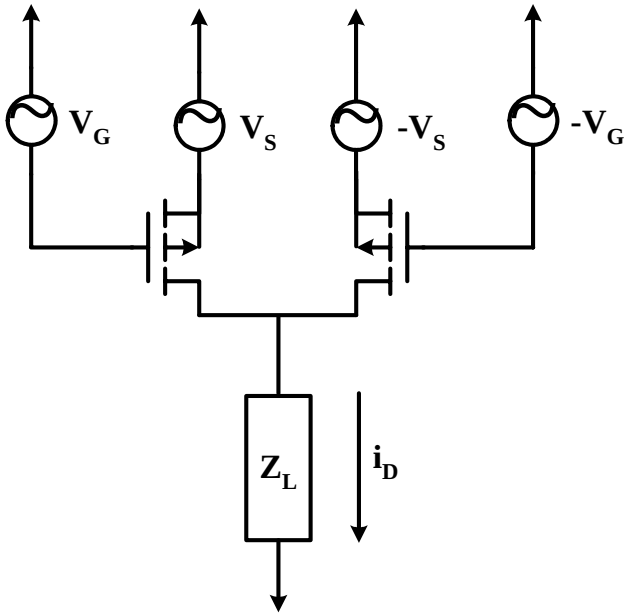


Fig. 14. Realizations of basic cell Y

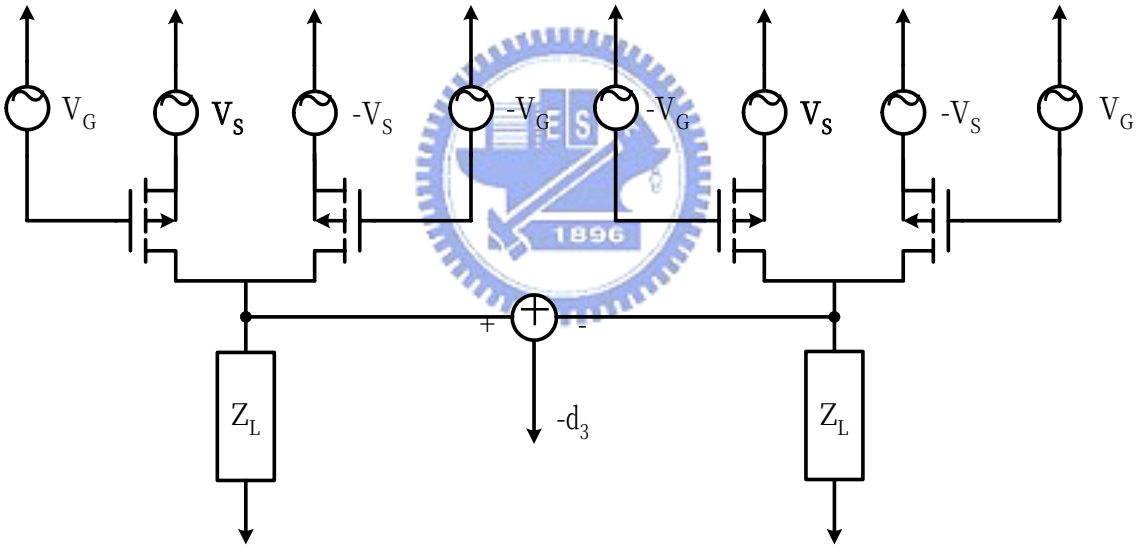


Fig. 15. Realizations of double-balanced combiner

All developments for the downconverter are originally based on equation (1), ideal square- law. Because of channel pinched-off, a MOS device works in saturation region. If a short-channel device is employed in circuit implementation, another mechanism causing saturation is involved [37]. In a short-channel device, velocity saturation occurs before pinched-off. Taking velocity saturation and mobility degradation into consideration, equation (7) presents an advanced formula modified from the ideal

square-law, where v_{sat} denotes saturated velocity and θ is a fitting parameter approximately equaling to $\frac{10^{-7}}{t_{ox}}V^{-1}$

$$I_D = \frac{1}{2}\mu_0 C_{OX}\frac{W}{L}\cdot\frac{(V_{GS}-V_T)^2}{1+\left[\frac{\mu_0}{2v_{SAT}L}+\theta\right]\cdot(V_{GS}-V_T)}$$

$$\approx \frac{1}{2}\mu_0 C_{OX}\frac{W}{L}\cdot\left[1-\left(\frac{\mu_0}{2v_{SAT}L}+\theta\right)\cdot(V_{GS}-V_T)\right]\cdot(V_{GS}-V_T)^2 \quad (7)$$

According to equation (7), equation (6) is modified to equation (8)

$$d3 = 8Z_L K\left(1-\left(\frac{\mu_0}{2v_{SAT}L}+\theta\right)\cdot(V_{GS}-V_T)\right)\cdot V_G\cdot V_S \quad (8)$$

The result indicates that the designed downconverter performs expected function on condition that MOS devices work in saturation region with sufficiently small overdrives. For circuit implementation, the V_G would be the RF signal and V_S is LO signal. Generally, the load and LO signal, Z_L and V_S, influences the d3, output voltage amplitude directly.

2.2.4 Noise and Linearity

The single-balanced configuration exhibits less input-referred noise for a given power dissipation than the double-balanced counterpart. However, the circuit is more susceptible to noise in the LO signal. It is more intensified by the high noise floor of typical oscillators. In both mixer topologies, a differential output provides much more immunity than single-ended output to feedthrough of the RF signal to the IF output. By contrast, if the output is sensed differentially, the effect of direct feedthrough is much less significant. It implies that the differential output have better noise figure than single-ended IF output. Accordingly, a differential band-pass filter is needed; the differential output of the downconverter can directly drive the filter [4].

After downconverter, the downconverter spectrum is around zero frequency, flicker

noise of devices has profound effect on the signal. Therefore the downconverter is the most critical stage in the receiver chain in combating the flicker noise. In most cases, the magnitude of the input-referred flicker noise component is approximately independent of bias current and voltage and is inversely proportional to the active gate area of the transistor. The latter occurs because as the transistor is made larger, a larger number of surface states are present under the gate, so that an averaging effect occurs that reduces the overall noise. It is also observed that the input-referred flicker noise is an inverse function of the gate-oxide capacitance per unit area. For a MOS transistor, the equivalent input-referred voltage noise can be written as [38]

$$\frac{\overline{v_i^2}}{\Delta f} \approx 4kT\left(\frac{2}{3}\frac{1}{g_m}\right) + \frac{K_f}{WLC_{OX}} \cdot \frac{1}{f} \tag{9}$$

$$K_f \approx 3\times 10^{-24} V^2 - F$$

It is also interesting to note that while all of downconverter are no, the MOS switches injecting noise to the output. Employing large LO swings or decreasing the drain bias current of the MOS switch can minimize the contribution of the thermal and channel thermal noise. The trade-offs described above require a careful choice of device size and bias currents so as to minimize the overall noise figure. Since holes are less likely to be trapped, P-MOS has less flicker noise than N-MOS.

In order to reduce the noise figure, the downconverter should have moderate NF and adequate conversion gain to minimize the noise. This can obtain by increased the downconverter load, as designated last subsection Z_L, to increasing conversion gain. With the constant bias current, the larger load impedance causes the larger voltage drop on it, thus decreases the voltage headroom of the remaining MOSFETs and degrades the linearity of the downconverter, especially for the low-voltage design. This is a trade-offs between noise and linearity. By the way, for the intrinsic nonlinearity of the transistors,

it is important to notice that the distortion in inversely proportional to the gate length and this effect will become even more important when going to deeper sub-micrometer technologies [39].

2.3 CIRCUIT REALIZATION

Based on the considerations in the previous section, a downconverter with DC offset compensation circuit is designed. Fig. 16 presents downconverter divided into I/Q-channel paths and lists the relative parameter information in Table2-1. The downconverter is double-balanced counterpart and fully differential configuration. In the aspect of low-voltage design, the downconverter doesn't use the conventional Gilbert cell. The V/I converter of Gilbert cell is removed and direct connects to designed VCO output in order to save the voltage headroom. It needs no re-bias on the source terminals. To realize the direct connection and flicker noise consideration, P-MOS devices are employed as the downconverter. Furthermore the load of downconverter is implemented with N-MOS device. Total DC-drop from sum of sufficient drain-source voltage is merely about 0.4 V by TSMC 0.18- μ m technology. In the condition, downconverter function is achievable at 1-V supply voltage.

Because of the corner frequency, f_L as shown in Fig.12, is obtained by the Rm and Cm product approximately, Cm will occupy a large area when the resister value smaller, vice versa. In order to save the chip area, the Cm is replaced by Cmi1 and Mmi12, for example, in the Fig. 16 (a). It uses the Miller effect to multiply Cmi1. With the proper design, the Cmi1 can be multiplied about 16, saving a lot chip area. The Rm is used high resister type such as the HRI P-poly resister without silicide. The Rri1 or Rrq1 is used to make the load of downconverter more flatness in the interesting band. The differential circuit is very sensitive to device symmetrization. Using Mmq7 and Mmq8, or Mmi7 and Mmi8, with off-chip bias, the adjustable bias, VMi# and VMq#, can

cancel the offset voltage brought by the device mismatch. It is also option to compensate the DC offset using varying bias controlled by the DACs, such as in [25], but this will make circuit more complexity.

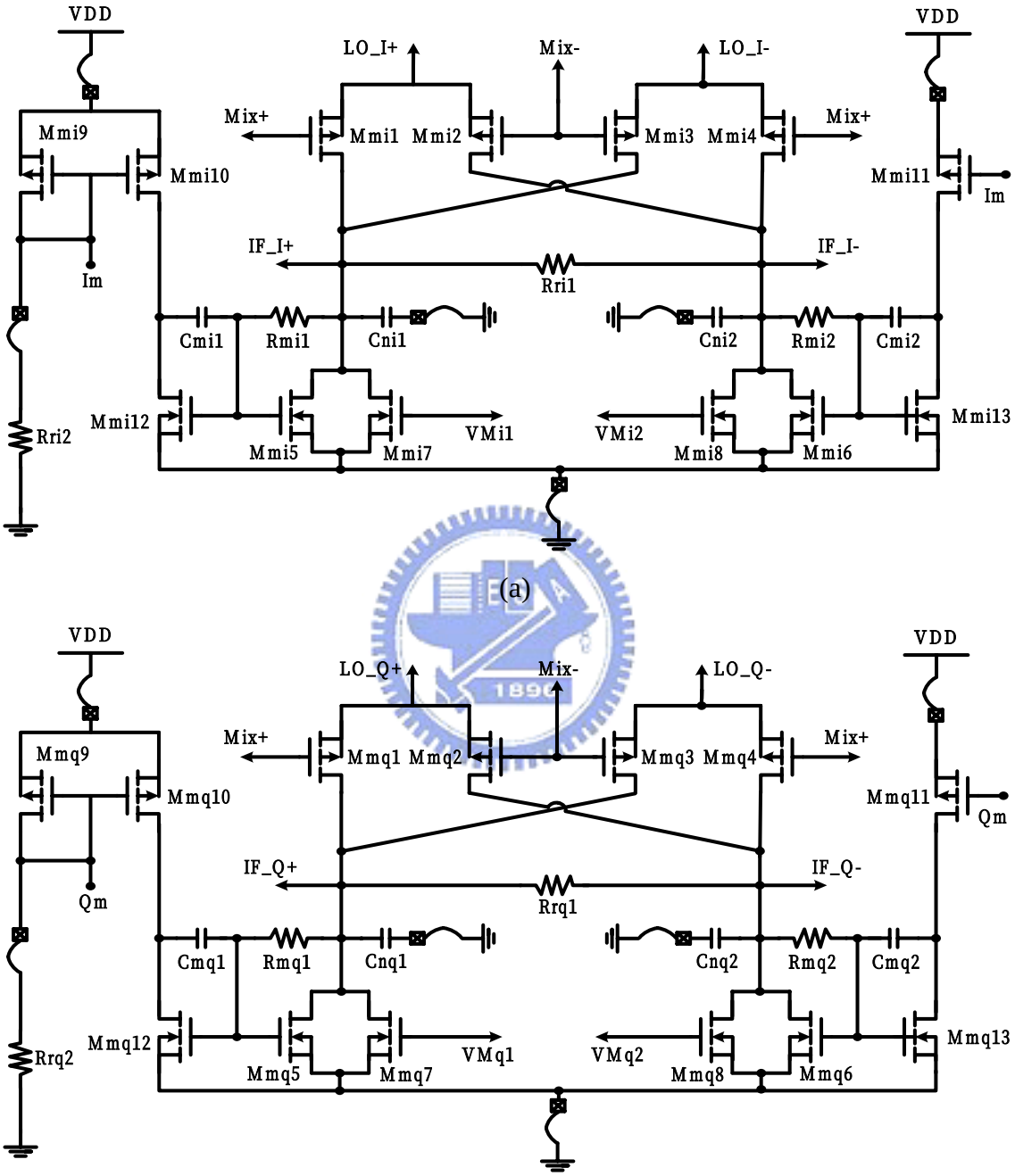


Fig. 16. (a) I-channel and (b) Q-channel of double-balanced downconverter with DC offset compensation circuit

Table 2-1 Parameter information of Fig. 16

Mmi1 ~ Mmi4 and Mmq1 ~ Mmq4	45 μm/0.25 μm
Mmi5 ~ Mmi6 and Mmq5 ~ Mmq6	60 μm/0.5 μm
Mmi7 ~ Mmi8 and Mmq7 ~ Mmq8	10 μm/0.5 μm
Mmi9 ~ Mmi11 and Mmq9 ~ Mmq11	15 μm/0.18 μm
Mmi12 ~ Mmi13 and Mmq12 ~ Mmq13	12.5 μm/0.18 μm
Rri1 and Rrq1	2k Ω
Rri2 and Rrq2	800 Ω
Rmi1 ~ Rmi2 and Rmq1 ~ Rmq2	152 kΩ
Cmi1 ~ Cmi2 and Cmq1 ~ Cmq2	6 pF
Cni1 ~ Cni2 and Cnq1 ~ Cnq2	5 pF

2.4 SIMULATION RESULTS ON DOWNCONVERTER

Post-simulation is completed by ADS simulator with process parameters of TSMC 0.18-μm mixed signal 1P6M RF SPICE models. Fig. 17 presents the simulated voltage conversion gain of the downconverter. The conversion gain is about 0 dB at the interesting band and the corner frequencies are at 150 KHz and 30 MHz respectively.

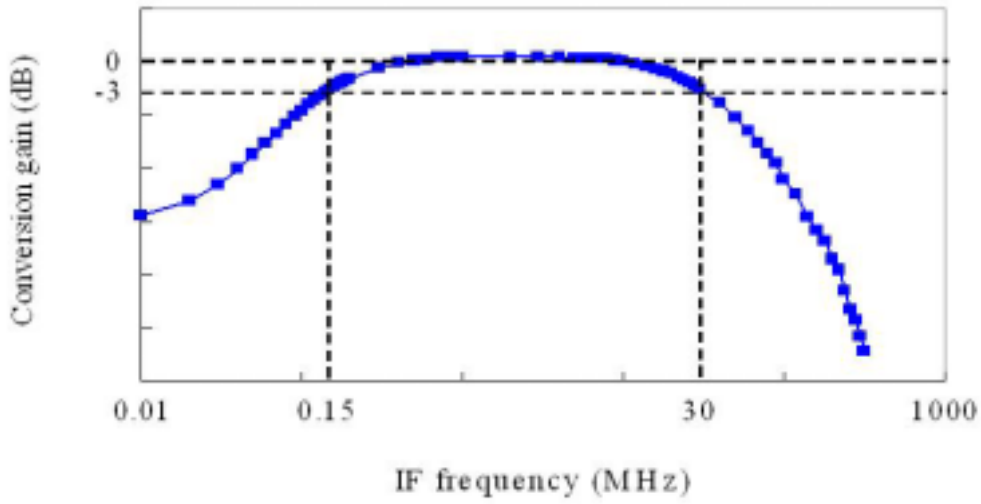


Fig. 17. Simulated voltage conversion gain of the downconverter

The Cmi#, for example, is enlarged by Miller's amplifier, Mmi12 and Mmi13. When the gain of the Miller's amplifier is varied due to process variation, the corner frequency is influenced by the gain variation directly. While Miller's amplifier is with +/- 6% dimension variations, Fig. 18 presents the each voltage gain versus frequency on gain variations and the relative corner frequency is listed in Table 2-2. The normal Miller's gain is designed at 24.66 dB. If the dimension variation is set to +/- 3%, the fL is about 150 kHz +/- 30 kHz.

Fig 19 presents output noise voltage spectral density of downconverter. The noise bandwidth of this circuit is from 150 KHz to 10 MHz and the total noise figure of the downconverter is given approximately by

$$F = \int_{150K}^{10M} \frac{Nout}{Gain \cdot Nin} \tag{10}$$

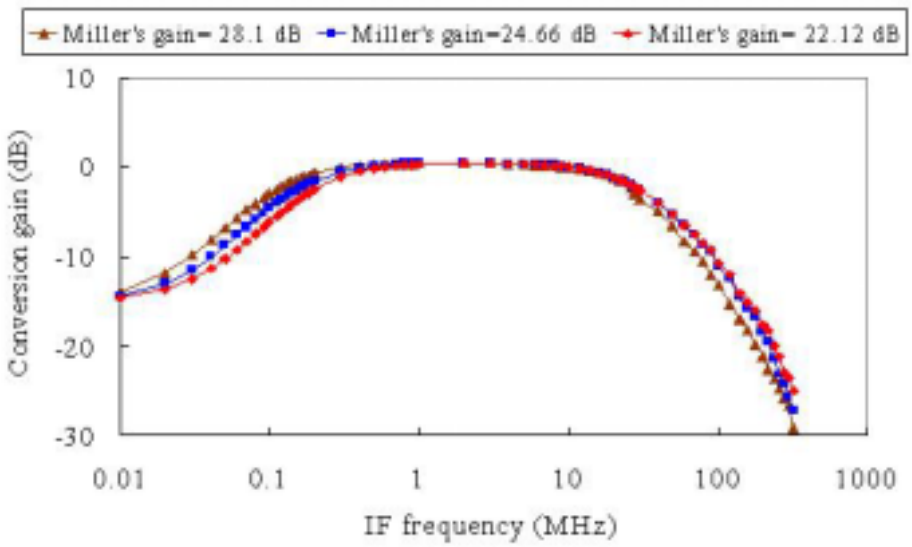


Fig. 18 Voltage gain versus frequency on gain variations

Table 2-2 Relative corner frequency of Fig.18

Miller's gain	fL	fH
28.1 dB	0.11 MHz	27 MHz
24.66 dB	0.15 MHz	30 MHz
22.12 dB	0.19 MHz	32 MHz

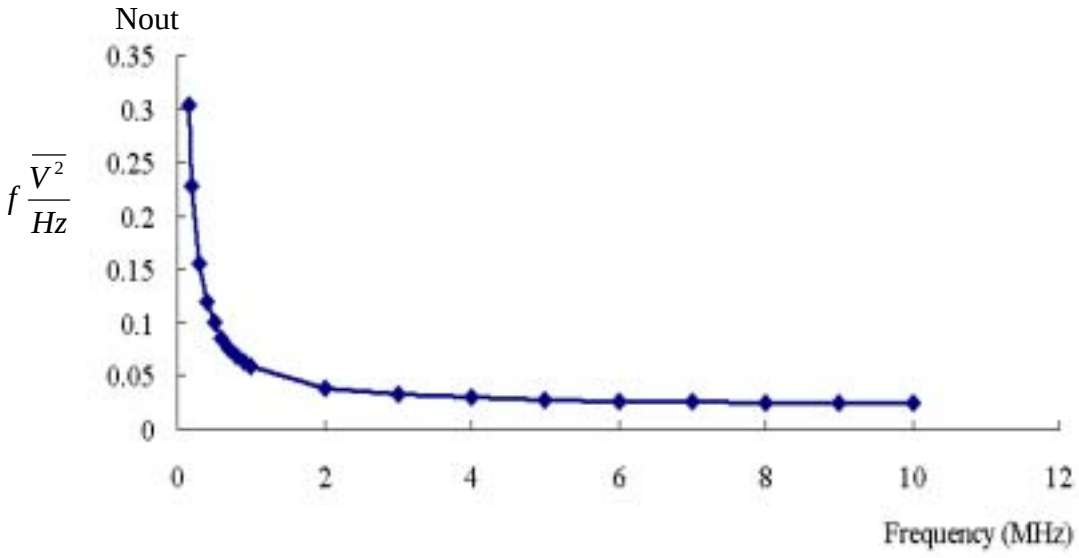


Fig. 19. Output noise voltage spectral density of downconverter

, where the Nout is the output noise power, Nin is the input noise power and Gain is the voltage conversion gain of the downconverter. The noise figure of downconverter at the interesting band is 17.2dB.

Two-tone test is applied to simulate linearity of the downconverter circuit. This response was obtained by feeding two signals at 5.209-GHz and 5.211-GHz to the RF port. The combined two-tone RF signal was mixed with a 0-dBm LO signal at 5.21-GHz. This setup was used to extract the 1-dB compression point and the third-order intercept point (IP3) by sweeping the input power level. Fig. 20 plots output power of first and third order terms relative to input power. A high input intercept of approximately 10 dBm was extrapolated, and a 1-dB compression point was observed near –0.7 dBm.

Fig. 21 shows simulated results of the DC offset compensation. The RF port is fed one tone signal which frequency is same as LO frequency. After self-mixing, a signal current will appear at DC on the each output terminals of the downconverter and influence its bias level. This setup is used to estimate the circuit ability of withstand un-wanted signal leakage. By sweeping the input power level, the DC offset voltage at the differential output terminals will increase, as shown in Fig.21. The DC offset

voltage is about 3-mV at single output with injected power of –30-dBm and about 6-mV at differential output in same condition. The power consumption is about 1mW for the compensation circuit.

At the last of chapter 2, a post-simulation summary of the downconverter is listed in Table 2-3. The power consumption shown in the table is included two paths of downconverters. The downconverters is fed with 0-dBm LO signal at 5.25-GHz and the RF port is fed with –40-dBm RF signals at 5.26-GHz during simulation.

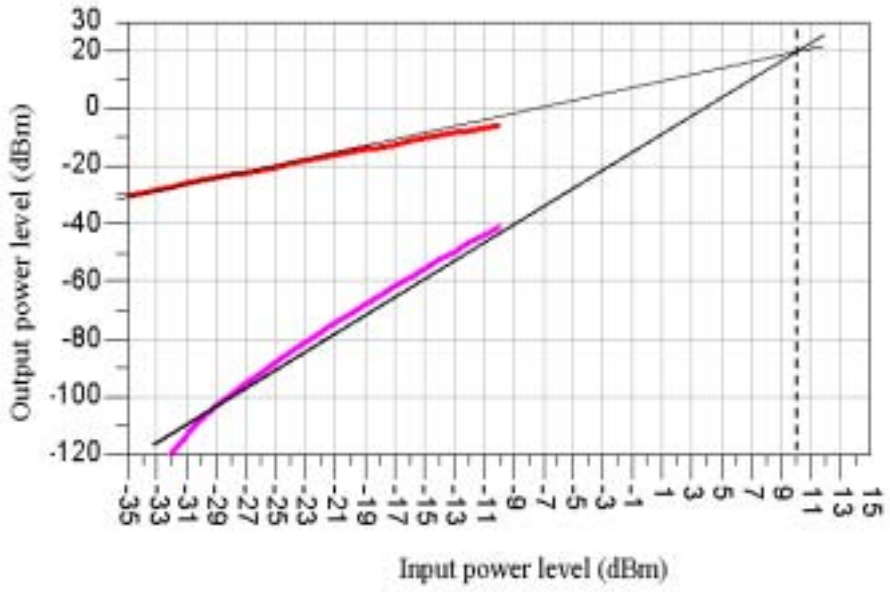


Fig. 20. Extrapolation of downconverter IIP3

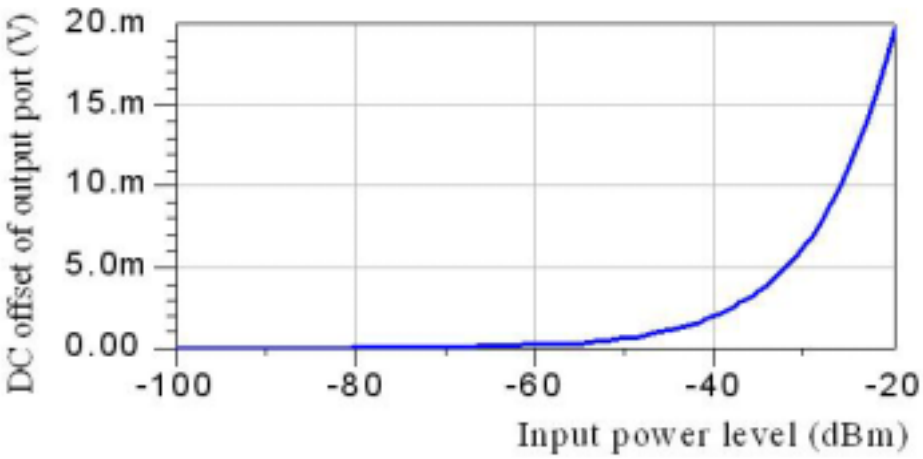


Fig. 21. DC offset voltage caused by injected leakage powers

Table 2-3 Post-simulation summary of the downconverter

Technology	TSMC 0.18- μ m 1P6M
Frequency	5.25 GHZ
Supply Voltage	1.0 V
Power Consumption	3.83 mW
Conversion Gain	0 dB
SSB NF	17.2 dB
P-1dB	-0.7 dBm
IIP3	10 dBm
DC Offset (injected -30dBm at downconverter input)	6mV

CHAPTER 3

1-V 5-GHz DIRECT-CONVERSION FRONT-END RECEIVER

Direct-conversion receiver is mentioned in Chapter 1. In addition to a LNA and downconverters, the designed receiver requires a quadrature VCO. Fig. 22 gives an illustration with a block diagram. The downconverters are implemented to a double-balanced downconverter as chapter 2 mentioned. The LNA is fully differential with common-source-cascode architecture. The quadrature VCO generates quadrature LO signal and quadrature IF signal comes from downconverter of the RF and LO signals. The output buffer is used for measurement.

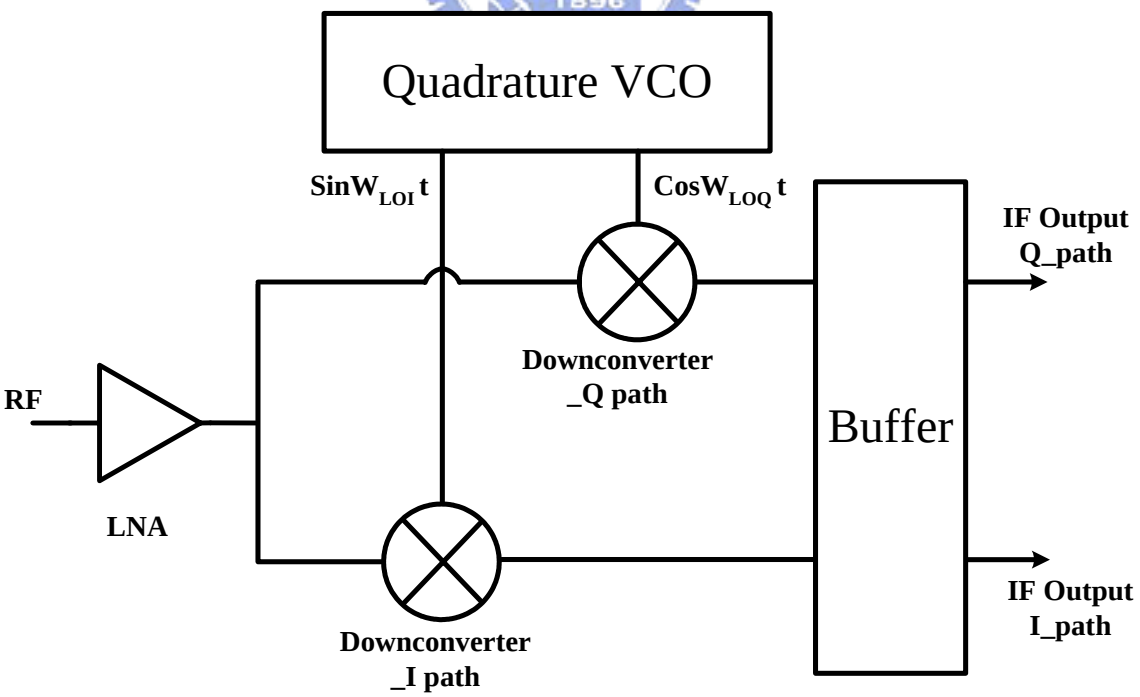


Fig. 22 Block diagram of direct-conversion receiver

3.1 IEEE 802.11A PHY STANDARD AND LINK BUDGET

The IEEE 802.11a standard specifies over a generous 300-MHz allocation of spectrum for unlicensed operation in the 5-GHz block. Of that 300-MHz allowance, there is a contiguous 200-MHz portion extending from 5.15 to 5.35 GHz, and a separate 100-MHz segment from 5.725 to 5.825 GHz. It incorporates orthogonal frequency division multiplexing (OFDM) modulation, a technique that uses multiple carriers to mitigate the effect of multipath. IEEE 802.11a standard provides for OFDM with 52 subcarriers in a 16.6-MHz bandwidth (channel spacing of 20-MHz), 48 subcarriers are for data, the rest are for pilot signals. Each of the subcarriers can be either a BPSK, QPSK, 16-QAM, or 64-QAM signals. It provides nearly five times the data rate and as much as ten times the overall system capacity as currently available 802.11b wireless LAN systems. Information data rates of 6~54 Mb/s are supported. The standard further requires a maximum transmit constellation error at –25dB for 64-QAM modulated OFDM signal, whereas the output power cannot exceed 40 mW for channels from 5.15 to 5.25 GHz or 200 mW for channels from 5.25 to 5.35 GHz. Fig. 23 shows a lower frequency band of the channel allocation [40].

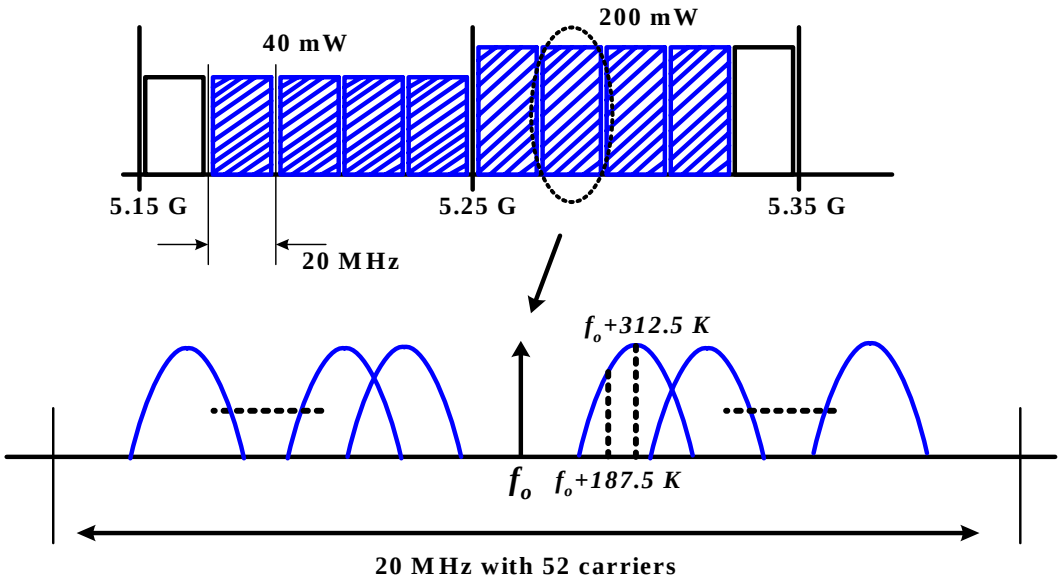


Fig. 23 IEEE 802.11a lower frequency band of the channel allocation

The spectral efficiency of 802.11a standard comes at the expense of a more complicated receiver with strict requirements on the radio performance. For example, the use of 64-QAM modulation requires a signal-to-noise ratio (SNR) of 30 dB, which is substantially greater than required by the FSK modulation in Bluetooth and the QPSK modulation in 802.11b. This high SNR translates to tight I/Q matching constraints for the receiver. It also results in the stringent demands for the performances of both noise figure and image rejection.

To determine the precise target value, the specification set to frequency range, noise figure, maximum input signal level or input-referred 1-dB compression point. For frequency range, it is often acceptable to cover only the lower 200-MHz band. The upper 100-MHz domain is not contiguous with that allocation, so its coverage would complicate somewhat the design of the synthesizer. Furthermore, that upper 100-MHZ spectrum is not universally available, such as HIPERLAN. Hence the choice here is to span 5.15~5.35GHz. The specification simply recommends a noise figure of 10dB, with a 5-dB implementation margin, to accommodate the worst-case situation. A 10-dB maximum noise figure is the design goal for the thesis. The standard also specifies a value of –30 dBm as maximum input signal that a receiver must accommodate (for a 10% packet error rate). Converting this specification into a precise IIP3 target or 1-dB compression requirement is nontrivial. However, as a conservative rule of thumb, the 1-dB compression point of receiver should be about 4 dB above the maximum input signal power level that must be tolerated successfully. Based on this approximation, the target of worst-case input-referred 1-dB compression point is to set at –26 dBm [41]. The IEEE 802.11a specification for this thesis required is listed in the Table 3-1.

Therefore, the link budget of each circuit can be calculated by the following equation. For the noise figure of cascaded stages, the total NF can be written as

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{p1}} + ... + \frac{NF_m - 1}{A_{p1}\Lambda\ A_{p_{(m-1)}}} \tag{11}$$

, where NF_m express the noise and A_{pm} express the gain of each stage. For the linearity of a general expression for cascaded stages

$$\frac{1}{A^2_{IP3}} \approx \frac{1}{A^2_{IP3,1}} + \frac{A_{P1}{}^2}{A^2_{IP3,2}} + \frac{A_{P1}{}^2 \cdot A_{P2}{}^2}{A^2_{IP3,3}} + \Lambda \tag{12}$$

, where A_{IP3},m denotes the input IP_3 and Apm denotes the fundamental gain of each stage. It is also instructive to find the relationship between the 1-dB compression point and the input IP3 for a third-order nonlinearity, which the two can be related by

$$\frac{A_{1-dB}}{A_{IP3}} \approx -9.6dB$$

Based on the analysis previously, the design target of the front-end receiver and its each circuit is listed in Table 3-2. The buffer will be used behind the downconverter for measurement. According to (11) and (12), the design target of receiver is decayed by the buffer for cascaded stages. The Table 3-2 list design target without buffer erosion.

Table 3-1 IEEE 802.11a specification for this thesis required

Frequency bands	5.15 ~ 5.35 GHz
Max RX input power	-30 dBm
Noise Figure	< 15 dB
P-1dB	> -26 dBm
Channel numbers	8
Channel bandwidth	20 MHz

Table 3-2 Design target of the front-end receiver and each circuit

Front-End Receiver	VDD	1 V
	Gain	23 dB
	NF	< 10 dB
	P-1dB	> -26 dBm
	DC offset	< 10 mV
	Power	< 25 mW
LNA	Gain	23 dB
	NF	2 dB
	P-1dB	-14 dBm
Downconverter	Gain	0 dB
	NF	17.7 dB
	P-1dB	0 dBm
Quadrature VCO	Tuning range	5.15 ~ 5.35 GHz

3.2 CIRCUIT REALIZATION

3.2.1 Differential Low Noise Amplifier

In RF system, the LNA, one of front-end circuits, locates on the receiving path of transceiver. The main functions are amplifying RF signal received from the antenna, providing input impedance matching and contributing as minimal noise as possible for the system working well.

Input matching is an important consideration for connection with external components. Described by microwave theoretic, signal is partially reflected if passing through the interface between two different mediums. The meaning in circuit design is unequal input/output impedances between two stages. To minimize the reflection, input

impedance of an LNA has to be designed to match 50-Ω characteristic impedance.

As passive device, an active device such as MOS or BJT contributes impedance. In the design with CMOS process, MOS device is applied with inductor in matching strategy. Fig. 24 helps the analysis by a simple small-signal model of MOS device.

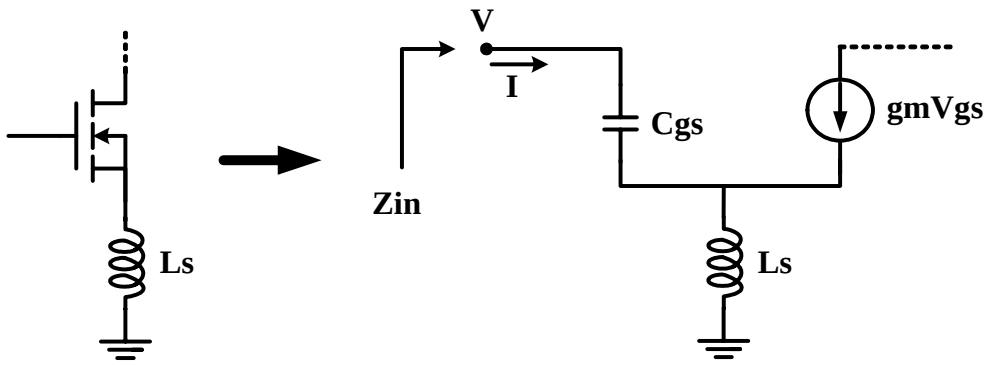


Fig. 24. Input impedance matching

According to Kirchhoff's Voltage Law,

$$V = j\omega \cdot L_S \cdot \left(I + g_m \cdot V_{gs}\right) + \frac{I}{j\omega \cdot C_{gs}}$$

$$= j\omega \cdot L_S \cdot \left(I + g_m \cdot \frac{I}{j\omega \cdot C_{gs}}\right) + \frac{I}{j\omega \cdot C_{gs}}$$

$$\Rightarrow Zin = \frac{V}{I} = \frac{g_m}{C_{gs}} \cdot L_S + j\omega \cdot L_S + \frac{1}{j\omega \cdot C_{gs}}$$

$$= \frac{g_m}{C_{gs}} \cdot L_S + j\left(\omega \cdot L_S - \frac{1}{\omega \cdot C_{gs}}\right) \qquad (13)$$

As described in (1), the source inductor can be designed to eliminate the reactance; the transconductance g_m, parasitical capacitance C_{gs} and source inductance L_S can be designed to achieve 50-Ω resistance.

Actually, input matching is also affected by other inevitable factors. There exists parasitical capacitance on input/output pads. If a chip under test is bonded on a board for measurement, bond-wires contribute parasitical inductance. The parasitic can be practically treated as a part of matching network so that the impedance, *Zin* in Fig. 24, cannot be designed to equal 50-Ω. Fig. 25 depicts a modified model with parasitic of a

pad and a bond-wire. Smith chart is useful for designing a proper value of *Zin*.

Fig. 26 is an impedance Smith chart and designed *Zin* locates on point 1. C_{pad} makes point 1 move to point 2 and L_{bw} makes point 2 move toward point 3. *Zin*' of 50-Ω is available by this more practical method of matching design.

Many of modern technologies provide on-chip spiral inductors. The benefit makes it possible that input matching is achieved with fewer discrete components.

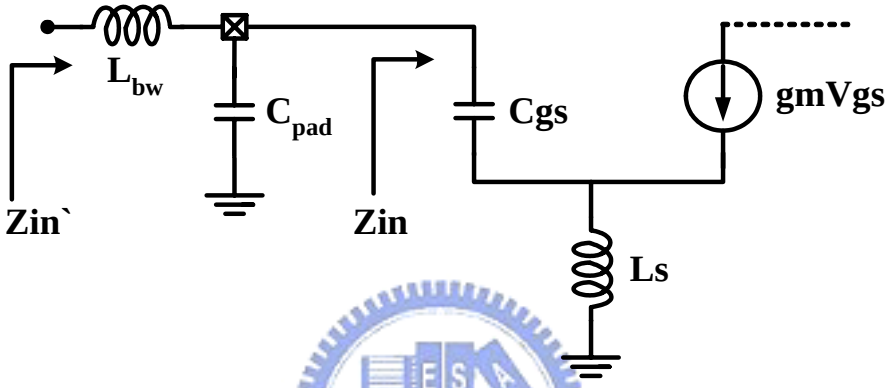


Fig. 25. Modified impedance model

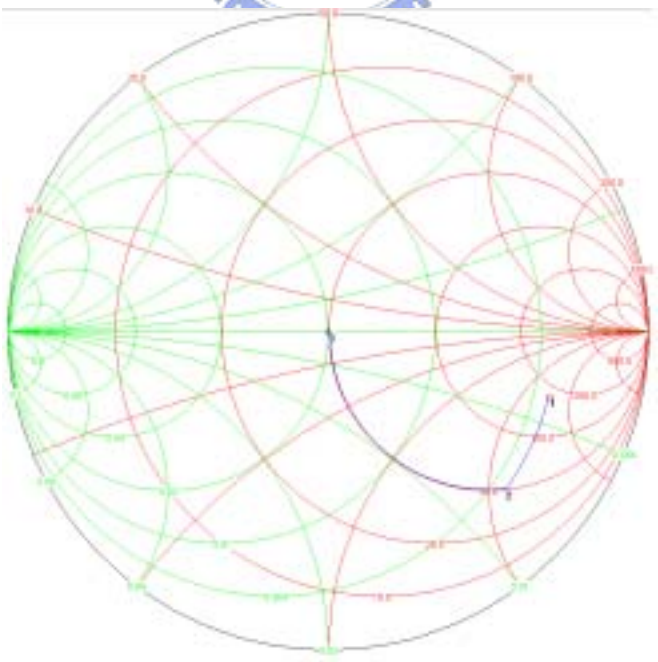


Fig. 26. Impedance Smith chart

Next, Noise figure (NF) is a quantity generally used to estimate noise performance of an LNA. The noise performance on the inductor-degeneration configuration and designing an optimal dimension of the MOS devices will obtain the minimal noise contribution [42]. The following is a definition for noise figure, where SNR denotes signal to noise ratio.

$$NF \equiv \frac{total\_output\_noise}{total\_output\_noise\_due\_to\_input\_source} = \frac{SNR_{input}}{SNR_{output}}$$

Consider a MOS device on the inductor-degeneration configuration. Channel thermal noise and induced gate current noise are main sources in LNA design. The former occurs because of channel resistance. The later appears for the reason that channel charge fluctuates and then induces a physical current toward gate by capacitive coupling. A designer may not care about the later for general analog circuit design. In RF circuit, induced gate current noise, present as blue noise, becomes an inevitable noise contribution. Fig. 27 shows a noise model of the input stage, where $\overline{V_{Rg}^{\ 2}}$ and $\overline{I_g^{\ 2}}$ corresponds to the mentioned noise power.

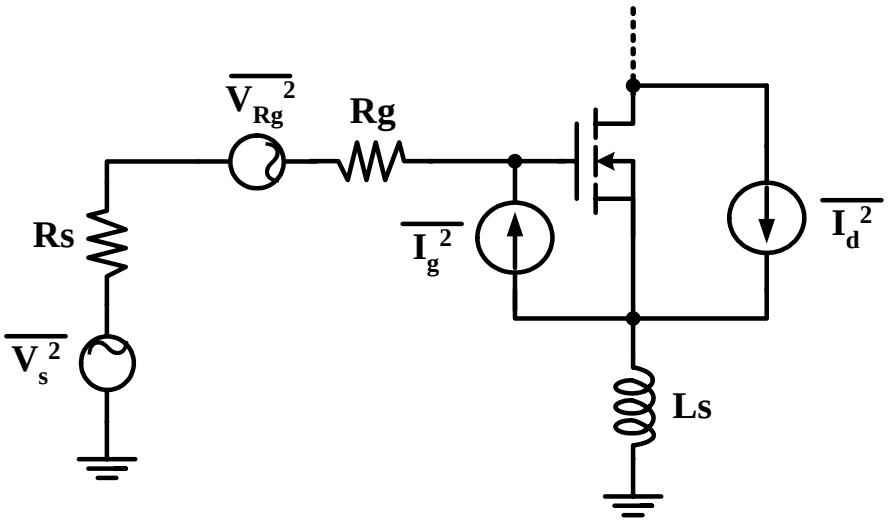


Fig. 27. Noise model of input stage

In the figure, R_S and R_g are resistances of input terminal and gate; $\overline{V_{Rg}^{\ 2}}$ and $\overline{I_g^{\ 2}}$

correspond to two noise powers induced by R_S and channel resistance, respectively. Based on the model, theoretically minimal noise figure formulates as

$$NF_{\min} = 1 + \frac{\gamma \omega_0 L}{3 v_{sat}} p\left(\frac{V_{od}}{L \varepsilon_{sat}}, P_c \right) \tag{14}$$

, where γ is bias-dependent factor, L is channel length, v_{sat} is saturation velocity, V_{od} is overdrive voltage, ε_{sat} is velocity saturation field strength and P_c is power consumption. $P\left(\frac{V_{od}}{L \varepsilon_{sat}}, P_c \right)$ denotes ratio of two high-order polynomials. More details can be investigated in [41]. Channel width (W) is also an important parameter for the dimension decision and formulates as

$$W = \frac{P_c \left(V_{od} + L \varepsilon_{sat} \right)}{V_{dd} C_{ox} v_{sat} V_{od}^{\ 2}} \tag{15}$$

(14) with (15) reveals that channel width is an implicit function of NF_{min}.

For circuit designer, decidable parameters are V_{dd}, W, L and P_c. Minimal L is generally used for minimum NF_{min}. The designed LNA optimizes the noise performance by choice of W and P_c, since V_{dd} has been specified on 1 V. Fig. 28 plots NF_{min} curves based on analysis of [42].

Transconductance of input-stage MOS and load impedance dominate voltage gain in common-source-configuration amplifier. The transconductance is fixed while DC condition and dimension of the MOS has been decided for noise optimization and input matching. Sufficiently high load impedance or other advanced circuit structure with the identical input stage is then expected. In RF field, LC-tank is a proper choice for load impedance if fabrication technology is able to provide inductors with adequate Q-factors. Theoretically, the higher Q-factor load causes the higher gain. Common source cascode with LC-tank load is a popular structure in plenty of LNA designs. Not only Miller effect can be avoided but also reverse isolation is enhanced.

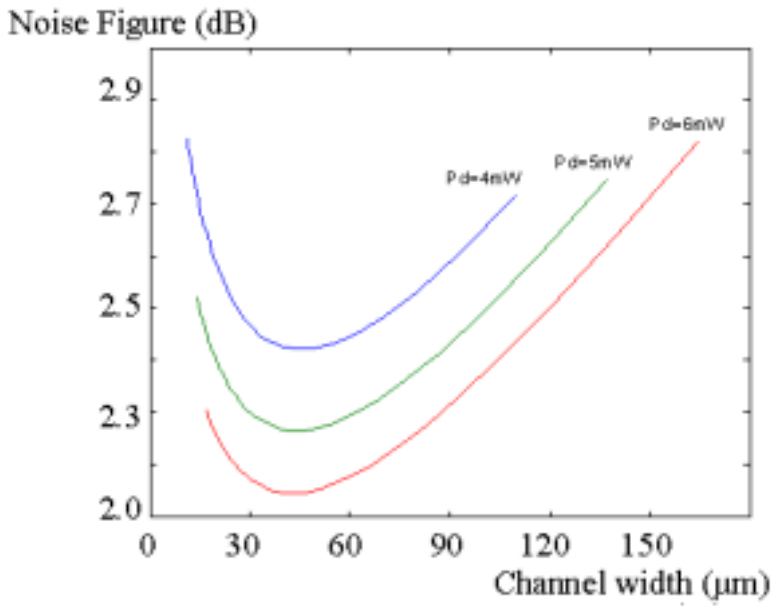


Fig. 28. NF_{min} curves to W and P_c

Although high-Q load increases gain effectively, linearity is contrarily degraded. In wireless communication, channel type is narrow band. An LNA operating with nonlinearity causes intermodulation while signals at various frequencies are received simultaneously [4]. The phenomenon produces other signals locating at frequencies close to those of received signals. There is an illustration in Fig. 29 for example. An LNA receives two signals of near frequencies ω_1 and ω_2, and then outputs signals of ω_1, ω_2, $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$. As the power of ω_1 and ω_2 increases, the power of $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ grows up in cube. The additional signals may fall on the adjacent channels and corrupt normal receiving.

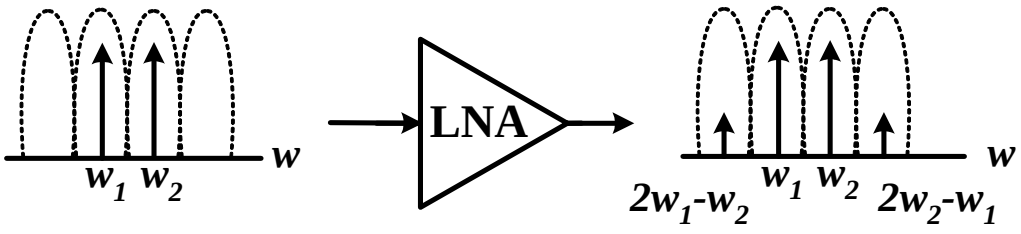


Fig. 29. Intermodulation phenomenon

For acceptable linearity, extremely high voltage gain is not proposed. The gain is generally designed in an appropriate range of 15 ~ 25 dB in a conventional LNA for wireless communication.

RF receiver may easily suffer from noise coming from power supply because the input belongs to small signal. Differential circuit is a prevalent topology for the noise rejection. A differential amplifier is ideally designed to operate with differential signal. The function is also simulated with pure differential signal. However, there exists common-mode issue in differential amplifier. Actually, a differential LNA may receive RF signal with a common-mode fraction. If one end of a differential pair does not perfectly match with the other, common-mode signal still appears on the single output terminal combined from the differential terminals. Too large common-mode signal corrupts desired signal or even saturates the amplifier. Even if the two ends match perfectly, large common-mode swing may saturate the circuit and then make the function inactive. Therefore, capability of common-mode rejection is considerable in differential amplifier design.

MOS device as current source is usually applied in analog integrated-circuit design. The high drain-impedance providing source degeneration helps suppressing common-mode signal. However, the drain-impedance decreases to a very low value at a radio frequency. Common-mode feedback circuit may be another solution but consumes extra power. The design of LNA proposes applying LC-tank as source degenerator to suppress common-mode signal. LC-tank provides much higher impedance than a MOS device being current source in desired RF range. Besides, the LC-tank is appropriate in low-voltage low-power design.

Based on the considerations in the previous section, an LNA circuit is designed, shown in Fig. 30 with parameter information in Table 3-3. The LNA is common-source-cascode and fully differential configuration. Input matching and noise optimization are designed in LI1, LI2, MI1 and MI2. LC-tank constructed with LI3, LI4 and its total parasitical capacitance provides impedance for voltage gain. The other tank comprising LI5 and its total parasitical capacitance works as a common-mode source degenerator. In

the aspect of low-voltage design, the output can swing over supply voltage because of the inductor character. Furthermore, the source degenerator hardly causes voltage drop. Total DC-drop from sum of sufficient drain-source voltages is merely about 0.4 V by TSMC 0.18-μm technology. In the condition, LNA function is achievable at 1-V supply voltage. Most inductors applied are spiral inductors supported by TSMC 0.18-μm technology. The 1.2-nH inductor is provided by National Chip Implementation Center (CIC). The equivalent circuit of spiral inductor is complicated due to obstacles in fabrication. There are also restrictions for usage, such as maximum operating frequency and various Q-factors at different frequencies.

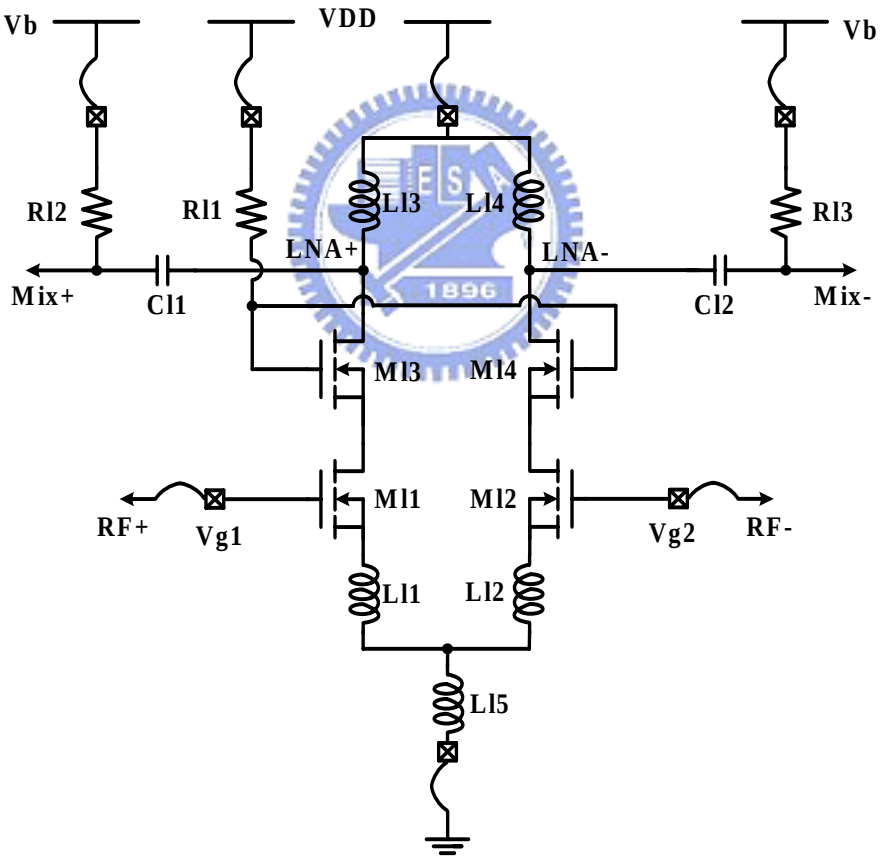


Fig. 30. Designed LNA circuit

Table 3-3 Parameter information of Fig. 30

Ml1 and Ml2	50 μm/0.18 μm
Ml3 and Ml4	70 μm/0.18 μm
Ll1 ~ Ll4	2.4 nH
Ll5	1.2 nH
Rl1	5.4 kΩ
Rl2 and Rl3	33 kΩ
Cl1 and Cl2	0.55 pF

3.2.2 Quadrature Voltage-Controlled Oscillator

A giga-hertz oscillator usually comprises a resonator including inductor, capacitor and negative resistor. Fig. 31 depicts the resonator structure. The design of quadrature VCO follows the basic way, too. In order to generate quadrature signal, a structure of ring oscillator is also introduced [8]. Combing two resonators and two inverters, the quadrature VCO is implemented. Fig. 32 presents the conceptual diagram of the quadrature VCO.

INV_I and INV_Q are two identical inverters of common-source configuration. The inverter circuit is shown in Fig. 33. Finally, realization of the conceptual diagram of Fig. 32 is shown in Fig. 34 with parameters listed in Table 3-4.

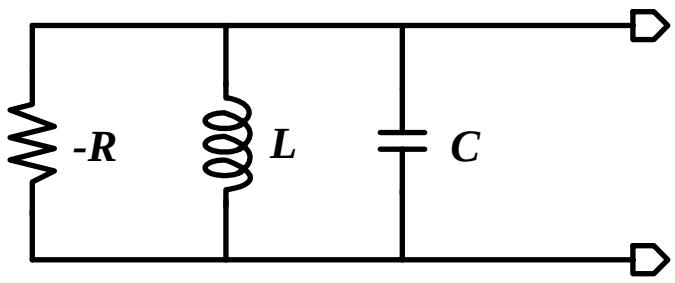


Fig. 31 General resonator

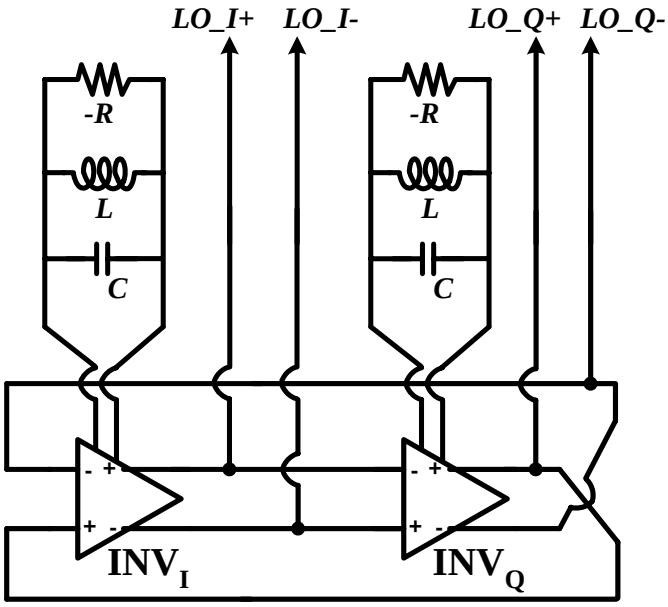


Fig. 32. Conceptual diagram of the quadrature voltage-controlled oscillator

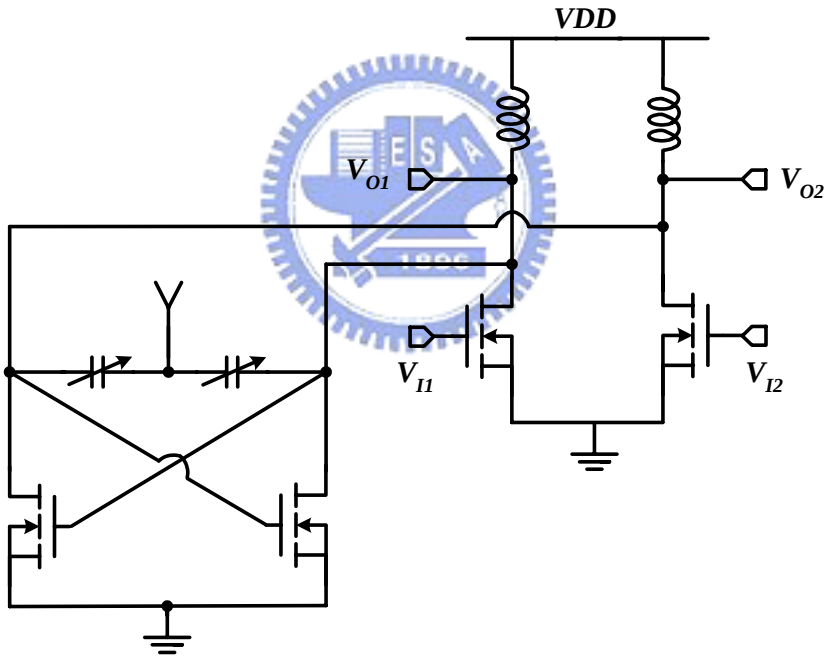


Fig. 33. Inverter circuit applied in the quadrature voltage-controlled oscillator.

For low-voltage consideration, the two LC-tanks perform not only resonator components but also loads. Thus the output voltage swing can exceed VDD to achieve sufficiently large amplitude and keep sinusoidal waveform. Moreover, there is an obvious feature that the four output terminals have equal DC levels, and the output terminals could directly connect to next-stage circuit without re-bias.

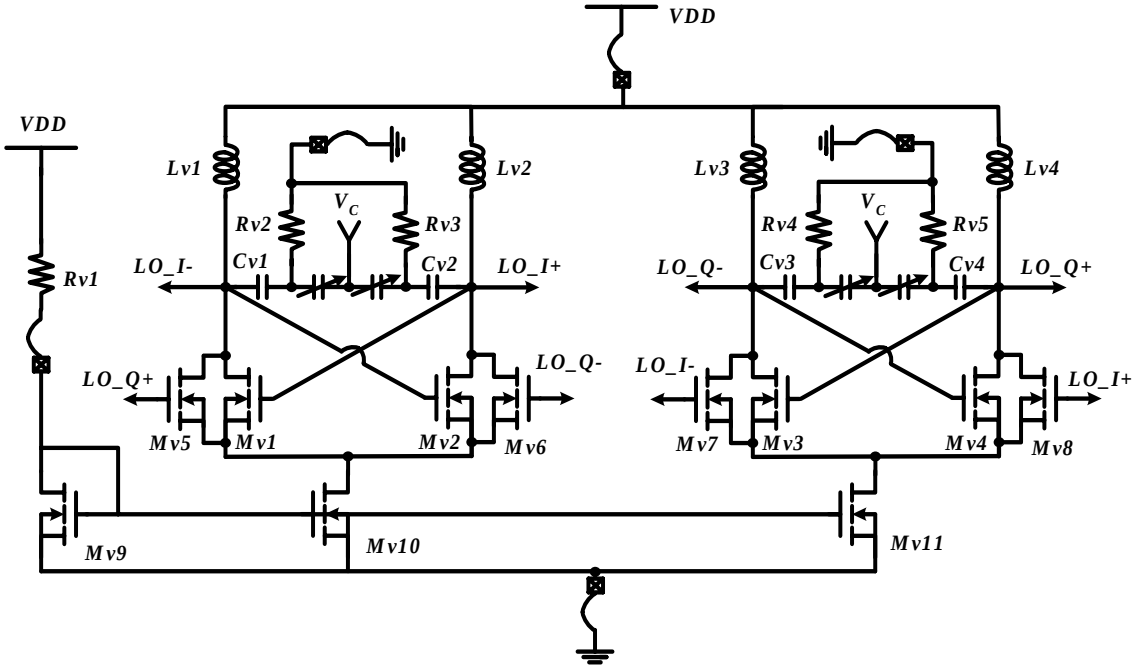


Fig. 34. Quadrature voltage-controlled oscillator

Table 3-4 Parameter information of Fig. 34

Mv1 ~ Mv8	35 μm/0.18 μm
Mv9	12.5 μm/0.18 μm
Mv10 ~ Mv11	75 μm/0.18 μm
Lv1 ~ Lv4	1.2 nH
Rv1	150Ω
Rv2 ~ Rv5	5.4 kΩ
Cv1 ~ Cv4	0.57 pF

3.2.3 Output Buffer

A buffer circuit as output stage follows the downconverter for measurement. The circuit comprises four common-source amplifiers with complementary load, following the four output terminals of the downconverter respectively. Fig. 35 is one channel of the buffer circuit with two common-source stages. According to (11) and (12), the performance of the receiver is interacted by each stage in the cascaded stages. In order

to keep the minimum damage of the linearity, the output buffer circuit is used the Class A concept and the power supply is used 1.6V/-0.4V to make the output DC level at half of the supply voltage. Normally, the output terminal of buffer is connected a DC block capacitance to protect the instrument. But this will obstruct measurement for DC offset. Based on this consideration, the output buffer load is connected to a off-chip element, it can be realized by the thick film chip resistor (SMD resistor) or the oscilloscope load, and the DC offset can be measured from the output terminal easily. The low frequency gain of buffer is designed about 0 dB and the corner frequency is at 100 MHz. The frequency response is showed in Fig. 36.

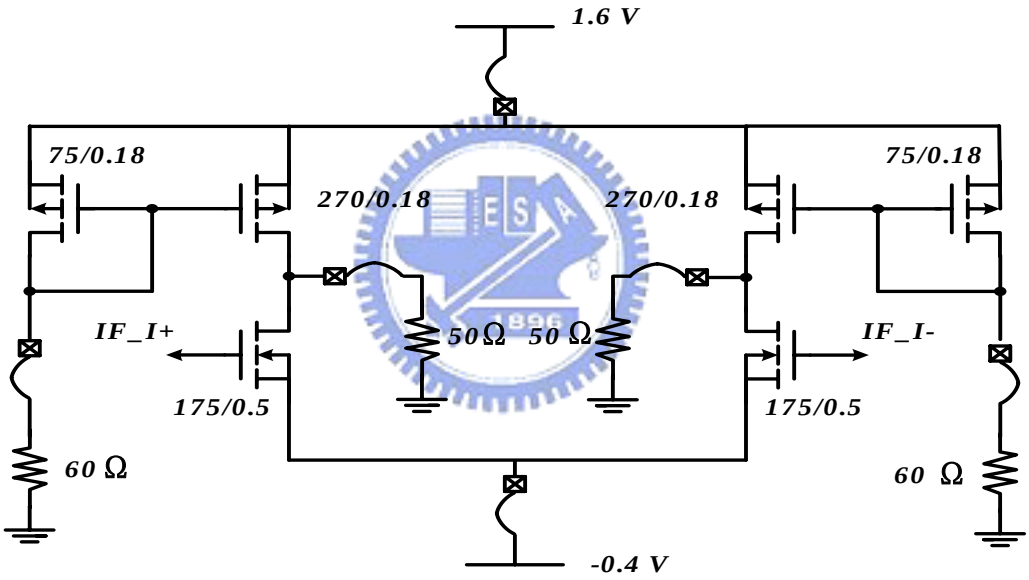


Fig. 35. One channel of the output buffer circuit.

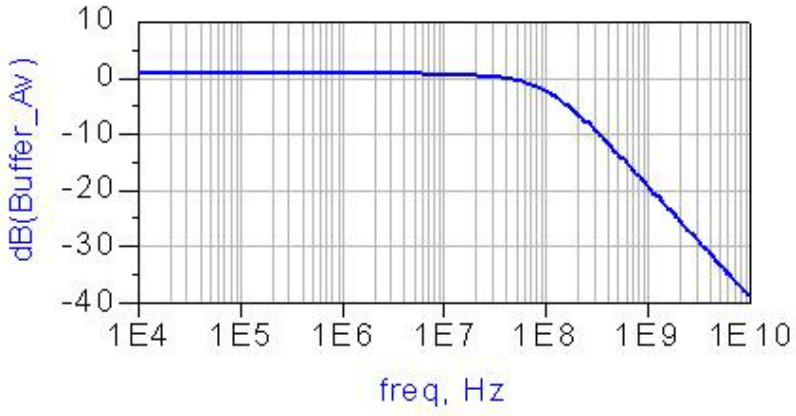


Fig. 36. Frequency response of output buffer

3.3 SIMULATION RESULTS ON FRONT-END RECEIVER

Post-simulation is completed by ADS simulator with process parameters of TSMC 0.18-μm mixed signal 1P6M RF SPICE models. The following are post-simulation results of all circuits constructing the receiver. All inductors employed are spiral inductors made of top thick metal; varactors are n-well structure; resistors are HRI P-poly resistor without silicide. To avoid body effect, all N-MOS devices contain deep n-well for equal voltage potential between respective bodies and sources. The model is supported by TSMC.

- *Low-noise amplifier*

LNA, locating on the first stage of the receiver, provides input matching, voltage gain and low noise contribution for the receiver in specific frequency band. Fig. 37 presents the simulated input matching (S11) lower than –10 dB between 5.11 GHz and 5.62 GHz. Fig. 38 shows voltage gain about 23 dB at desired bands. Fig. 39 is the simulation result of noise figure (NF) to frequency. If the dimension of MOS devices on input stage is optimized for noise, the NF value falls closely on the minimum. To evaluate the linearity performance, two-tone test is introduced [4]. Let the LNA receive two near-frequency signals and then output signals of first order and third order, the later produced due to intermodulation. Fig. 40 plots power relation of the two terms in logarithmic scales. The horizontal coordinate of the two-line intersection, called IIP3 (input third intercept point), is a parameter for linearity estimation. The P-1dB compression point also can be obtained from this estimation. A summary of the LNA is listed in Table 3-5.

Fig. 37. Simulated S11 of the LNA

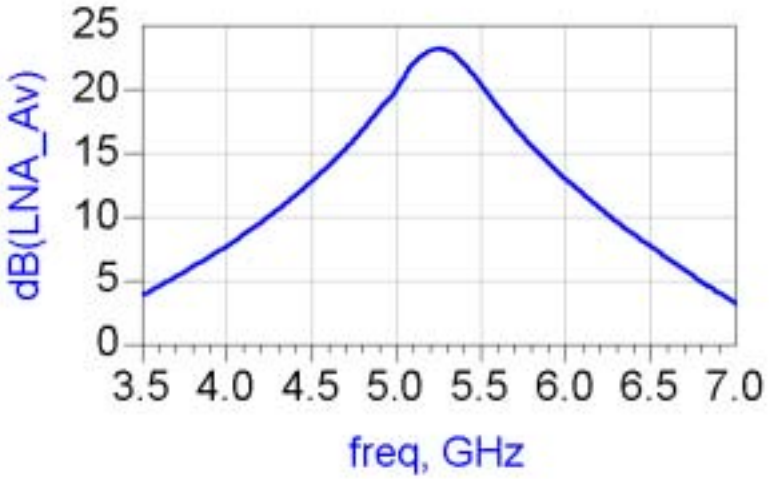


Fig. 38. Simulated voltage gain of the LNA

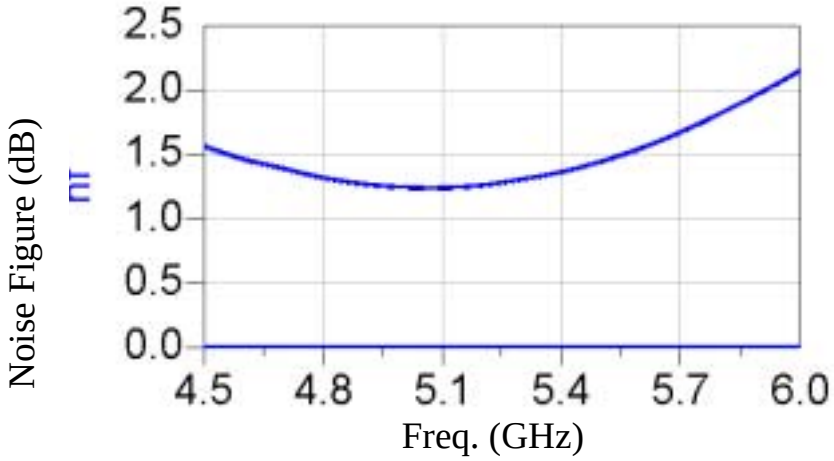


Fig. 39. Simulated noise figure of the LNA

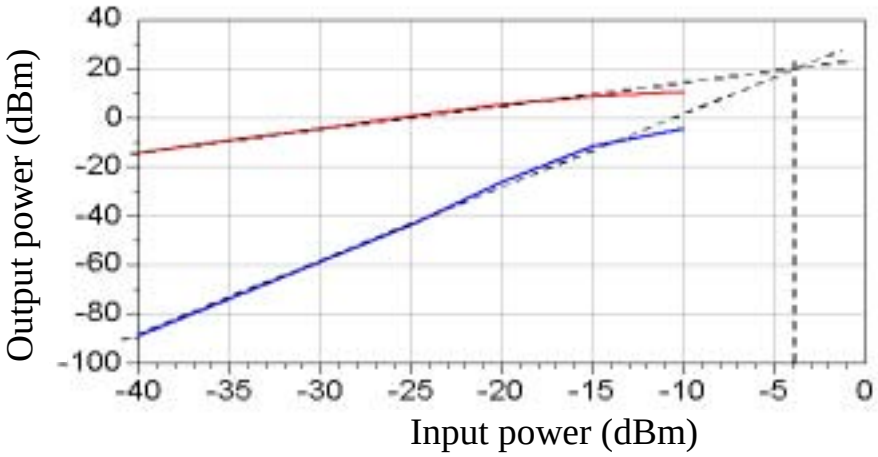


Fig. 40. Two-tone-test plot for simulated IIP3 of the LNA

Table 3-5 Post-simulation summary of the LNA

Technology	TSMC 0.18- μ m 1P6M
Frequency	5.25 GHZ
Supply Voltage	1.0 V
Power Consumption	3.56 mW
S11 (< -10 dB)	5.11 ~5.62 GHz
Voltage Gain	23 dB
Common-mode gain	-10 dB
SSB NF	1.3 dB
P-1dB	-13 dBm
IIP3	-4 dBm

■ *Quadrature voltage-controlled oscillator*

Fig. 41 presents the differential output of LO spectrum, a desired tone at 5.24 GHz observed. Fig. 42 and Fig. 43 are sequentially quadrature LO waveform and tuning-range plot. The quadrature VCO oscillates 5.13 ~ 5.37 GHz by control voltage 0 ~ 1 V. A summary of the quadrature VCO is listed in Table 3-6.

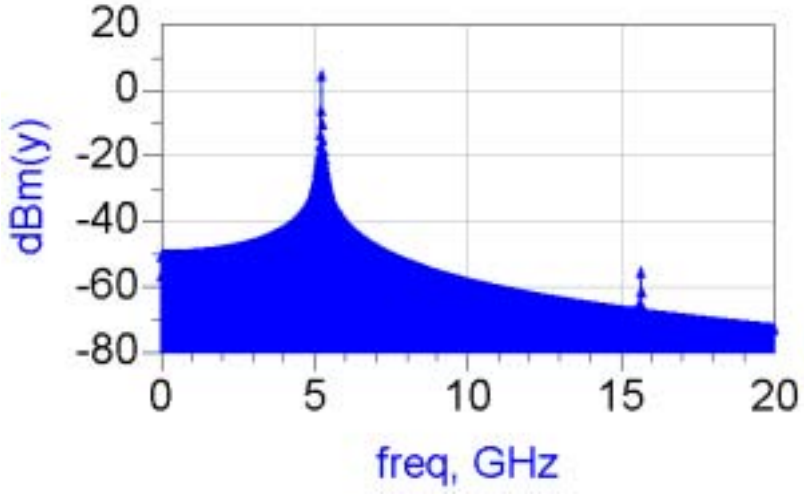


Fig. 41 Differential output of LO spectrum

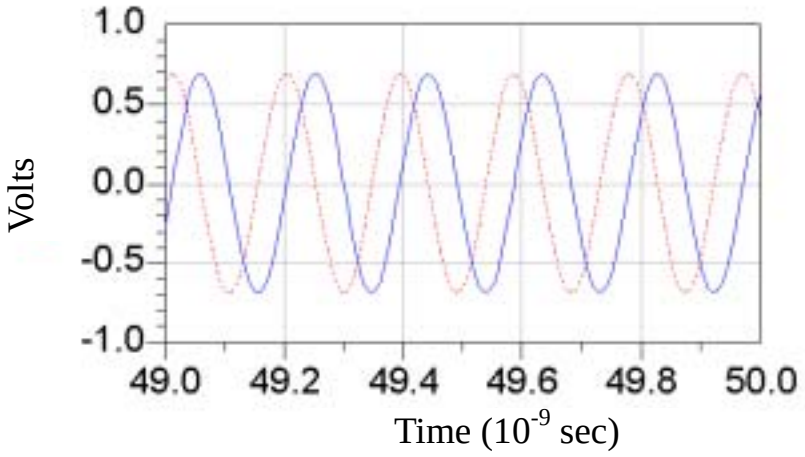


Fig. 42. Quadrature LO waveform (solid-line：I-channel；dash-line：Q-channel)

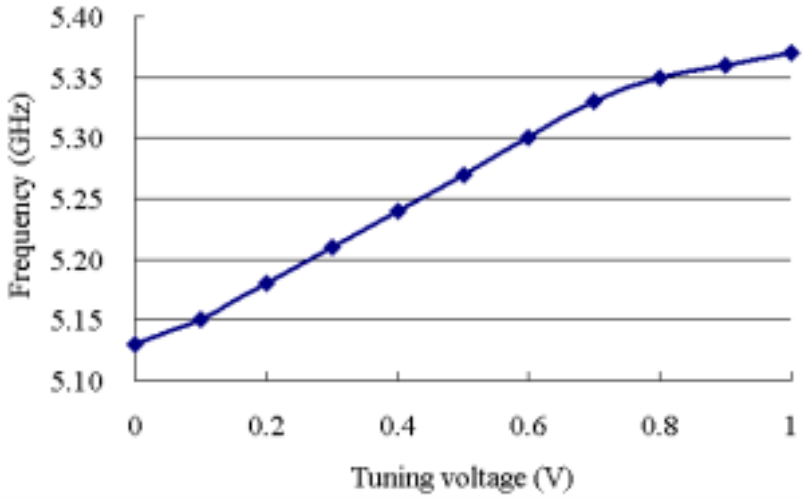


Fig. 43. Simulated VCO tuning range

Table 3-6 Post-simulation summary of the quadrature VCO

Technology	TSMC 0.18- μ m 1P6M
Supply Voltage	1.0 V
Power Consumption	13.51 mW
Tuning range	5.13 ~5.37 GHz
KVCO	240 MHz/V
Output power	0 dBm

■ *Overall*

Fig. 44 is IF waveform probed on output of the buffer. The IF signal is 6 MHz with 23 dB conversion gain. Two-tone test is applied to simulate linearity of the receiver circuit. Fig. 45 plots output power of first and third order terms relative to input power. This simulation includes the output buffer, and the P-1dB compression point can increase about 3.8 dB if the output buffer is removed. Fig 46 presents output noise voltage spectral density of receiver. The noise bandwidth of this circuit is from 150-KHz to 10-MHz. The total noise figure of the receiver is calculated approximately by (10), the noise figure of receiver at the interesting band is 7.8dB. Fig. 47 shows simulated results of the receiver DC offset at each sub-circuit with differential output. The simulation method mentions at chapter 2. The DC offset voltage is about 6-mV at buffer output with input injected power of –50-dBm. The related offset is listed in Table 3-7. Based on same condition, the Fig. 48 ~ Fig. 50 shows DC offset Monte Carlo simulation at buffer output with only LNA channel-length variations, both LNA and Mixer channel-length variations, whole receiver channel-length variations, respectively. It sets uniform distribution of 10% variations with 200 times Monte Carlo simulation. The results imply that layout symmetry is important especially for the preceding stage.

If the uniform distribution of variations is set to 3%, the DC offset is kept in 10-mV. Last, Table 3-8 lists the corner-case simulation results and Table 3-9 lists a summary of the receiver.

Fig. 44. Simulated I-channel and Q-channel IF waveform

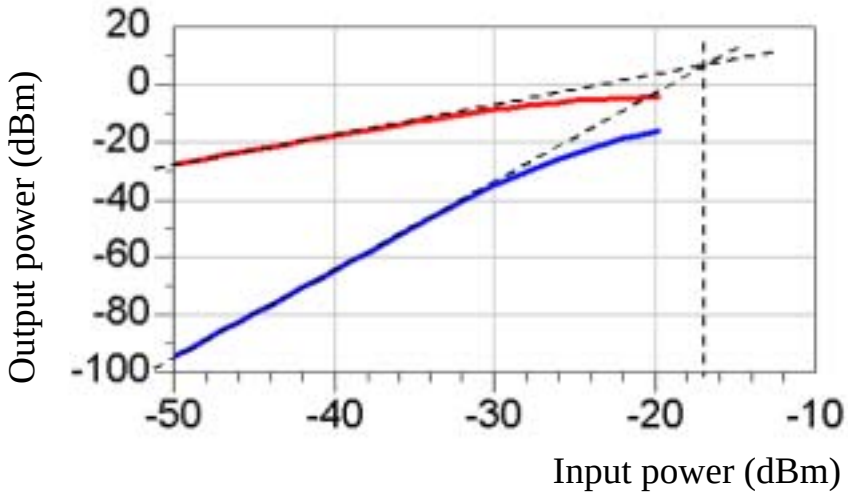


Fig. 45. Two-tone-test plot for simulated IIP3 of the receiver

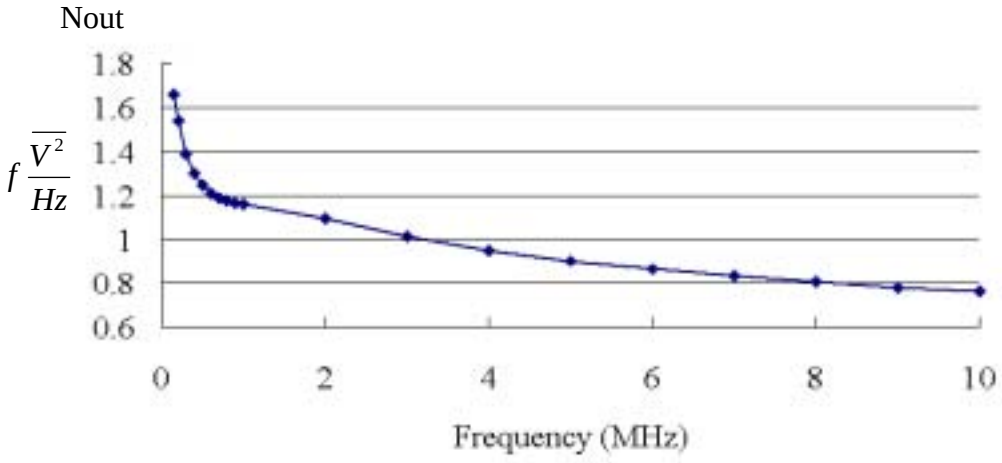


Fig. 46. Output noise voltage spectral density of receiver

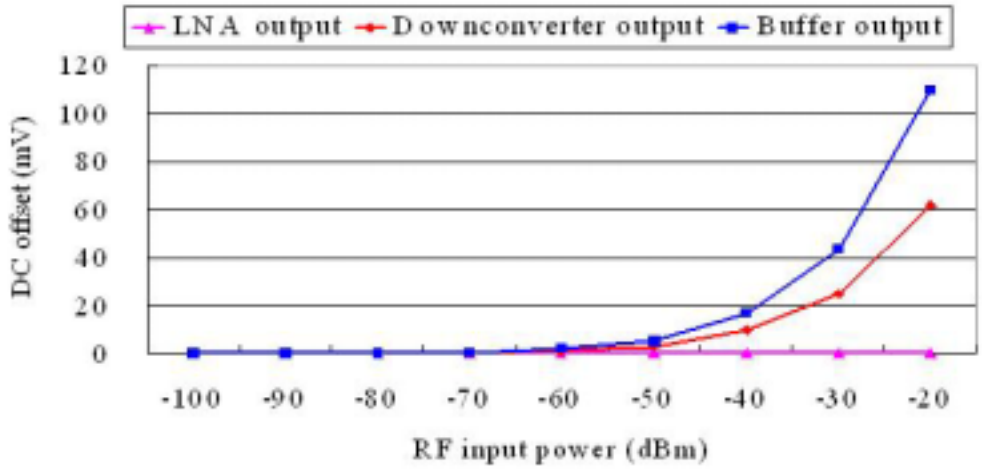


Fig. 47 DC offset at each sub-circuit with differential output

Table 3-7 DC offset information of Fig. 47

injected power	LNA output	Downconverter output	Buffer output
-60 dBm	0.81 μV	1 mV	2 mV
-50 dBm	1.39 μV	3 mV	6 mV
-40 dBm	2.21 μV	10 mV	17 mV
-30 dBm	3.63 μV	25 mV	44 mV
-20 dBm	24.6 μV	62 mV	110 mV

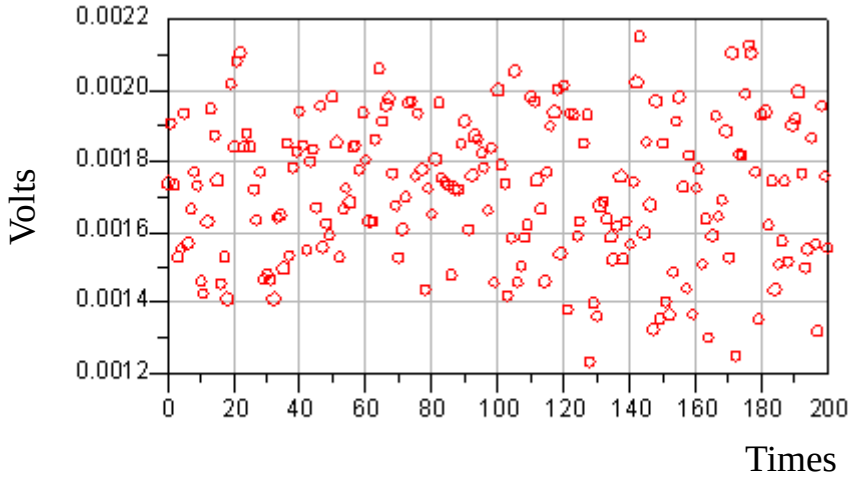


Fig. 48. Monte Carlo simulation with only LNA channel-length variations

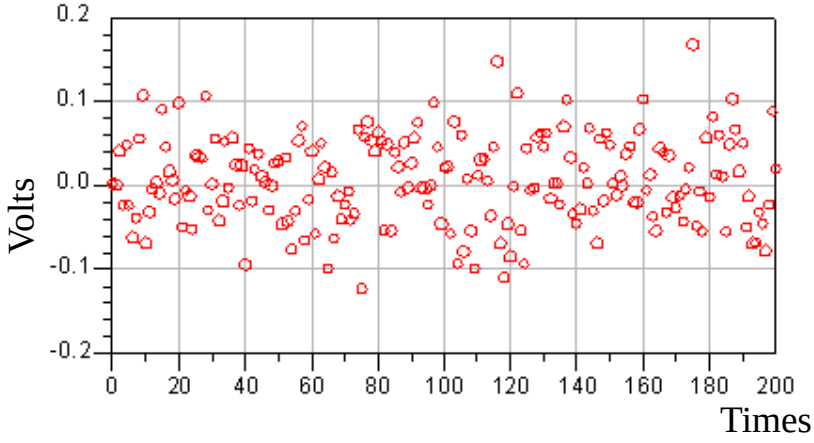


Fig. 49. Monte Carlo simulation with LNA and Mixer channel-length variations

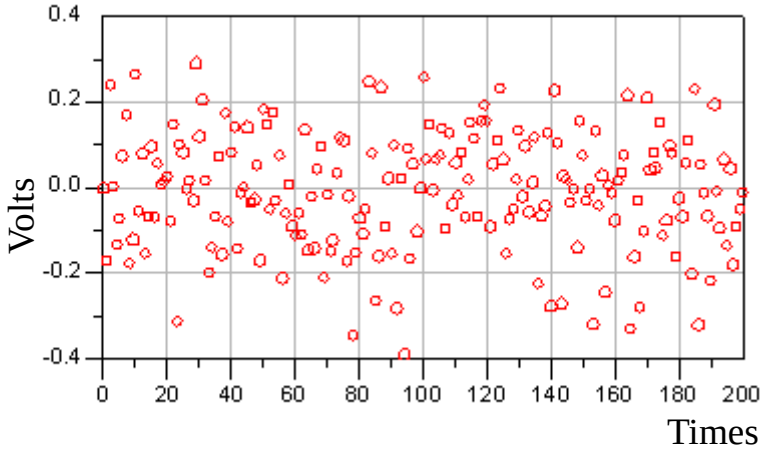


Fig. 50. Monte Carlo simulation with whole receiver channel-length variations

Table 3-8 Corner-case simulation summary of the receiver

Corner Type	FF	SS
Technology	TSMC 0.18- μ m 1P6M	
Supply Voltage	1.0 V	
Frequency Band	5.15 ~ 5.35 GHz	
Power Consumption	20.1 mW	21.3 mW
S11 (< -10 dB)	5.05 ~ 5.42 GHz	5.04 ~5.66 GHz
Conversion Gain	23.4 dB	24.6 dB
SSB NF	7.6 dB	6.85 dB
P-1dB	-26.2 dBm	-26.6 dBm
IIP3	-16 dBm	-17 dBm
fL	0.15 MHz	0.14 MHz
fH	32 MHz	29 MHz
Tuning Range	5.10 ~ 5.36 GHz	5.09 ~ 5.36 GHz
DC Offset (injected –50 dBm at receiver input)	1 mV	3 mV

Table 3-9 Post-simulation summary of the front-end receiver

Technology	TSMC 0.18- μ m 1P6M
Supply Voltage	1.0 V
Frequency Band	5.15 ~ 5.35 GHz
Power Consumption	20.9 mW
S11 (< -10 dB)	5.11 ~5.62 GHz
Conversion Gain	23 dB
SSB NF	7.8 dB
P-1dB	-23.8 dBm (without buffer)
	-27.6 dBm (with buffer)
IIP3	-17 dBm
fL	0.15 MHz
fH	30 MHz
Tuning Range	5.13 ~ 5.37 GHz
DC Offset (injected –50 dBm at receiver input)	6 mV

CHAPTER 4

EXPERIMENTAL RESULTS

A front-end receiver are designed and fabricated. This chapter is presenting chip layout, test environment and experimental results. Measured performances are taken into discussion and comparison with post-simulations.

4.1 LAYOUT DESCRIPTION

The receiver chip is fabricated in CMOS process with TSMC 0.18-μm, a single poly layer, six layers of metal, and option of metal-insulator-metal (MIM) capacitors, thick-metal inductor and high sheet HRI P- poly resistors without silicide. All N-MOS devices are arranged with deep n-well technique. The technique allows source and substrate of an individual N-MOS to be connected to avoid body effect. As all circuits are fully differential configuration, the components are disposed symmetrically as far as possible. Dummy gates and dummy resistors are equipped at the margins of every MOS device and resistor respectively to cope with process variation. The each sub-circuit is surrounded with guard rings and two output buffers are used double guard rings for stable electric potential on substrate. Every spiral inductor keeps proper distances with the others and the core circuit to prevent mutual inductance and disturbance on circuit working. For the input matching consideration, the two RF input pads are designed individually. The layout is done according to RF design guidelines, keeping DC traces thin and AC connections wide and short. Signal paths are also as short as possible in metal route to alleviate transmission line effect. Every gate-bias pad feeds a DC voltage via a k□-order resistor for gate reliability. Every DC pad is recommended not to locate

between two differential-signal pads so that signal lines, connected to signal pads with bond-wires, on the external board is not restricted by DC lines. Fig. 51 shows the receiver layouts, the total die area is less than 2.1 mm^2.

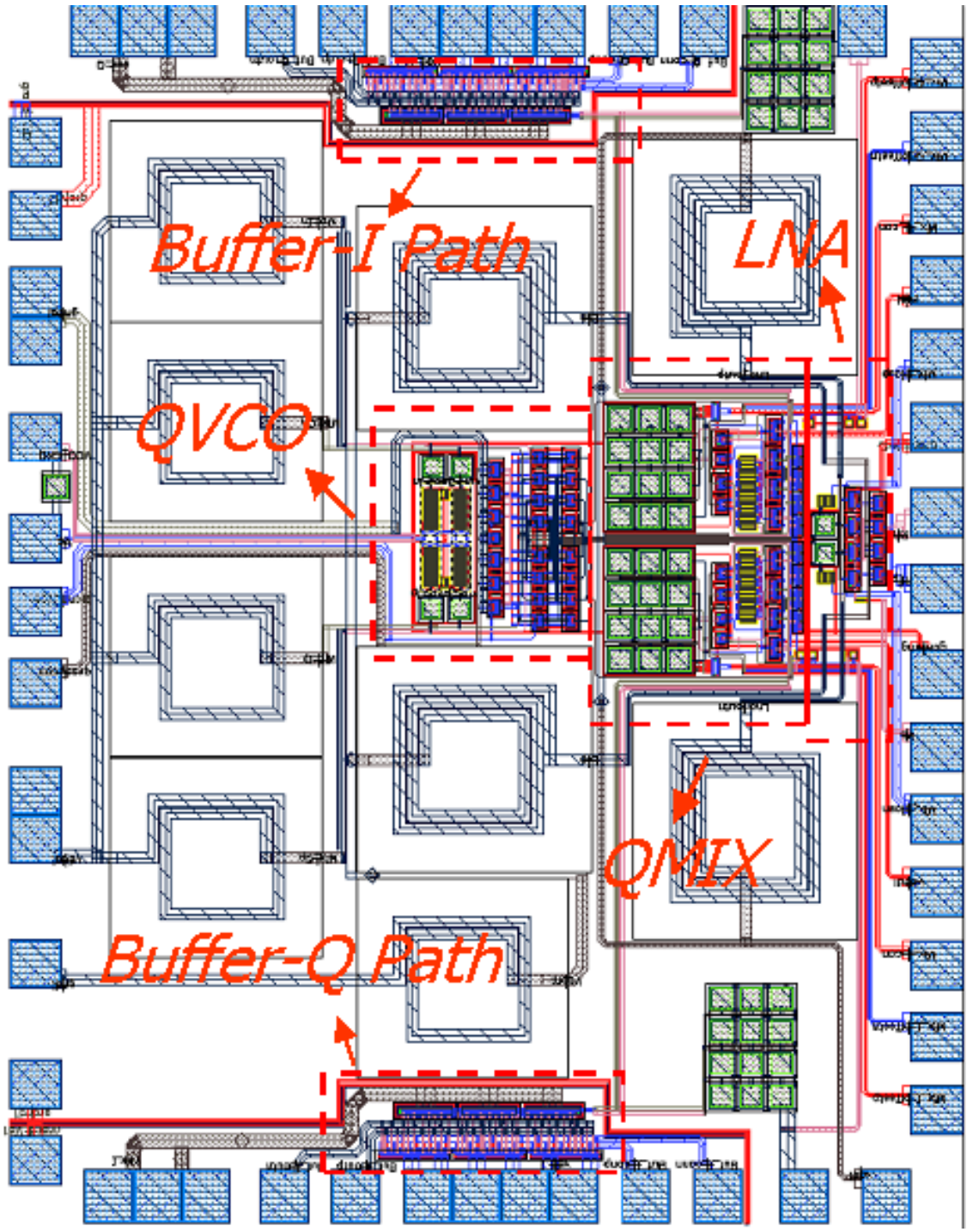


Fig. 51 The receiver layout

The LNA and downconverter of the receiver are complicated in implementation and suffer from process variation easily. Mismatches between two supposedly identical devices are due to localized geometric, material gradient and temperature gradient variation during the fabrication processes. The MOS disposition with the same orientation and stacked wide structure are used for process-variation tolerance and symmetrical signal route. Besides, an additional guard ring surrounds each channel of the downconverter to alleviate LO affection due to substrate couple.

4.2 MEASUREMENT SETUP AND CONSIDERATION

The receiver chip is bare dies and need to be bonded on board. Packaged chips are excluded because of more complicated parasites. The chip microphotographs and the respective bonding board are shown in Fig. 52 and Fig. 53.

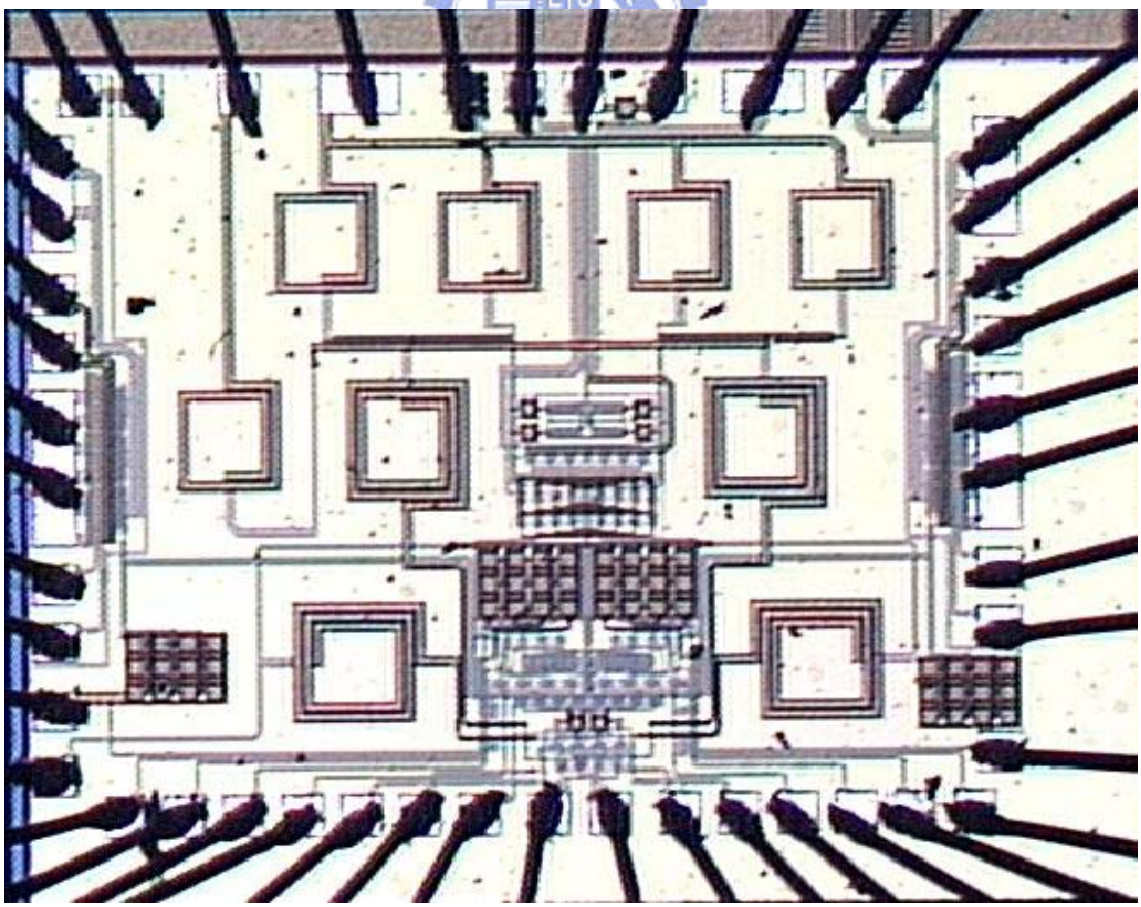


Fig. 52. Chip microphotographs

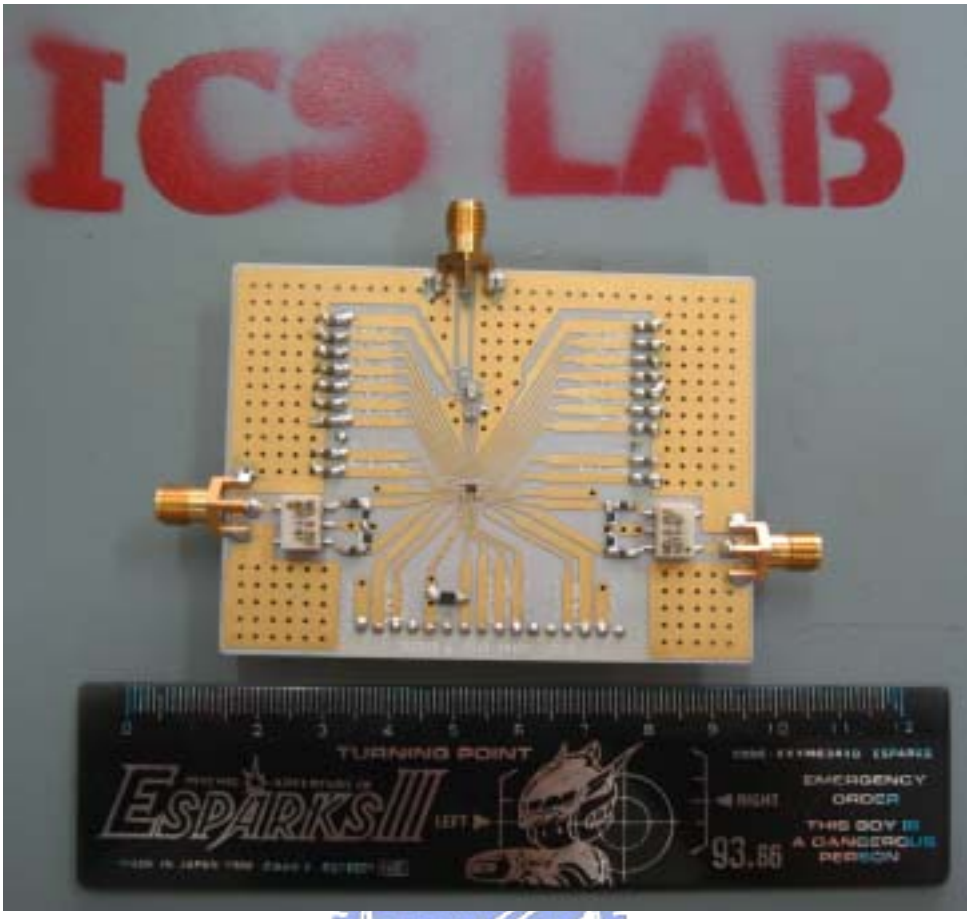


Fig. 53. Bonding board for the receiver

The chips is fully differential circuit so baluns and transformers are necessary for RF and IF terminals in measurement. The baluns with part number BL2012-10B5388 are made by Advanced Ceramic X Corporation. The transformers with module number ADT1-6T are made by Mini-circuits. Inductance variation of bond-wire may affect input matching. Matching network of micro-strip and discrete capacitor are employed to compensate the input matching. Fig. 54 presents the half circuits of input matching network. The C_P and L_P express the pad capacitance and inductance of bound-wire respectively. The C_S is the discrete capacitor that straddles the micro-strip and divides it into two parts, Z_{01} and Z_{02}. The length of micro-strip is fixed and C_S slides on it to achieve optimum input matching. The discrete capacitor with part number CC0603BRNPO9BN0R5 are made by YAGEO. Fig. 55 shows the matching network by photograph.

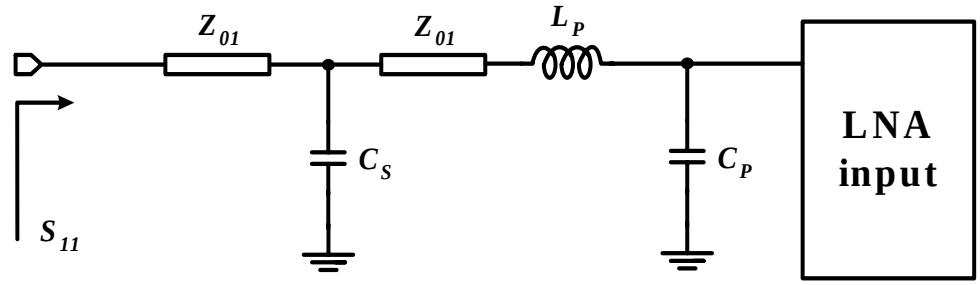


Fig. 54. The half circuits of input matching network

Fig. 55. Photograph of matching network

Signal attenuation caused by the baluns, transformers and matching network is measured for compensating back to relative apparent performances. Every bias terminal is fed externally for flexible adjustment. A tunable resistor can provide an adjustable voltage source. Three parallel capacitors, 0.1 μF, 4.7 μF and 470 μF, connect the voltage source and ground to filter noise from the power supply. Fig. 56 presents the scheme. The receiver chip under test needs several of the modules. As shown in Fig. 57, the modules are integrated in a DC board for the bonding board of receiver.

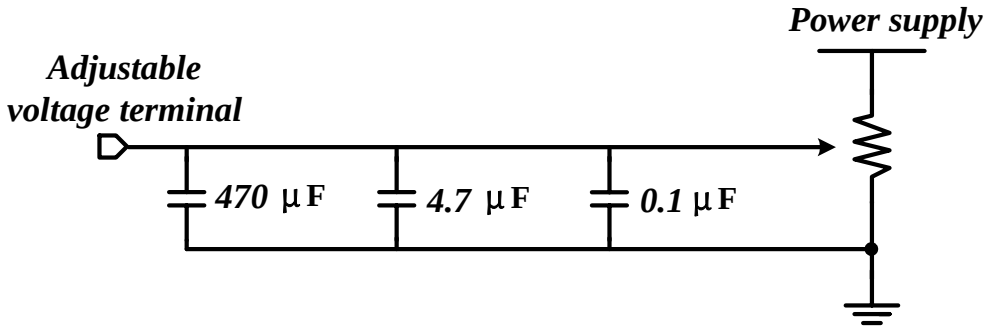


Fig. 56 Adjustable voltage modules

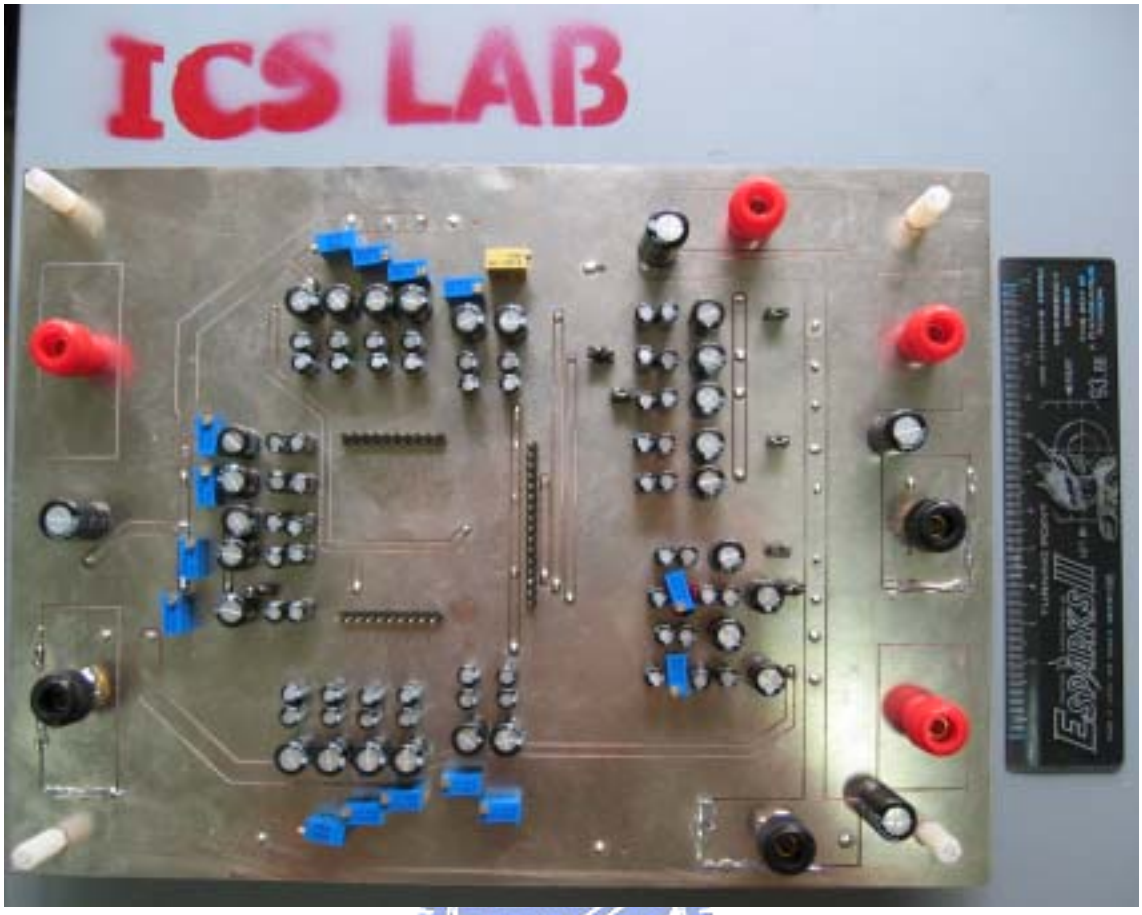


Fig. 57. DC board for the bonding board of receiver

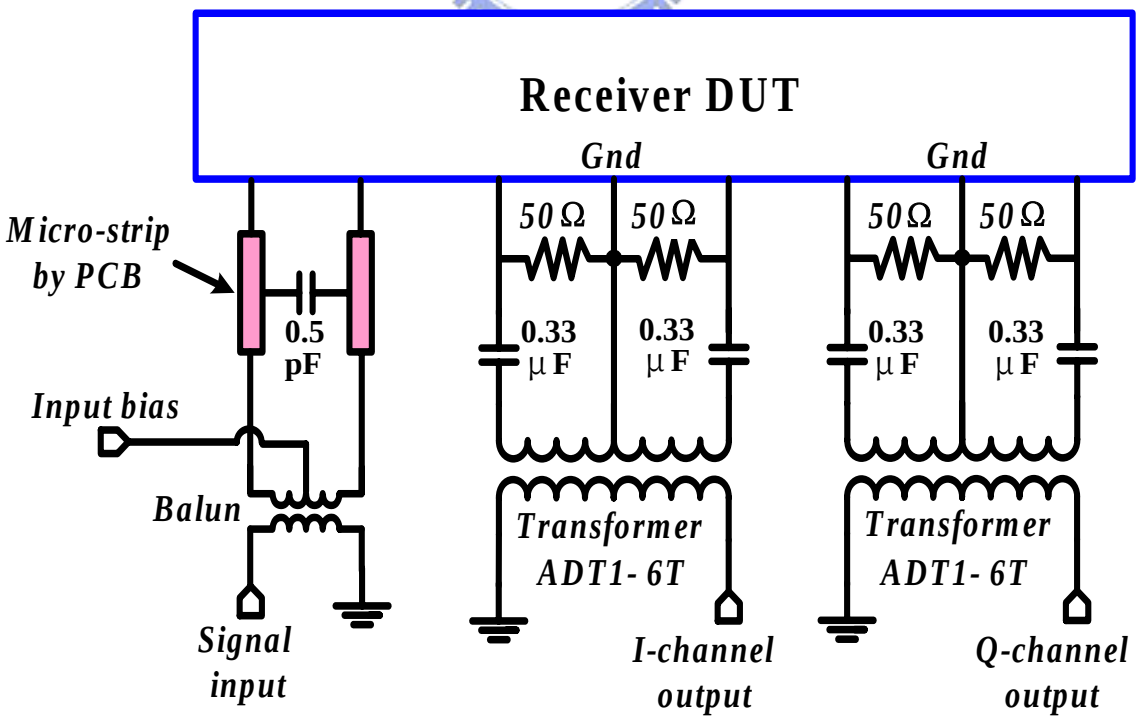


Fig. 58. (a)The receiver chip integrated with discrete component

Essential fixtures are integrated on the bonding boards, depicted in Fig. 58 (a). The external 50-Ω is connected before the DC blocking capacitor in order to measure DC offset voltage. The measurement method of DC offset voltage is depicted in Fig. 58 (b). The receiver is inputted a signal tone, ω_1, which frequency is the same as quadrature VCO generated, ω_2. When they are downconverted to DC, it imply the DC offset voltage is appeared on the buffer output. As the input power more strong, the DC voltage is more conspicuous.

In order to obtain stable LO, the battery is used as supply voltage and the bypass capacitor are connected on the bonding board of the receiver. Those capacitors would filter out the external noise into QVCO and the IF signal would more stable. The related disposition of bypass capacitors is showed in Fig. 59.

Plugging the DC boards with the bonding boards and then the test platform is completed. All kinds of measurements depend on various instruments. S-parameter analysis requires a network analyzer; spectrum analysis requires a signal generator and a spectrum analyzer; noise analysis requires a noise source and a noise analyzer; waveform analysis requires a signal generator and an oscilloscope.

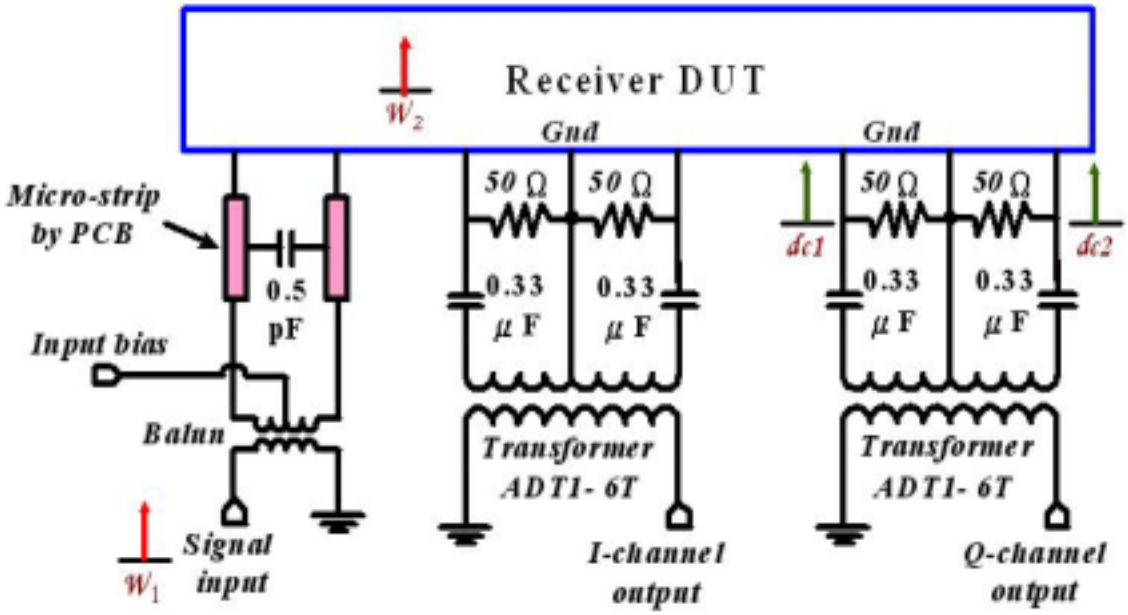


Fig. 58. (b) The measurement of DC offset voltage

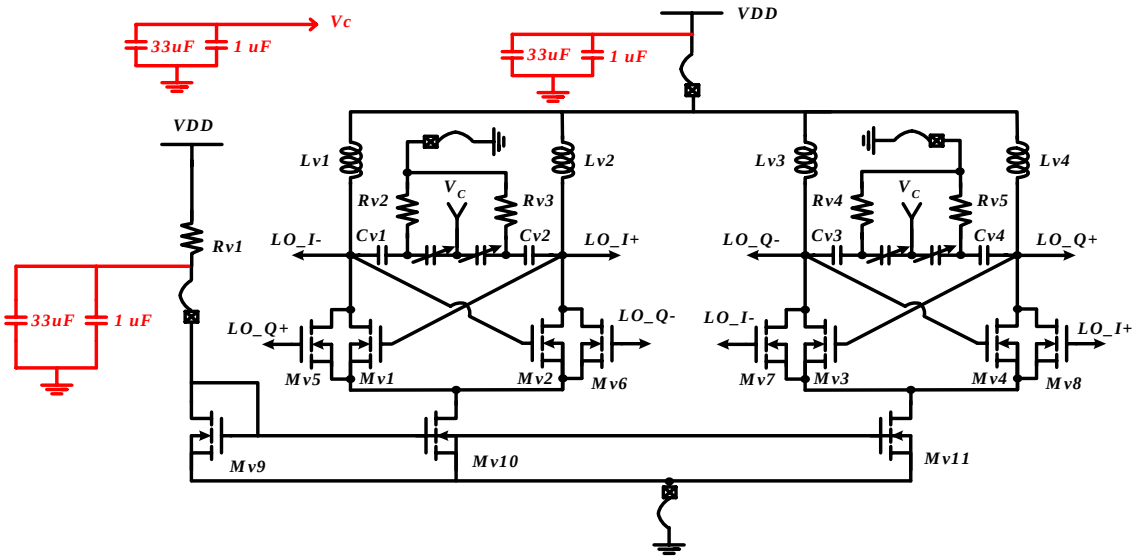


Fig. 59. Using bypass capacitors to obtain stable LO

4.3 EXPERIMENTAL RESULTS

Before measuring the receiver, the loss of passive component should be measured first. The loss of the external input matching network (balun and micro-strip line), output transformer and DC blocking capacitor (0.33 μF) are measured by the network analyzer. The loss of input matching network is about 1.94 dB among interesting band and is showed in Fig. 60. The lose of output transformer and DC blocking capacitor is about 0.15 dB among interesting band and is showed in Fig. 61. Because the instrument is paralleled with external 50-Ω, this loss is about 4.8 dB by simulation estimation. The cable loss is about 2.7 dB. Furthermore, the resistor of metal line at the output on the bonding board is about 0.057Ω ~ 0.087Ω. This loss is about 0.01 dB ~ 0.015 dB by simulation estimation but it doesn't be compensated in the measurement.

The receiver performs S11 better than –15-dB in interesting band, observable in Fig. 62, with a 0.5-pF external capacitor and 78 Ω complex characteristic impedance of the micro-strip line. It is found by several tested chips that optimum input matching could be achieved by sliding the capacitor across the micro-strip line. Bond-wire inductance is estimated to have approximately 1-nH.

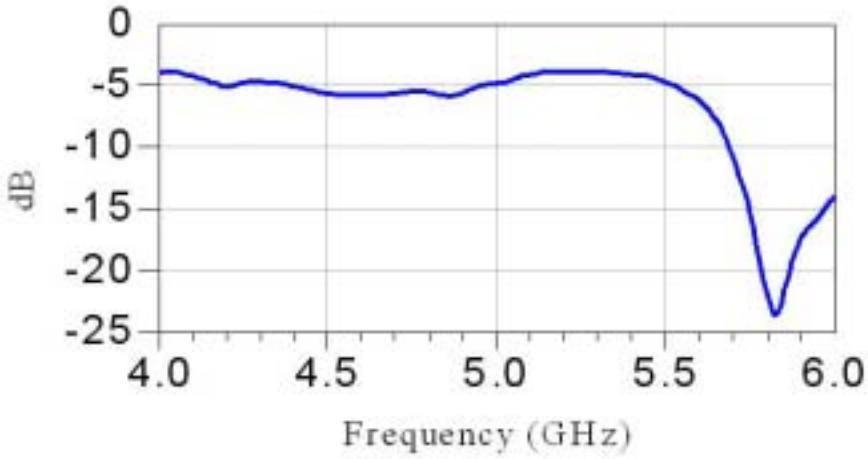


Fig. 60. Loss of balun and micro-strip line

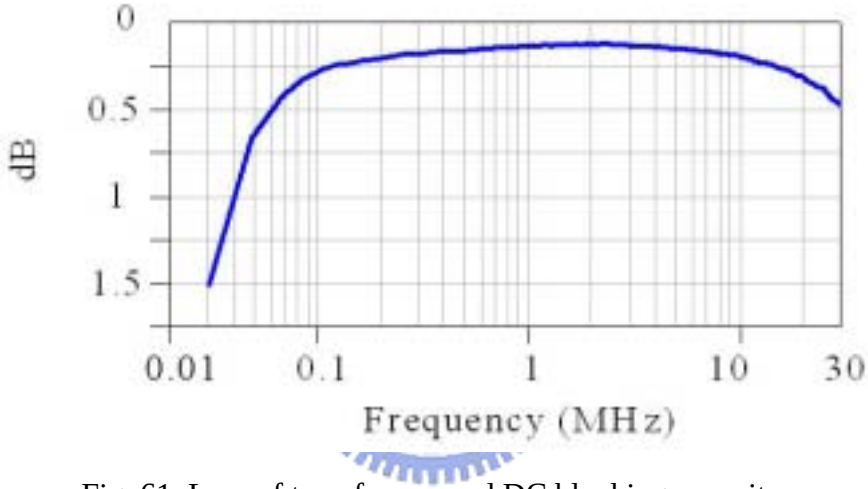


Fig. 61. Loss of transformer and DC blocking capacitor

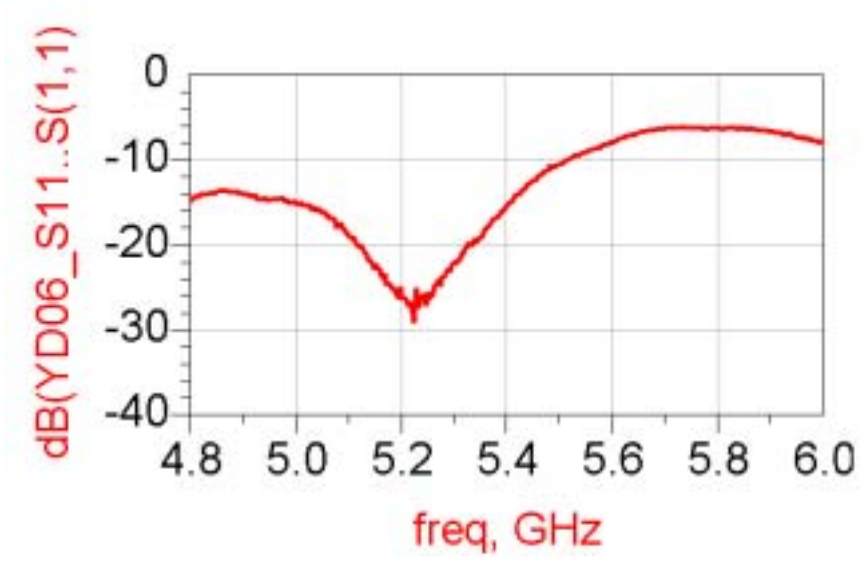


Fig. 62. Apparent S11 of the receiver

VCO tuning range can be analyzed by LO leakage observed on spectrum, as shows in Fig. 63. The leakage power level is about –56 dBm. The oscillation frequency can be tuned from 5.08 GHz to 5.3 GHz under tuning voltage of 0 ~ 1 V and the VCO gain is 220 MHz/V. Fig. 64 show the QVCO tuning-range plot.

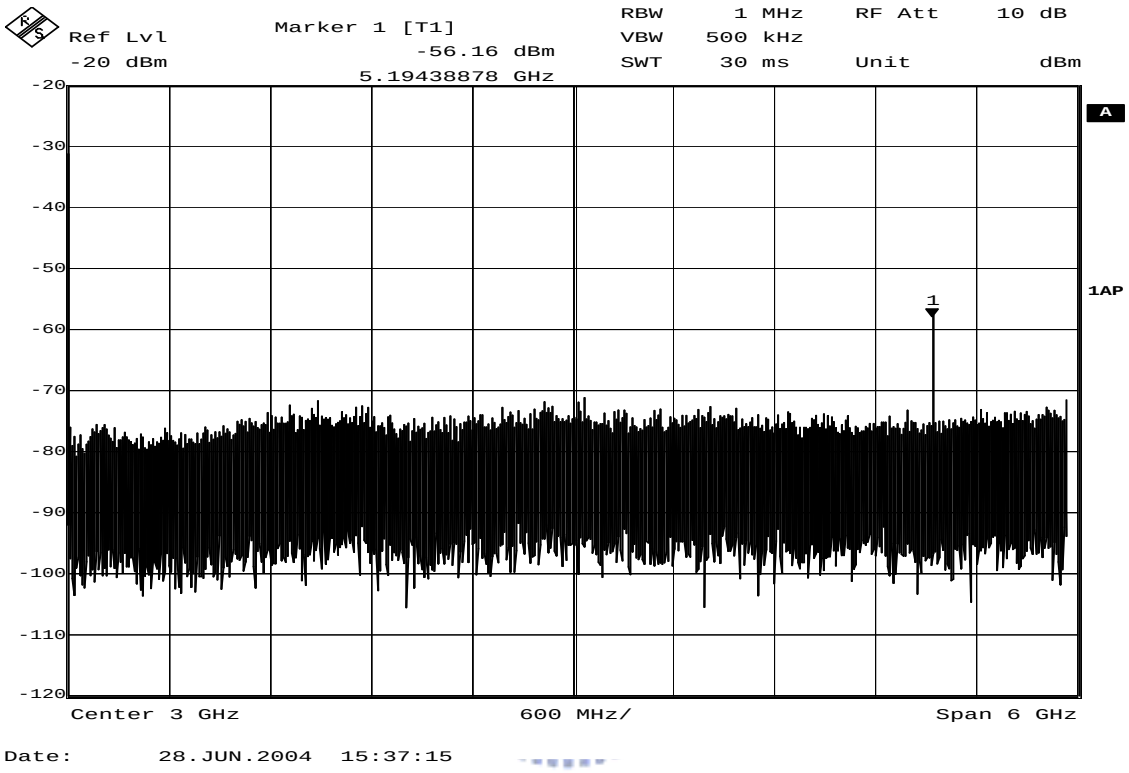


Fig. 63. Spectrum of LO leakage

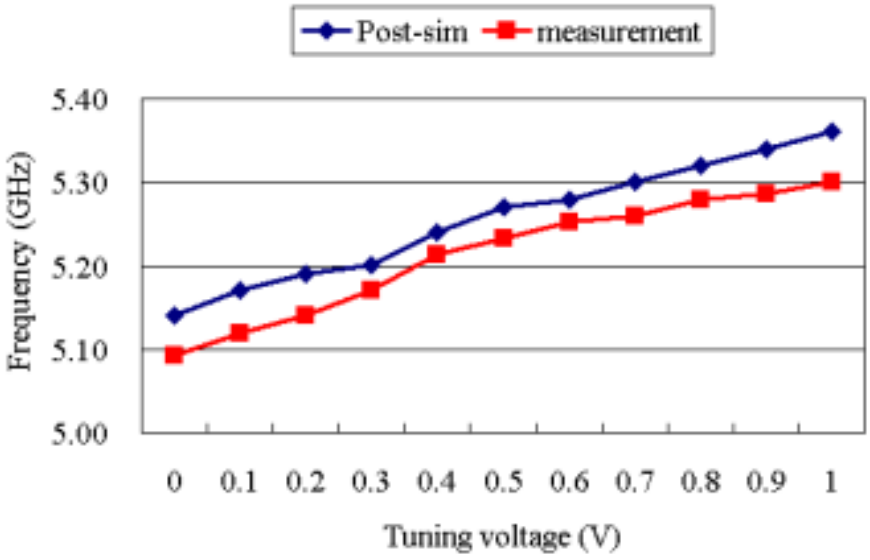


Fig. 64. QVCO tuning-range plot

Two-port network of S-parameter analysis cannot be applied for gain estimation because frequencies of input and output terminals are different. Spectrum observation is a substitutive way. The receiver works at 1.1 V in order to provide sufficiently conversion gain. Compensated back with loss of cable and external components, the receiver performs about 17.8-dB gain in band. Fig. 65 shows the IF spectrum when RF is 5.205-GHz with –60 dBm and LO is 5.2-GHz. The receiver quadrature IF output waveforms are showed in Fig. 66, the noise is due to QVCO phase noise and transformer noise. The frequency of IF is 10 MHz.

Because of the conversion gain is very low at low frequency, it is measured by increasing input power to obtain detectable signal. Fig. 67 shows the IF output waveform with 10 KHz when input power is -23 dBm and measured output power is -47 dBm. The conversion gain is about -14.6 after compensating loss (without transformer). Fig. 68 displays the measured receiver conversion gain by oscilloscope. The corner frequencies are at 150 kHz and 30 MHz respectively.

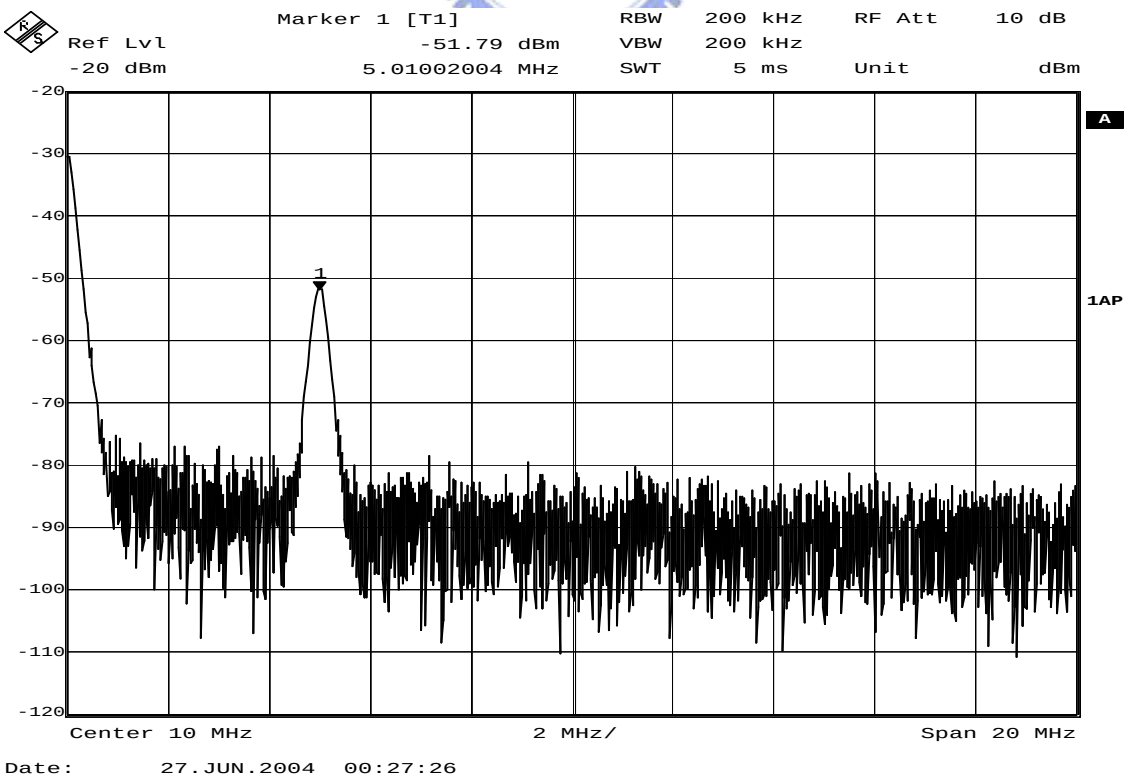


Fig. 65. The IF spectrum

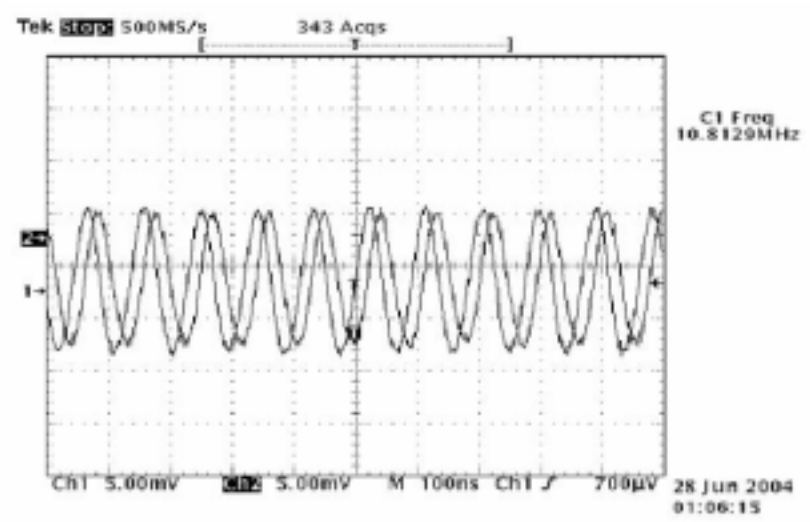


Fig. 66. Quadrature IF output waveforms of receiver

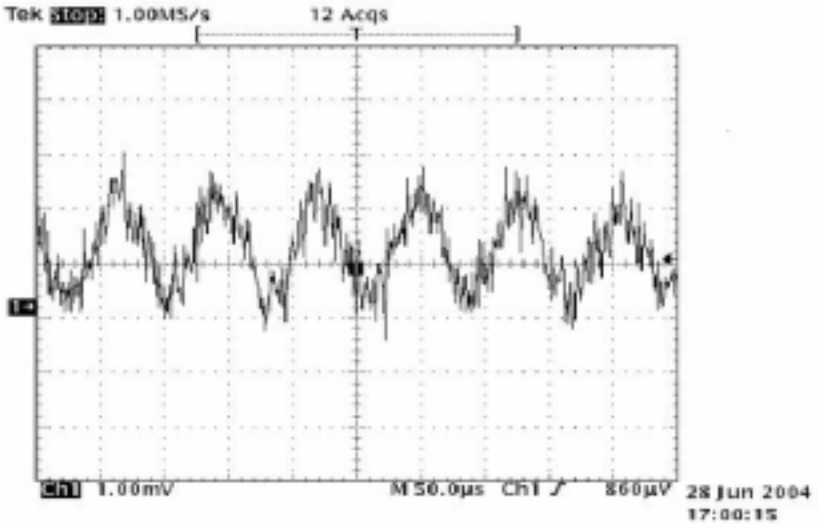


Fig. 67. IF output waveform with 10 KHz

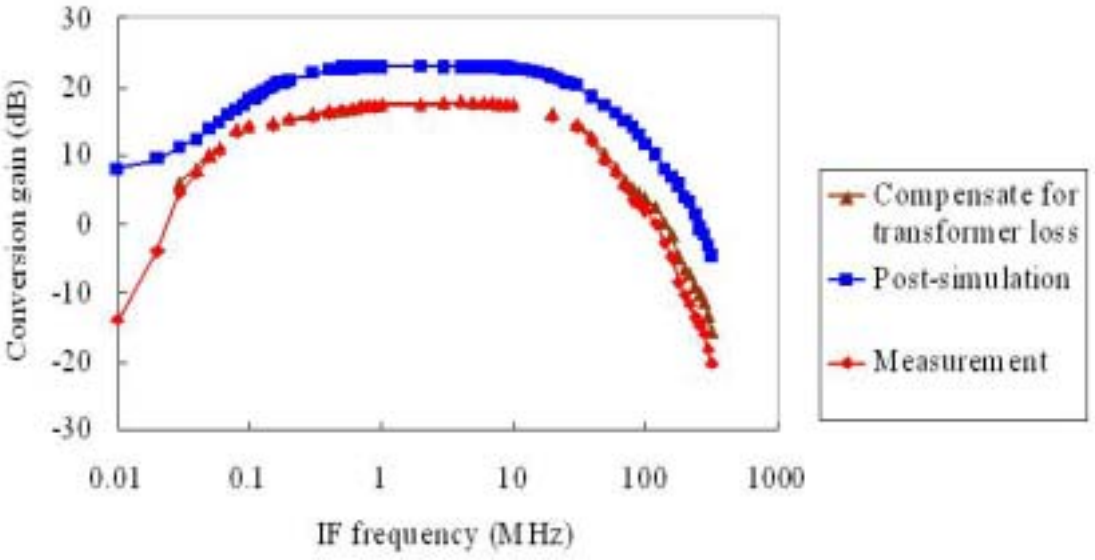


Fig. 68 Measured receiver conversion gain

Noise figure spectrum of the tested receiver is presented in Fig. 69. The noise bandwidth calculation is from 150 kHz to 10 MHz and let the input noise power is constant. The SSB noise figure is 14.9 dB after calculation. The result indicates that the receiver satisfies the specification. Fig. 70 shows the results of a two-tone third-order intercept point (IP3) measurement performed on the signal path. The 1-dB compression point is observed near –23 dBm. The IIP3 is about –14dBm.

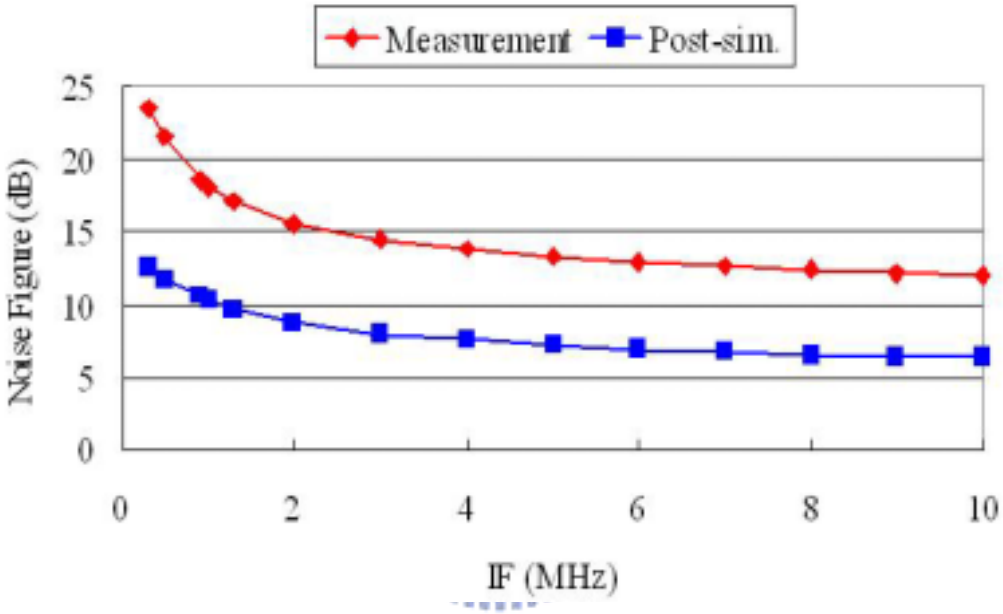


Fig. 69. Measured spectrum of noise figure

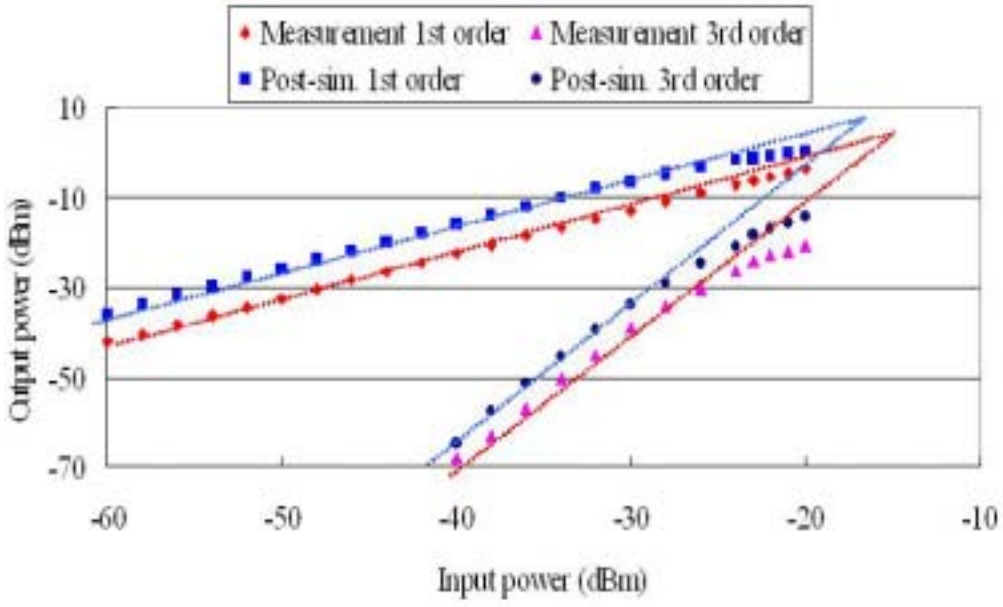


Fig. 70. Two-tone IIP3 measurement for the receiver

Fig. 71 shows measure results of the receiver DC offset voltage. The differential output is about 1 ~ 3 mV with input injected power of –50-dBm and 18.1 ~ 22.4 mV with input injected power of –30-dBm. The power consumption is about 1mW for the compensation circuit.

Values of fine-tuned gate biases and bias resistors are listed and compared with the post-simulation and measurement in Table 4-1. Due to the parasitical resistor of metal line, the QVCO require more tail current to oscillate. Base on this reason, the Rv1 is set to 1 Ω, VDD extend to 1.1 V and Vb is adjusted to 0.52 V. The other parameters are arranged deservedly. Table 4-2 lists a summary of the tested receiver, including a comparison between post-simulation and measurement. When QVCO overcome the parasitical resistor and start to oscillate, the amplitude of QVCO is smaller. According to (8), the conversion gain depends on amplitude of signal. Thus the amplitude of QVCO is small and conversion gain is small, too. The amplitude is increased by increasing QVCO power and achieves appropriate gain. The measured performance differ from the post-simulation is discussed in detail at next sub-section.

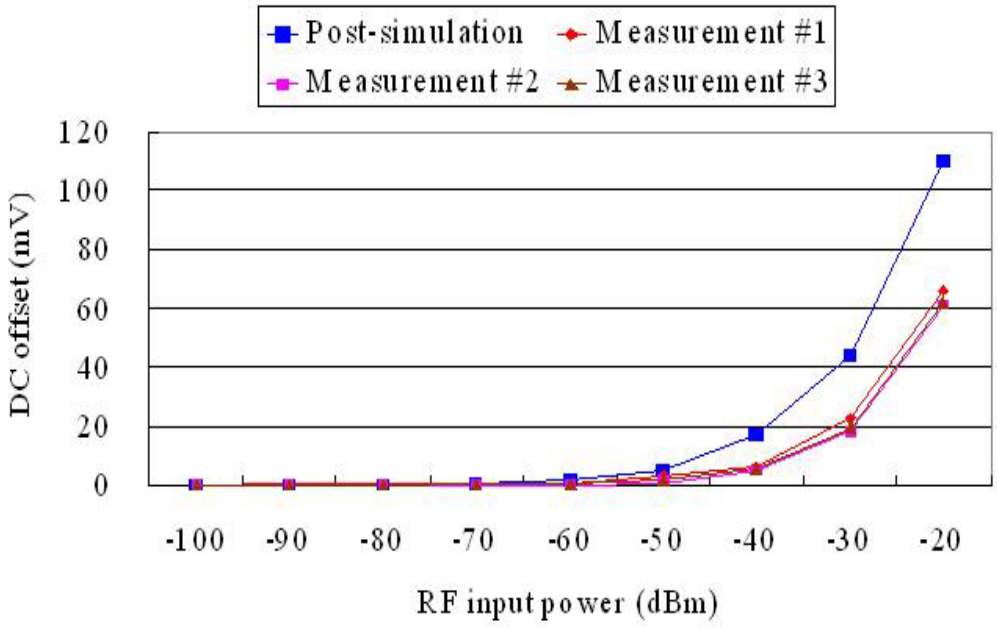


Fig. 71 Measurement of receiver DC offset voltage

Table 4-1 Comparison on gate biases and bias resistor

	Post-simulation	Measurement
VDD	1 V	1.1 V
Vg1 and Vg2	0.69 V	0.7 V
Vb	0.3 V	0.52 V
VMi1 and VMi2	0.8 V	0.54 V
VMq1 and VMq2		
Rri2 and Rrq42	800 Ω	500 Ω
Rv1	150 Ω	1 Ω

Table 4-2 Summary of the tested receiver

	Design target	Post-simulation	Adjustment on meas.: start of oscillation	Adjustment on measurement: increase VDD
Technology	TSMC 0.18- μ m 1P6M			
Frequency band	5.15 ~ 5.35 GHz			
VDD	1 V			1.1 V
S11 (< -10 dB)	5.15 ~ 5.35 GHz	5.11 ~ 5.62 GHz	4.7 ~ 5.5 GHz	4.7 ~ 5.5 GHz
QVCO power	NA	13.51 mW	17.28 mW	31 mW
Conversion gain	23 dB	23 dB	-3 dB	17.8 dB
Tuning range	5.15 ~ 5.35 GHz	5.13 ~ 5.37 GHz	5.05 ~ 5.27 GHz	5.08 ~ 5.3 GHz
P-1dB	> -26 dBm (without buffer)	-27.6 dBm	NA	-23 dBm
SSB NF	< 10 dB	7.8 dB		14.9 dB
DC offset	< 10 mV	6 mV		1 ~ 3 mV
Total power	< 25 mW	20.9 mW		37.56 mW

4.4 DISCUSSIONS AND COMPARISON

Initially, the QVCO doesn't oscillate with the post-simulation bias condition. The QVCO start to oscillate until the two paths of downconverter is turn off. It implies that another component provide positive resistor to counteract the negative resistor in the QVCO besides the two downconverters. For the receiver circuit, the metal routes contribute the parasitical resistors between each component and that won't be calculated in the Dracula post-simulator. This damages the Q value of inductor especially. Refer to the circuit layout and calculate the parasite with related metal routes at output terminals of QVCO as shown in the Fig. 72.

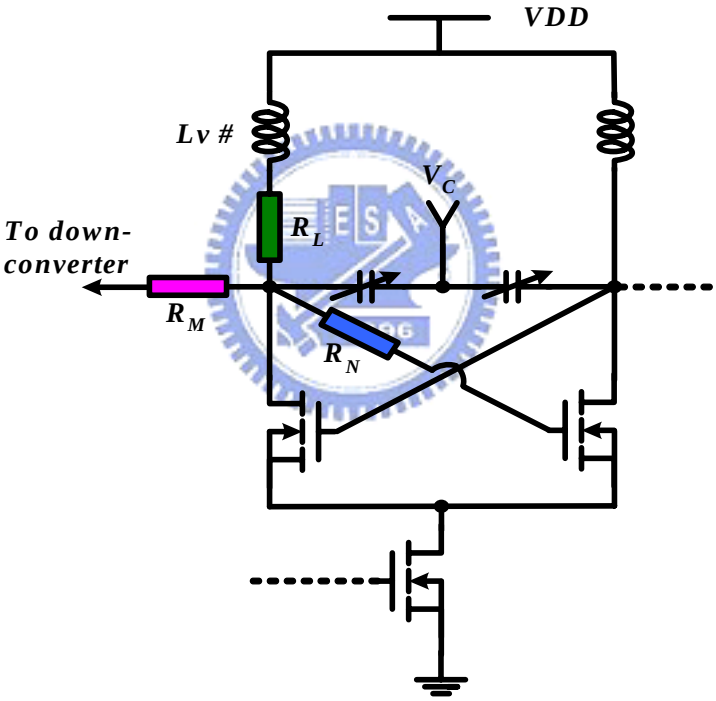


Fig. 72. Conceptual diagram of the QVCO with parasitical effect

The R_L is parasitical resistors from inductor of QVCO to the contact of the varactor. The R_M is parasite from source of downconverter to the contact of the varactor. The R_N is parasite from NMOS gate of QVCO to the contact of the varactor. Using sheet resistance from TSMC document, the related parasitical resistors values are shown in the Table 4-3. For the Q value of inductor impaired by parasite R_L, it is calculated by ADS Momentum. The equivalent inductance and Q value are shown in Fig. 73 and Fig.

74. The average equivalent inductance of I-path is about 1.52nH and Q-path is about 1.49nH. The Q value is down to 5.4 ~ 5.8 around. Those parasitical components are added into the circuit and re-simulation again. The gate biases and bias resistor are same as Table 4-1 measurement condition and the oscillation frequency can be tuned from 4.96 GHz to 5.2 GHz under tuning voltage of 0 ~ 1 V. The power strength of the QVCO is about –3.5dBm. The amounts of positive resistor provided by downconverter decrease the QVCO amplitude. Adjust the bias of downconverter, Vb, and compare the start of oscillation condition between measurement and re-simulation. The comparison is listed in Table 4-4 and the result is similar.

Table 4-3 Related parasitical resistors of QVCO

	R_L	R_M	R_N
Lv1	6.79Ω	4.11Ω	17.76Ω
Lv2	4.22Ω	1.84Ω	13.3Ω
Lv3	4.15Ω	2.57Ω	13.3Ω
Lv4	6.72Ω	4.72Ω	19.24Ω

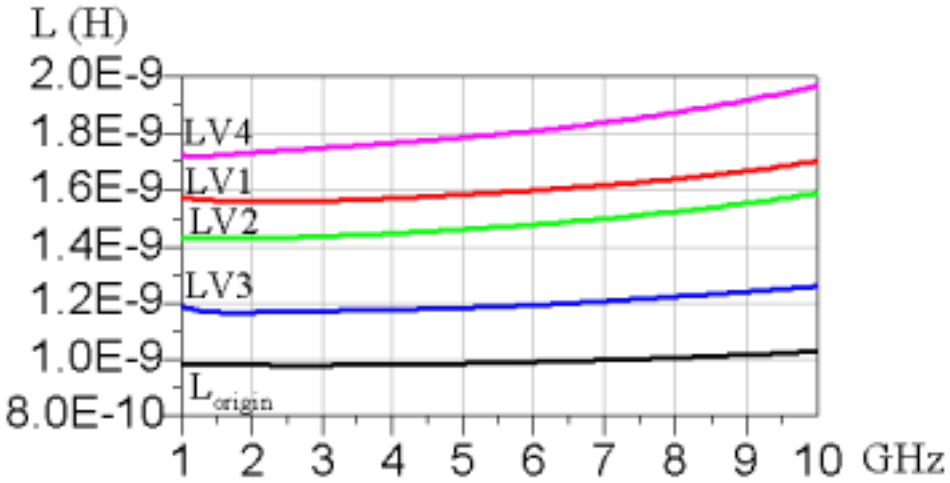


Fig. 73. Equivalent inductance in the QVCO

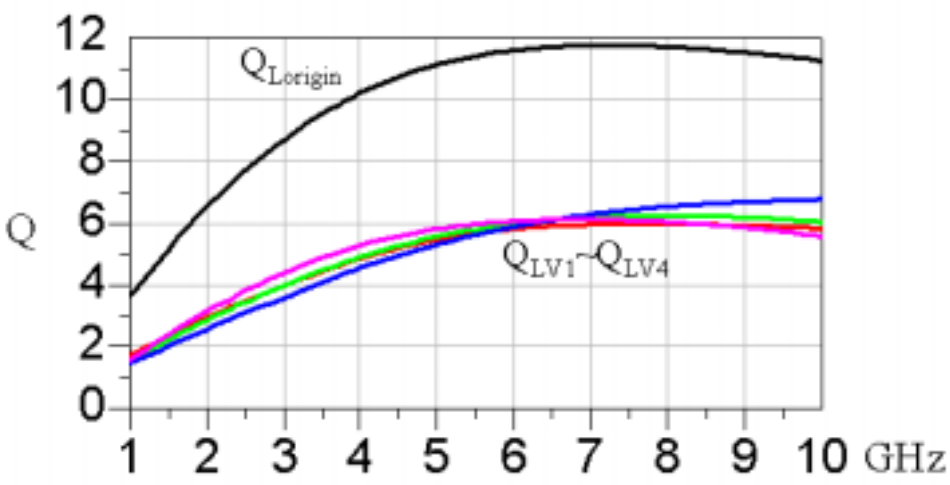


Fig. 74. Equivalent Q value in the QVCO

Table 4-4 Comparison on start of oscillation condition

	Vb	QVCO current	VDD
Measurement	0.42 V	17.28 mA	1 V
Re-simulation	0.38 V	17.48 mA	1 V

For the LNA, the analysis is identical with QVCO. Refer to the circuit layout and estimate the related metal routes of LNA as shown in the Fig. 75. The Z_{dp} and Z_{dn} are parasitical impedances from inductor to the drain of MOS. The Z_{sp} and Z_{sn} are parasite from inductor to source of MOS. Using TSMC document and simulator; the related parasitical impedances are shown in the Table 4-5. Those parasitical components are added into the circuit and re-simulation the whole circuit again. The conversion gain of receiver is 19.5 dB and shows in Fig. 76. DC offset voltage is 3 mV with input injected power of –50-dBm and shows in Fig. 77. The offset voltage decreases due to lower gain and QVCO amplitude decrease. Noise figure spectrum of the receiver is presented in Fig. 78. The SSB noise figure is 13.7 dB with re-simulation. Fig. 79 presents the relation of input to output power. The 1-dB compression point is –24 dBm. It indicates that the re-simulation result is close to the measurement.

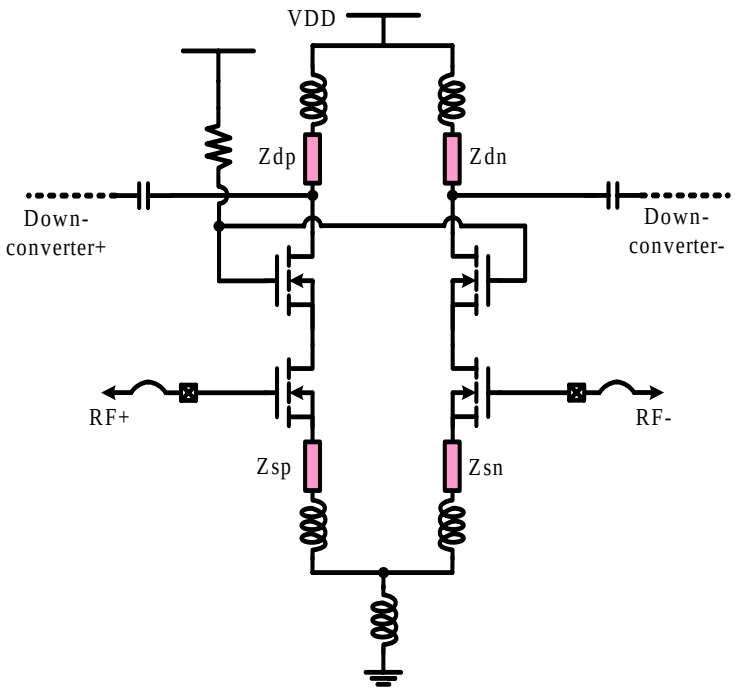


Fig. 75. Conceptual diagram of the LNA with parasitical effect

Table 4-5. The related parasitical resistors of LNA

	Z_{dp}	Z_{dn}	Z_{sp}	Z_{sn}
Resistance	2.79Ω	3.996Ω	5.64Ω	4.86Ω
Inductance	0.22 nH	0.25 nH	0.33 nH	0.31 nH

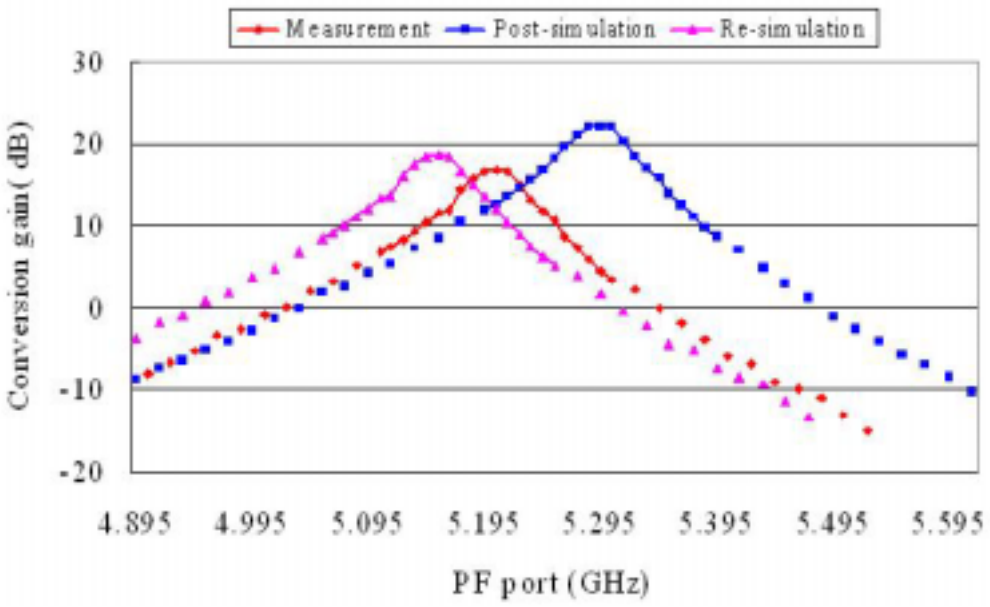


Fig. 76. Conversion gain of re-simulation

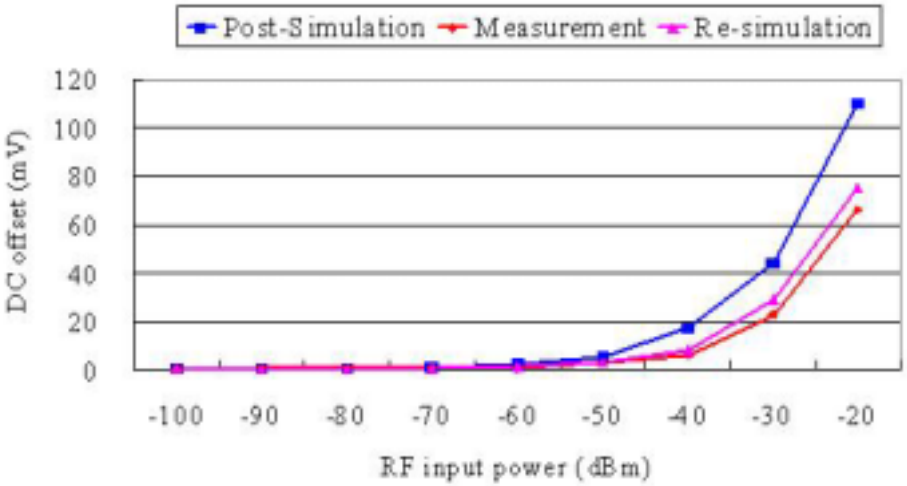


Fig. 77. DC offset voltage of re-simulation

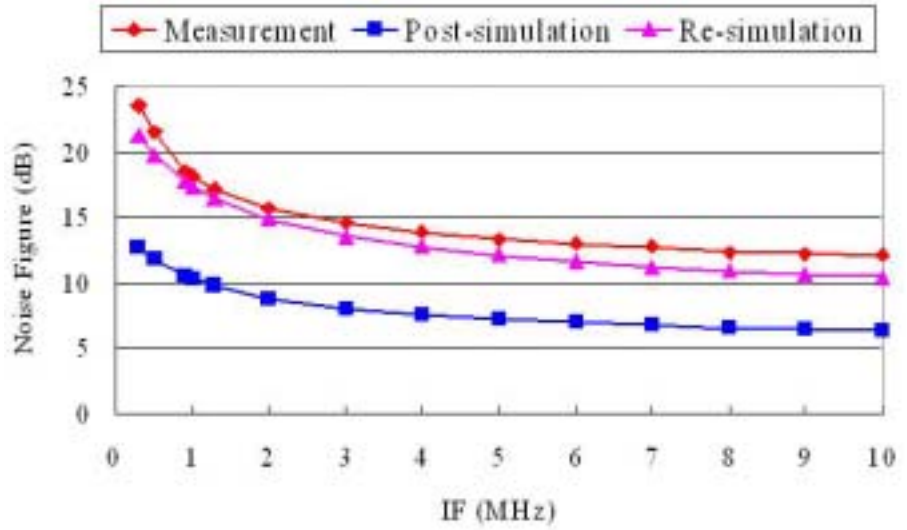


Fig. 78. Noise figure of re-simulation

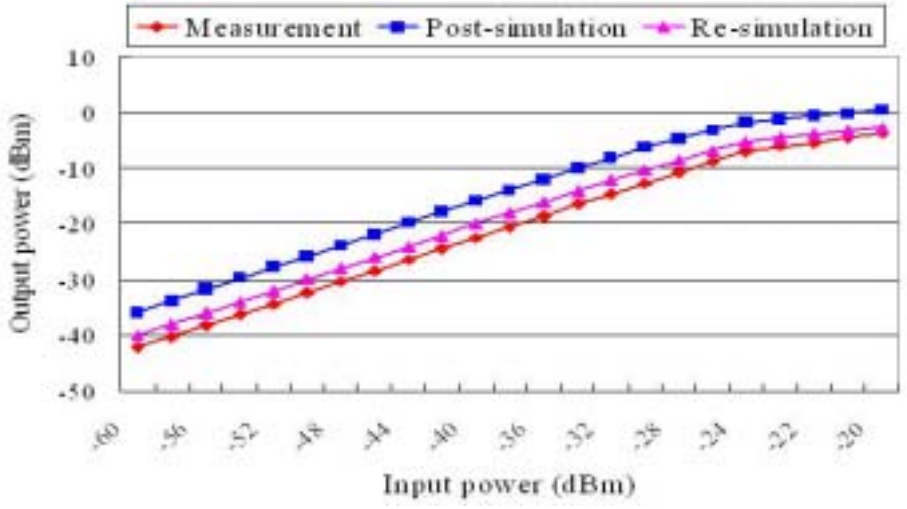


Fig. 79. 1-dB compression point of re-simulation

Further, take the parasite elements into consideration and re-design the receiver. The downconverter is the most critical stage in the receiver chain in combating noise. In order to reduce the NF of the overall system, there are used three ways to minimize it: 1. larger LNA gain, 2. adequate LO amplitude and 3. adequate downconverter sizes. The NF of downconverter can be degraded by the preceding LNA. Without oscillation, the gain of LNA is designed as large as possible. Employing large LO swings can minimize the contribution of the channel thermal noise from switching pair transistors. However, larger LO swings also consume larger power. It is important to design the optimum LO power region. Finally, in equation (9), the input-referred flicker noise is an inverse function of the downconverter size. But larger size has larger parasitical capacitance, it affect the LC tank frequency of LNA. It is a tradeoff in choosing the proper downconverter size. The re-designed circuits are simulated again with a supplied voltage of 1 V. The changed parameters in the re-designed circuit are listed in Table 4-6.

Table 4-6 Comparison on the re-design parameter

Parameter	Original value	Re-design value
Ml1 and Ml2	50 μm/0.18 μm	35 μm/0.18 μm
Ml3 and Ml4	70 μm/0.18 μm	75 μm/0.18 μm
Mmi1 ~ Mmi4 Mmq1 ~ Mmq4	45 μm/0.25 μm	60 μm/0.25 μm
Mv1 ~ Mv4	35 μm/0.18 μm	40 μm/0.25 μm
Cl1 and Cl2	0.55 pF	0.45 pF
Cv1 ~ Cv4	0.57 pF	0.53 pF

The size of Mv1 ~ Mv4 is increased to obtain large negative resistor, the QVCO could oscillate easily and obtain larger LO amplitude with lower power. The size of downconverter is increased to reduce the noise figure and the LC tank frequency of LNA is still in the interesting band. The size of LNA is re-arranged for higher voltage gain. Table 4-7 lists the performance parameter of each sub-circuit and Table 4-7 lists the post-simulation summary of the re-design receiver.

Table 4-7 Performance parameter of each sub-circuit

Sub-circuit	Performance parameter	Post-simulation	Post-simulation of re-design components
LNA	Gain	23 dB	21 dB
	NF	1.3 dB	1.8 dB
	P-1dB	-13 dBm	-11.5 dBm
	Power consumption	3.56 mW	3.4 mW
Downconverter	Gain	0 dB	2 dB
	NF	17.2 dB	16 dB
	P-1dB	-0.7 dBm	-6 dBm
	Power consumption	3.83 mW	4.83 mW
QVCO	Tuning range	5.13 ~ 5.37 GHz	5.13 ~ 5.37 GHz
	Power consumption	13.51 mW	18.47 mW

Table 4-8 Post-simulation summary of re-design receiver

	Post-simulation	Measurement	Post-simulation of re-design receiver
Technology	TSMC 0.18- μ m 1P6M		
Frequency band	5.15 ~ 5.35 GHz		
VDD	1 V	1.1 V	1 V
Tuning range	240 MHz	220 MHz	230 MHz
Conversion gain	23 dB	17.8 dB	23 dB
P-1dB	-27.6 dBm	-23 dBm	-27.5 dBm
SSB NF	7.8 dB	14.9 dB	8.7 dB
DC offset (injected –50 dBm at receiver input)	6 mV	1 ~ 3 mV	2 mV
Total power	20.9 mW	37.56 mW	26.7 mW

Table 4-9 compares the designed receiver with similar art [33] and [35]. [33] uses homodyne architecture, implement in 0.25- μ m CMOS technology and operated at 3-V. It consumes higher power dissipation to achieve low noise figure. Besides the differential circuit topology is employed to minimize the undesired coupling and LO leakage, there isn't DC offset circuit cancellation design.

The sub-circuits in [35] are identical with this thesis but it uses heterodyne architecture. That receiver performs high linearity and low noise figure. In order to get proper conversion gain and low-voltage design, it uses many inductors and occupies larger die area. Furthermore, the LNA circuit is based on a folded-cascode topology, in order to reduce the required supply voltage. The transistors are biased deeper into saturation, leading to an improved linearity. Since the mixer is to operate from a 0.8-V supply, transistors with relatively large widths are used. In order to lower the threshold

voltage, it is required to bias the transistors in saturation. But those consume more power. Moreover, the image-reject capability is another major issue and should take into consideration in circuit design.

Table 4-10 compares the receivers with DC offset removal design [17],[19],[20]. When the injected power at receiver input is –50 dBm, the injected power is about –32 dBm at downconverter input after LNA amplified. This power level is approximately similar to leakage power caused by substrate or coupling. Table 4-11 lists a performance comparison with IEEE 802.11a specification.

Table 4-9 Comparison with other 5-GHz receivers

	This work	Post-simulation of re-design	Reference [35]	Reference [33]
Architecture	Homodyne	Homodyne	Heterodyne	Homodyne
Technology	TSMC 0.18 μm 1P6M			0.25 μm 1P5M
Frequency band	5.15 ~ 5.35 GHz			
VDD	1.1 V	1 V	0.8 V	3 V
Chip area	2.09 mm^2	NA	5.44 mm^2	4 mm^2
Power consumption	37.56 mW	26.7 mW	56 mW	114 mW
S11 @ 5.2 GHz	-26 dB	-26 dB	-20 dB	-9.4 dB
Conversion gain	17.8 dB	23 dB	6 dB	18 dB
Noise figure	14.9 dB	8.7 dB	7 dB	6 dB
P-1dB	-23 dBm	-27.5 dBm	-10.3 dBm	-21 dBm
VCO tuning range	220 MHz	230 MHz	200 MHz	1600 MHz
DC offset (injected -50 dBm at receiver input)	1 ~ 3 mV	2 mV	NA	NA

Table 4-10 Comparison on DC offset removal design

	This work	Ref. [17]	Ref. [19]	Ref. [20]
Technology	0.18 μ m	0.6 μ m	0.25 μ m	0.25 μ m
Frequency band	5 GHz	2.4 GHz	2.4 GHz	5 GHz
Supply voltage	1.1 V	3 V	2.7 V	2.5 V
DC offset	1 ~ 3 mV	7 mV	< 20 mV	25 mV
Lower cutoff frequency	150 KHz	70 KHz	10 KHz	1.5 KHz
Input power level (LO leakage)	-50 dBm	-47 dBm	NA	-57 dBm

Table 4-11 Performance comparisons with IEEE 802.11a specification

	Post-simulation	Measurement	Post-simulation of re-design	Requirement
Frequency band	5.13 ~ 5.37 GHz	5.08 ~ 5.3 GHz	5.13 ~ 5.36 GHz	5.15 ~ 5.35 GHz
SSB NF	7.8 dB	14.9 dB	8.7 dB	< 15 dB
P-1dB	-23.8 dBm (Without buffer)	-23 dBm	-23.6 dBm (Without buffer)	> -26 dBm
Channel bandwidth	20 MHz	20 MHz	20 MHz	20 MHz

Due to the QVCO output signal is connected directly to downconverter; the output load of QVCO depend strongly on the layout route and nest stage. It augments the complex on design. A modified design to decouple the current in QVCO and downconverter is a spontaneously way. Using a current source between QVCO and

downconverter and re-simulate again. It reduces power consumption on QVCO. Fig. 80 presents the conceptual diagram. The VCO buffer or I/V converter could realize the current source. Although the power consumption is reduced, the noise figure is still too large. In order to reduce the noise figure, the re-design parameter of LNA and downconverter in the Table 4-6 is used and post-simulation again. The power of QVCO is increased to obtain larger amplitude. The post-simulation summary of modified design is listed in Table 4-12.

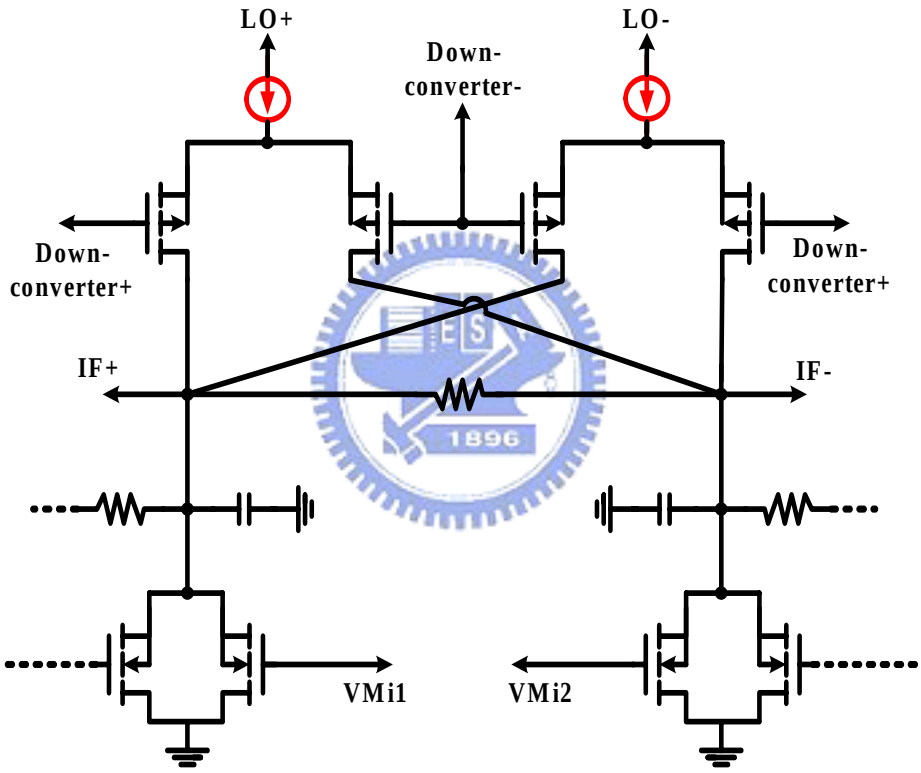


Fig. 80. Conceptual diagram of decouple the current in QVCO and downconverter

Table 4-12 Post-simulation summary of modified design

	Post-simulation	Measurement	Post-simulation of modified design: use current source*	Post-simulation of modified design: with parameters in table 4-6 **
Technology	TSMC 0.18- μ m 1P6M			
Frequency band	5.15 ~ 5.35 GHz			
VDD	1 V	1.1 V	1 V	1 V
VCO power	13.51 mW	31 mW	13.745 mW	15.42 mW
Tuning range	240 MHz	220 MHz	240 MHz	240 MHz
Conversion gain	23 dB	17.8 dB	19.5 dB	23 dB
P-1dB	-27.6 dBm	-23 dBm	-24 dBm	-27.4 dBm
SSB NF	7.8 dB	14.9 dB	13.7 dB	8.05 dB
DC offset (injected –50 dBm at receiver input)	6 mV	1 ~ 3 mV	3 mV	2 mV
Total power	20.9 mW	37.56 mW	21.135 mW	23.65 mW

* The size of receiver is unchanged. It is an observation on power reduction by adding the current source.

** Although the power can be reduced by adding the current source, but NF is still large. Using the parameters in the table 4-6 (but Mv1 ~ Mv4 and Cv1 ~ Cv4 use original value), the NF is reduced.

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 CONCLUSIONS

A 1-V 5-GHz direct-conversion front-end receiver with integrated LNA, quadrature VCO and downconverter for low-power and wireless application is designed, fabricated and tested in a 0.18-μm CMOS technology. A new DC offset voltage compensation circuit with band-pass filter has been proposed, and the DC offset voltage is 1 ~ 3 mV with input injected power of –50-dBm. The architecture of new compensation circuit is simple and is suited for low-power design, and the compensation circuit consumes only 1mW. In addition to be designed with common-source-cascode configuration that performs the best performance currently, the LNA is specially equipped with a LC-tank as common-mode source degenerator. The tank causing almost no DC drop helps the LNA to preserve acceptable linearity. There are 9 inductors in the receiver, but the chip occupies small area, 2.09mm^2, even including the quadrature buffer. The low-voltage direct-conversion front-end receiver is tested under 1 and 1.1 V supply. 14.9-dB noise figure, –23-dBm 1-dB compression point are adequate for IEEE 802.11a applications. With the low-voltage design, the power consumption of receiver is 37.56mW lower than the identical technology [35].

The parasite in the metal line route is a critical parameter in the analogy circuit design. It will destroy design productivity. Sine wires have never been completely free at the board or system-level, future chip design will be very similar to board-level design, instead of dealing with chips on a board. For the measurement would close to

simulation as possible, the parasite, especially for resistor and inductor, should take into consideration during post-simulation.

5.2 FUTURE WORKS

The re-design circuit could be fabricated again to verify the function. For more practicability, the automatic gain control (AGC), channel selection low-pass filter (LPF) and analog-to-digital converter (ADC) are included to measure the received packet error rate (PER), which indicates linearity, noise and DC offset of integer performance.

To avoid the QVCO amplitude decreasing problem, decoupling the current in the QVCO and downconverter is spontaneously. The VCO buffer or I/V converter would accomplish the decoupling circuit. The frequency shift and parasite of metal is needed to consider at next design. Finally, a frequency synthesizer can include to obtain a stable local frequency.

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