國 立 交 通 大 學

電機資訊學院 電子與光電學程

碩 士 論 文

超寬頻無線網路應用之
低功率互補金氧半射頻前端接收器設計

Low Power CMOS RF Receiver Front-End Design for
Ultra-wideband Wireless Applications

研 究 生：吳昌慶　　Chang-Ching Wu

指導教授：溫瓌岸　博士　　Dr. Kuei-Ann Wen

中 華 民 國 九 十 四 年 一 月

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低功率互補金氧半射頻前端接收器設計

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國立交通大學電機資訊學院 電子與光電學程（研究所）碩士班

摘　要

本論文針對超寬頻(UWB)無線網路應用提出低功率互補式金氧半(CMOS)射頻前端接收器之設計。本文提出之低雜訊放大器(LNA)採用兩級堆疊交錯調整之共射級放大器架構，其中兩級分別諧振於不同頻率，以達成低功耗和超寬頻之設計目標。經由 0.18-μm CMOS 製程進行電路實作，量測出 2.4G-9.4GHz 的超大頻寬與 7.3mW 的極低功耗，同時具有 9.7dB 的最大功率增益、4.17dB 的最低雜訊值和-3.5dBm 的第三階互調線性度，驗證此兩級堆疊交錯調整之低雜訊放大器電路架構之優點。將此優異低雜訊放大器架構應用於超寬頻射頻前端接收器，加上被動式混波器，以符合低功耗與低閃爍雜訊之要求，並且增加一組偏壓接地之低雜訊基頻放大器，以補償被動式混波器之增益損失，進而有助於提升整體射頻接收器之雜訊績效。此超寬頻射頻前端接收器參考多頻帶正交頻率多重分割技術規格草案的第一頻帶組需求，運作頻帶從 3GHz 到 5GHz，並以射頻/基頻共同模擬來驗證其低雜訊，高增益以及良好線性度之特性。

Low Power CMOS RF Receiver Front-End Design for Ultra-wideband Wireless Applications

Student：Chang-Ching Wu　　Advisors：Dr. Kuei-Ann Wen

Degree Program of Electrical Engineering Computer Science

National Chiao Tung University

ABSTRACT

This thesis presents a low-power design of a direct conversion CMOS RF receiver front-end for ultra-wideband (UWB) wireless applications. To achieve low power consumption and wide operating bandwidth, the proposed LNA employing stagger tuning technique consists of two stacked common-source stages with different resonance frequencies. A circuit implementation in 0.18-μm CMOS process shows a 2.4-9.4-GHz bandwidth. The amplifier provides a maximum forward gain (S21) of 9.7 dB while drawing 7.3 mW from a 1.8-V supply. A noise figure as low as 4.17 dB and an IIP3 of –3.5 dBm have been measured. In this thesis, design optimization for the power-constrained stacked amplifiers in wide bandwidth applications is also presented. The novel topology of low power UWB LNA is applied to the RF front-end design for the UWB direct conversion receiver. In the RF front-end, a wideband passive mixer is designed for the purpose of low power, little flicker noise and high linearity

after the LNA. A baseband amplifier biased at ground level is designed with consideration of low noise for compensating the gain loss of the passive mixer and consequently help improving overall noise performance of the receiver. The UWB receiver front-end referenced to the band group #1 of the Multi-Band OFDM with operation frequency range 3-5 GHz demonstrates low noise figure, low power, high gain, and wide bandwidth. It is also verified by a RF/Baseband co-simulation.

致謝

這本論文能在短期內完成又不失內容的豐富性，應該要感謝家人、師長、和實驗室的伙伴們。

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讓我鼓起勇氣重返校園的人是妻子翠梅，若非她的全力支持和承擔家務，我無法專注於許多夜以繼日的研究生活並順利取得學位。母親和岳母不辭辛勞的遠道而來，輪流幫忙照顧可愛的幼子柏均，使我有充分的時間用於學業。在此，謹以感謝的心，將本論文獻給我親愛的家人。

吳昌慶

2005 年 1 月

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Recently, the Federal Communications Commission (FCC) in US approved the use of ultra-wideband (UWB) technology for commercial applications in the 3.1-10.6 GHz [1]. UWB performs excellently for short-range high-speed uses, such as automotive collision-detection systems, through-wall imaging systems, and high-speed indoor networking, and plays an increasingly important role in wireless local area network (WLAN) applications. This technology will be potentially a necessity in our daily life, from wireless USB to wireless connection between DVD player and TV, and the expectable huge market attracts various industries. The IEEE 802.15.3a task group (TG3a) is currently developing a UWB standard from the proposals submitted by different companies. It is now left with two primary proposals, Multi-Band OFDM and Direct Sequence UWB. The newly unlicensed UWB opens doors to wireless high-speed communications and has been exciting tremendous academic research interest.

1.1 Motivation

The IEEE802.15.3a task group set targets of low power consumption and low cost. The complementary metal-oxide semiconductor (CMOS) technology is the best candidate to make

it since the physical layer implemented in CMOS process consumes less power than others and can be easily integrated with existing MAC layer implemented in CMOS technology and consequently lowers cost much [2]. The research goal of this thesis is to implement a low-power receiver front-end in the low-cost CMOS technology for wireless UWB applications. As a consequence, a low noise amplifier of ultra-wide bandwidth and succeeding mixers are required to cover all the frequency of interest, and the low-power consumption is one of the key points.

1.2 Organization

The organization of this thesis is overviewed as follows. Chapter 2 gives some basic concept in RF receiver design. Chapter 3 deals with ultra-wideband low noise amplifier (UWB LNA) design. A novel topology with low power feature is proposed. Chapter 4 demonstrates the application of the proposed LNA in the UWB system with verification by RF/Baseband co-simulation. The low power UWB LNA is implemented in 0.18μm CMOS technology and performs excellent in measurement results in Chapter 5. The LNA is further modified and integrated with down-conversion mixers to constitute a UWB receiver front-end to specifically fit the requirements of Band Group #1 of the MB-OFDM proposal in Chapter 6. Chapter 7 concludes with a summary of contributions and suggestions for future work.

Chapter 2

Basic Concepts in RF Receiver Design

This chapter presents some basic concepts in RF Receiver which are fundamental of the following chapters. Beginning with introduction to noise, section 2.1 describes noise sources in MOSFET. In section 2.2, linearity issues are discussed, including intermodulation and compression point. Section 2.3 gives a general introduction to low noise amplifiers.

2.1 Noise in MOSFET

The sensitivity of a receiver system is limited by noise. Well-understanding of noise source in RF circuits is important in component design and system architecture plan. The noise sources of interest about CMOS RF circuit design include thermal noise and flicker noise. A simplified noise model is built as in Figure 1 [3], and

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f + \frac{K_1}{f}\Delta f \tag{2-1}$$

$$\overline{v_{ng}^2} = 4kT\gamma r_g \Delta f\ ,\quad r_g = \frac{1}{5g_{d0}}. \tag{2-2}$$

where g_{d0} is the drain-source conductance at zero V_{DS}. The parameter γ is one at zero V_{DS}, and, in long channel device, decreases toward 2/3 in saturation. In deep-submicron CMOS process, γ increases by a large factor. Equation (2-1) represents the drain noise where the first term at right side is the thermal drain noise and the second is the flicker noise which is

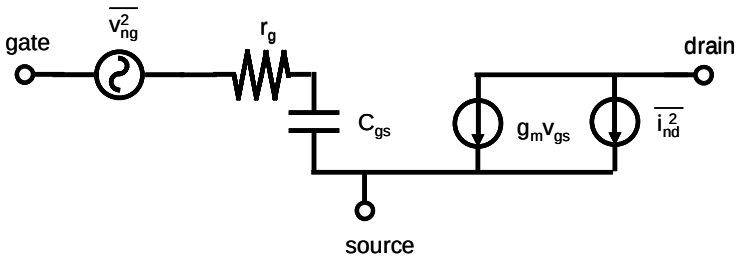


Figure 1. MOS noise model.

frequency-dependent. Equation (2-2) shows the thermal gate noise in the form of voltage source that is frequency-independent. The two thermal noise sources are correlated with a correlation coefficient defined as

$$c \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} . \qquad (2\text{-}3)$$

2.2 Nonlinearity

Small-signal gain is normally used to evaluate RF circuits. However, nonlinearity of circuits may cause signal distortion when power level increases or strong interferers are adjacent to the input signals. Gain compression and intermodulation are important indices of nonlinearity for the design in the RF circuits and systems. 1-dB compression point is often used to represent the gain compression feature. As illustrated in Figure 2, when the input power increases to some level, the nonlinearity of the circuit cause apparent slow-down of output power growth. When the actual output power level is 1dB below the linear value, the 1-dB compression point is herein defined.

On the other hand, signals affected by intermodulation of the strong adjacent interferers in circuits or systems are characterized by the parameters of n^{th}-order interception point (IPn). Third-other interception point (IP3) is often used in the performance evaluation as illustrated in Figure 3. In a two-tone test, as the fundamental term of the output signal increases, the

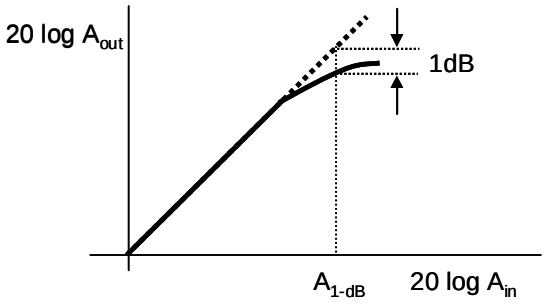


Figure 2. Definition of 1-dB compression point.

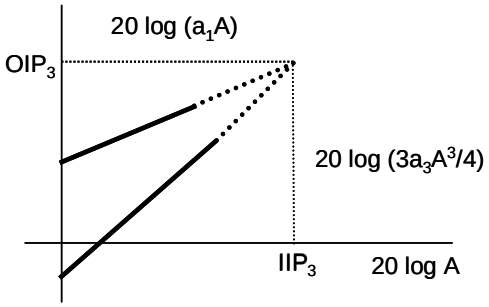


Figure 3. Definition of IP3.

third-order term caused by intermodulation appears and gradually impacts the fundamental. The extrapolation of the two curves defines the IIP3.

By comparing the equations of 1dB compression point and IIP3, the relationship between the two nonlinearity representations can be found as [4]

$$\frac{A_{1-dB}}{A_{IP3}} \approx -9.6dB. \tag{2-4}$$

2.3 Low Noise Amplifier General

The low noise amplifier (LNA) is the first module in the receiving path of a transceiver, which affects the performance of signal bandwidth, noise figure, and power dissipation of the entire system. A LNA of ultra-wide bandwidth is required to cover all the frequency of interest in the UWB applications so that the chip size can be compacter and the cost much

more reduced. Besides, a LNA for UWB is expected to consume as little power as possible that enable mobility of hand-held devices with UWB without the load of heavy battery.

2.3.1 Basic Concerns

In designing a LNA, noise optimization and input impedance match are usually more discussed. Inductive source degeneration is widely employed for input match in the narrow-band design of common-source amplifier [3]. It provides a real term $\omega_T L$ for the input impedance while generating little noise and consuming tiny voltage headroom. It is also found in the broadband design with narrow-band approach [5].

In LNA circuits, noise sources close to the input contribute more weight since they are amplified by the circuits and then appear at the output. That is why the input network and the input devices are the main targets in noise reduction. Resisters are not good for input matching in LNA designs because they produce lots of thermal noise. While on-chip spiral inductors are widely used for impedance matching, they do generate thermal noise due to low quality factor; i.e. noticeable parasitic resistance.

The power-constrained noise optimization was discussed in narrow-band LNA design [3]. It calculates the optimum device size that minimizes noise while keeping reasonable power consumption and good power matching. The method was extended to the broadband LNA design and in-band average noise figure was optimized [5].

2.3.2 Recent Research Reviews on Broadband LNA

Several CMOS LNA design techniques had been reported for broadband communication applications. The well-developed distributed amplifier is known as its wide bandwidth. However, as shown in Figure 4, it requires several area consuming inductors to perform signal

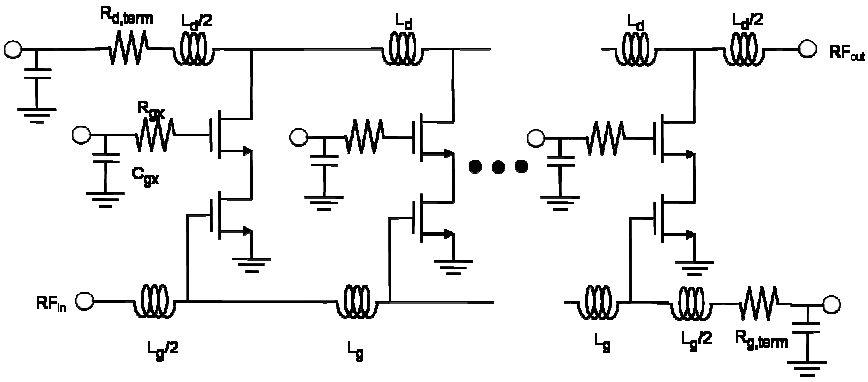


Figure 4. Distributed amplifier.

delay and many stages to provide a given gain that consumes much power [6].

A feed-forward noise-canceling technique was proposed to minimize noise figure at the price of power dissipation as well. In addition, its -3dB bandwidth is limited by device dimensions and difficult to achieve the frequency band requirement of UWB applications [7].

To get flat gain performance over wide bandwidth, serial resistor is used to improve the gain at low frequency as shown in Figure 5 [5]. The inductive source degeneration is used together with a three-section Chebyshev filter to provide broadband input match. A capacitor is added in parallel with the gate-drain parasitic capacitance to help design flexibility. The cascade configuration is employed to improve reverse isolation and mitigate the Miller effect. The noise optimization used in narrow-band design is employed and in-band average noise figure is optimized. The design begins with narrow-band-like topology and results in good broadband performance. However, the additional resistor exhibits some drawbacks. It apparently dissipates extra power which would be an issue in the low power design. Besides, it may suffer from process variation.

For the UWB technology to be widely employed in the hand-held wireless applications, it cannot be avoided that power consumption is one of the main issues. How to achieve wide bandwidth, low noise and enough power gain while keeping low power dissipation will be discussed in the next chapter where a low power UWB LNA topology is presented.

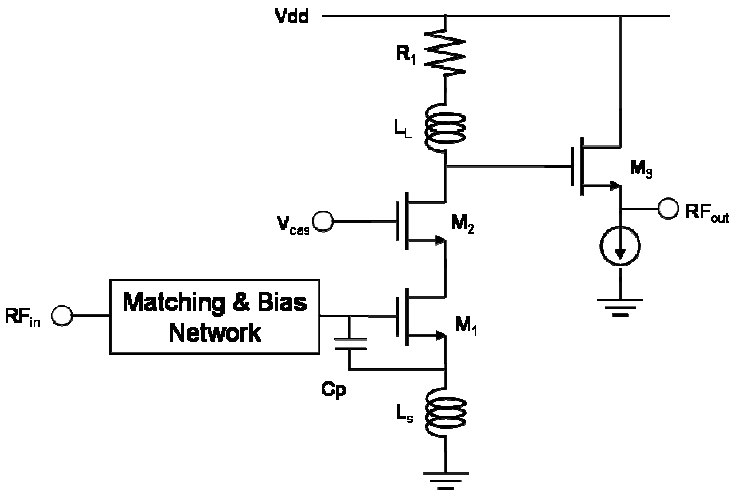


Figure 5. UWB LNA with serial resistor.

Chapter 3

Low-Power Low Noise Amplifier Design

This chapter presents a CMOS low noise amplifier (LNA) for low-power ultra-wideband wireless applications. Section 3.1 addresses design concepts of wideband approaches and low power means. The proposed LNA employing stagger tuning technique consists of two stacked common-source stages with different resonance frequencies and is described in section 3.2. A circuit design in 0.18-μm CMOS process is shown in section 3.3. The simulation results demonstrate ultra-wide bandwidth, low noise and satisfying power gain while drawing much low power in section 3.4.

3.1 Design Concept

The goal of this work is to cover the 3-8 GHz frequency range for the band groups #1 ~ #3 of MB-OFDM proposal. The initial idea was to use two LNAs in parallel that each covers half of the total frequency range. However, it resulted in higher noise figure around the middle frequency band and, more importantly, high power consumption. Thus, one LNA should be designed to achieve the goal and avoid the issues.

It is a challenge to design an ultra-wideband LNA in 0.18um CMOS technology where the Fmax is only around 35 GHz. While the distributed amplifiers are popular in extremely extending the bandwidth, the power dissipation comes to be an issue. In addition, the input

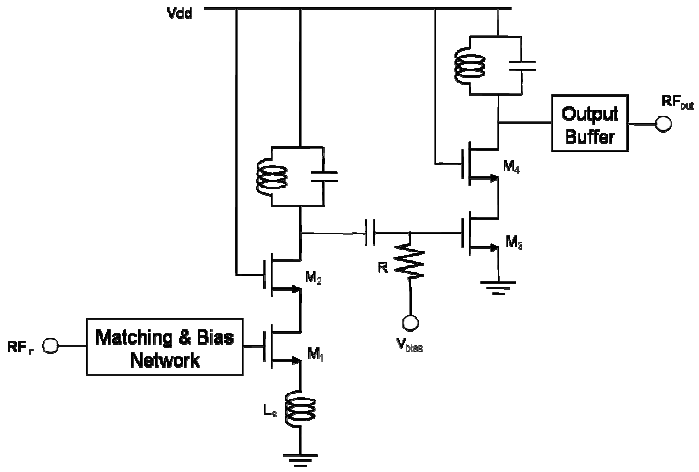


Figure 6. Two-stage LNA with stagger tuning technique.

matching network for a wide bandwidth exhibits difficulties, especially with on-chip components which are necessary for compact and highly integrated system-on-chip designs. Some technologies for achieving wide bandwidth and low power consumption, respectively, are discussed below. Afterwards, a novel topology combing the two features is proposed.

3.1.1 Wide Bandwidth

Two-stage LNA with stagger tuning technique was reported to have good gain flatness within a frequency range, which is defined by the resonance frequency of each amplification stage as shown in Figure 6 [8].

The theorem of the stagger-tuned amplifiers can be found in the fundamental microelectronics textbook [9]. The maximum flatness around a center frequency ω_0 can be achieved by transforming the response of a Butterworth low-pass filter up the frequency axis to ω_0. As illustrated in Figure 7, a fourth-order bandpass filer can be stagger-tuned maximally flat with its two tuned circuits which have specifications as follows [9],

$$\omega_{01}, \omega_{02} = \omega_0 \pm \frac{B}{2\sqrt{2}}, \qquad B_1, B_2 = \frac{B}{\sqrt{2}}, \qquad Q_1, Q_2 = \frac{\sqrt{2}\omega_0}{B}, \tag{3-1}$$

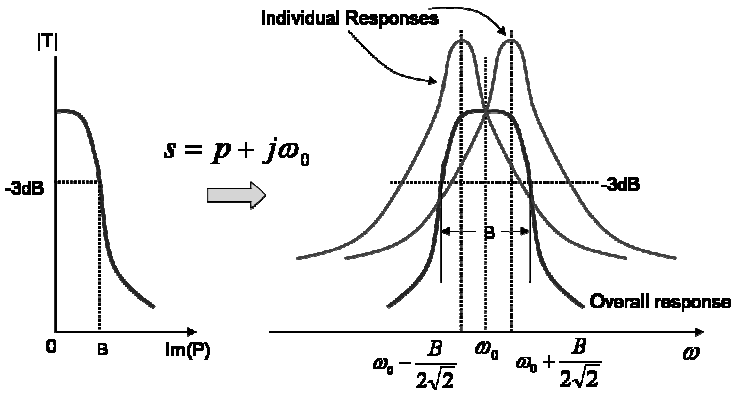


Figure 7. Low-pass to bandpass transformation for stagger tuning.

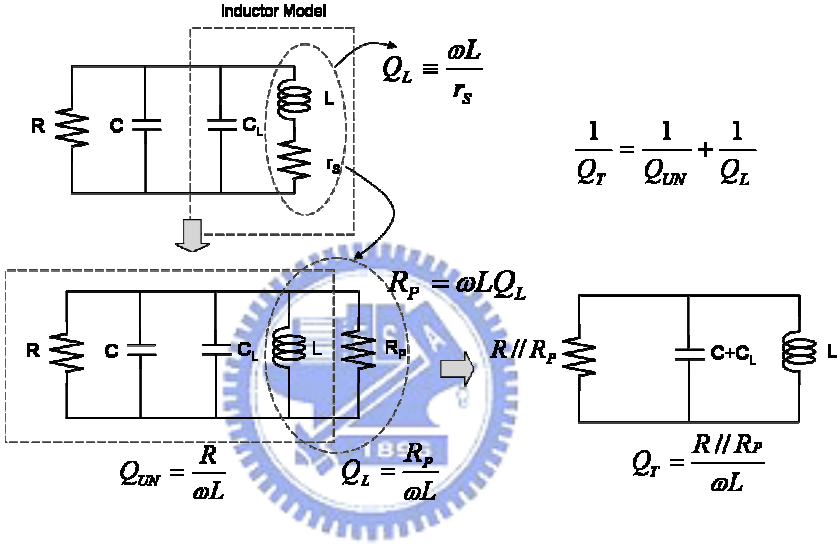


Figure 8. Relationship between Q factors.

where B is the 3-dB bandwidth and Q is the quality factor. For narrow-band designs, high Q is preferred since the bandwidth is small. However, in the UWB applications, where the system Q is less than one, it seems difficult to employ relatively high Q on-chip inductors for obtaining low Q circuits. Some adjustments and compensation may be required.

As illustrated in Figure 8, with definition of $Q_L \equiv \frac{\omega L}{r_S}$ for an inductor, the parasitic resistance r_s can be transformed to the equivalent parallel resistance $R_P = \omega L Q_L$. When the inductor is employed in a tank, the total tank Q is $Q_T = \frac{R // R_P}{\omega L}$, where R is the native resistance of the tank. It would be easier to understand the relationship between the inductor

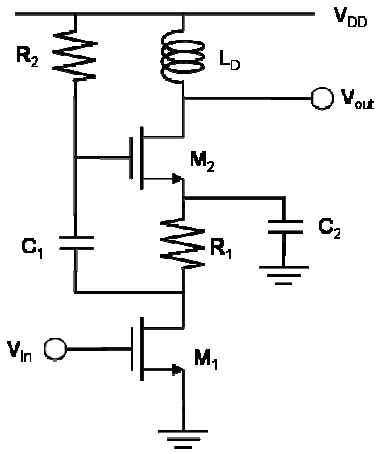


Figure 9. Current reuse topology.

Q and the total tank Q if we express Q_T in the following equation,

$$\frac{1}{Q_T} = \frac{1}{Q_{UN}} + \frac{1}{Q_L}, \tag{3-2}$$

where $Q_{UN} = \frac{R}{\omega L}$ and can be considered as the unloaded Q of the tank, and $Q_L = \frac{R_P}{\omega L}$ as the external Q. From the above equation, it is clear that a relatively high Q inductor can be applied to a low Q circuit. Equation (3-2) is useful in selecting suitable inductors for the tuning circuits. When the center frequencies and Q of the tuning circuits are calculated according to (3-1), the required inductance can be decided to resonate with the tank (parasitic) capacitance at the center frequency. Then the inductor is selected based on the calculation with (3-2) as illustrated in (3-3),

$$L_1 = \frac{1}{\omega_{01}^2 C_1}, \quad Q_1 = \frac{R_{01} // R_{L1}}{\omega_{01} L_1} \rightarrow \text{get } R_{L1}. \text{ With } L_1 \text{and } R_{L1}, \text{ we have } Q_L = \frac{R_{L1}}{\omega_{01} L_1}. \tag{3-3}$$

It is possible that the required Q_T is too low to find a low Q_L for use and the assumption of high Q to derive (3-1) is invalid. As a result, the Q_T should be decided by Q_L through a reverse flow of (3-3), and other means may be required to flatten the stagger-tuned response. A solution will be presented in section 3.2.

3.1.2 Low Power

Multi-stage amplifiers usually come with the power consumption issue. Figure 9 shows a current reuse topology that is widely employed to fix the issue [10]. The circuit consists of two common-source stages which share the same bias current. The capacitor C_1 provides signal coupling between the two stages, and the bypassing capacitor C_2 functions as AC grounding link. Through the same bias current path, the circuit thus saves power. With Metal-Insulator-Metal (MIM) capacitor used for C_1 in chip layout, the parasitic capacitance between the bottom plate and the ground may impact the high frequency gain.

3.2 The Proposed Stagger-Tuned Topology

With the advantages of the above discussed circuits, the proposed LNA employing stagger tuning technique consists of two common-source stages with different resonant frequencies as shown in Figure 10.

In a cascaded two-stage amplifier, the first stage is designed with concern of noise factor (F) based on (3-4) [11],

$$F_{total} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1}. \tag{3-4}$$

where F_{total} is the total noise factor and G_1 is the power gain of the first stage. The second stage is targeted at linearity performance according to (3-5) [12],

$$IP3 = 10\log\left[\frac{1}{\frac{1}{IP_1} + \frac{1}{IP_2}}\right]. \tag{3-5}$$

The first stage of the proposed design is optimized for noise performance and the second for linearity. The minimum noise factor (F_{min}) is give by [3]

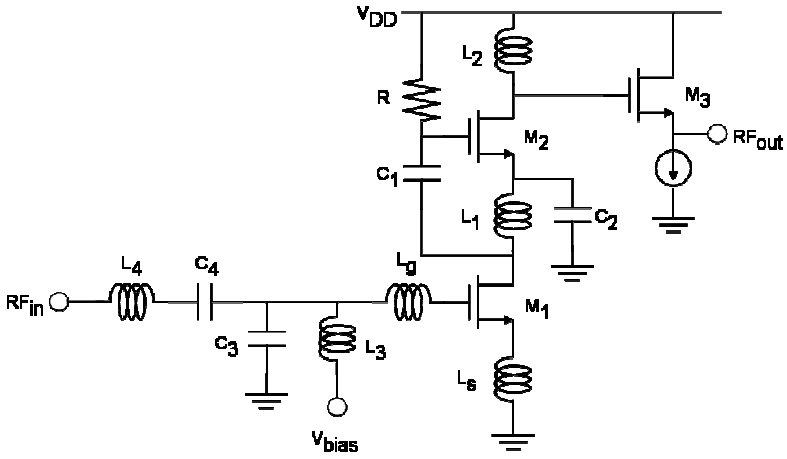


Figure 10. Proposed UWB LNA schematic (bias circuit is not shown).

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1-|c|^2)}, \qquad (3\text{-}6)$$

Equation (3-6) shows noise performance is better at lower frequency. Accordingly, the first stage is designed to resonate at the lower bound of the frequency band. The second stage, on the other hand, resonates at the upper bound of the frequency band. The resonance frequencies of the first and second stages together cover the whole bandwidth for UWB applications. The source inductor L_s is used to generate a real term for input impedance matching. The passive components L_g, L_3, L_4, C_3, and C_4 are adopted for matching network at the input to resonate over the entire frequency band. The output transistor M_3 works as a buffer for measurement purpose that can be removed when a down-converter follows on chip. The resistor R is used to provide bias voltage for the transistor M_2.

To achieve the goal of power saving, the second stage is stacked on top of the first stage. A coupling capacitor and a bypass capacitor are required for this topology. The capacitor C_1 provides signal coupling between the two stages, and the capacitor C_2 functions as an AC ground link at the source of transistor M_2. Both C_1 and C_2 are metal-insulator-metal (MIM) capacitors. The choice of large value of capacitor C_1 is preferred to perform better signal coupling. However, large MIM capacitors may suffer from parasitic capacitance between the

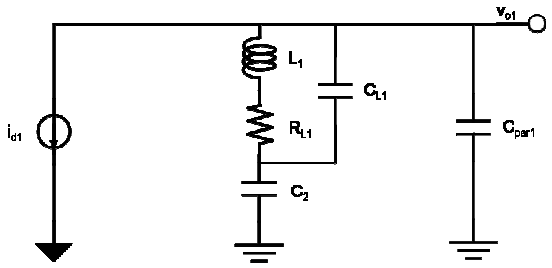


Figure 11. Small signal equivalent tank circuit of the first stage.

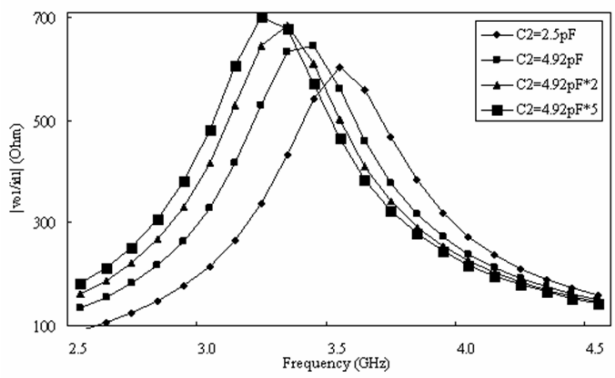


Figure 12. An example of tank gain with the variation of capacitor C_2, assuming L_1=5 nH, R_{L1}=14 Ω, and C_{par1}=495 fF.

bottom plate of the capacitor and ground, which degrade circuit gain. The value of capacitor C_2 is chosen to be as large as possible to provide ideal AC ground in conventional narrow band designs as well. Nevertheless, the value of capacitor C_2 affects gain flatness in the design employing stagger tuning technique. As sketched in Figure 11, i_{d1} is the small signal drain current of the transistor M_1. L_1 is the inductor load of the first stage. Its parasitic resistance and capacitance are R_{L1} and C_{L1}, respectively. C_{par1} represents all the parasitic capacitance at the drain node of the transistor M_1, and v_{o1} is the small signal voltage. The tank gain v_{o1}/i_{d1} can be expressed as Equation (3-7),

$$\frac{v_{o1}}{i_{d1}}(s) = \frac{1}{\dfrac{1}{\dfrac{sL_1 + R_{L1}}{1 + sC_{L1}(sL_1 + R_{L1})} + \dfrac{1}{sC_2}} + sC_{par1}} \approx \frac{1}{\dfrac{1}{sL_1 + R_{L1} + \dfrac{1}{sC_2}} + sC_{par1}}$$

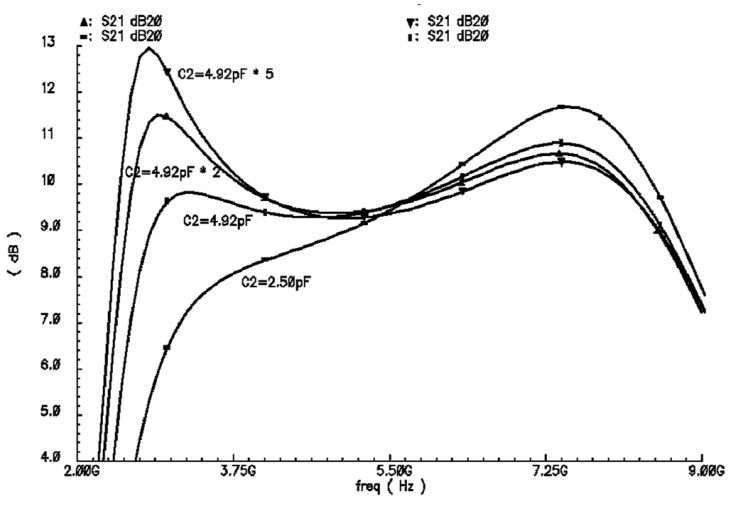


Figure 13. Selection of the optimum value of the bypass capacitor C2

$$\frac{v_{o1}}{i_{d1}}(\omega) = \frac{R_{L1} + j(\omega L_1 - \frac{1}{\omega C_2})}{1 - \omega^2 L_1 C_{par1} + \frac{C_{par1}}{C_2} + j\omega C_{par1} R_{L1}} \tag{3-7}$$

which shows the gain drops as the value of capacitor C_2 decreases around the resonant frequency of the first stage. The parasitic capacitor C_{L1} is about several femto-farads and ignored in the equation. This characteristic dominates the modification of the gain flatness in stagger-tuned UWB LNA where system Q is less than one and the available inductor Q_L is relatively high.

An example of the tank gain with the variation of capacitor C_2 illustrating (3-7) is shown in Figure 12. By controlling the gain peak at the lower bound of the frequency range, a very flat gain curve can be obtained over wide bandwidth. As shown in Fig. 13, an optimized value of the bypass capacitor C_2 exists for wideband design using the proposed topology.

3.3 Circuit Design

In the reference [5], a resistor of 90 Ohm used to improve the gain at lower frequency

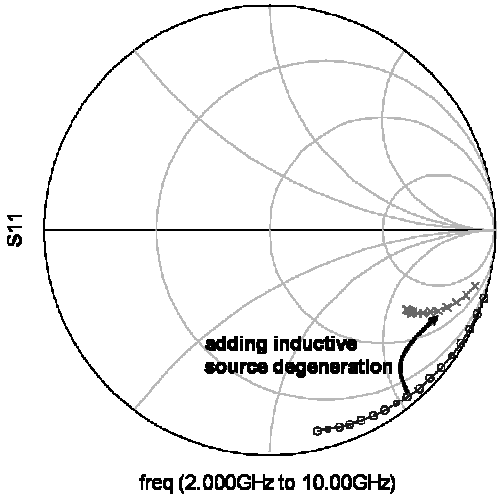


Figure 14. Real term generated by inductively source degeneration.

consumes 2.25mW with 5mA bias current and 1.8V power supply. A low power UWB LNA is designed based on the above design concepts and expected to save the power dissipation while keeping performance. To meet the expectation, the bias current is chosen to be 4mA. The United Microelectronics Corporation (UMC) 0.18-μm 1.8-V RF CMOS models are applied to this design. The input transistor size of 140 μ m and the associated bias point of 0.65V are selected according to noise performance simulation. Multi-finger technology is applied to lower the noise resulting from the transistor gate resistor.

The source inductor L_s of 0.6nH is used to generate a real term for broadband input impedance match without suffering from noise of real resistors as shown in Figure 14. The value of 0.6nH is adopted for it is close to the minimum value of available inductors in the model and will not degrade high-frequency gain too much.

The second stage is designed to meet linearity requirement as mentioned earlier and the device width is 100 μ m. For a low power design, a small device is preferred and biased to VDD [12]. The resistor R of 10K Ohms is used to provide bias voltage for the transistor M_2.

As shown in Figure 15, the two tuning circuits constitute the stagger tuned UWB LNA. $|T_1(j\omega)|=|Gm_1(j\omega)Z_1(j\omega)|$ is the voltage gain of the first stage with inductive source

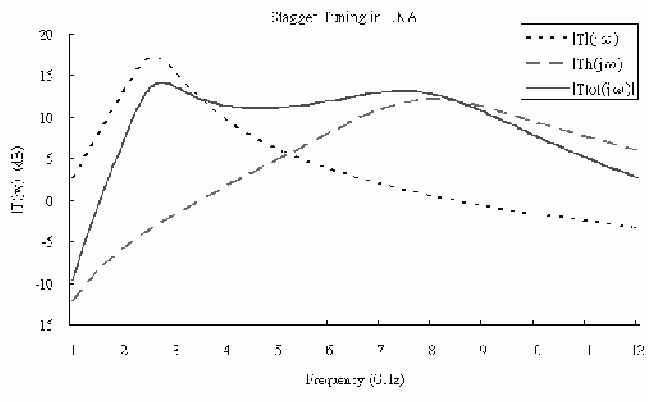


Figure 15. Stagger tuning in UWB LNA design.

degeneration, and $|T_h(j\omega)|=|Gm_2(j\omega)Z_2(j\omega)|\approx gm_2|\ Z_2(j\omega)|$ is the voltage gain of the second stage. $|T_{tot}(j\omega)|= |T_l(j\omega)\ T_h(j\omega)|$ with assumption of linear time invariant system. To achieve the goal of 3-8 GHz LNA, a wider bandwidth is considered for calculation in the initial design stage. Conservatively, 2.7GHz (10% below 3GHz) ~10.4GHz (30% above 8GHz) is set for -3dB bandwidth. The center frequency $f_0 = \sqrt{f_1 \cdot f_2}$ =5.3 GHz, and according to (3-1), f_{01}=2.6 GHz, f_{02}=8 GHz. Since the system Q is too low to find available inductor Qs, the tuning tank Qs are modified to be 2.4 and 2.1 for the first and second stages, respectively. The load inductor of the first stage is chosen to be 5nH to resonate with capacitance at the drain node of the transistor M_1, which includes the device parasitic and the capacitance between the bottom plate of C_1 and ground. The load inductor of the second stage is chosen to be 1.2nH. The resonance frequencies of the first and second stages are conservatively able to cover the 3-8-GHz bandwidth for UWB applications.

At the frequencies of interest, the inductor Q's are around 7~10 and the unloaded tank Q's are about 3~4 which can be calculated from the output resistance of the tuning stages. According to (3-2), the tuning tank Q's are around 2~2.5. Therefore, selection of optimized value of C2 is required to achieve maximum gain flatness.

The capacitance of capacitor C_1 is selected to be 4.92 pF for signal coupling and without

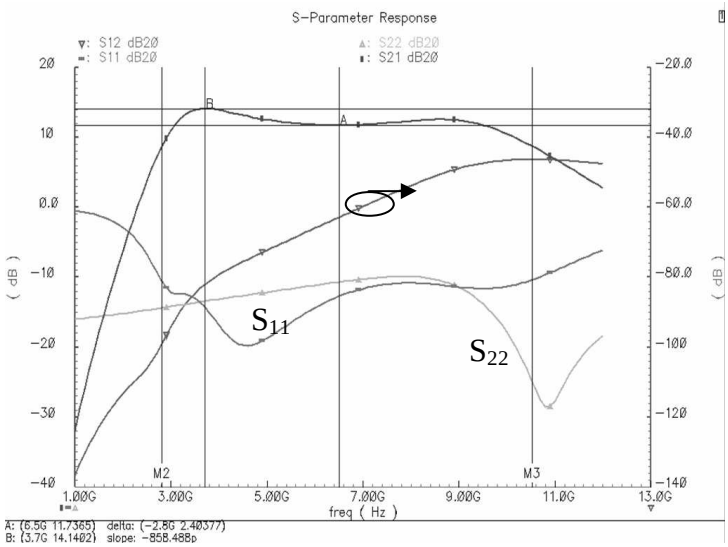


Figure 16. Power gain, isolation and return loss.

suffering from severe parasitic. From Fig. 14, the best gain flatness can be obtained while the value of capacitor C_2 is 4.92 pF. With the resonance matching technique for broadband match [13], the passive components L_g=2.5nH, L_3=1.8nH, L_4=0.9nH, C_3=350fF and C_4 =1000fF are adopted for noise and impedance matching to the 50-Ohm source. The output is matched to 50 Ohm with the buffer stage for measurement purpose. The buffer stage is added for RF measurement and biased at 4.3 mA.

3.4 Simulation Results

The circuit simulation was accomplished with Cadence SpectreRF simulator. Figure 16 shows the return losses are well below –10 dB throughout the entire frequency band. The –3 dB frequency band is 2.8-10.5 GHz. The maximum power gain with 50 Ohm matched load is 14.1 dB. The gain curve at the left side of 3.2 GHz, the resonance frequency of first stage, is much deeper than that at the right side of 7.4 GHz, since –3 dB frequency drops faster in the lower frequency band for the similar Qs.

The LNA has a lowest noise figure of 3.02 dB as shown in Figure 17. Two-tone signals

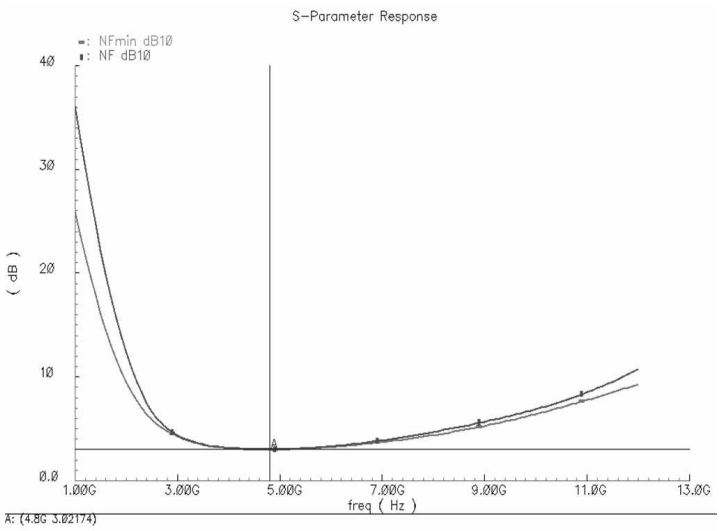


Figure 17. Noise figure

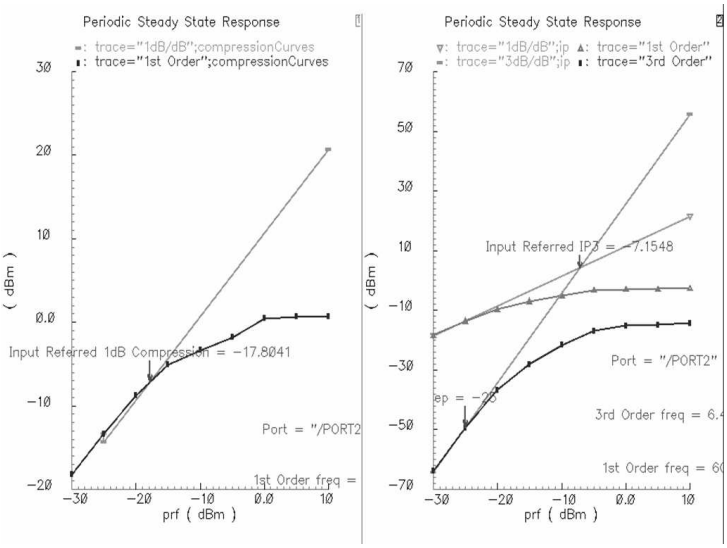


Figure 18. Two-tone test and 1dB compression

around 6 GHz are applied to the LNA to observe the input referred IP3 (IIP3). One-tone test at 6 GHz is performed to obtain the input referred 1dB compression point (IP1dB). The simulated IIP3 is –7.2 dBm and the simulated IP1dB is -17.8 dBm, respectively, as shown in Figure 18. The simulation results show the LNA topology and design perform very well and thus encourage the application in UWB system which will be verified in the next chapter.

Chapter 4

LNA Application in UWB System

Since the proposed low-power UWB LNA performs well in the simulation results, the LNA circuit is put in the UWB system for verification in this chapter. Section 4.1 introduces in brief the MutiBand OFDM proposal and focuses on RF related information. Section 4.2 discusses RF/Baseband co-simulation. The simulation results for LNA application in the UWB system is shown in section 4.3.

4.1 MB-OFDM Proposal Brief

In the MB-OFDM proposal [14], the FCC approved spectrum, 3.1-10.6 GHz, is divided into 14 bands where each band has bandwidth of 528 MHz. As shown in Figure 19, the 14 bands are categorized into 5 band groups where a time-frequency code (TFC) is utilized to interleave coded data over up to three frequency bands. Each band uses a total of 122 modulated and pilot subcarriers out of a total of 128 subcarriers whose bandwidth is 4.125 MHz each. The OFDM subcarriers are modulated using QPSK. To avoid difficulties in DAC and ADC offsets and carrier feed-through in the RF system, the subcarrier falling at DC (0th subcarrier) is not used. The support of transmitting and receiving at data rates of 53.3, 110, and 200 Mb/s is mandatory, while the maximum capability can achieve 480 Mb/s. Devices operating in band group #1 are denoted Mode 1 devices, and it shall be mandatory for all

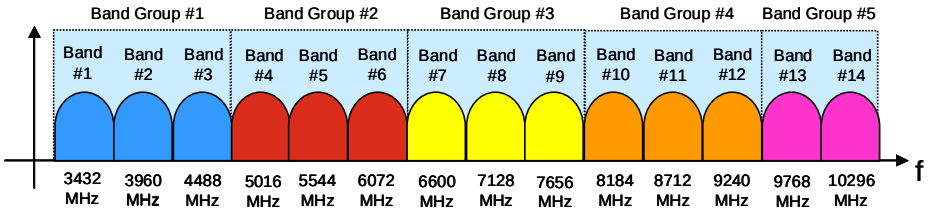


Figure 19. Band assignment in Multi-Band OFDM proposal.

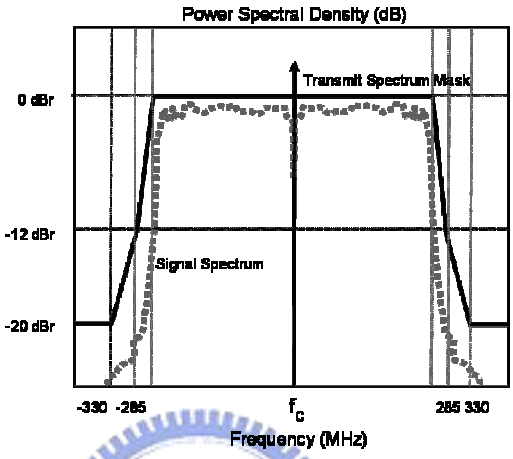


Figure 20. Transmitter power spectral density mask in MB OFDM proposal.

Table 1. Receiver performance requirement in MB OFDM proposal.

Data Rate (Mb/s)	Minimum Sensitivity for Mode 1 (dBm)
53.3	-83.6
80	-81.6
110	-80.5
160	-78.6
200	-77.2
320	-75.5
400	-74.2
480	-72.6

devices to support Mode 1 operation, with support for the other band groups being optional and added in the future. The transmitted spectrum shall have a 0 dBr (dB relative to the maximum spectral density of the signal) bandwidth not exceeding 260 MHz, –12 dBr at 285 MHz frequency offset, and –20 dBr at 330 MHz frequency offset and above. The transmitted spectral density of the transmitted signal mask shall fall within the spectral, as shown in

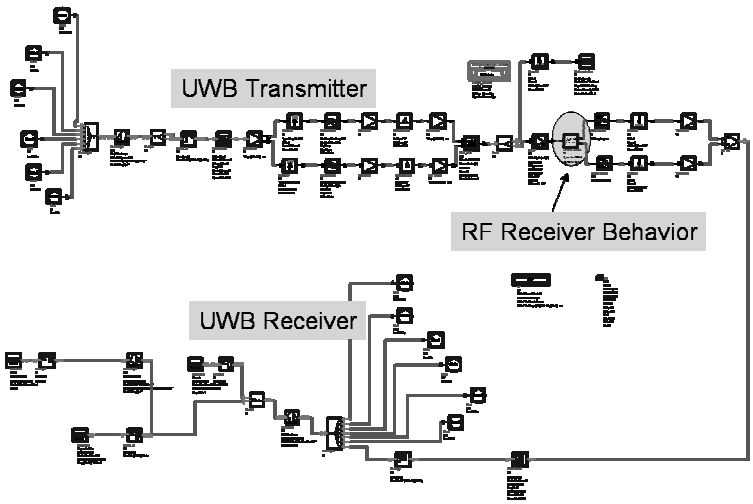


Figure 21. RF/Baseband co-simulation model.

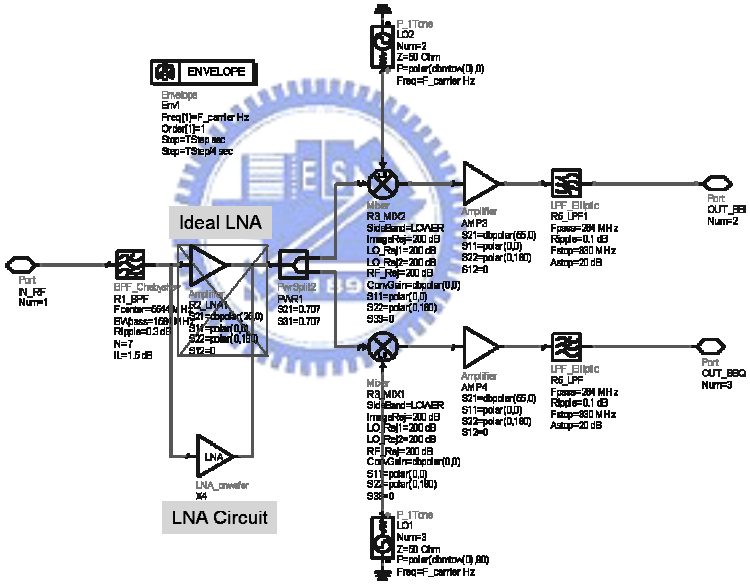


Figure 22. RF receiver behavior model.

Figure 20. For a packet error rate (PER) of less than 8% with a PSDU of 1024 bytes, the minimum receiver sensitivity numbers for the various rates and modes are listed in Table 1.

4.2 RF/Baseband Co-simulation

The tradeoff of RF receiver front-end includes noise figure, power gain, linearity, bandwidth,

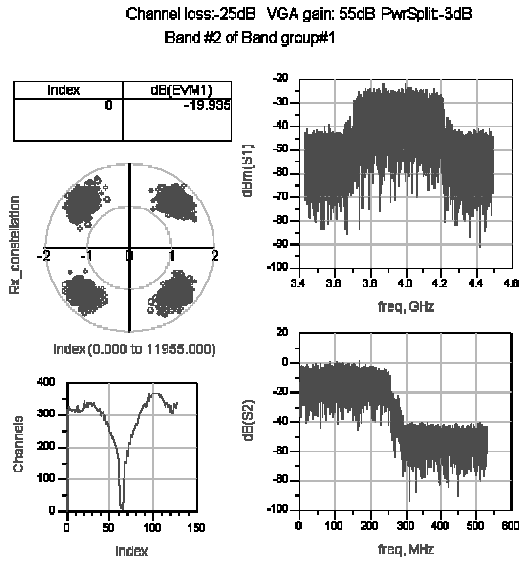


Figure 23. Co-simulation results – band group#1.

and power consumption. The performance greatly affects baseband signals. The co-simulation of circuit-level RF with algorithm-level baseband can be applied to evaluate the effects on error vector magnitude (EVM). The co-verification platform is fulfilled in the DSP environment of Agilent ADS. The data flow simulator and circuit envelope simulator enables co-simulation of algorithm-level baseband with circuit-level RF front-end. A tentative algorithm-level of UWB baseband transceiver is used to co-simulate with this LNA circuit design. The RF/Baseband co-simulation model is shown in Figure 21. One of the building blocks is the RF receiver behavior model which consists of RF front-end and analog modules as shown in Figure 22. Band selection filer, LNA, mixer, variable gain amplifier, and low-pass filter in discrete modules are included.

4.3 Simulation Results

The RF/Baseband co-simulation with the LNA circuit is conducted for Band Groups #1~#4

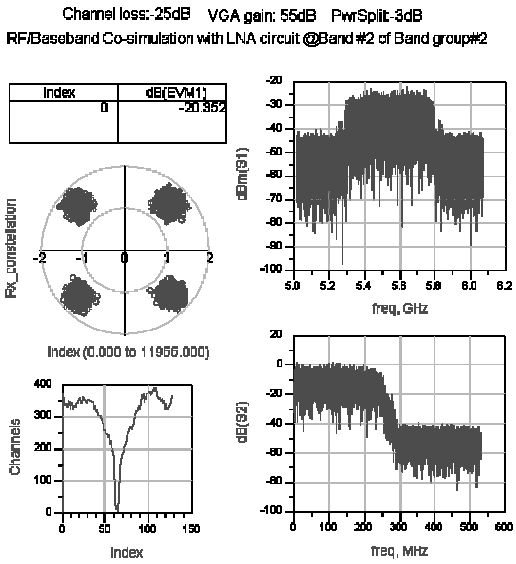


Figure 24. Co-simulation results – band group #2.

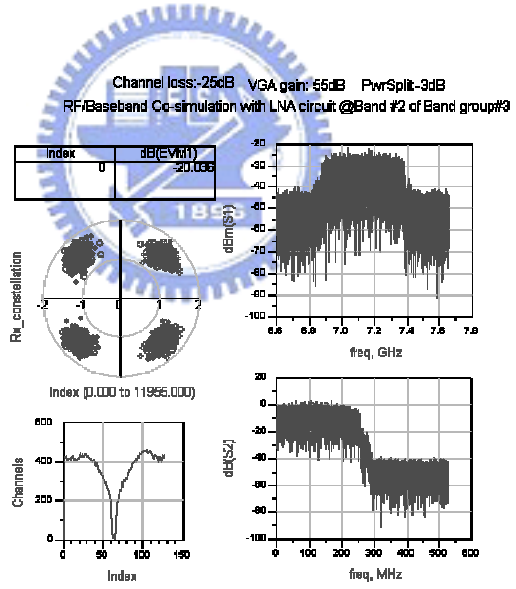


Figure 25. Co-simulation results – band group#3.

and the simulation results are shown in Figure 23~26, respectively. The power spectrum density at the transmitter output is plotted. The power spectrum at the Q-path of the RF behavior output is displayed. The figures also show clear QPSK signal constellation. The EVM results are close to those with behavior building block of LNA which means little

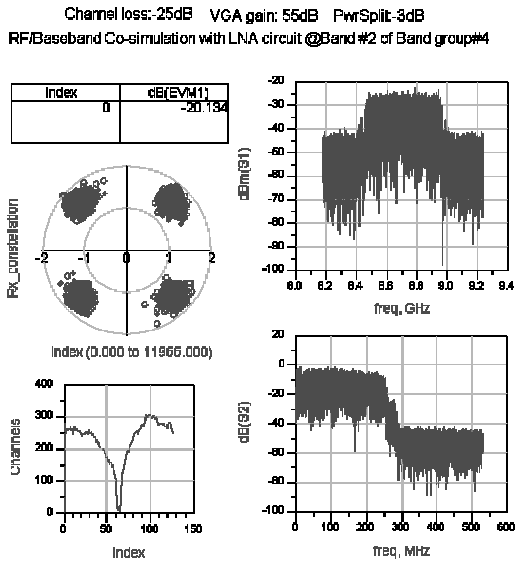


Figure 26. Co-simulation results – band group#4.

degradation caused by the proposed LNA circuit. The co-simulation results show that the proposed LNA circuit performs well in the UWB applications. With the verification of RF/Baseband co-simulation, the proposed LNA design is further studied by chip implementation and measurement which are described in the next chapter.

Chapter 5

Implementation and Experimental Results

With verification through the RF/Baseband co-simulation, the proposed low-power LNA design is to be implemented on chip for further research in this chapter. Section 5.1 addresses consideration of layout which is one of the key points for RF circuit to perform as expected. Section 5.2 presents the chip layout of the proposed LNA and the post-layout simulation results. The measurement results and analysis are shown in section 5.3. Section 5.4 summarizes the proposed LNA design.

5.1 Consideration of Layout

Since RF signal is very sensitive to the parasitic capacitance, the signal path should be arranged as short and straight as possible. Overlapping of RF paths should be avoided too. Besides, noise coupling via the substrate may interfere with RF signal, so metal 6 is assigned for signal path and a grounding metal layer below it for noise shielding is necessary. Obviously, metal layer 1 is usually the choice because the space between metal layers 1 and 6 is the biggest and hence the parasitic effect is the smallest. Whenever metal-insulator-metal (MIM) capacitors are used, the parasitic capacitance between the bottom plate and the grounding layer always affects the circuit performance. It should be kept in mind prior to layout work. As the on-chip spiral inductors are necessities in radio frequency circuit design,

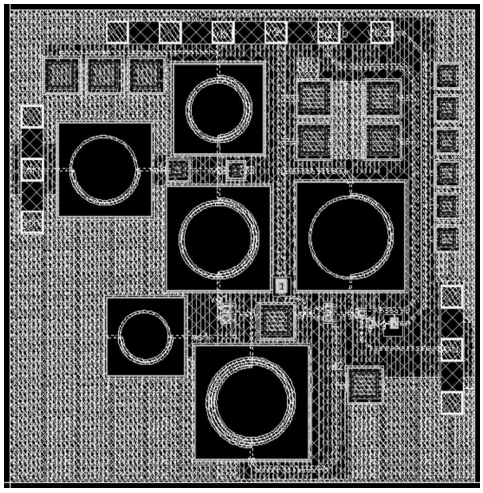


Figure 27. Layout of the proposed UWB LNA.

their huge footprint always decides the chip area. The inductors should be arranged in the way that the RF signal flows in the shortest and most straight route. Also, proper space between inductors is required to mitigate mutual inductance effect. If the layout is designed for on-wafer testing, the smaller RF pads are preferred for less parasitic capacitance. However, too small pads can result in difficulty in chip measurement because the testing probes are hard to land right on the pads. The test rule should be checked before layout work. While different building blocks are integrated on the same chip, power supplies of RF, baseband and ESD should be separately fed to avoid interference. In addition, bypassing capacitors can be added on the nodes of power supplies to filter noise. Regarding the four quadrature signal paths of LO feeding to the mixer, they should be wired symmetrical and close to one another to reduce phase errors and hence DC offsets.

5.2 Chip Layout and Post-Layout Simulation

The layout of proposed LNA is shown in Figure 27 and the die area is 1.76 mm^2. The post-layout simulation was accomplished with Cadence SpectreRF simulator.

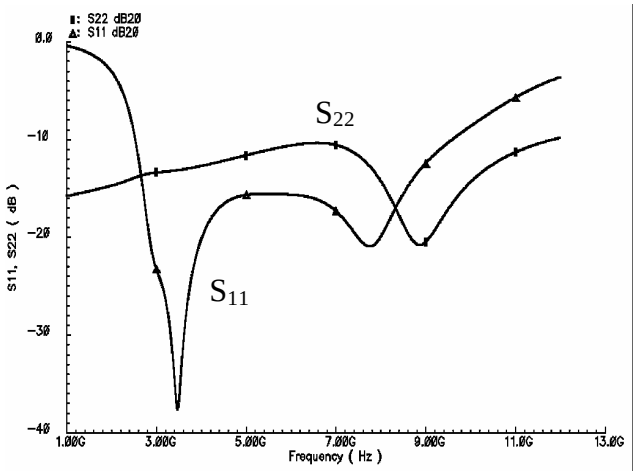


Figure 28. Input and output match.

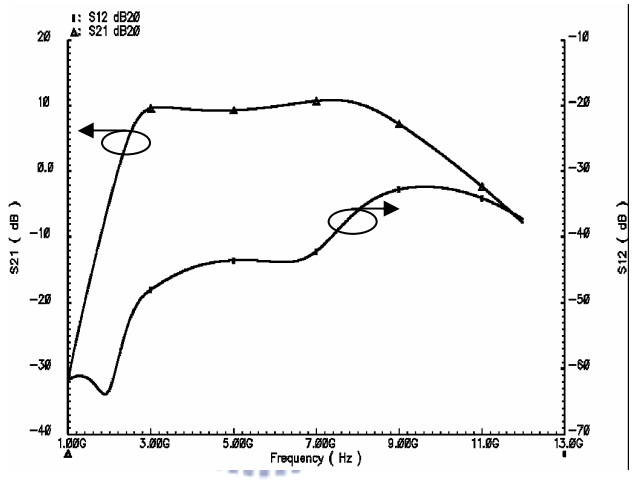


Figure 29. Power gain and reverse isolation.

Figure 28 shows the return loss S11 is well below –10 dB throughout the entire frequency band. The –3 dB frequency band is 2.6-9.2 GHz. The maximum power gain with 50 Ohm matched load is 10.9 dB as shown in Figure 29. The gain curve at the left side of 3.2 GHz, the resonance frequency of first stage, is much deeper than that at the right side of 7.4 GHz, since –3 dB frequency drops faster in the lower frequency band.

The LNA has a lowest noise figure of 3.5 dB as shown in Figure 30. Two-tone signals around 6 GHz are applied to the LNA to observe the input referred third-order intercept point (IIP3). One-tone test at 6 GHz is performed to obtain the input referred 1dB compression point (IP1dB). The simulated IIP3 is –5.1 dBm and the simulated IP1dB is -15.3 dBm,

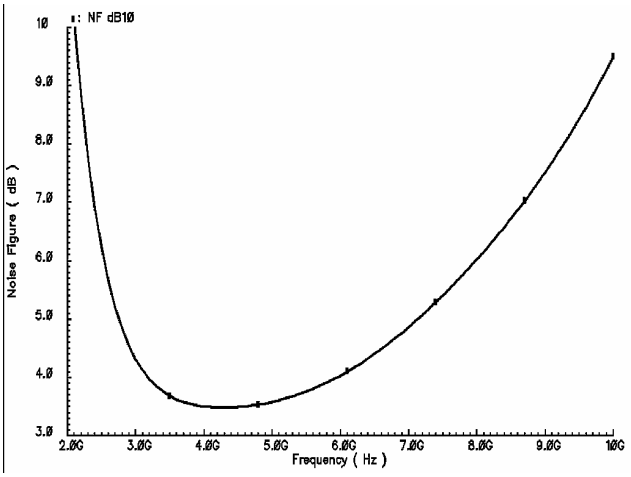


Figure 30. Noise figure.

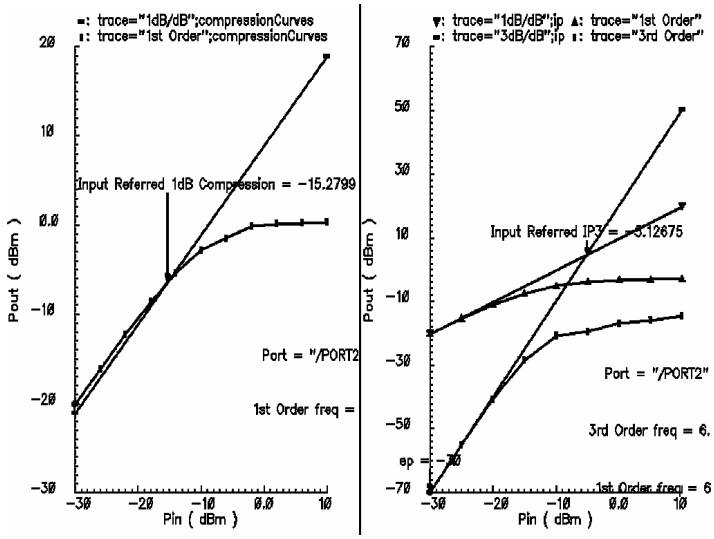


Figure 31. Two-tone test and 1dB compression.

respectively, as shown in Figure 31. To establish more confidence about the circuit design and layout for tapeout, a post-layout simulation is also conducted with Agilent Advance Design System (ADS). Figure 32 and 33 show the simulation results of power gain, reverse isolation and return loss of the design which do not deviate much from those simulated by Cadence SpectreRF. Figure 34 also performs the similar trend of noise figure as Figure 30. Frequency response plots in magnitude and phase of S21 are shown in Figure 35, where zeros and poles can be observed.

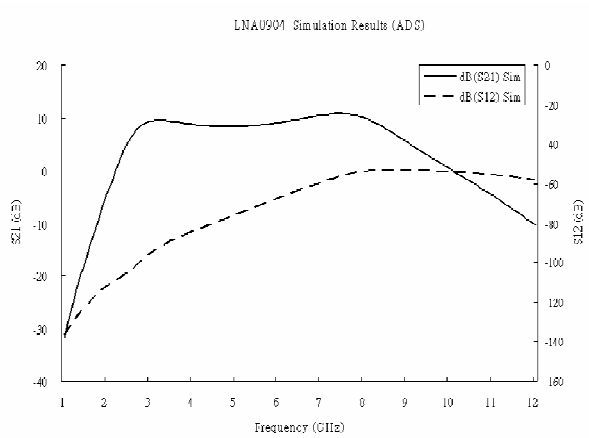


Figure 32. Power gain and reverse isolation with Agilent ADS.

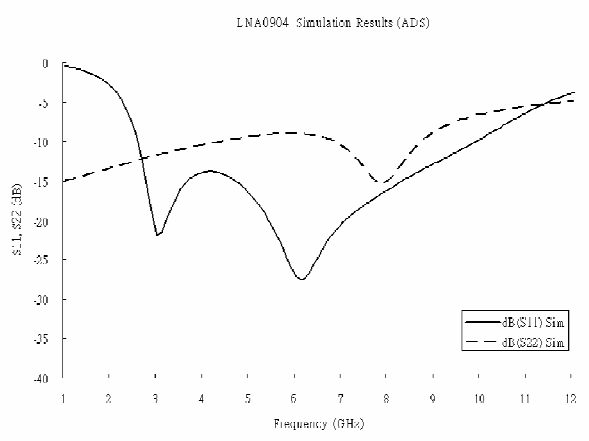


Figure 33. Return loss with Agilent ADS.

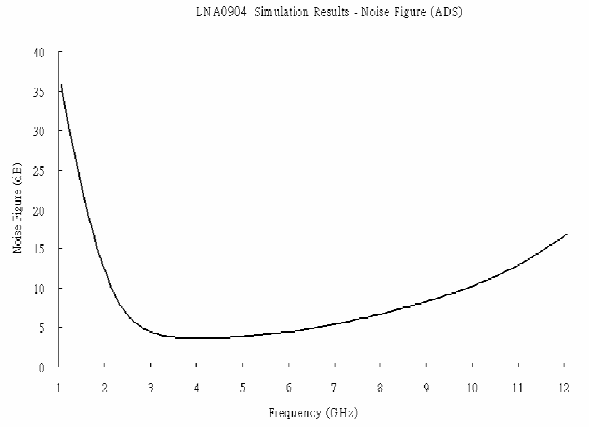


Figure 34. Noise figure with Agilent ADS.

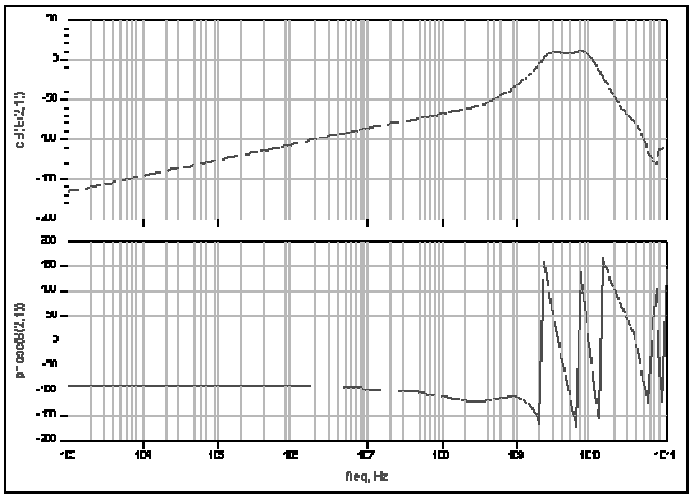


Figure 35. Frequency response of S21.

5.3 Measurement Results and Analysis

The circuit is measured on wafer with RF probes and the HP8510C network analyzer. The photography of the LNA chip is shown in Figure 36. The measurement results are attached in the following figures where the simulation results are also sketched for comparison. As shown in Figure 37, a 2.4-9.4-GHz ultra-wideband LNA is achieved and the maximum power gain is 9.7dB while the gain flatness is also demonstrated. It can be observed that the power gain degrades at the middle frequency band but rises at the band close to the higher end of the measurement frequency. It can be explained as the resonance frequency of the 2nd stage tank shifts towards higher frequency. The cause is possibly the process downwards variation of the inductor or device parasitic capacitance at the 2nd stage which is designed to resonate at higher bound of the frequency range.

The measured minimum noise figure is as low as 4.17dB at 4.1GHz as shown in Figure 38. It is only 0.54dB above the simulated value and positioned at same frequency. The average noise figure over the entire bandwidth is about 5.2dB. In Figure 39, the input impedance

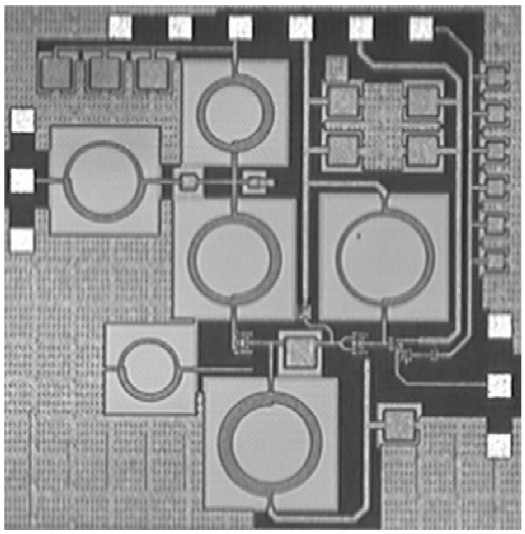


Figure 36. Photography of LNA chip.

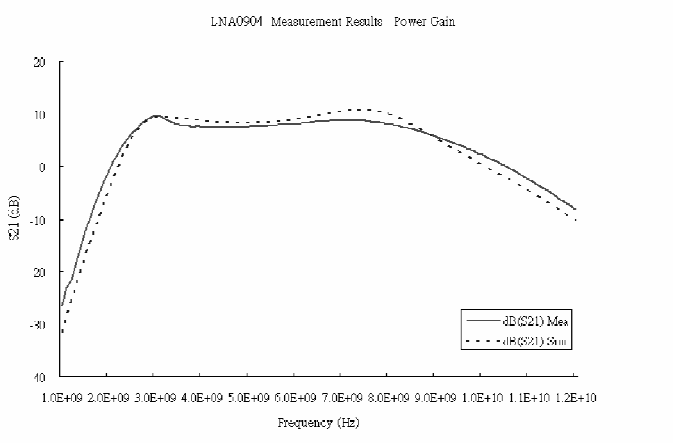


Figure 37. LNA measurement results - power gain.

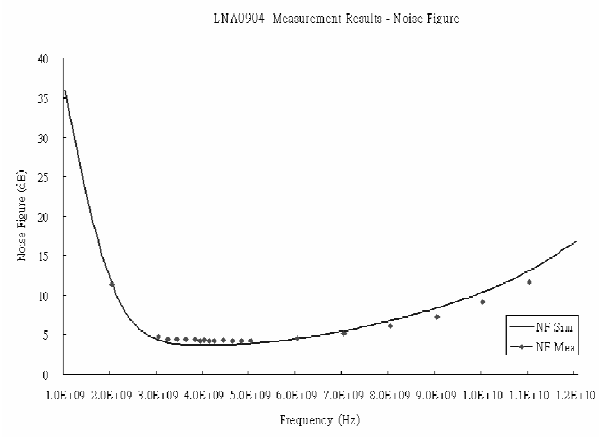
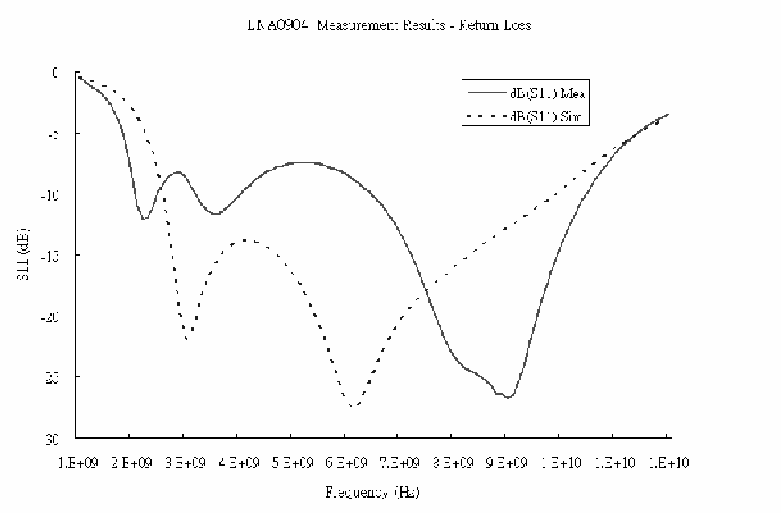
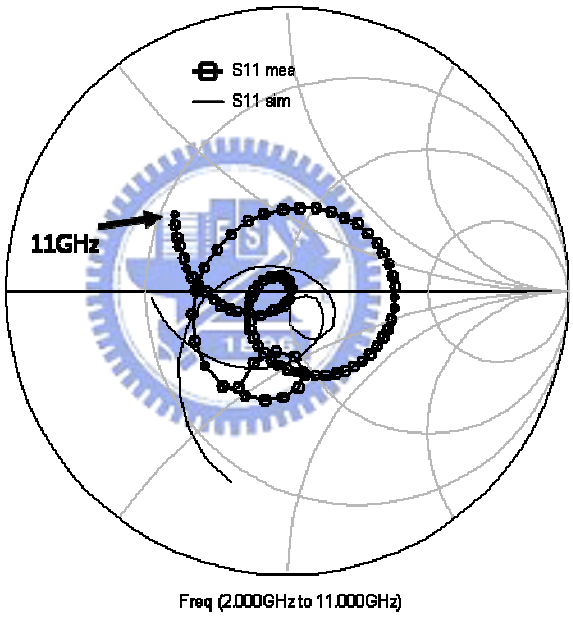


Figure 38. LNA measurement results – noise figure.



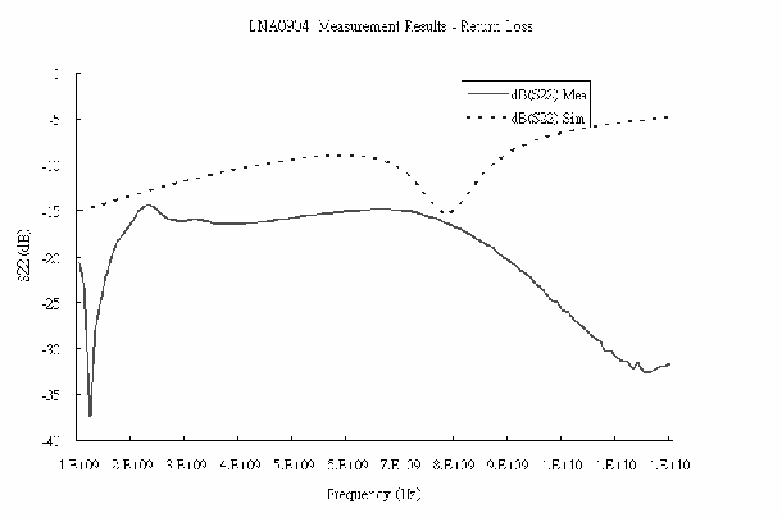
(a)



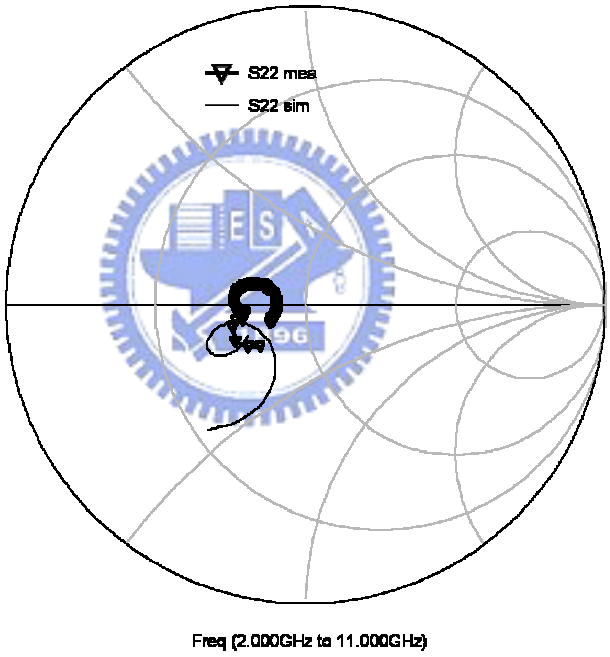
(b)

Figure 39. LNA measurement results - (a) input return loss; (b) S11 in Smith Chart.

match S11 is measured less than -7.4dB in the frequency range and in Figure 40, the output impedance match S22 is well below -15dB. With return loses plotted on the Smith Chart, it is easier to observe the broadband match condition. The relatively higher deviation of the S11 between simulation and measurement results is possibly due to the process variation of the input matching network, especially the inductors. It can be verified by simulation tools.



(a)



(b)

Figure 40. LNA measurement results - (a) output return loss; (b) S22 in Smith Chart.

The measured reverse isolation is better than 40dB for the most of the frequency of interest as shown in Figure 41. This good isolation is much helpful to prevent the LO leakage from the down-conversion mixer to the antenna.

As regards the linearity test, the Agilent E4440A PSA series spectrum analyzer is used. A

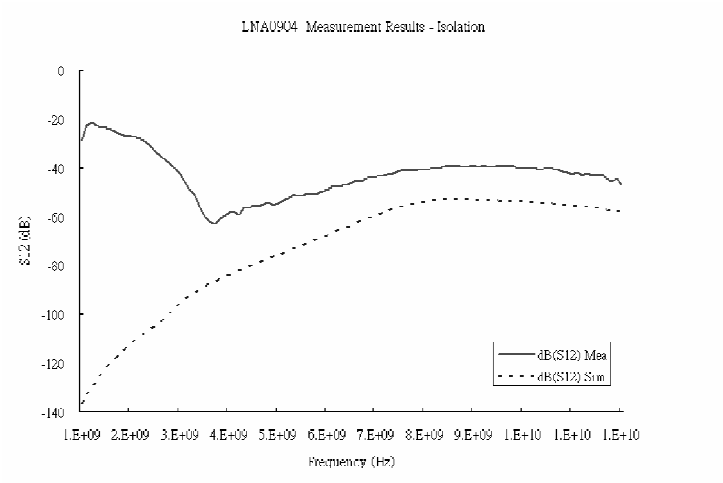


Figure 41. LNA measurement results – reverse isolation.

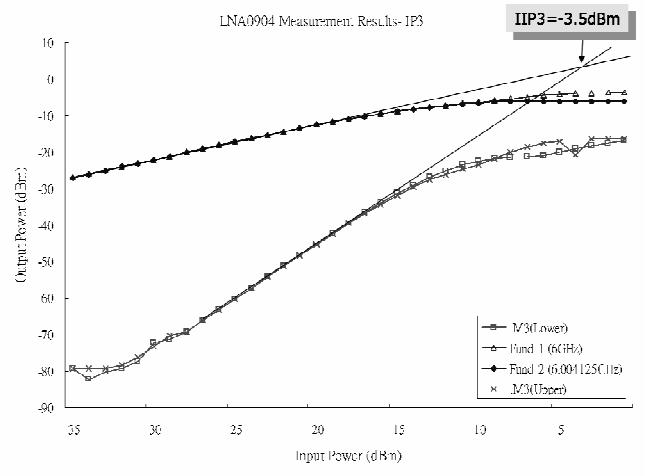


Figure 42. LNA measurement results –IP3.

two-tone test is conducted at 6GHz with the spacing of 4.125MHz which is the bandwidth of the OFDM sub carrier in the MB-OFDM proposal. The measured results reveal in Figure 42 that the LNA exhibits good input IP3 of -3.5dBm. A one-tone test is applied individually at 6GHz to get the input referred 1-dB compression point of -14dBm as sown in Figure 43. The LNA dissipates only 7.3 mW with a power supply of 1.8V. The total power consumption is detailed in Table 1.

In this work, both Cadence SpectreRF and Agilent ADS are used in simulation. Cadence Virtuoso is applied in layout editing. In Figure 44, the measured power gain is displayed

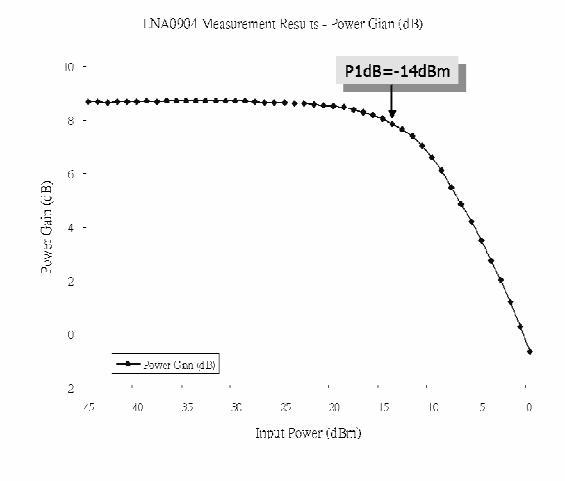


Figure 43. LNA measurement results –P1dB.

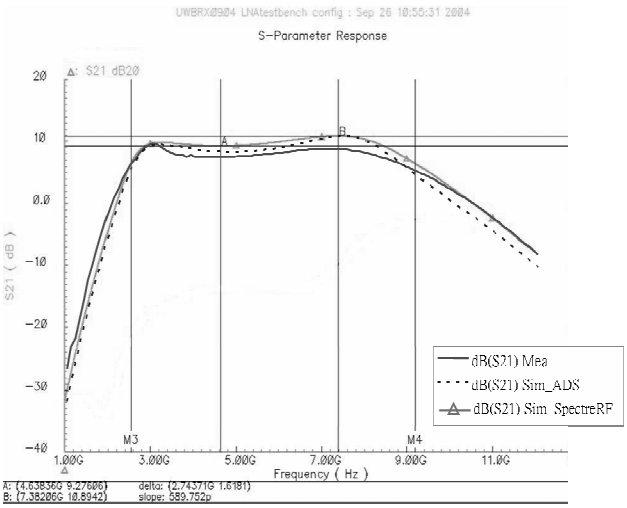


Figure 44. Comparison between simulation tools and measurement

Table 2. LNA measurement results - power consumption

Unit: mW	Simulated Power Consumption	Measured Power Consumption
LNA Core	7.15	7.33
Buffer	7.79	7.60
Total	14.94	14.93

together with the post-layout simulation results by the two circuit simulator. There is no much difference between them in this case and the maximum deviation between the

simulation and measured results is 2.2dB.

The performance of the proposed LNA is summarized in Table 3, with comparison to other recently published wideband LNAs. The power consumption of the proposed LNA is much lower than that of the others, while the other performance indices are competitive. For clear comparison, a figure of merit (FOM) for the wideband LNAs is employed as (5-1)

$$FOM = \frac{G_{\max,(mag)} \cdot IIP3_{(mag)}}{(NF_{\min,(mag)} - 1) \cdot P_{dc(mW)}} \cdot \frac{f_{H,(GHz)}}{f_{L,(GHz)}}, \quad (5\text{-}1)$$

The higher the FOM is, the better the performance. Since the average values of power gain and noise figure are not all available for the LNAs in the table, the maximum gain and minimum noise figure are adopted in the formula. The FOM is not applicable to [6] and [7] whose low-3dB frequencies are near DC. The proposed LNA is obviously a good candidate for low power UWB applications.

5.4 Summary

A two-stage stacked topology employing stagger tuning technique has been presented for low power UWB LNAs. The quality factors for circuit design and inductor selection are discussed. In addition, the optimization of gain flatness is proposed. Implemented in 0.18-μm CMOS technology, the measurement results demonstrate that the proposed LNA is paving the way to a new generation of low power UWB applications.

With complete research on the low power LNA which has strong backup of measurement data, the next chapter will go further to develop a RF receiver front-end for the integration of the UWB transceiver.

Table 3. Performance summary and comparison to other wideband LNAs

	Tech.	S11 (dB)	Gmax (dB)	BW (GHz)	NFmin (dB)	IIP3 (dBm)	IP1dB (dBm)	Pdc (mW)	FOM*
This work (Measured)	0.18μm CMOS	<-7.4	9.7	2.4-9.4	4.17	-3.5	-14	7.3	1.39
This work (Sim_ADS)	0.18μm CMOS	<10.6	10.8	2.6-9.1	3.63	-3.6	-13.3	7.2	-
This work (Sim_SpectreRF)	0.18μm CMOS	<-11.5	10.9	2.6-9.2	3.48	-5.1	-15.3	7.2	-
[5]-1	0.18μm CMOS	<-9.9	9.3	2.3-9.2	4.0	-6.7	-15	9	0.53
[5]-2	0.18μm CMOS	<-9.4	10.4	2.4-9.5	4.2	-8.8	-18	9	0.39
[6]-1	0.18μm CMOS	<-10	11.5	0.01-14	3.4	9.4	0.4	52	N.A.
[6]-2	0.18μm CMOS	<-8	8.1	0.01-22	4.3	8.7	-1	52	N.A.
[7]	0.25μm CMOS	<-8	13.7	0.002-1.6	1.9	0	-9	35	N.A.

Chapter 6

UWB Receiver Front-End Design

Wireless UWB transceivers are expected to replace lots of lousy wiring for various consumer electronic devices and computer peripherals. In the near future, it is possible to build up wireless entertainment centers at home and mobile business work in office with wireless UWB technology. Although the IEEE 802.15.3a standard is not yet firmed, the move of UWB products toward market has never been stopped. This chapter integrates the proposed low power UWB LNA topology with down-conversion mixers to develop a RF receiver front-end for the integration of the UWB transceiver. In section 6.1, the UWB transceiver architecture is introduced and the advantages and issues of the direct conversion receivers are discussed. The passive mixer for the receiver front-end is presented in section 6.2. The considerations about layout and package are given in section 6.3. The implementation of the RF front-end is provided in section 6.4. In section 4.5, the simulation results of the UWB receiver front-end and the RF/baseband co-verification are shown. Section 6.6 summarizes this RF front-end design work.

6.1 System Architecture

The UWB transceiver architecture is referenced to the band group #1 of the Multi-Band

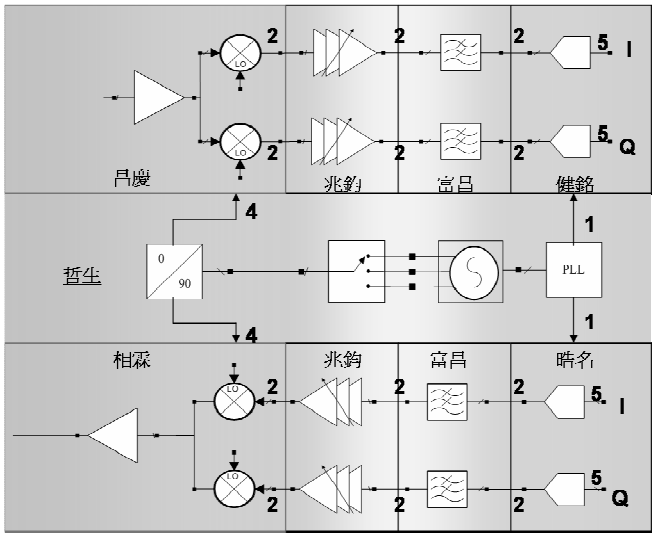


Figure 45. System architecture of UWB transceiver.

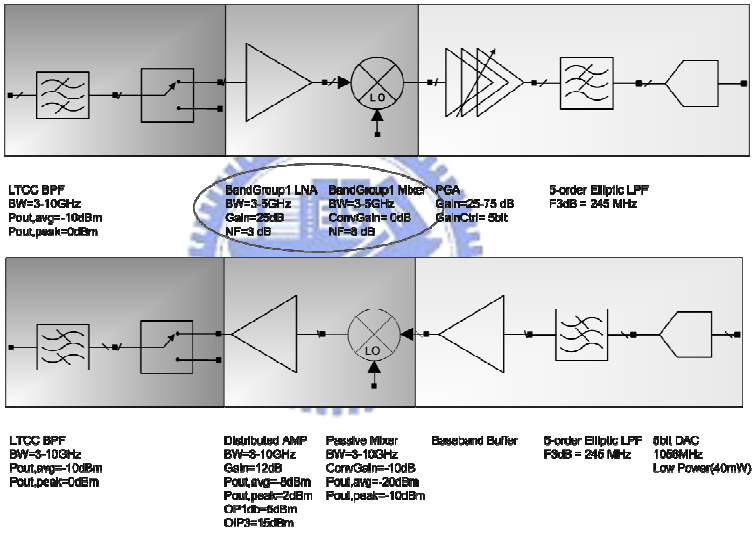


Figure 46. Behavior model and specification.

OFDM proposal with operation frequency between 3GHz to 5GHz. Direction-conversion is adopted in the system architecture as shown in Figure 45. The bulky image rejection filters are not necessary any more and system-on-chip (SOC) integration is more accessible with this compacter architecture. Besides, it is more important that power consumption can be much reduced. Figure 46 shows the behavior model and module specifications. On the other hand, the direct-conversion architecture exhibits several issues such as DC offsets, I/Q mismatch, even-order distortion, and flicker noise.

6.1.1 DC Offsets

When the downconverted band extends to zero frequency, extraneous offset voltages can corrupt the signal and saturate the following stages. The main cause of DC offsets is that strong LO signal leaks to RF port through capacitive and substrate coupling and the self-mixing occurs in the mixer. The problem of offset gets worse if self-mixing varies with time. This happens when the LO signal leaks to the antenna and is radiated and subsequently reflected from moving objects back to the receiver.

There are various means of offset cancellation. High pass filtering or capacitive coupling can be a good solution for wideband channels that contain little energy near DC. In the MB OFDM proposal, the subcarrier falling at DC (0th subcarrier) is not used, and the lower corner frequency can be higher than 1 MHz.

6.1.2 I/Q Mismatch

The phase errors and amplitude mismatches of quadrature LO signal corrupt the downcoverted signal constellation , thereby raising the bit error rate. Suppose the received signal is $x_{in}(t) = a\cos\omega_c t + b\sin\omega_c t$, and assume the I and Q phases of the LO signals are

$$x_{LO,I}(t) = 2\cos\omega_c t \tag{4-1}$$

$$x_{LO,Q}(t) = 2(1+\varepsilon)\cos(\omega_c t + \theta), \tag{4-2}$$

where ε and θ represent amplitude and phase errors, respectively.

The normalized error vector magnitude (EVM) can be expressed as

$$EVM = \frac{(1+\varepsilon)(b\cos\theta + a\sin\theta) - b}{\sqrt{a^2 + b^2}}, \tag{4-3}$$

and can be used as the performance index for the receiver and be regarded as the inversed

signal-to-noise ratio if we consider noise as error vector [15]. To mitigate the I/Q mismatch issue, the quadrature LO signal generation should be designed carefully.

6.1.3 Even-Order Distortion

Suppose two strong interferers close to the channel of interest enter the LNA, the second order intermodulation distortion of the LNA will induce a low-frequency beat at the LNA output. The mismatch of differential switching transistor pair results in direct feedthrough from the RF input to the IF output which corrupts the baseband signal. The RF port of the mixer also suffers from the same even order distortion effect. To mitigate the even order distortion, the LNA and mixer should present good second-order nonlinearity performance characterized by the second-order intercept point (IP2). Besides, an on-chip ac coupling capacitor between the LNA and the succeeding mixers can effectively prevent the low-frequency beats at the LNA output from entering the mixers. However the parasitic capacitance of the capacitor should be noted not to impact the signal too much.

6.1.4 Flicker Noise

Since the downcoverted spectrum extends to zero frequency, the 1/f noise of devices significantly corrupts the baseband signal. This is a severe problem in the circuits employing MOSFETs. Several means may be applied to reduce the flicker noise in the receiver. In baseband circuits, PMOS can be used to lower 1/f noise. Devices with larger size also help. An on-chip AC coupling capacitor between the LNA and the succeeding mixers can effectively prevent the 1/f noise at the LNA output from entering the mixers.

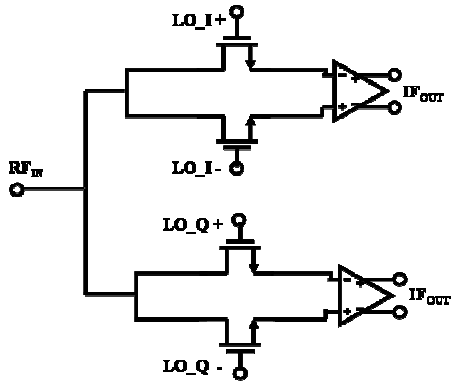


Figure 47. UWB Mixer topology.

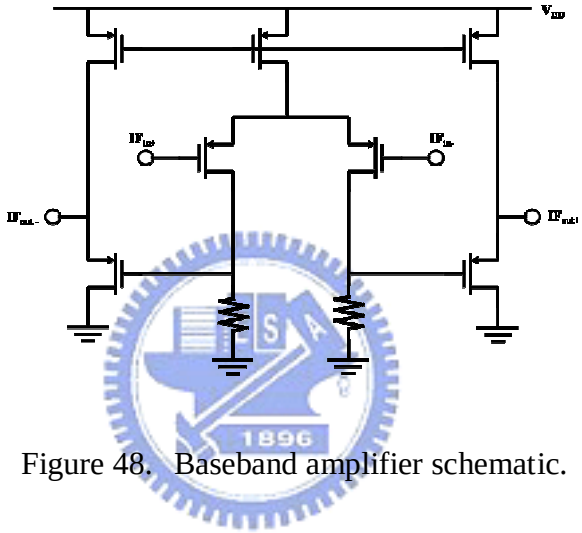


Figure 48. Baseband amplifier schematic.

6.2 Mixer Design

A down-conversion mixer is used to convert the RF frequency to IF frequency. In the direct conversion receiver structure, zero IF is required in the design.

6.2.1 Circuit Topology

A wideband passive mixer is designed for the purpose of low power, little flicker noise and high linearity following the LNA, as shown in Figure 47. The conversion gain and noise

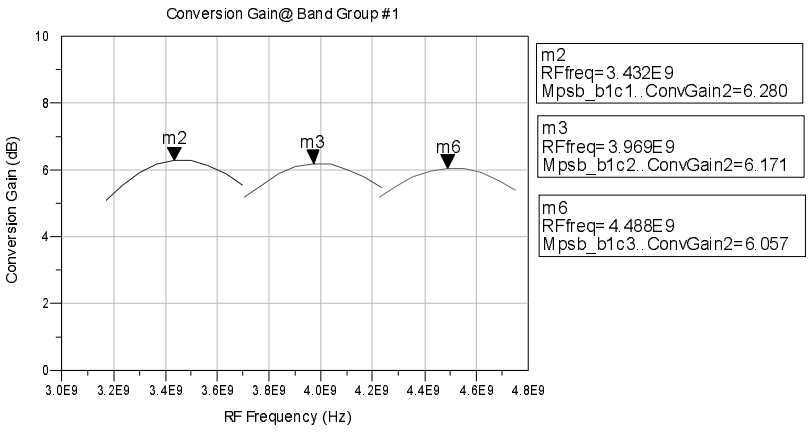


Figure 49. Conversion gain of mixer with baseband amplifier.

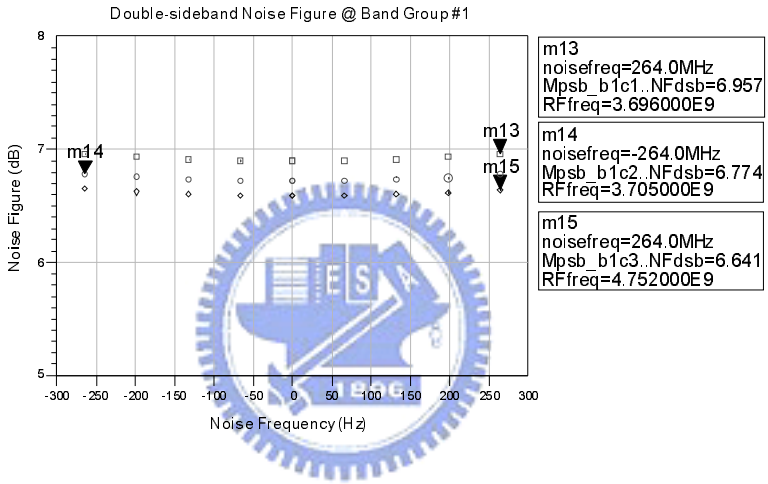


Figure 50. Noise figure of mixer with baseband amplifier.

figure of passive mixers are well analyzed in [16]. Some trade-offs exist between voltage conversion gain and linearity. A baseband amplifier is designed with consideration of low noise for compensating the gain loss of the passive mixer and consequently helps improving overall noise performance of the receiver as shown in Figure 48. PMOS devices with large width and resistor loads are adopted in the design of the differential baseband amplifier for as little 1/f noise as possible, while the enough bandwidth larger than 264 MHz is maintained. The input devices of the amplifier is designed to be biased at ground level for eliminating demand and hence disturbance of DC source. A pair of source followers serves as the output buffer for measurement purpose. With some modification, it can also function as DC level

shift for the succeeding variable gain amplifier whose DC offset cancellation circuit can prevent the DC offset nature of the mixer from impacting the whole system performance.

6.2.2 Simulation Results

The down-conversion mixer with baseband amplifier and output buffer is simulated in Agilent ADS. The even curves of conversion gain in Figure 49 show that this mixer is suitable for UWB applications. Figure 50 shows good noise figure in double sideband.

6.3 Consideration of Package and ESD Protection

As fabrication process deeply affects RF circuit performance, post-layout simulation with appropriate package model is vital to successful chip design. In addition, electro-static-discharging (ESD) protection is a critical issue in thin oxide process. Some key points are highlighted in this section.

6.3.1 ESD Protection

As MOS device shrinks with technology, the tolerance of the gate voltage goes down and the high potential at gate terminal easily pierces the thin oxide. Therefore, ESD circuits are imported as shown in Figure 51. Diode chain protection guides the tremendous charge to VDD or GND, and a large gate ground NMOS will break down once a large potential across the VDD and GND, and induces the charge in VDD flows through NMOS to GND.

The devices used in ESD have special restrictions. The gate ground MOS should avoid lightly-doped-drain which is common in deep submicron process. The distance between drain

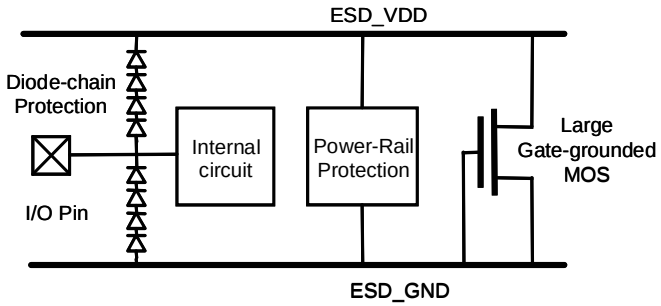


Figure 51. ESD protection schematic for package model.

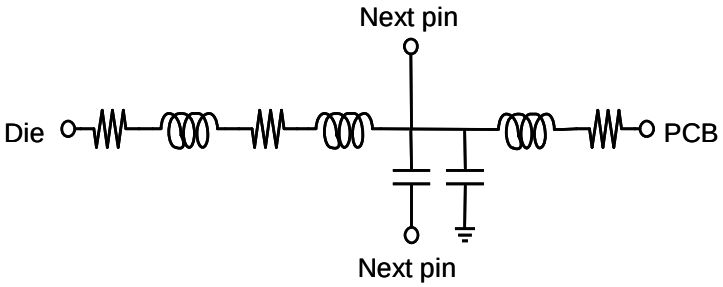


Figure 52. Package model.

contact and boundary of gate and diffusion must be large too sustain higher static charge. Contacts on guard ring are also prohibited because that makes the break down of ESD device harder. The ESD circuits provided by UMC ensure 3.6kV in human body mode (HBM) test but induce about 40fF nonlinear capacitance in each pad.

6.3.2 Package Topology

The package QFN20D is provided by SPIL and is applied to this design. The package model for bond-wire is built as shown in Fig 52. The issues of bond-wire include serial inductance and parasitic capacitance between pins. The serial inductance makes the DC supply a non-ideal AC ground while the capacitance between pins causes adjacent coupling. The serial inductance is about 1nH/mm with the length of bond-wire and high quality factor compared with on-chip inductor. The model provided by SPIL has details about 1nH serial inductance

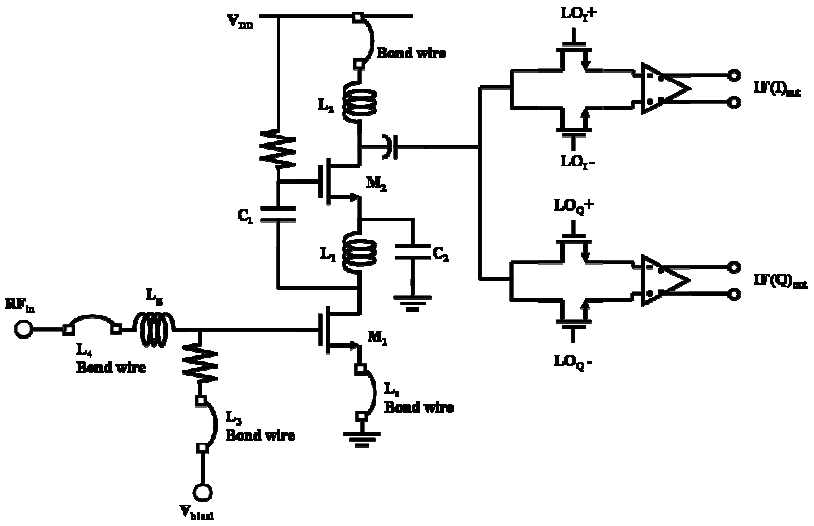


Figure 53. UWB receiver front-end circuit.

for each pin. For DC supply pins, especially VDD and GND, the 1nH parasitic inductor can change circuit performance or induce oscillation. However, the high Q nature of the bonding wires can replace the on-chip spiral inductors to improve the circuit performance. Since different pins have different inductance values, with maximum difference of 0.2 nH, detailed inspection on the package model is required before using it.

6.4 Circuit Implementation

A UWB receiver front-end referenced to the band group #1 of the Multi-Band OFDM with operation frequency between 3GHz to 5GHz is designed for the goals of low noise figure, low power, high gain, and wide bandwidth. As shown in Figure 53, the high-Q bond wires are fully used to reduce the chip area and improve the noise figure in this design. The load inductor of the first stage is chosen to resonate at 3.1 GHz with capacitance at the drain node of the transistor M_1, which includes the device parasitic and the capacitance between the bottom plate of C_1 and ground. The load inductor of the second stage is chosen to generate a resonance at 4.6 GHz. The resonance frequencies of the first and second stages together cover

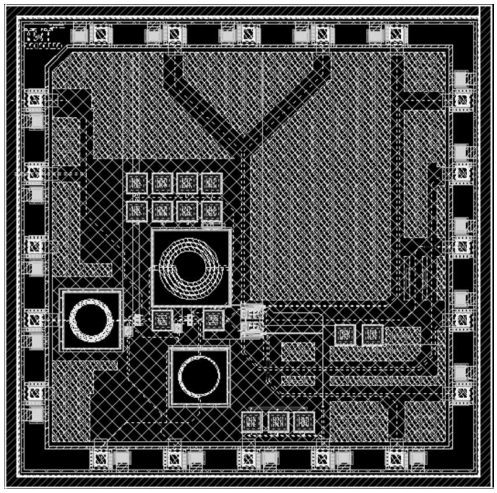


Figure 54. UWB receiver front-end circuit chip layout.

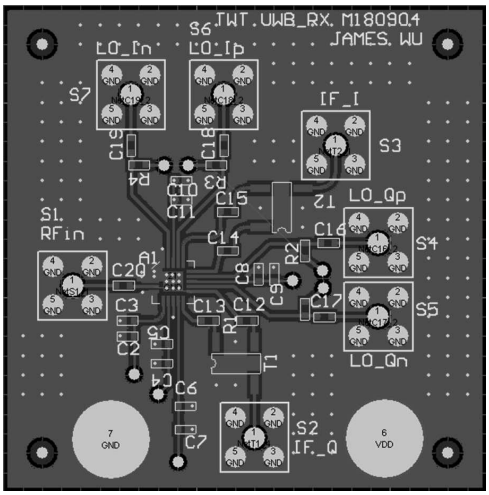


Figure 55. UWB receiver front-end PCB layout.

the 3-5-GHz bandwidth for UWB band group #1 applications.

The capacitance of capacitor C_1 is selected to be 4.92 pF for signal coupling and without suffering from severe parasitic. With simulation, the best gain flatness can be obtained while the value of capacitor C_2 is 39.36 pF. Since the LNA and mixers are integrated on chip, the original buffer stage at the LNA output is no longer required.

Figure 54 shows the layout of the receiver front-end. The die area is much reduced since the bond-wires are fully used to replace most of the on-chip spiral inductors. The PCB layout is shown in Figure 55. The RF signal path is arranged with the shortest distance and the

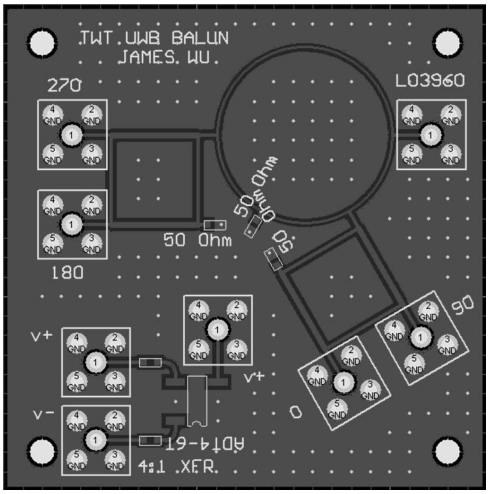


Figure 56. Balun for LO quadrature output.

differential LO signals are routed symmetrically for both I and Q. The transformers of 4:1 Ohm ratio are to be installed on the board for differential IF converting to single ended-output. Figure 56 shows the balun for LO quadrature output at 3960 MHz. The pattern is simulated with Momentum of Agilent ADS for 0°, 90°, 180°, and 270° outputs.

6.5 Simulation Results

The post-layout simulation was accomplished with Cadence SpectreRF simulator and Aglient ADS. Individual simulation of LNA and mixers are conducted first. As shown in Figure 57, a buffer circuit is added to the LNA for simulation. Figure 58 shows simulation setup and results of single mixer and two mixers in parallel. The individual simulations prepare for the integration of the LNA and mixers in the receiver front-end. Since there are three 528MHz-bands in the band group #1, each kind of test is run for all three bands. Figure 59 shows the double-sideband noise figure of the receiver is well below 3 dB. Since the receiver adopts direct-conversion architecture, the double-sideband noise figure is reasonable to represent the noise performance. The lowest conversion gain is 18dB as shown in Figure 60.

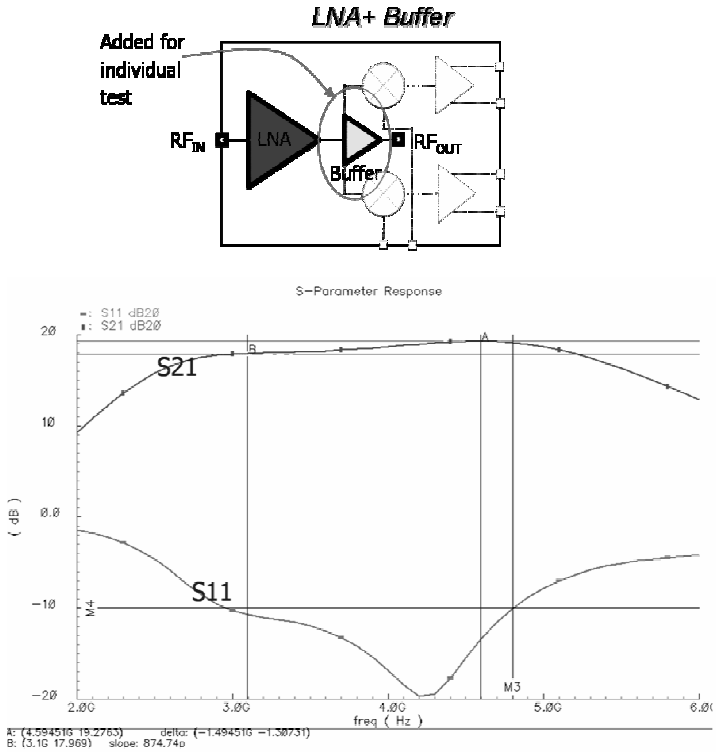


Figure 57. Individual simulation results of LNA circuit in RX package.

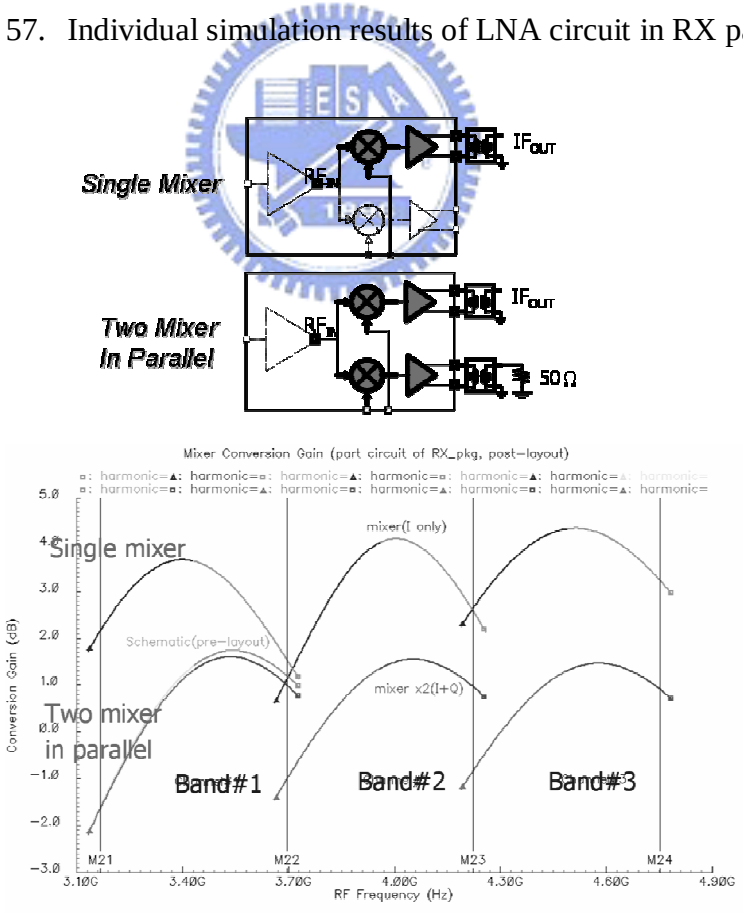


Figure 58. Individual simulation results of Mixer circuit in RX package.

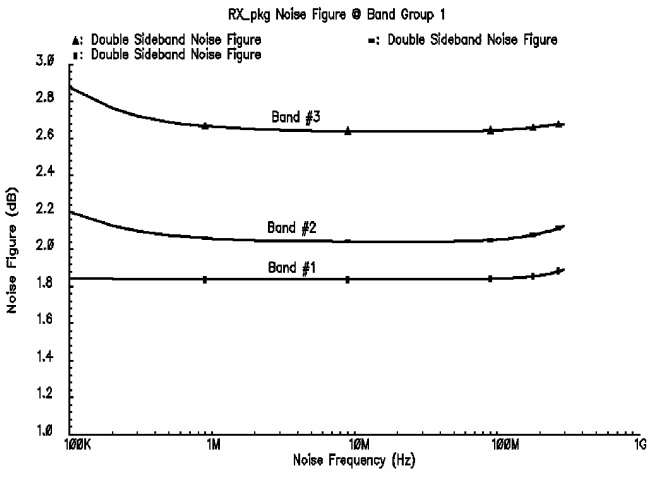


Figure 59. RX Simulation results- noise figure (double-sideband)

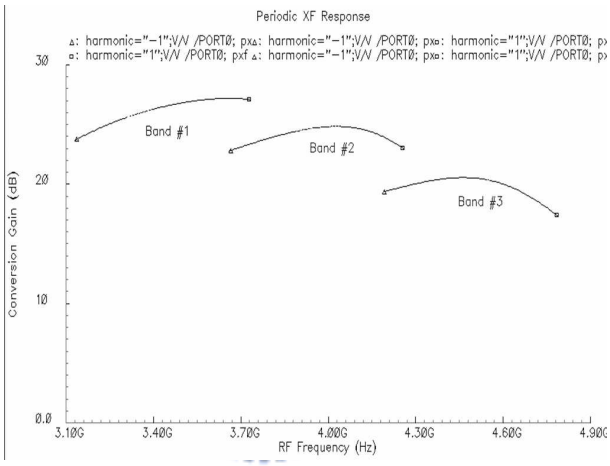


Figure 60. RX Simulation results- conversion gain

The gain curve tends to fall with higher band for the input impedance at the RF port of the mixers is lower at higher frequency band. A buffer between the LNA and mixers can improve that, but suffers from additional power consumption. Since the noise figure of the receiver is well below the specification, the gain difference can be compensated with the succeeding variable gain amplifier. Two-tone signals with 4.125MHz spacing are applied to the receiver to observe the input referred third-order intercept point (IIP3). One-tone test is performed to obtain the input referred 1dB compression point (IP1dB). The simulated IIP3 is higher than –30.4 dBm and the simulated IP1dB is better than -46.7 dBm, respectively, as

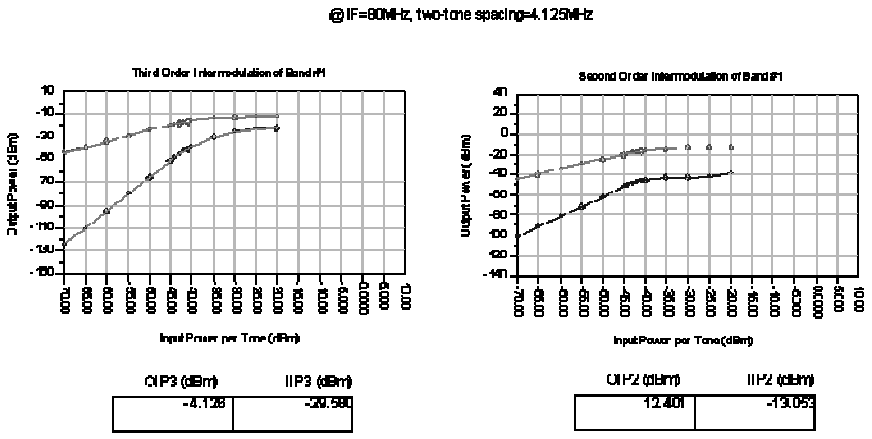


Figure 61. RX Simulation results- IP2 and IP3 at band#1

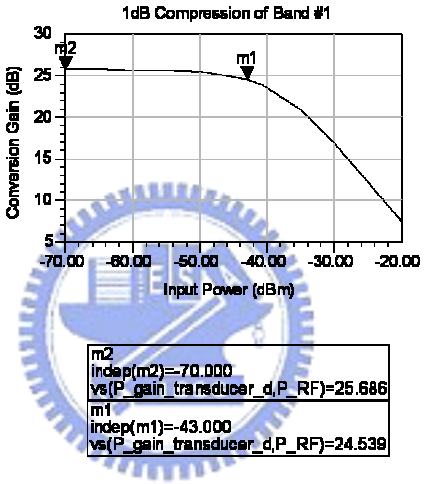


Figure 62. RX Simulation results- P1dB at band#2

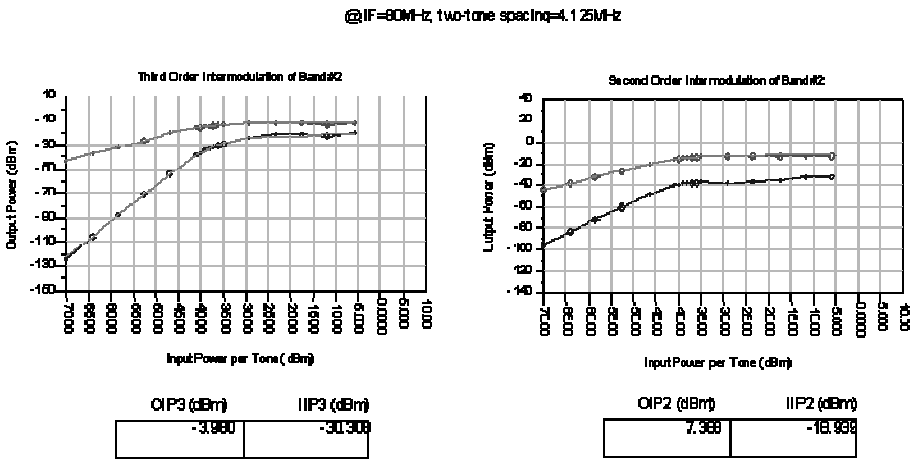


Figure 63. RX Simulation results- IP2 and IP3 at band#2

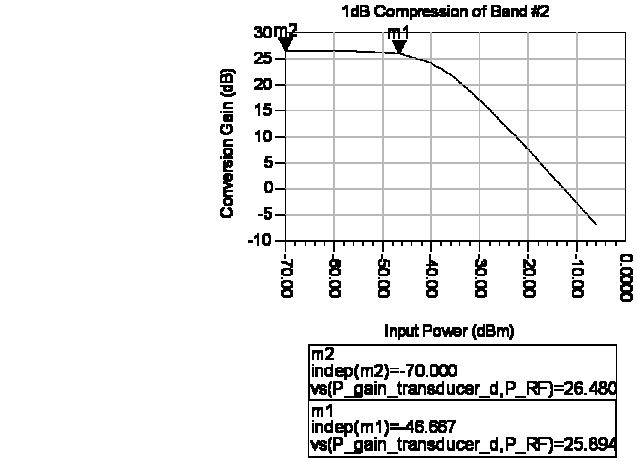


Figure 64. RX Simulation results- P1dB at band#2.

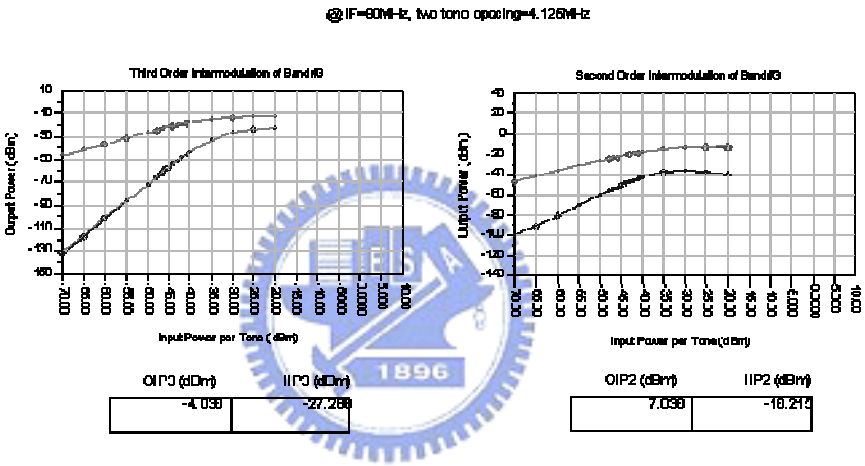


Figure 65. RX Simulation results- IP2 and IP3 at band#3.

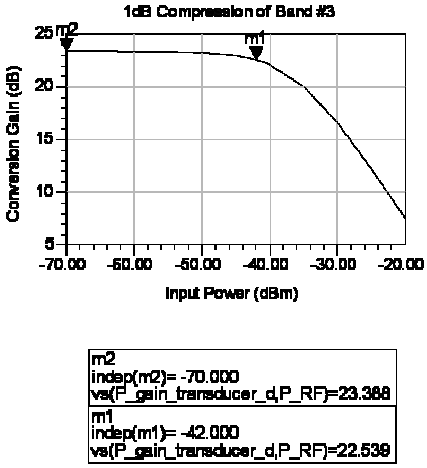


Figure 66. RX Simulation results- P1dB at band#3.

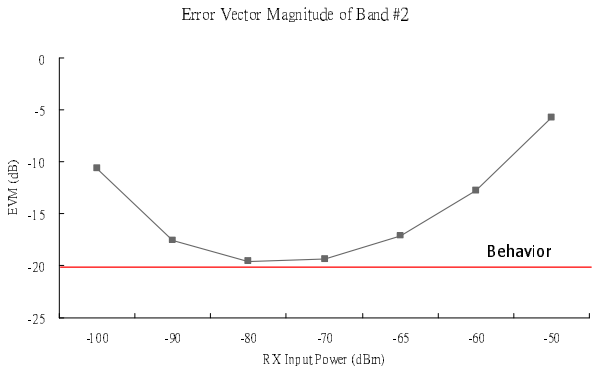


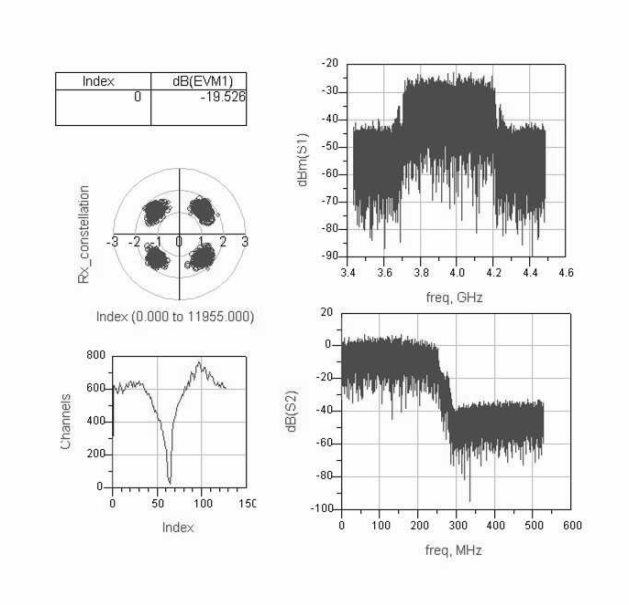
Figure 67. Summary of RF/Baseband co-simulation.

Table 4. Power consumption details of receiver front-end

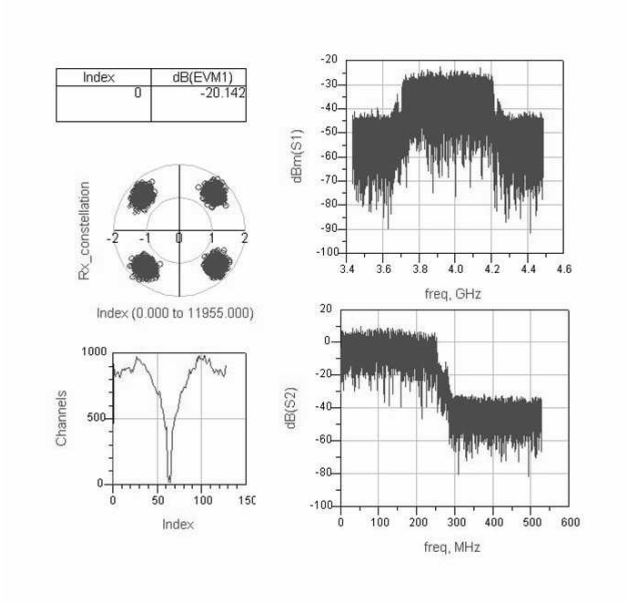
Component	Power Dissipation (mW)
LNA	8.5
Mixer(x2)	0
Baseband Amplifier(x2)	3.2
Buffer(x2)	9.6
Total	21.3

shown in Figure 61~66. The power dissipation of the whole receiver front-end including the output buffers is 21.3 mW as detailed in Table 4.

Figure 67 shows the summary of the circuit-level co-simulation of EVM with various input power of the receiver. The EVM goes higher as the input power goes below -90 dBm as well as above -65 dBm. The lower bound is limited by the sensitivity of the receiver and the upper bound by the linearity. Since the minimum sensitivity requirement of the band group #1 is -83.6 dBm, the receiver front-end can work well for this specification. When a complete version of algorithm-level of UWB baseband transceiver is available, the co-verification results will be closer to the real performance. Figure 68 shows a comparison of co-simulation results between the circuit-level RF front-end of this design and the behavior building block.



(a)



(b)

Figure 68. Comparison of co-simulation results: (a) with circuit-level RF front-end, (b) with behavior building block.

6.6 Summary

The proposed topology of low power UWB LNA with staggering tuning technique has been applied to the RF front-end for the UWB direct conversion receiver. The RF front-end performs low power, wide bandwidth and low noise. The system is verified by RF/baseband co-simulation. Implemented in 0.18-μm CMOS technology, the results demonstrate that the presented RF front-end is paving the way to a new generation of low power UWB applications. In addition, the design can be easily modified to fit other band groups of MB OFDM proposal.

Chapter 7

Conclusions

This thesis has presented a two-stage stacked topology employing staggering tuning technique for low power UWB LNAs. It has enabled the implementation of a 2.4-9.4 GHz low power LNA in a 0.18 μm CMOS technology. This novel topology has been applied to the RF front-end for the UWB direct conversion receiver which performs low power, wide bandwidth and low noise. In conclusion, the key contributions presented in previous chapters are summarized below.

7.1 Summary

A two-stage stacked topology employing staggering tuning technique has been presented for low power UWB LNAs in Chapter 3. The quality factors for circuit design and inductor selection are discussed. In addition, design optimization for the power-constrained stacked amplifiers in wide bandwidth applications is also presented. The LNA is put in the UWB system for verification in Chapter 4. The LNA circuit implemented in 0.18-μm CMOS process shows a 2.4-9.4-GHz bandwidth in Chapter 5. The amplifier provides a maximum forward gain (S21) of 9.7 dB while drawing 7.3 mW from a 1.8-V supply. A noise figure as low as 4.17 dB and an IIP3 of –3.5 dBm have been measured. In chapter 6, the novel topology of low power UWB LNA has been applied to the RF front-end for the UWB direct

conversion receiver. In the RF front-end, a wideband passive mixer is designed for the purpose of low power little flicker noise and high linearity after the LNA. A baseband amplifier biased at ground level is designed with consideration of low noise for compensating the gain loss of the passive mixer and consequently help improving overall noise performance of the receiver. The UWB receiver front-end referenced to the band group #1 of the Multi-Band OFDM with operation frequency range 3-5 GHz demonstrates low noise figure, low power, high gain, and wide bandwidth. It is also verified by a RF/Baseband co-simulation.

7.2 Recommendations for Future Work

The stagger tuning LNA employs on-chip spiral inductors which dominate the chip area. An optimization of the spiral inductors would help reduce the area and drive the circuit performance toward perfection. In addition, a tentative algorithm-level of UWB baseband transceiver is used to co-simulate with this RF front-end circuit design. When a complete version of algorithm-level of UWB baseband transceiver is available, the co-verification results would be closer to the real performance.

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1. Chang-Ching Wu, Mei-Fen Chou, Wen-Shen Wuen and Kuei-Ann Wen, “A low power CMOS low noise amplifier for ultra-wideband wireless amplifications,” accepted by 2005 IEEE International Symposium on Circuits and Systems, Kobe, May 2005.

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Vita

Chang-Ching Wu

jameswu.eic91g@nctu.edu.tw

Education

M.S. Degree in Electronics and Electro-Optical Engineering, National Chiao Tung University 2005

B.S. Degree in Mechanical Engineering, National Central University 1992

Experience

Applied Materials Taiwan	Senior Engineer ~ Lab Supervisor	1999~2003
TSMC-Acer Semiconductor	Engineer ~ Associate Manger	1994~1999
Military service in the Army	Platoon Leader / Ordnance Officer	1992~1994