

Chapter 1:

Introduction.....	1
1.1 General Description for Flash Memory.....	1
1.2 Flash Memory Application.....	3
1.2.1 Communication Applications.....	3
1.2.2 Consumer Market.....	4
1.2.3 Smart Cards.....	4
1.2.4 Automotive Applications.....	5
1.3 NAND or NOR Flash.....	5
1.4 The Trend of Future Application for Flash Memory.....	8
1.5 Low power consumption approach.....	9

Chapter 2:

Design Concept and Approach.....	11
2.1 Design Background.....	11
2.2 Other Approach.....	11.
2.3 Reading Operation of Flash Memory.....	12
2.4 Design Approach.....	13
2.4.1 Bit Line Pre-charge Scheme.....	13
2.4.2 Data Sensing.....	15
2.4.3 Data Valid.....	16

Chapter 3:

Novel Sense Amplifier Operating Introduction.....	18
3.1 Low Power Dissipation Architecture Sense Amplifier Sensing Scheme...18	
3.2 Sense Amplifier Architecture.....	19

3.2.1 Bit Line Pre-charge Path.....	21
3.2.2 Reference Current Path.....	23
3.2.3 Data Sensing.....	25
3.2.3.1 Data “1” Sensing.....	25
3.2.3.2 Data “0” Sensing.....	28
3.3 Pre-charge Path Consideration.....	29
3.3.1 Pre-charge Path Consideration Versus Performance.....	29
3.3.2 Pre-charge Path Consideration Versus Process Condition.....	31
3.4 Low Power Supply Voltage Sense Amplifier Architecture Introduction...33	

Chapter 4:

Simulation and Silicon Result.....	35
4.1 Test Chip’s Information.....	35
4.2 Simulation Result for Low Power Consumption Architecture.....	41
4.2.1 Simulation Result for Access Speed.....	41
4.2.2 Simulation Result for Access Power Consumption.....	52
4.3 Silicon Result.....	57
4.4 Simulation Result for Low Power Supply Sense Amplifier.....	57
4.5 Layout.....	59

Chapter 5:

Conclusion.....	61
Reference	63

List of Figures:

Figure 3.1: Sense Amplifier architecture.....	19
Figure 3.2: Bit line pre-charge control logic.....	20
Figure 3.3: Timing waveform for bit line pre-charge logic.....	20
Figure 3.4: Bit line pre-charge path.....	21
Figure 3.5: Reference current path.....	24
Figure 3.6: Buffer for sensing device.....	26
Figure 3.7: Schematic for bit line pulled down.....	26
Figure 3.8: Control logic for turning off reference current.....	27
Figure 3.9: Schematics for data “0” latch.....	28
Figure 3.10: Sense Amplifier architecture for low power supply.....	33
Figure 3.11: Pre-charge path for low VDD application.....	34
Figure 4.1: Simplified circuit of word line boost.....	36
Figure 4.2: The difference for speed and word line level between with word line boost and without word line boost.....	37
Figure 4.3: Word line bias after boosted. (VDD=1.6, 1.8 and 2.0v).....	38
Figure 4.4: Array architecture.....	39
Figure 4.5: Access path.....	40
Figure 4.6: Timing waveform of word line and bit lines bias for different cell data those related to sense amplifier active signal (SE).....	42
Figure 4.7: The waveforms for bit line bias; flash cell current and source line.....	43
Figure 4.8: Simulation waveform for word line, bit line, source line and the bit line pre-charge signal.....	44
Figure 4.9: Trip point of the sensing device.....	46
Figure 4.10: Trip point of the voltage detector (INV7).....	46

Figure 4.11: The trip point comparison between the sensing device and INV7.....	47
Figure 4.12: Timing waveform under SF process condition, 1.6v, -45	47
Figure 4.13: Waveform under SF, 1.4v and 125	48
Figure 4.14: Trip point under different process corner.....	49
Figure 4.15: Timing waveform under FS process condition, 1.6v, 125	50
Figure 4.16: Icell versus Iref under 1.8v and 1.6v.....	51
Figure 4.17: Sense amplifier turned off signals for different data pattern.....	52
Figure 4.18: Waveform for power dissipation.....	53
Figure 4.19: Bit line pre-charge waveform for low power supply SA.....	58
Figure 4.20: Test chip layout.....	60
Figure 4.21: Layout for the proposed sense amplifier.....	60



List of Tables:

Table 1.1: Comparison between the proposed sense amplifier and conventional design	10
Table 1.2: Comparison between the proposed sense amplifier and prior art.....	10
Table 2.1: Simulation result of prior art.....	12
Table 4.1:Read operation active power dissipation.....	54
Table 4.2: Read operation access speed for access “0”.....	55
Table 4.3: Read operation access speed for access “1”.....	56
Table 4.4: Silicon result for access speed. (read “1”).....	57
Table 4.5: Silicon result for read active power dissipation.....	57
Table 4.6: Simulation result for low power supply architecture.....	59

