國立交通大學

電機資訊學院電子與光電學程

碩士論文

一個具有電流匹配之新電荷泵與低寄生雜頻之互補式金氧半 5-GHz 頻率合成器

A Low Spurious Tones of 5-GHz CMOS Frequency Synthesizer with New Current-Match Charge Pump

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碩 士 論 文

A Thesis
Submitted to Degree Program of Electrical Engineering and Computer Science
College of Electrical Engineering and Computer Science
National Chiao Tung University
In Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in
Electronics and Electro-Optical Engineering
June 2004
Hsinchu, Taiwan, Republic of China

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摘要

本篇論文是用台灣積體電路 0.18um CMOS 製程來實現一個 5-GHz 擁有低寄生雜頻之良好特性的頻率合成器。整個電路包含兩個具有良好電流匹配的電荷泵，能有效的降低寄生雜頻。整個迴路所產生的寄生雜頻能有效的抑制在小於 -69.52dBc。

此頻率合成器也搭配加上一個佈局面積較小的高速除法電路(÷2)，此架構能比一般使用電感所組成的除法器擁有較少的花費。而這頻率合成器的輸出是以正交相位產生四個輸出，可應用在 IEEE 802.11a 之 RF 通訊協定的傳輸與接收器上!

整個電路最高工作在 5.62-GHz，且整個迴路最快能在 13.5uS 達到穩定。此頻率合成器的雜訊也壓制在小於 -107dBc。整個頻率合成器工作在 1.8 伏特與可程式控制除法器工作在 1.4 伏特時所產生的功率消耗小於 18.8mW。

A Low Spurious Tones of 5-GHz CMOS Frequency Synthesizer with New Current-Match Charge Pump

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Abstract

The thesis use TSMC 0.18um CMOS process to implement a 5-GHz frequency synthesizer that has perfect characteristic of low spurious tones. In this synthesizer which includes two perfect current-match of charge pump and they reduce spurious tones validly. The spurious sidebands at the center of adjacent channels are less than -69.52dBc.

The frequency synthesizer collocate a small layout area of divide-by-2 divider, which structure of layout area and cost are smaller than other structure which like inductances loading type divider. The quadrature phase output of synthesizer can support IEEE 802.11a transceiver. The chip working frequency reach 5.62 GHz, and the loop settling time was small than 13.5uS. The frequency phase noise is restrained at -107dBc@1MHz. The chip total power is 18.8mW based on 1.4V power supply for program counter and swallow counter and 1.8V power supply for other block.

誌　　謝

首先，我要感謝我的指導教授 吳重雨教授並獻上我最誠摯的謝意。 感謝吳老師在我研究所兩年半的期間，帶領著我一窺混合積體高頻電路設計研究的博大精深與奧妙，並且在學習的旅程上不斷的給予我指導與啟發。讓我受益良多!

其次，在這三年內，承蒙揚智科技的同意得以進修，在此感謝幫助過我的同仁給予我的支持與鼓勵。特別是洪衛周部經理與朱允康經理，因為有了他們兩位的支持才得以順利完成研究所的學業。

另外，我要感謝積體電路與系統實驗室的助理、學長、同學、以及學弟妹們，特別是周忠昀及王文傑。感謝他們幫忙我解決課業的疑問、處理學校的雜務以及協助實驗過程的種種，並且參與此篇論文的討論並適時提供寶貴意見得以使其順利完成。

最後，我要感謝我最敬愛的父母、親愛的妻子、家人和朋友，感謝他們給予我的關懷與照顧，使我在人生的過程裏得到快樂、健康與幸福。

僅以此篇論文獻給所有關心我的每一個人。

許德賢 2004.12

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CHAPTER 1

INTRODUCTION

1.1 Background

The growing of the wireless LAN market has generated increasing interest in technologies that will enable higher data rates and capacity than initially deployed system. There are much advantages of application in wireless LAN communication, so the entire world of the electronics industries researches high frequency circuit is very hard. Much kind of effect has devoted to the integration of such circuit in low cost technology in order to reach the goal.

Being intended for mobile operations, the radio transceiver has a limited power budget. In high frequency synthesizer, the high power consumption is mainly due to the first stages of the frequency divider that often dissipates half of the total power. So, the structure of divide-by-2 stage affects power disputation and chip area seriously. Anyway, costs have been driven down by technology improvement and better design. The rapidly growing market and ever emerging new applications create a high demand for a low cost, low power, high portability transceiver solution.

Many efforts are underway to increase the integration level of the transceiver. The ultimate goal would be a signal chip transceiver in a signal technology with a minimum number of off-chip components. This signal chip would act as an interface between the analog RF world and the digital baseband world.

In a conventional double conversion received signal spectrum is shifted down to the baseband in two steps. During the first step, a local oscillator signal at RF is mixed with the RF signal, shifting the signal to a fixed IF frequency. To achieve this, the RF LO needs to be tunable and the minimum frequency step must be smaller or equal to the channel spacing of the standard.

To find ways to realize low-phase-noise synthesizers with low Q components is a major challenge. One approach is to use a wide synthesizer control bandwith to couple a noisy on-chip oscillator to a very low phase noise crystal more closely than a conventional narrow band PLL so that the output is more dependent on the clean reference. The phase noise contribution from the on chip oscillator to the output close to the carrier within the synthesizer control bandwidth is thus suppressed. And the spurious tone contribution from charge pumps up with down charge current not equal. This in turn requires the synthesizer maintain its phase noise and spurious tone performance in the presence of components with deliver significant current and voltage perturbations to both the substrate ground and supply. Some loop bandwidth of PLL designed in narrowband that ignore loop settling time to decrease spurious level is not our objective.

As illustrate in Fig. 1.1, the RF front end need a high frequency synthesizer in transmitter and receiver to control mixer to generator internal carrier frequency. So designing a low phase noise and low spur frequency is very important. Charge pump up and down current equal to decrease spurious tone of the PLL path is important for this reason.

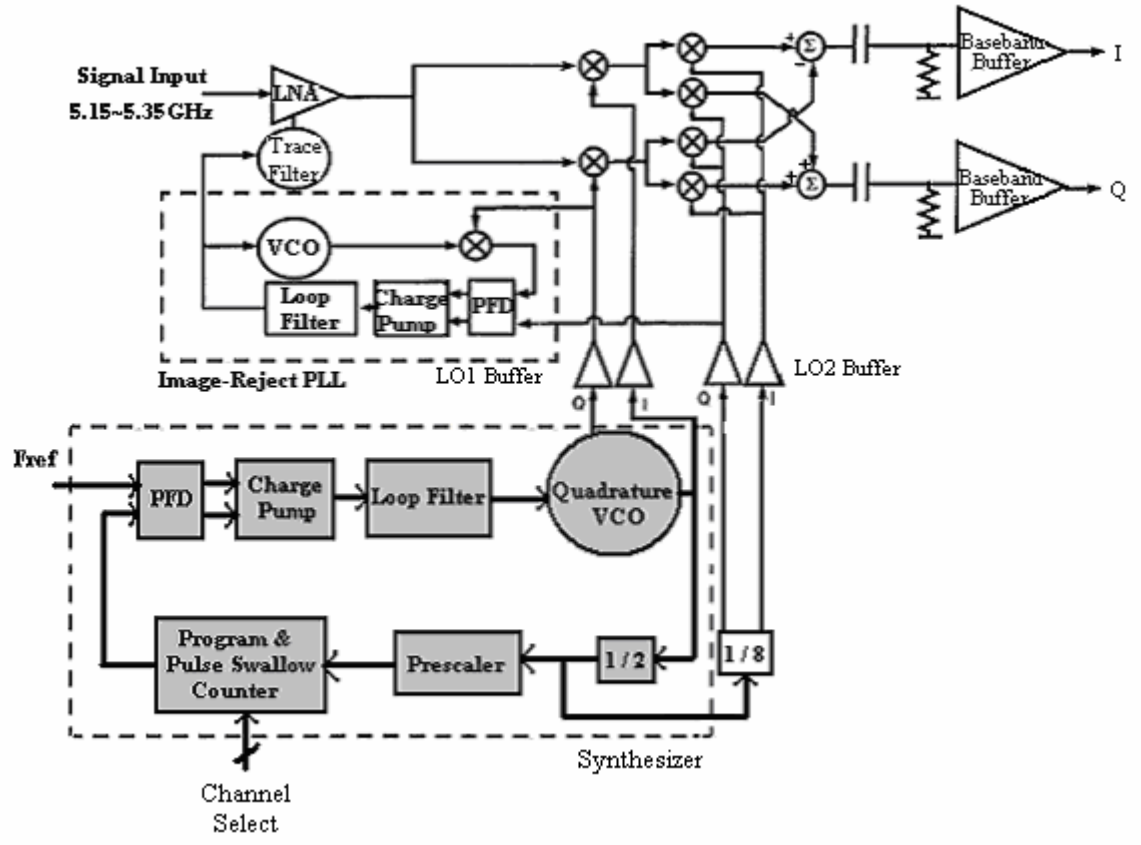


Fig. 1.1 Architecture for the 5-GHz CMOS WLAN receiver

1.1.1 High frequency synthesizer

The growing demand for wireless connectivity has motivated the industry to evolve beyond today's voice-based cellular services. Data-centric third-generation (3G) services now under development seek to provide substantially higher data rate, low noise interfere and wide channel bandwidth to supplement, and occasionally supplant, wired networks. At the same time, there is a constant desire to keep power consumption and layout size. Fortunately, continuing advances in integrated circuit technology have made possible the low-cost, compact implementation of transceivers capable of operating at 5-GHz carrier frequency with data rates competitive with established wired alternatives.

The applications of wireless communication device include cellular phones and wireless local area networks, transmitting either voice or data. For voice, example includes GSM, CDMA, PCS and DECT. For data, there are 802.11 WLAN, Bluetooth and Home RF. As illustrate in Fig. 1.2, the 802.11a standard operates in the 5-GHz unlicensed national information infrastructure band. And there are eight channels be selected to carrier data.

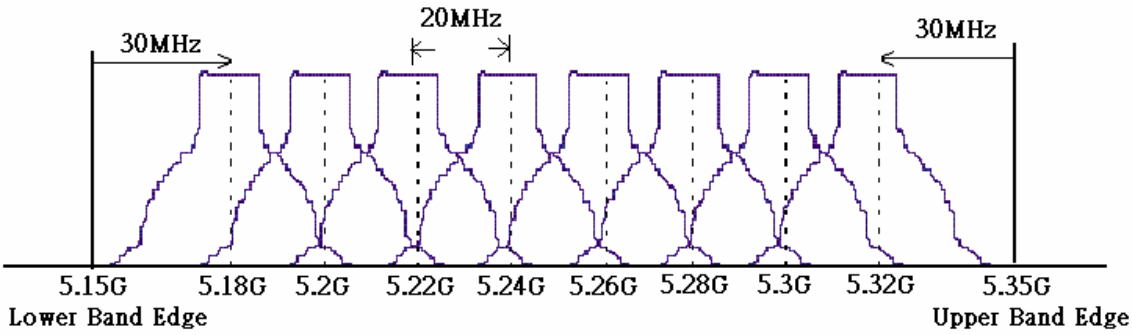


Fig. 1.2 Lower and Middle U-NII Bands: 8 Carriers in 200MHz Spacing

The frequency synthesizer illustrate in Fig. 1.3, usually implemented by a phase-locked loop (PLL), is one of the most critical blocks in terms of high frequency and average current dissipation since it operates extensively for both receiving and transmitting. The LO signals are generated by an integer-N frequency synthesizer. The loop employs a conventional phase-frequency detector (PFD) with the standard delay in the reset path to mitigate dead-zone effects arising from runt pulse. The PFD generating low-skew complementary representations of the *UP* and *DOWN* output that through low-pass filter to control VCO and generate the availability of accurate quadrature signals. The quadratue signals was divided by integer-N and backed to PFD.

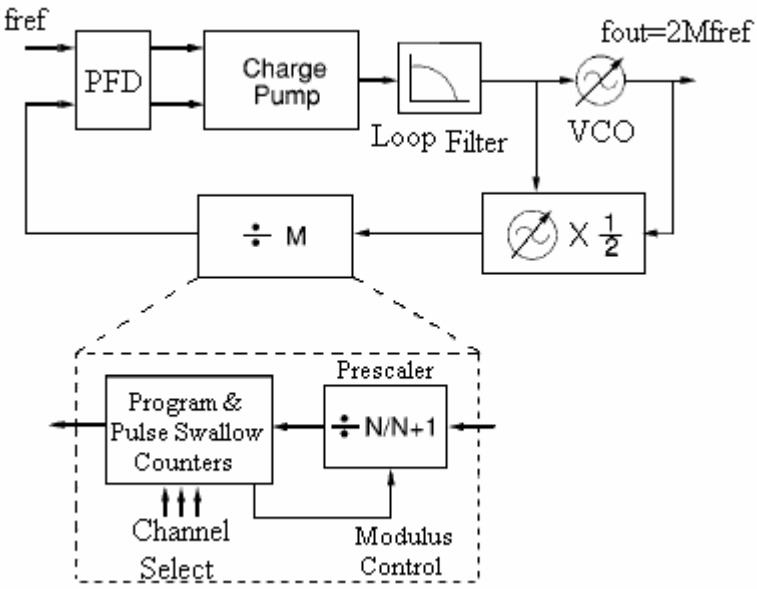


Fig. 1.3 Frequency synthesizer block diagram

1.1.2 The current mismatch of charge pump increases spurious tones

The ideal output spectrum of a frequency synthesizer should be a single tone at the desired frequency in order to provide the reference frequency for frequency translation. A single tone in the frequency domain is equivalent to a pure sinusoidal waveform in the time domain. The random and systematic amplitude and phase deviations from the desired value produce energy in the frequencies other than the desired frequency. When this energy is mixed with the received RF signal or modulated base-band signal, undesired sidebands are created. In Fig. 1.4 shows the phase noise and spurious tones are the two key parameters to measure the quality of a frequency synthesizer.

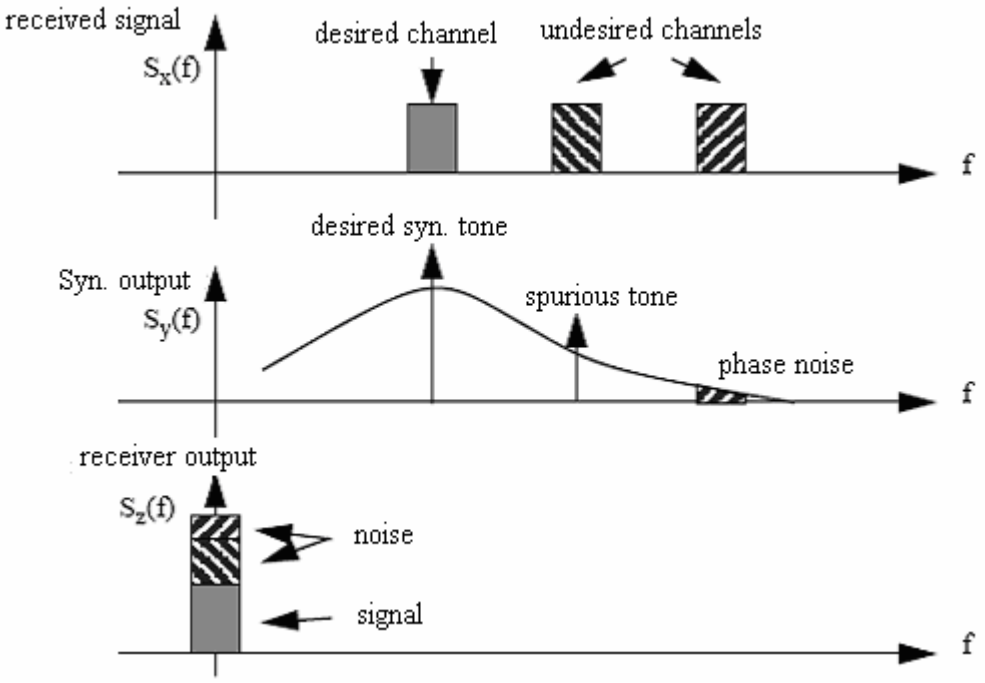


Fig. 1.4 Effect of phase noise and spurious tones in a receiver

In a receiver, the spurious tones and phase noise of the frequency synthesizer can mix with the undesired signal and produce noise in the desired channel. This reduced the sensitivity and selectivity of a receiver. Similarly, in a transmitter, the spurious tones and the phase noise of the frequency synthesizer can mix with the modulated base-band signal and produce undesired spectral emissions, increase adjacent channel interference, and reduce the modulation accuracy.

The spurious tones of frequency synthesizer will interfere with adjacent channel in RF receiver and produce undesired spectral emission in RF transmitter. What noise source that will cause spurious tones in PLL and how does to suppress these noise? The source of spurious tone is either noise coupling V_{LP}, or mismatch of charge pump current I_{cp}, is depicted as Fig. 1.5.

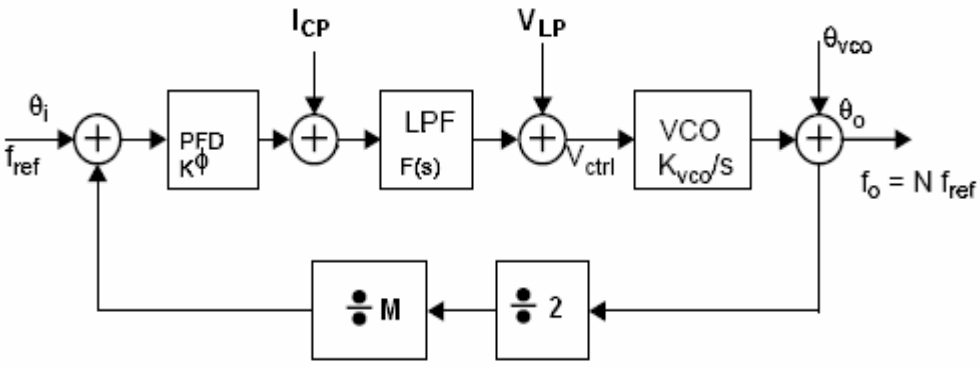


Fig. 1.5 PLL model for noise source that cause spurious tones

If the cause is noise coupling, either power supply noise or substrate noise, to control voltage of VCO then spurious tones can be mitigated from floor plan of whole chip, power plan and guard ring. If the spurious tones are caused from

mismatch of charge pump current then it can be mitigated from optimizing PLL loop or second order loop filter.

The transfer function of I_{cp}, due to current mismatch is

$$Wo / Icp = G(s)/(1+\beta(s)\cdot G(s))\mathrm{H} = s\cdot Kvco\cdot F(s)/(s+K(s)) \qquad (1\text{-}1)$$

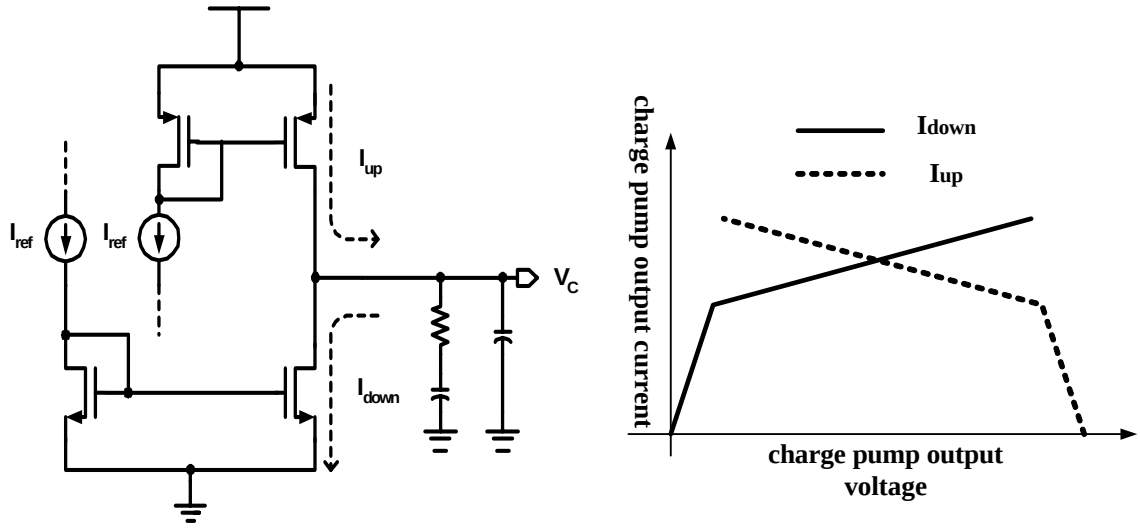
Where

$$G(s) = Kvco\cdot F(s)\, And\, \beta(s) = K\phi/(s\cdot 2M) \qquad (1\text{-}2)$$

It is a low pass function and the frequency of I_{cp} is at least 10 times large than K. Therefore optimizing K can attenuate the spurious tone.

Briefly, we can mitigate the spurious tones, that noise source is V_{LF}, by decoupling noise from power and substrate. And mitigates the spurious tones, that noise source is I_{cp}, by loop filter optimized and make perfect current match of charge pump.

When PLL is locked, reference and VCO frequency after divided by ($2\cdot M$) is equal and in phase. Theoretically, charge pump circuit is high impedance and charge and discharge current is zero while PLL is locker, but in order to solve the dead zone problem, the charge and discharge current, which is a non-zero and equal value, still applies for a moment, the charge pump circuit remains high impedance. In practice, voltages stored on the loop filter will vary depend on the channel selected, thus the charge and discharge current will mismatch due to channel length modulation of MOS, as depicted in Fig. 1.6.



(a) (b)

Fig. 1.6 (a) Sinking/Sourcing current in charge pump (b) Sinking/Sourcing current always mismatch unless charge pump output voltage is *1/2* power supply.

Although the dead zone problem has been solved but there is a new problem be happened. Current difference between I_{up} and I_{down} flow into or from the loop filter while PLL is locked. The current mismatch of the charge pump generates a phase offset, which increase spurious tones in the PLL output. But if the PLL loop bandwidth design in narrow band application will decrease the power lever of spurious tones, as illustrated in Fig. 1.7, the delta V is the control voltage of VCO after to compare with low bandwidth and high bandwidth. Assume K_{vco} be fixed, the delta V ripple amplitude is small which cause VCO output phase offset small, too. So, the spurious tones power level in narrow bandwidth was batter than high frequency bandwidth. But narrow bandwidth caused loop settling time to become slow.

The spur level is

$$Spur\_level \propto Kvco \cdot Vctrl / Wclk \qquad (1\text{-}3)$$

And the ripple affects the control voltage and spurious tones, as illustrated in Fig. 1.8.

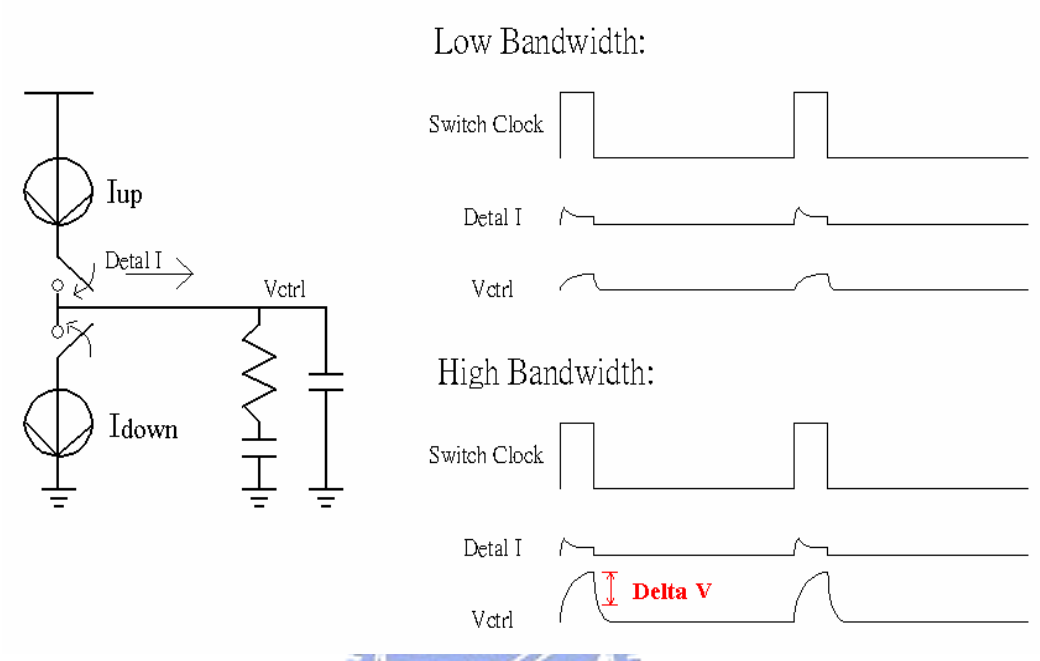


Fig. 1.7 Narrow bandwidth caused spurious tones

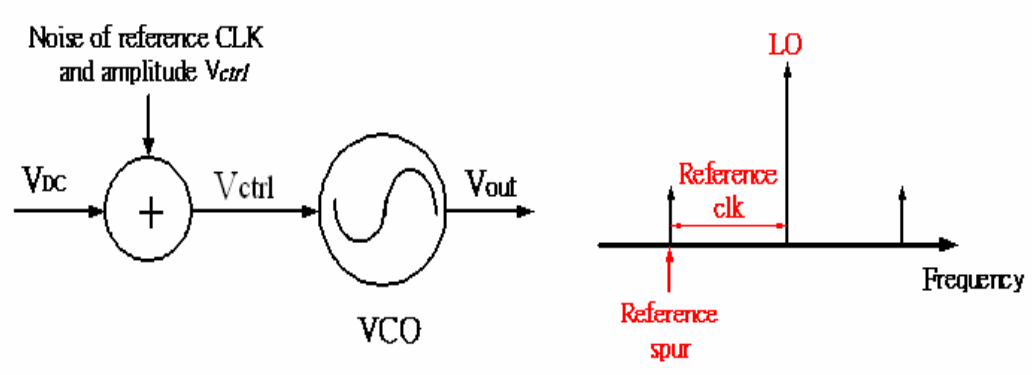


Fig. 1.8 The voltage of *Vctrl* control VCO and general spurious tones

1.1.3 The interplay of settling time and spur level

Wireless LAN systems apply in the 5~6 GHz band, such as HiperLAN II and IEEE 802.11a, are recognized as the leading standards for high rate data transmissions. And the specification of loop settling time must small than 16uS. As mention in section 1.1.2, the power level of spurious tones is affected with charge pump current mismatch and loop bandwidth. In narrowband design, assume VCO's gain K_{vco} is fixed and anyone of the K_f or I_{cp} is decreased than settling time increase. In wideband design, assume VCO's gain K_{vco} is fixed and anyone of the K_f or I_{cp} is increased than settling time decrease. So, loop bandwidth and loop settling time are tradeoffs. Anyway, in narrowband design will increase the layout area of low pass filter that is not batter for SOC application.

The PLL loop bandwidth is

$$K = Icp \cdot Kf \cdot Kvco / N \qquad \text{(N: Total divides value)} \qquad (1\text{-}4)$$

In this work, we choose large charge pump current to implement fast loop settling time.

1.2 Review current match charge pump

How does the synthesizer to decrease the level of spurious tones? The answer is focused to decrease the current mismatch of charge pump. Many structures of charge pump can solve the current mismatch problem after understand the reasons of spur be generated. Below listing, there are four reasons to make current mismatch in charge pump.

(1) Sourcing current I_{up} and sinking current I_{down} are not mirrored from the same current source path.

(2) Charge pump output range and channel length modulation cause charge pump current mismatch.

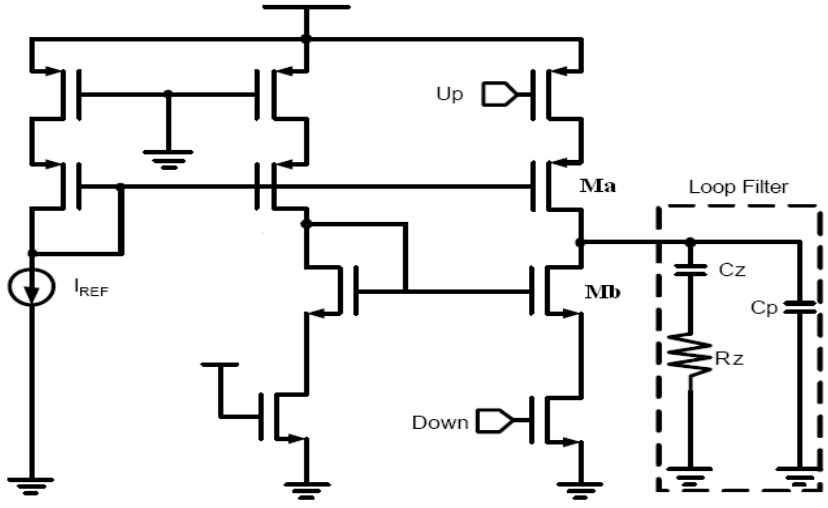
(3) Charge sharing happen in the output of charge pump to effect the VCO input voltage.

(4) The *Up/Down* signals from PFD to control the switches of the charge pump aren't switching at the same time.

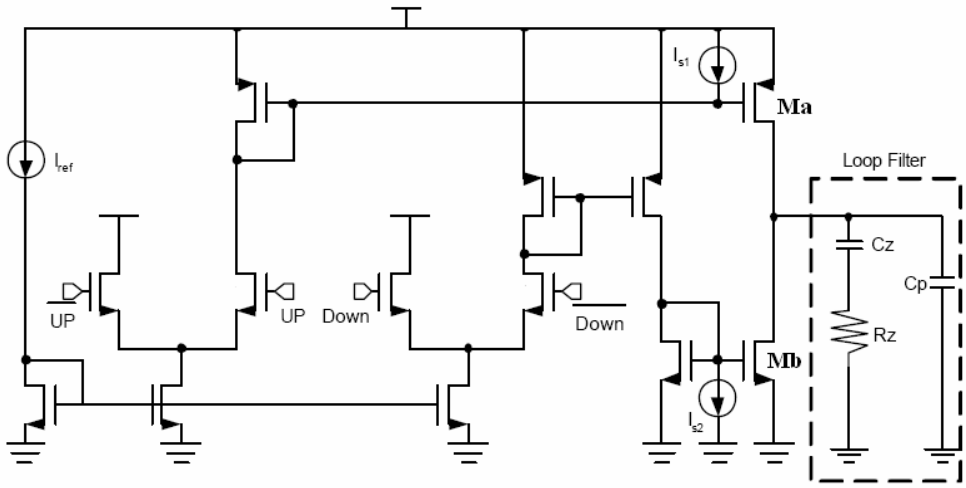
A perfect current match of charge pump needs those four conditions to apply in low spur frequency synthesizer. Review the structures of charge pump in the past, the circuit of "Current switching charge pump [15]" and "Current steering charge pump [16]" shown in Fig. 1.9 (a),(b). From those schematic, the drain current of sinking and sourcing will vary with drain voltage of M_a and M_b. The sinking and sourcing current difference is relatively large when the voltage of loop filter is near supply voltage or ground in those conventional charge pump circuit.

There are some conventional charge pumps circuits have been improved to

perfect current match on [17]-[18]. In Fig. 1.10 (a) [17], by using an error amplifier and reference current source, one can achieve a charge pump with good current matching characteristics. But the structure has some current mismatch problem when M_a and M_b have channel length modulation effect. In Fig. 1.10 (b) [18], it provided a charge pump with good current matching characteristics and a bootstrapping buffer forces the unused output in charge pump core to the same voltage as the main output [19]. The structure can't work in high output voltage range application.

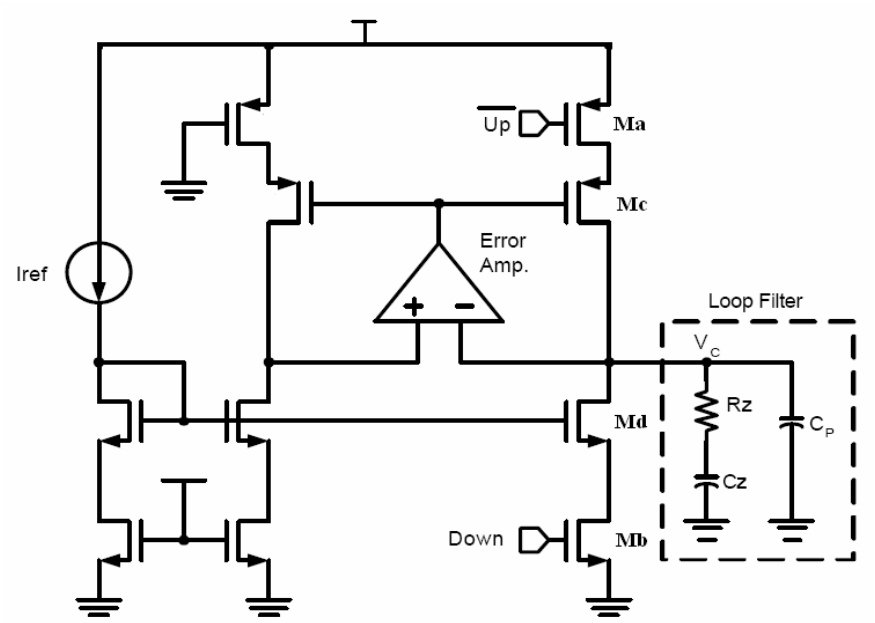


(a)

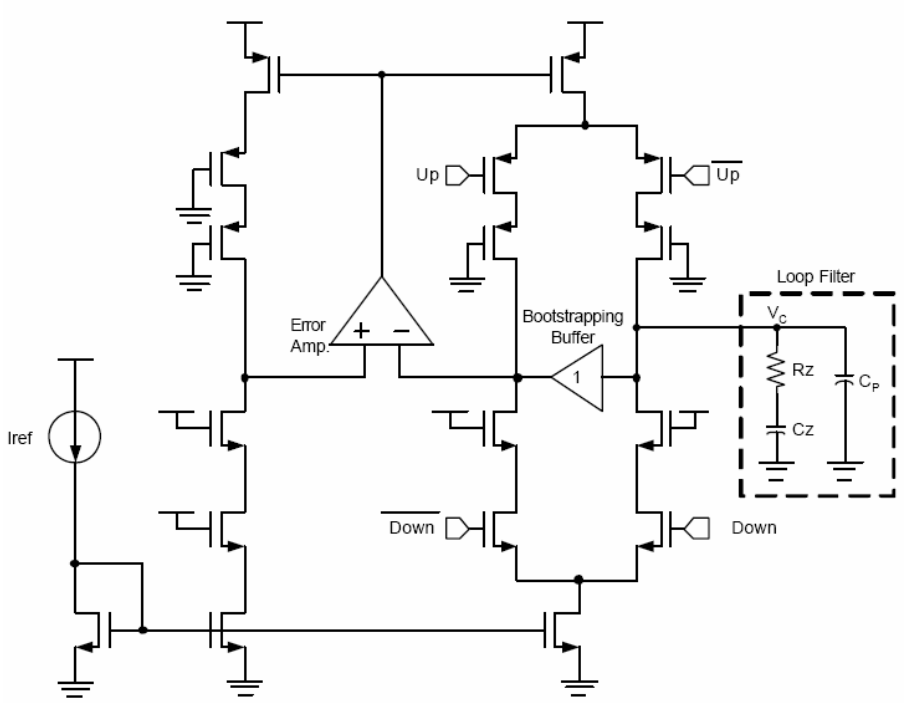


(b)

Fig. 1.9 Conventional charge pump circuits



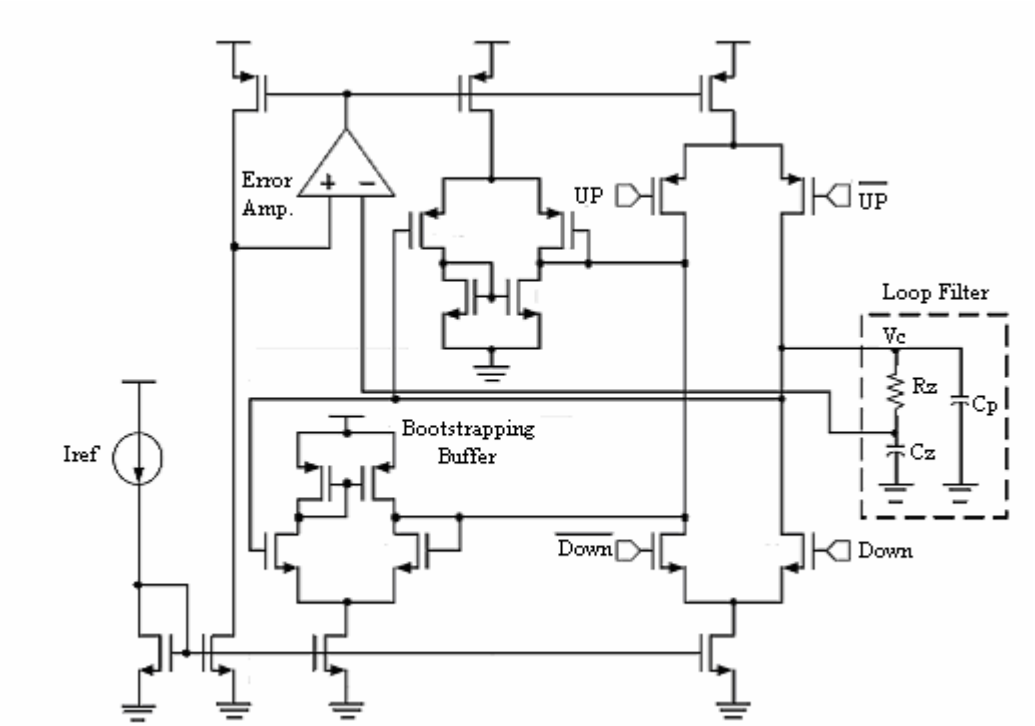
(a)



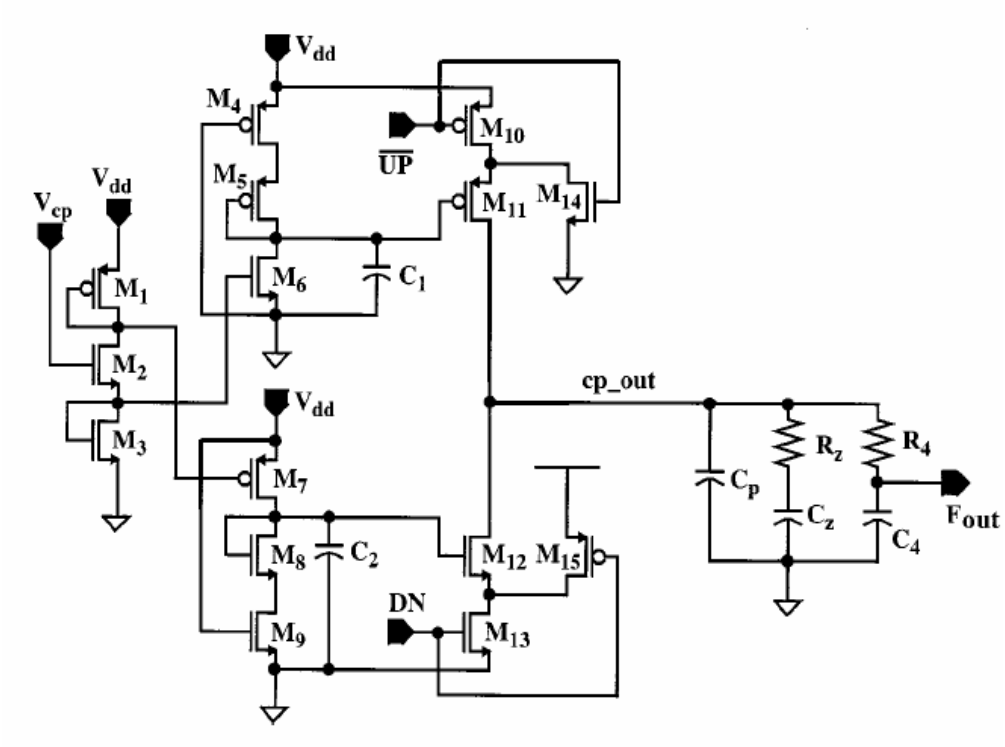
(b)

Fig. 1.10 Perfect current-match characteristic of charge pump circuits

Fig. 1.11 (a), the structure of charge pump has perfect characteristic of current-match. But the structure still has a problem about output voltage range cause current mismatch.



(a)



(b)

Fig. 1.11 The structures of current-match charge pump circuit

In [4], Fig. 1.11 (b) shows a conventional charge pump, the switches controlled by the *UP* and *DN* signals are directly connected between the current source transistors and output node. When the switches are turned off, the drain voltages of M_1 and M_2 are *VDD* and *0V*, respectively. When one of the switches is turned on, the charges on the capacitors in the low pass filter.

The structure of charge pump reduces this charge-sharing problem, but the up/down current has not to source from the same current path and it has serious problem of channel length modulation. We can see that current of M_{11} mirror from M_5 and the current of M_{12} mirror from M_8, but the current in M_5 and M_8 are not equal.

Anyway, the circuits of charge pump from Fig. 1.9 to Fig. 1.11 can't promise the current mirror can generate equal current to sink and source current of devices when the process has variation. Because the voltage of three thermals of current mirror device and sink/source current devices are not equal. In this work, there are two structures of charge pump circuit be implemented and compared at next chapter. Those charge pump circuit had perfect current match characteristic to decrease the power level of spurious tones.

1.3 Review 5-GHz frequency synthesizers

The role of the frequency synthesizer is to provide the reference frequency for frequency translation. There are many ways to implement a frequency synthesizer. We want the synthesizer to be able to generate a tunable frequency in the gigahertz range with low phase noise and low spurious tones using minimum power and small layout area. And the divide-by-2 divider dominated the power and layout area in frequency synthesizer.

In synthesizer architecture, a direct digital frequency synthesizer is best known for its fast switching and very fine frequency resolution. It can also easily be integrated because no off chip components are required. But due to technology limitations, it takes large power consumption to synthesize very high frequency directly. A direct digital frequency synthesizer function block diagram show in Fig. 1.12. However, the spectral purity of the direct digital frequency synthesizer is limited by the DAC speed and resolution because the finite resolution in quantization leads to inaccurate representation of the sinusoid and hence spurious outputs. And high power consumption is needed for high frequency operation.

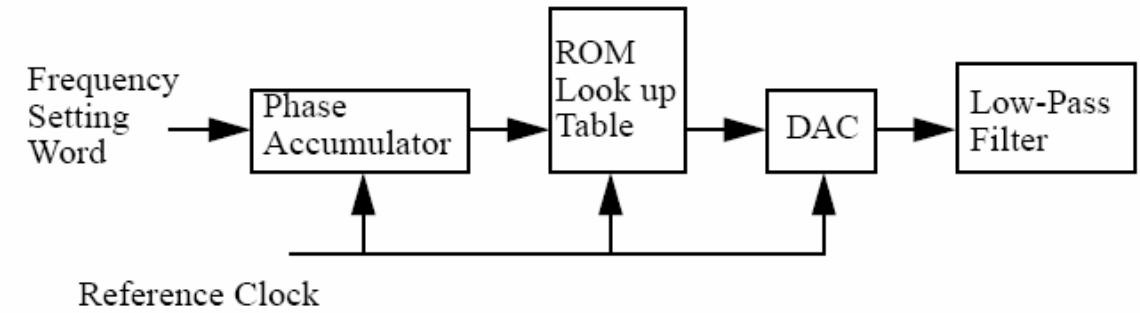


Fig. 1.12 Digital type of frequency synthesizer

Recently a new approach to a frequency synthesizer using a Delay-Locked Loop has been proposed [5]. A DLL is a PLL with the voltage controlled oscillator replaced by a voltage controlled delay line. Fig. 1.13 shows the block diagram of a frequency synthesizer with a DLL core. The advantage of the DLL based frequency synthesizer is that the jitter dose not accumulates from cycle as in the ring oscillator voltage and thus lower phase noise at close-in frequencies can be achieved. This approach is amenable to the integration of the frequency synthesizer because no high Q tank is needed.

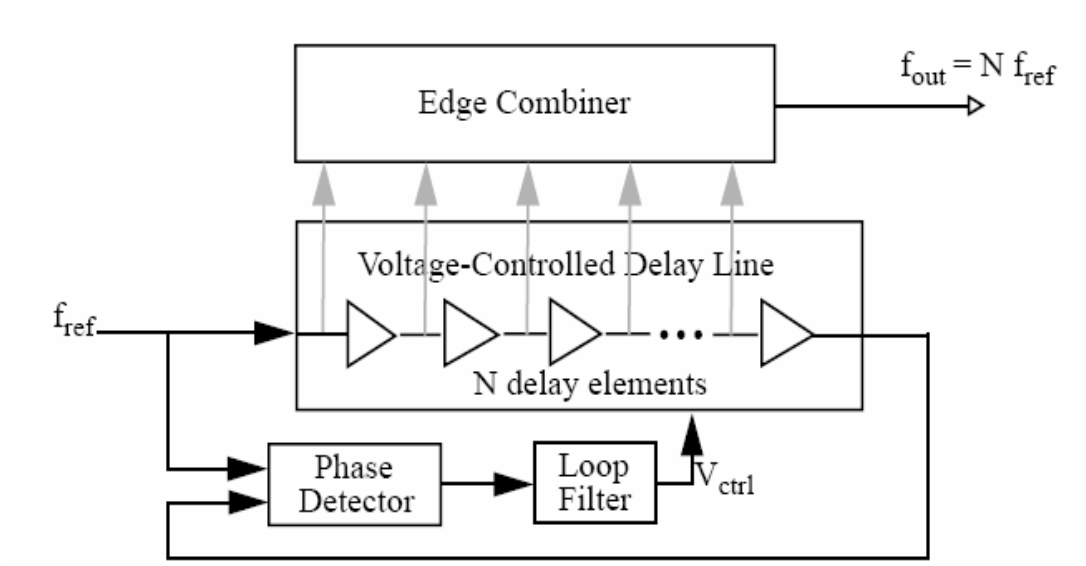


Fig. 1.13 DLL type of frequency synthesizer

Frequency synthesizer is to play the role of frequency conversion in RF front end circuit. It can be programmed to produce an exact frequency for up or down frequency. The greater parts of PLL-based researches are how does to decrease the effect from noise source. Because, noise effected the PLL's characteristic very

critical. We know the PLL noise source comes from “Phase Frequency Detector” and “Voltage Control Oscillator” and there are many technologies to solve low noise issue.

PLL base frequency synthesizer using charge pump type has some advantages about low power and low noise. So, there are three papers using the structure to implement 5-GHz frequency synthesizer and be presented in *IEEE journal of solid-state circuits*. In table 1, the parameters of those researches are showed up.

	[1]	[2]	[4]
Process	0.24um	0.25um	0.25um
Current match CP	NO	N.A	YES
Loop bandwidth	280KHz	30KHz	250KHz
Spurious tones	-45dBc	-70dBc	-69dBc
Settling time	N.A.	100uS	N.A.
Charge pump current	50uA	50uA	50uA
Power supply	1.5V / 2V	2.5V	1.5V
Total power	25mW	13.5mW	23mW
Chip size	1.6mm²	0.55mm²	N.A.
Off-chip low-pass-filter	No	Yes	Yes

Table 1 Review 5GHz frequency synthesizer

In [1], the power consumption of the synthesizer is significantly to reduce by using a tracking injection-locked frequency divider (ILFD) as the first frequency divider in the PLL feedback loop. On-chip spiral inductors with patterned ground shields are also optimized to reduce the VCO and ILFD power.

In [2], the adoption of dynamic dividers in CMOS PLL for multi-gigahertz

applications allows to reduce the power consumption substantially without impairing the phase noise and the power supply sensitivity of the PLL. The [2] had minimum spurious tones but loop settling time was too slow. The [2] had perfect power dissipation and small layout area but the loop bandwidth designed in 30 KHz.

In [4], a new charge-pump circuit is developed to reduce the current glitch at the output node. By incorporating a voltage doubler, the voltage dynamic range at the charge-pump output and thus the VCO control voltage range are increased.

In divide-by-2 architecture is very important in multi-gigahertz synthesizer; there are many ways to implement high speed divider. This work needs a high speed, smaller layout area and low power dissipation pre-divider between VCO and dual-modulus prescaler to gate 5.1GHz ÷*2* ~ 5.3GHz ÷*2* clock. So, the ÷*2* divider must operate at full speed and differential signals from VCO output frequency.

Conventionally, programmable dividers are implemented using a high speed dual-modulus prescaler along with low-speed programmable counters, which implement arbitrary division factors by “swallowing” pulses [7]. In [8], an asynchronous divider is presented in which pulse swallowing is accomplished by switching between different output phases of a ÷*2* stage implemented using a master-slave flip-flop.

The elimination of high-speed feedback loops around multiple flip-flops that would be present in a dual-modulus prescaler and reduced load on the VCO result in a higher maximum speed of operation and lower power consumption in a given technology. The high power consumption is mainly due to the first stage of the frequency divider that often dissipates half of the PLL total power.

The block most difficult to design is the first ÷*2* stage, which should operate at 5.3GHz or more. Fig. 1.14 (a) to (d) shows some published latches intended for high speed operation.

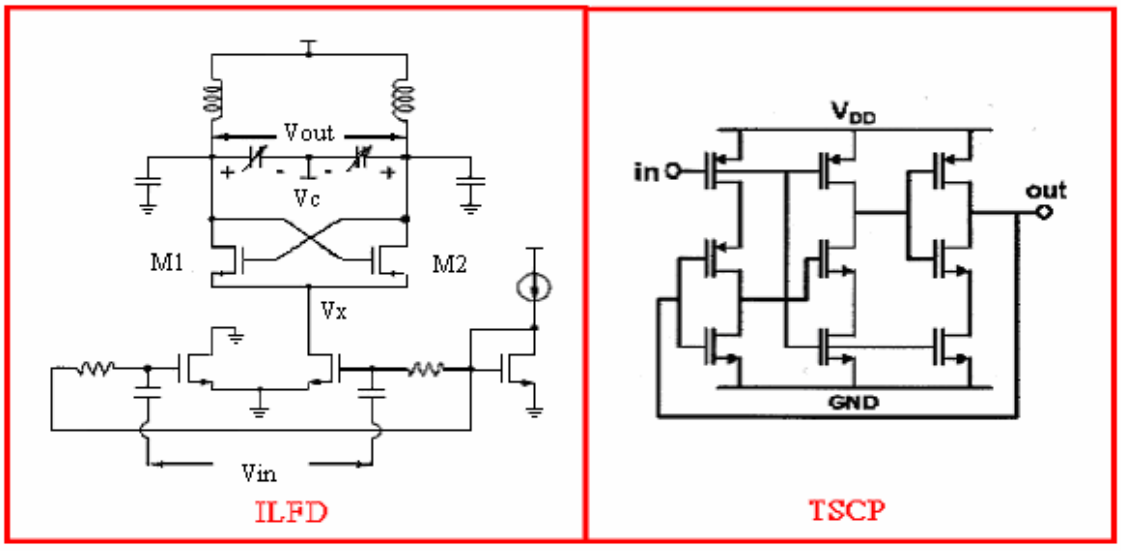
Fig. 1.14 (a) shows the schematic of the voltage controlled Injection-Locked Frequency Divider (ILFD) used in the frequency synthesizer. The incident signal (the VCO output) is injected into the gate of *M3* and is delivered with a sub-unity voltage gain to *Vx*, the common source connection of *M1* to *M2*. Transistor *M4* is used to provide a symmetric load for the VCO. The signal is fed back to the gates of *M1* and *M2* and is summed with the incident signal across the gates and source of *M1* and M2. As mentioned earlier the largest practical inductance L maximizes the locking range. However, reduction of power consumption demands maximization of the *LQ* product. The inductor has its largest value when the total capacitance that resonates with it is minimized. To reduce its parasitic bottom plate capacitance the inductor should be laid out with narrow topmost metal line. So, this divider needed large layout area and high cost.

Both a conventional CMOS latch and a single-phase latch is TSCP. As illusion in Fig. 1.14 (b), its bandwidth had been dominated too slowly for our purposes they have a large input capacitance due to the parallel connection of PMOS and NMOS gates. Due to its lower mobility and larger threshold voltage, the PMOS transistor contributes little to the current drive and much to the capacitances, considerably slowing down the circuit. The latch proposed uses TSCP in the clock path that *25%* duty cycle of the output signals is less convenient for phase switching. Another disadvantage of this structure is not differential signals path, but its layout area is

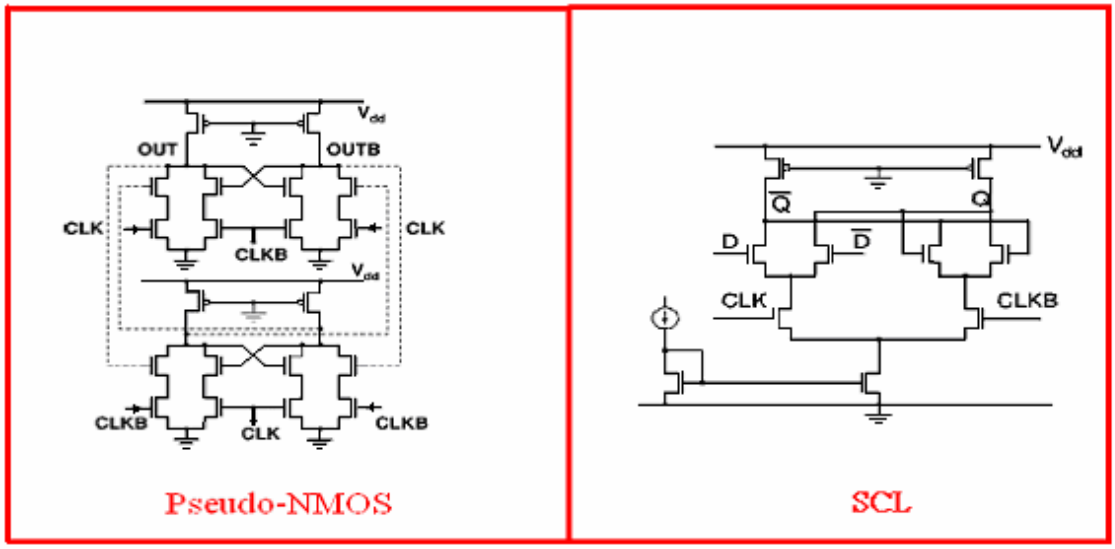
very small.

The source-coupled latch Fig. 1.14 (d) has a reduced output swing that facilitates high speed, but due to the stacking of many devices it cannot be accommodated in the intended low supply voltage. The SCL structure allows higher operating frequency, but burns more power.

Fig. 1.14 (c) shows a Pseudo-NMOS D-flip-flop (DFF) whose outputs are connected back to its inputs (show in dashed lines) to form a *÷2* stage. NAND gates are used to form the latch since they enable a compact layout where node parasites can be minimized. Form simulations, the *÷2* circuit were found to operate satisfactorily over process and temperature variations at 6GHz while operating from a 1.8V supply and TSMC 0.18um process. And the *÷2* circuit's layout area was small than Fig. 1.14 (a), (b) and (d).



(a) (b)



(c) (d)

Fig. 1.14 Divider structure (a) IFLD (b) TSCP (c) Pseudo-NMOS (d) SCL

The four types of dividers were being compared about power consumption and layout area. The IFLD structure has maximum layout area more than other but it has least power consumption. The SCL structure has maximum power consumption more than other. Anyway, the table 2 has some parameters about those dividers.

	[1]	[2]	[3]	[4]
Divider Structure	**ILFD**	**TSCP**	**Pseudo-NMOS DFF**	**SCL**
Power Supply	**1.5V**	**2.5V**	**2.5V**	**1.5V**
Process	**0.24um**	**0.25um**	**0.25um**	**0.25um**
Layout Area	**0.186mm²**	**0.05 mm²**	**0.09 mm²**	**0.12 mm²**
Divider Power	**0.8mW**	**6.25mW**	**26mW**	**10.5mW**

Table 2 Divider parameters compared

Anyway, the low spur, low power consumption, small layout area and fast settling time are our design feature. In the work, those characteristics are implemented.

1.4 Motivation

In RF transceivers, frequency synthesizer is one of the key components. Modern digital wireless system applications have demands on stringent specification, such as narrow channel spacing, large output power, high sensitivity and low bit error rate. So, a frequency synthesizer must have several advantages like low phase nose, low spur, fast setting time, lower power consumption and small layout area.

How does to design a high frequency, fast settling time and low phase noise synthesizer? Several import circuit to increase performance for synthesizer be present in this work. For example: a perfect current matching charge pump decrease spur noise, a 5-GHz of quadrature output voltage control oscillator, high speed and small layout area divider and programmable integral N feedback divider. All the blocks have been researched, designed, simulated and testing in this work.

Therefore, this thesis focuses on implementing the new circuit of current-steering charge pump, which incorporates with concept of perfect current matching. The new circuit of charge pump suffers no program of clock feed through and charge sharing, and has the perfect current matching characteristics. It is implemented in 5GHz CMOS frequency synthesizer.

1.5 Main results and organization

This thesis implements a new perfect current match of charge pump circuit in a 1.8V and 5GHz 0.18um CMOS frequency synthesizer. The spurious sidebands at the center of adjacent channels are less than -69.52 dBc. The PLL has a bandwidth of 250 KHz and a phase noise of -107 dBc at 1MHz. The PLL loop settling time is 13.5uS. The total power consumption is 20.8mW based on 1.8V power supply. And the total power consumption is 18.8mW based on 1.8V power supply with 1.4V power supply for PFD, program counter and swallow counter.

The thesis is organized as follows. In chapter 2, the fundamentals of frequency synthesizer include the synthesizer architecture, reason, circuit, simulation results and their advantages and disadvantages are discussed. In chapter 3, presents experimental results, compared the results and discussion. In chapter 4, concludes the thesis with a summary and future work.

CHAPTER 2

CIRCUIT ARCHITECTIRE AND SIMULATION RESULTS

In the previous chapter that propose wideband PLL architecture to implement a high performance frequency synthesizer with noisy on-chip components. In the chapter that also discusses the PLL design fundamentals, optimization of the loop bandwidth and pointed out the optimization of the loop bandwidth depends on the noise spectrum of each individual noise source. The important of the discusser are the structure of the current match charge pump and high speed frequency divider is chosen which has the trade off about power dissipation and layout area.

Anyway, in this chapter the circuit design of each block in a PLL will be discussed. The most important block is the integrated quadrature VCO and perfect current match charge pump. And the phase/frequency detector, loop filter, and frequency divider are also important in realizing a high performance frequency synthesizer. So, architecture of every block will be analysis, design and simulate detail.

2.1 Phase-Locked Loop Design Fundamentals

2.1.1 S-Domain model of PLL

The majority of all PLL design problems can be approached using the Laplace transform technique. All operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions.

Fig. 2.1 shows the basic block diagram of a PLL. The circuit is called a "Phase-Locked Loop" because the loop will automatically adjust the phase of the VCO output signal, θ_{out}, and synchronize the VCO output signal to the reference signal. After locked at the reference frequency, the signals can be represented as follows:

$$\begin{aligned} v_{out}(t) &= \sin\left(2\pi N f_{ref} t + \theta_{out}(t)\right) \\ v_{ref}(t) &= \sin\left(2\pi f_{ref} t + \theta_{ref}(t)\right) \\ v_{fb}(t) &= \sin\left(2\pi f_{ref} t + \theta_{fb}(t)\right) \end{aligned} \tag{2-1}$$

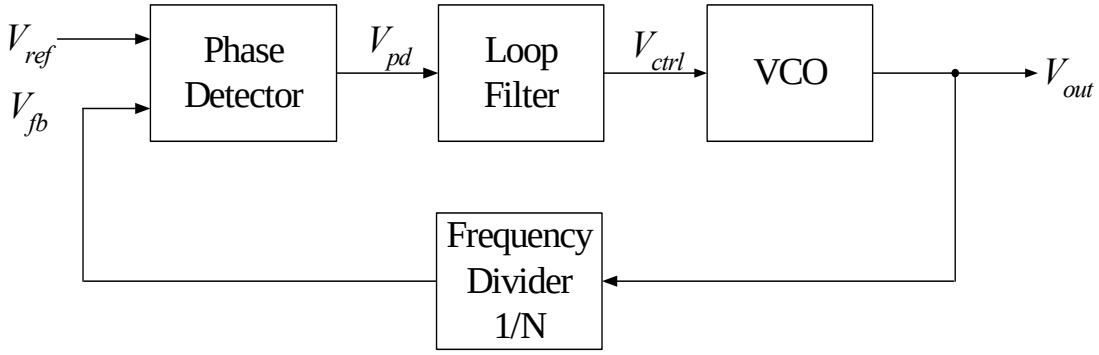


Fig. 2.1 PLL block diagram

The frequency divider divides both of the VCO frequency and phase by a factor

N, thus

$$\theta_{fb}(t) = \frac{\theta_{out}(t)}{N} \tag{2-2}$$

The phase detector gives an output voltage proportional to the phase difference between the reference signal and the feedback signal:

$$v_{pd}(t) = K_{pd}\left(\theta_{ref}(t) - \theta_{fb}(t)\right) \tag{2-3}$$

There K_{pd} is the phase detector gain and its unit is *V/rad*.

The voltage $V_{pd}(t)$ is then filtered by the low-pass *loop filter* whose transfer function is $F(s)$. The noise and the high-frequency components of $V_{pd}(t)$ are suppressed.

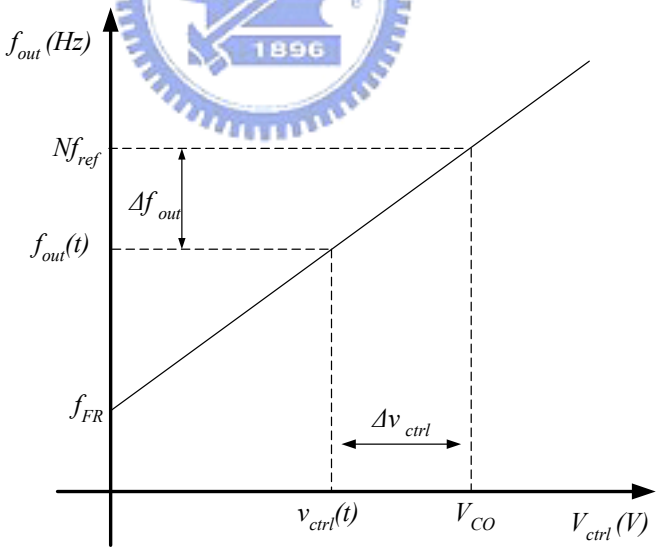


Fig. 2.2 VCO output frequency with control voltage curve.

As shown in Fig. 2.2, the control voltage V_{ctrl} determines the VCO output frequency. The relation between the VCO frequency and the control voltage can be written as

$$f_{out}(t) = f_{FR}(t) + K_{vco} \cdot v_{ctrl}(t) \tag{2-4}$$

There f_{FR} is the "free running" frequency which denotes VCO oscillation frequency when V_{ctrl} = 0 and K_{vco} is the VCO gai*n* in units of *Hz/V*. Further, f_{out} can also be written as

$$\begin{aligned} f_{out}(t) &= Nf_{ref}(t) + \Delta f_{out}(t) \\ &= Nf_{ref}(t) + K_{vco} \cdot (v_{ctrl}(t) - V_{CO}(t)) \\ &= Nf_{ref}(t) + K_{vco} \cdot \Delta v_{ctrl}(t) \end{aligned} \tag{2-5}$$

There V_{ctrl} is the VCO control voltage corresponding to the locked frequency Nf_{ref} . Because frequency is the derivative of phase, the excess phase θ_{out} in equation. (2-1) can be expressed as

$$\begin{aligned} \theta_{out}(t) &= 2\pi \int \Delta f_{out} dt \\ &= 2\pi K_{vco} \int \Delta v_{ctrl}(t) dt \end{aligned} \tag{2-6}$$

Taking the *Laplace transform*, the following result can be obtained

$$\theta_{out}(s) = \frac{2\pi K_{vco} \cdot \Delta V_{ctrl}(s)}{s} \tag{2-7}$$

The transfer function of the VCO is

$$\frac{\theta_{out}(s)}{\Delta V_{ctrl}(s)} = \frac{2\pi K_{vco}}{s} \tag{2-8}$$

An ac linear model of the PLL now can be shown in Fig. 2.3. The phase transfer function of the PLL is

$$H(s)=\frac{\theta_{out}(s)}{\theta_{ref}(s)}=\frac{K_{pd}\cdot F(s)\cdot 2\pi K_{vco}/s}{1+K_{pd}\cdot F(s)\cdot 2\pi K_{vco}/s\cdot(1/N)}$$
$$=\frac{N\cdot K_{pd}\cdot F(s)\cdot 2\pi K_{vco}}{N\cdot s+K_{pd}\cdot F(s)\cdot 2\pi K_{vco}} \qquad (2\text{-}9)$$

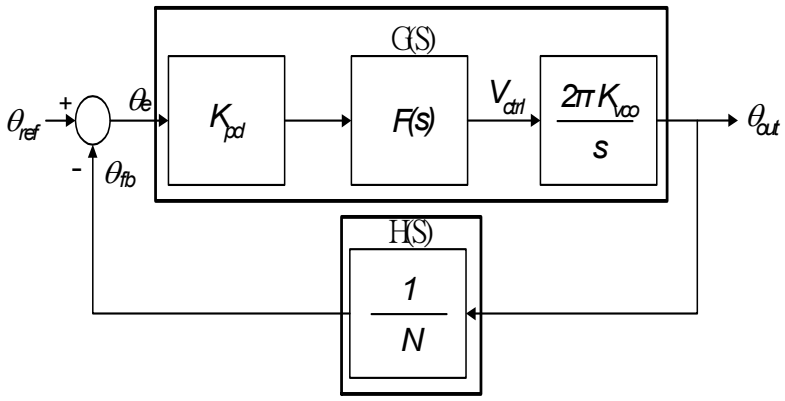


Fig. 2.3 PLL AC linear model

2.1.2 Steady state phase error analysis

Various inputs can be applied to a system. Typically, these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

In Fig. 2.3 θ_e represents the phase error that exits in the phase detector between the incoming reference signal θ_{ref} and the feedback $\theta_{out.}$ In evaluating a system, θ_e must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error θ_e resulting from the input θ_{ref} without transforming back to the time domain.

Simply stated

$$Lim\left[\theta(t)\right] = \lim\left[s\,\theta e(s)\right] \tag{2-10}$$

Where

$$\theta e(s) = \theta ref(s)/(1 + G(s)\cdot H(s)) \tag{2-11}$$

The input signal θ_{ref} is characterized as follows:

Step position: $\theta_{ref}(t) = Cp$, $t \geqq 0$

Or, in Laplace notation: $\theta_{ref}(s) = Cp / s$

There *Cp* is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by *Cp* radians:

Step velocity: $\theta_{ref}(t) = Cv \cdot t,\ t \geqq 0$

Or, in Laplace notation: $\theta_{ref}(s) = Cv / s^2$

The Cv is the magnitude of the rate of change of phase in radians per second. This corresponds to inputting a frequency that is different than the feedback portion of the VCO frequency. Thus, Cv is the frequency difference in radians per second seen at the phase detector.

Step velocity: $\theta_{ref}(t) = Ca \cdot t^2,\ t \geqq 0$

Or, in Laplace notation: $\theta_{ref}(s) = 2 \cdot Ca / s^3$

The Ca is the magnitude of the frequency rate of change in radians per seconds per second. This is characterized by a time variant frequency input.

Similarly, applying the three inputs into type 1, 2 and 3 systems and utilizing the final value theorem, the following table 3 can be constructed to show the respective steady state phase errors. So, we chose type 2 and four order system in this work.

	Type 1	Type 2	Type 3
Step position	Zero	Zero	Zero
Step velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

Table 3 Steady state phase error for various systems

2.1.3 PLL noise source

Any noise in the circuit or environment will create phase disturbance. In Fig. 1.4, a non-ideal frequency synthesizer spectrum is show. It is no longer a single frequency tone but rather a smeared version. The energy under the skirt is phase noise. Sometimes the energy is concentrated at frequencies other than the desired frequency, appearing as a spike above the skirt. This energy is due to a spurious tone. Phase noise and spurious tones are the two key performance parameters of a frequency synthesizer.

The PLL transfer function is easer to define from Fig. 2.3.

$$T(s) = G(s) / (1 + G(s) \cdot H(s)) \quad (2\text{-}12)$$

$$G(s) = Kpd \cdot Kvco \cdot F(s) / s \quad (2\text{-}13)$$

$$H(s) = 1/N \quad (2\text{-}14)$$

Below is table 4 showing various noise sources and the transfer functions that multiply each one.

Source	Transfer Function
Input Reference	$G(s) / (1 + G(s) \cdot H(s))$
Phase Detector	$(1 / Kpd) \cdot [(1 + G(s) \cdot H(s))]$
VCO	$1 / (1 + G(s) \cdot H(s))$
N divider	$G(s) / (1 + G(s) \cdot H(s))$

Table 4 PLL noise source

It should be apparent that the phase detector noise, input reference noise, and *N* divider noise all contain common factor T(s) in their transfer functions. For

this reason, all of these noise sources will be referred to as in band noise source.

But the VCO noise distribute in high frequency band. That the in band sources dominate within the loop bandwidth and the VCO noise dominates outside of the loop bandwidth. This can be seen in Fig. 2.4. The phase noise measured at an offset that is close to the carrier is basically independent of loop bandwidth, provided that the loop bandwidth is sufficiently wide to eliminate the VCO noise. However, the phase error is more dependent on the loop bandwidth. To theoretically design for the lowest phase error, this means that one needs to design such that VCO noise contribution at loop bandwidth is equal to the total noise contribution from the other source noise at bandwidth. If the VCO is noisily relative to the PLL, than this number would be smaller, and if the PLL is noisily relative to the VCO, than this number would be large.

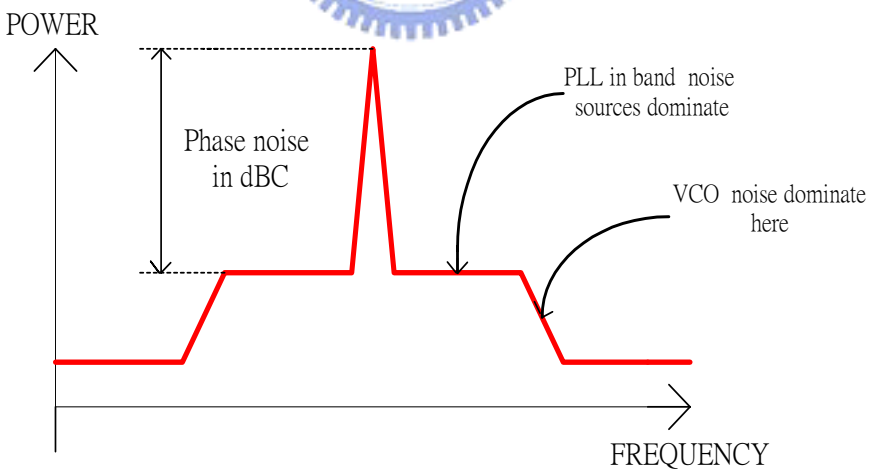


Fig. 2.4 Phase noise spectral for a PLL

2.2 Circuit realization

A Phase-Locked-Loop-Based frequency synthesizer with narrow loop bandwidth is the most commonly used techniques due to its high performance, namely, low phase noise and low spurious tones. But the need for off chip high-Q components is not amenable to the integration of the synthesizer. We used TSMC 0.18um process to implement the frequency synthesizer that has fast settling time and high Q devices on-chip. And the on-chip components are difficult to increase Q value more than off chip high Q components. So, the VCO's turning range and gain (frequency over control voltage) curve is hard to control!

First, we must to design a VCO before to design other block of frequency synthesizer. Because many key parameters like "VCO output frequency", "VCO turning range" and "VCO gain curve (K_{vco})" affect the all loop of properties seriously. And a frequency synthesizer loop characteristic determine from these key parameters.

A "Phase-Locked-Loop" is a loop which locks the output phase or frequency to an accurate reference. In Fig. 2.5 shows the function block diagram of this work. A voltage-controlled oscillator generates an output waveform at a frequency set by the control voltage V_{ctrl}. The Phase/Frequency Detector (PFD) compares the phase and frequency of a divided reference frequency F_{ref} with the divider output phase and frequency. When the loop is locked, the PFD sees two identical waveforms at its inputs and F_{out} equals to N times of F_{ref}. For some reason $F_{ref} > F_b$, V_{ctrl} goes up and the VCO output frequency increase. Vice versa, if $F_{ref} < F_b$, V_{ctrl} goes down and VCO

output decreases. A loop filter (LPF) is used to stabilize the loop by introducing zeros and poles into the loop. In this work include two perfect current match charge pumps to decrease spurious tones power level.

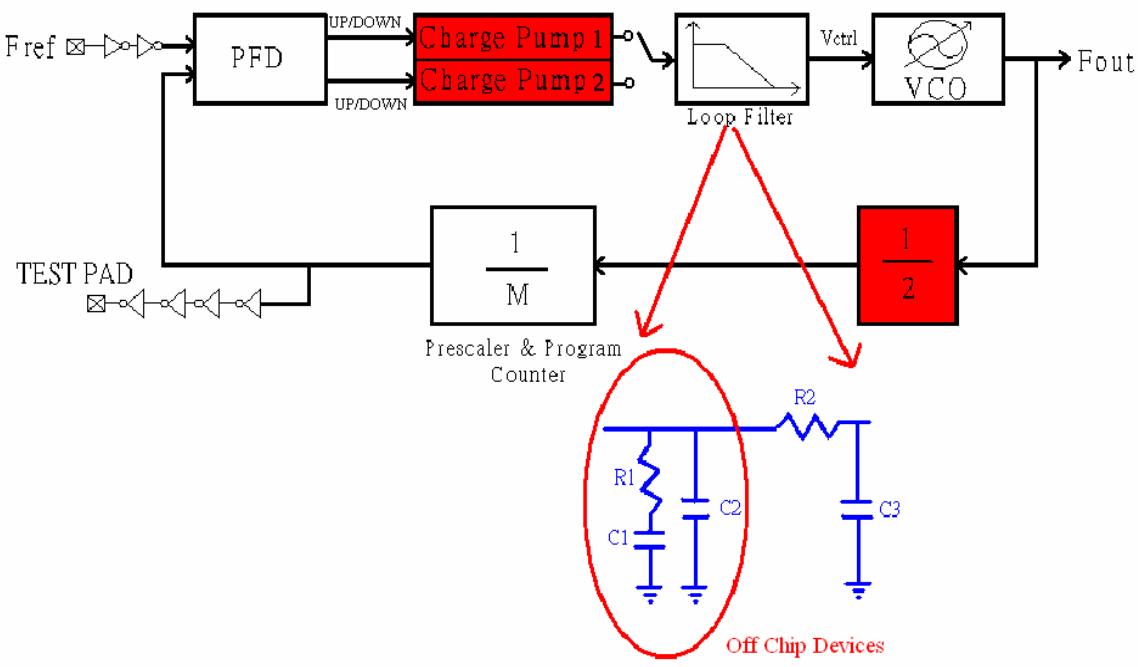


Fig. 2.5 Frequency synthesizer function block of this thesis

A typical PLL-based Frequency synthesizer comprises both high and low frequency blocks. The high frequency blocks, mainly the VCO and first stage of the frequency dividers, are main power consuming blocks, especially in a CMOS implementation. Anyway, several important design considerations about design frequency synthesizer in this these. One, the VCO input control voltage range must to collocate with charge pump output voltage range. In order to decrease spurious noise, charge pump driving and sourcing currents must be equal. So the cascode structure is used in this design to decrease MOS λ effect. The current mode LPF

maybe can be used but buffer input offset must low enough. Two, the high frequency ÷2 divider input signal must to AC couple from VCO output. Three, the quadrature VCO output signals need to add buffer to driver out for easy testing. Five, the signal from program counter feedback to PFD and add some buffer to drive to PAD. Other design considerations will be discussed in this chapter every sub-chapter.

2.2.1 Circuit realization of current-match charge pump

In cellular applications, narrow loop bandwidth is desired in order to minimize the spectral components due to spurious tones in the output spectrum. So, charge pump is a low frequency block and the current of driving and sourcing to low-pass-filter (LPF) equal each other is very important. The spurious tones are generated because different currents of driving and sourcing to drive LPF. In this work has two perfect current matching charge pump circuits be implemented that will be compared at following.

A simple implementation of the charge pump based on the current steering concept is shown in Fig. 2.6. Different *UP* and *DN* signals from the phase/frequency detector (PFD) are used to steer the current one way or the other in the differential pair in the charge pump.

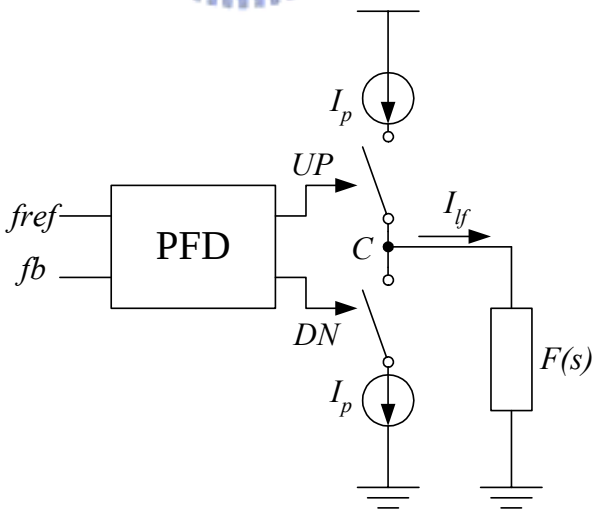


Fig. 2.6 Current steering of charge pump

There are several non-idealities resulting in a non-zero static phase error and

creation of spurious tones. The top leakage current may not equal the bottom leakage current at up and down turn on together, resulting a net charge flowing in or out of the loop filter in one comparison period. In the PLL locking condition, the net charge must compensated by a different on-time of the two switches. For example, if I_p leakage is small than I_n leakage, the *UP* signal must occur slightly earlier than the *DN* signal to compensate for the net charge flow out of the loop filter. This means the reference edge should come slightly earlier than VCO edge if we assume the PFD is ideal. The mismatch between the leakages is one form of static mismatch. Another form of the static mismatch is the DC current level difference when both switches are on. The effect is the same as in the case of leakage current mismatch. The switch has different finite switching on or off time is dynamic mismatch. Both dynamic and static mismatch result in net charge flows in or out of the loop filter periodically, at the rate of the comparison frequency. The result, the control voltage has a ripple at the comparison frequency, which modulates the VCO frequency and generates spurious tones at multiples of the comparison frequency away from the carrier. Fig. 2.7 shows the waveforms of the LPF with non-idealities and we can cancel the effect is delay balance in up and down path of PFD layout. And Fig. 2.8 shows the control voltage of VCO at up (*UP*) and down (*DN*) current mismatch and we can decrease the effect which use current match charge pump.

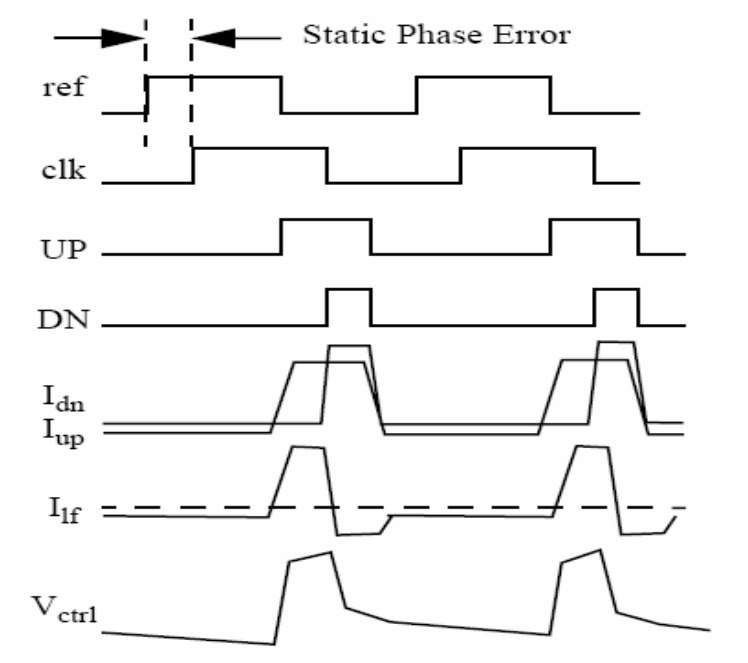


Fig. 2.7 Non-idealities waveform of the charge pump switch

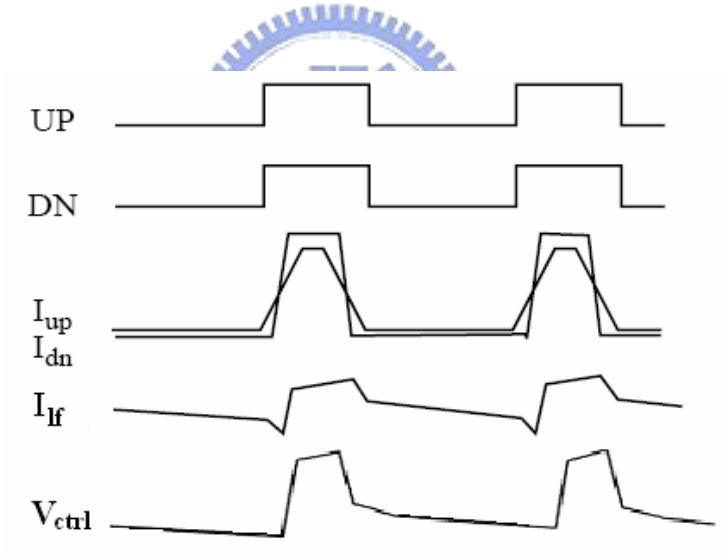


Fig. 2.8 Non-idealities waveform of the charge pump current-mismatch

In Fig. 2.9 shows the one of this work about the perfect current match of charge pump circuit [5]. In this structure, a wide input range OP. showing in Fig. 2.10 makes negative feedback to apply the voltage of V_{ctrl} and V_{trac} are equal and makes sure I_{ref}, I_{up} and I_{down} are equal. This structure has perfect current match characteristic but that still has three problems to make some current mismatch.

(1) I_{up} and I_{down} current mirror source is not the same path. I_{up} is mirrored from M_5 and I_{down} is mirrored from M_6. If process has some variations then M_5 and M_6 drain current are not equal.

(2) Even through the V_{ctrl} and V_{trace} will be lock at the same voltage (assume no offset of OP.). The drain voltage of M_3 and M_7 or M_4 and M_8 are not equal because V_{ctrl} voltage sometime close to power and sometime close to ground. The drain voltage of M_3 and M_1 are not equal, too.

(3) Assume the drain current of M_1 with M_3 and M_2 with M_4 are equal. But the structures haven't guaranteed the voltage of V_a with V_{a1} and V_b with V_{b1} are equal. So, the charge pump has current mismatch in I_{up} and I_{down}.

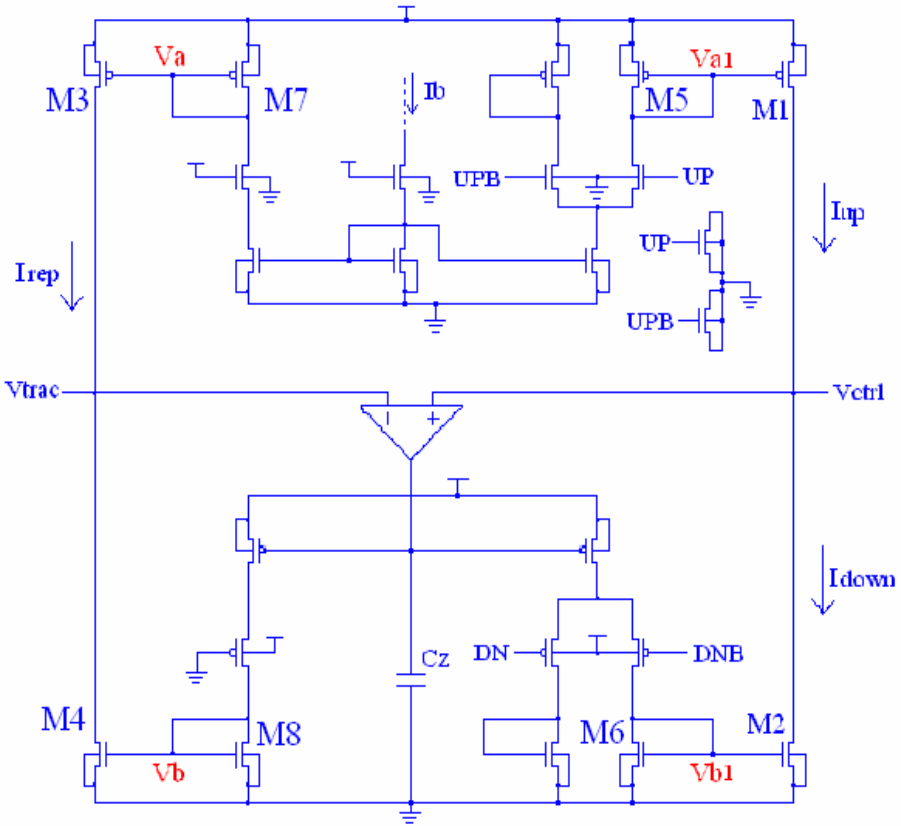


Fig. 2.9 perfect current-match of charge pump circuit in this work (charge pump type 1)

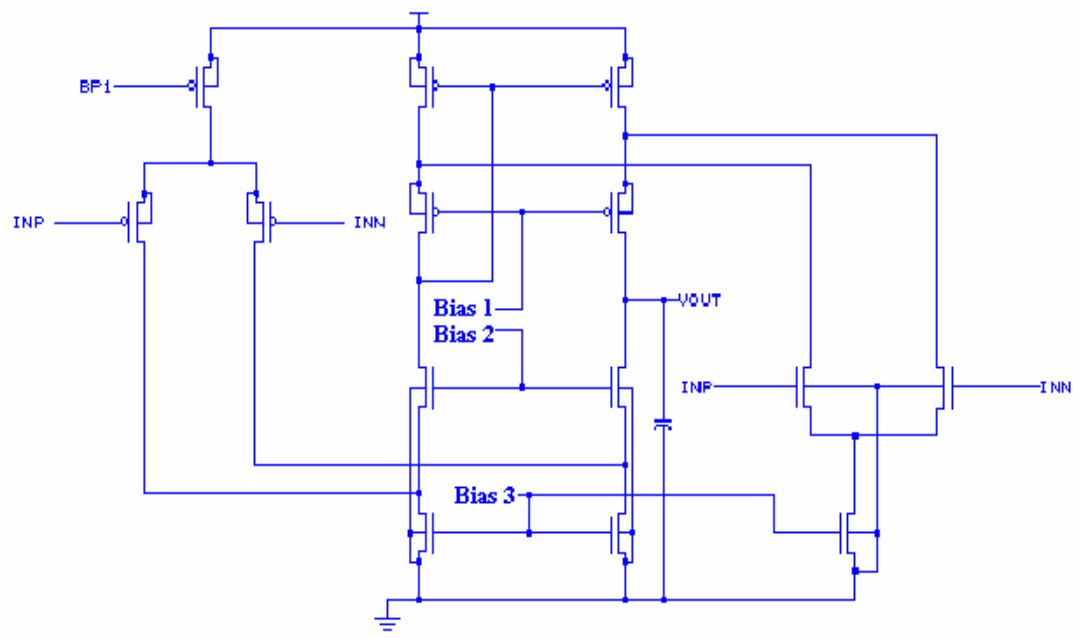


Fig. 2.10 Wide input range OP. circuit

One important design technique to decrease the I_{up} and I_{dn} mismatch about charge pump is in charge pump bias block. Anyway, many ways has to decrease the I_{up} and I_{dn} mismatch about charge pump at one time, but if we can not let I_{up} and I_{dn} currents mirrored from equal original only one source, that decrease the I_{up} and I_{dn} mismatch is insufficient. So, another perfect current match charge pump circuit to add a bias block let I_{up} and I_{dn} currents mirrored from equal original current showing in Fig. 2.11 to improve those drawbacks in Fig. 2.9.

In order to cancel the parasitical capacitors at terminal drain to source on M_2 and M_4 to happen charged shelling with loop filter capacitors each other. We added a unit gain buffer connects from point V_e to point V_{ctrl} and it let two point voltages been equal. The unit gain buffer need rail to rail input and rail to rail output, because the voltage of VCO input turning range is wide. Fig. 2.12 shows the rail-to rail unit gain buffer circuit and another function of the buffer is sinking current from M2

when UP is low and sourcing current from M_4 when UP is high. In this charge pump, there are three techniques to improve current match.

(1) I_p / I_n of up/down current are mirrored from the same path is I_{cp}.

(2) OP_2 and OP_3 make sure the voltage of V_a close to V_b and the voltage of V_c close to V_d.

(3) Cascode devices of M_5 and M_6 are increasing impedance and decreasing channel length modulation effect.

(4) Use transmission gate switches to increase control range, decrease switch on resistance, decrease clock feed-through and increase speed.

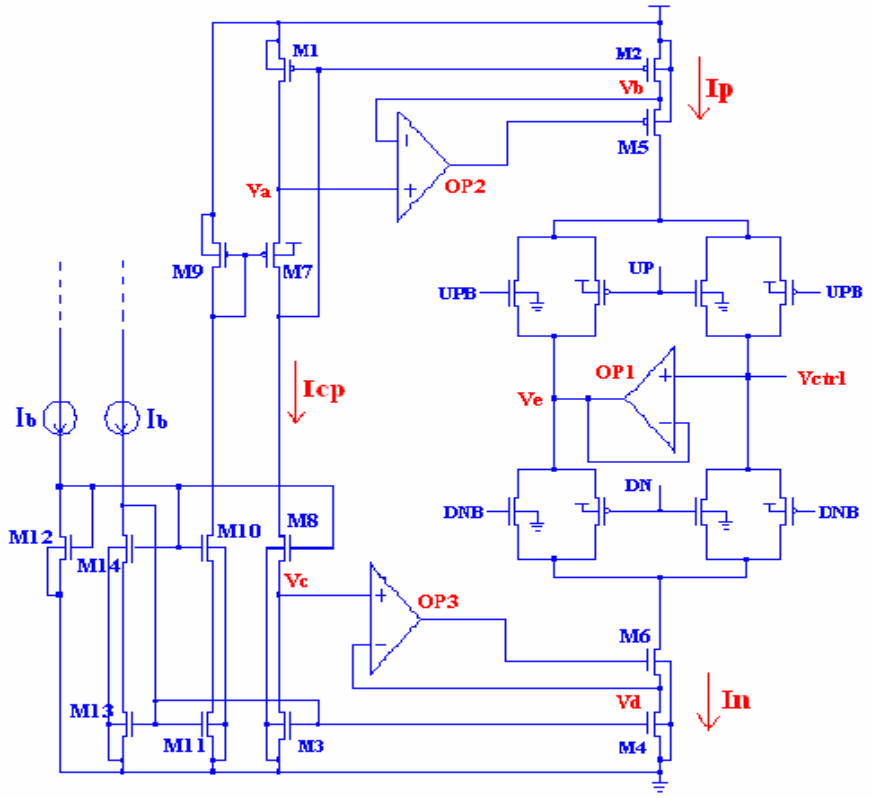


Fig. 2.11 Improve the current-match of charge pump circuit in this work

(Charge pump type 2)

Cascode structure of current source can be used to reduce the current mismatch when charge pump output voltage varies between the top and bottom current source.

But the charge pump output swing needs to meet the VCO's turning range. And minimum length devices can be used as switches to reduce the switching time at switches on/off, hence reduce the dynamic mismatch.

The circuit working principle is two current paths of I_b be generated from a bias circuit show in Fig. 2.13. Those current paths provide M_8, M_7 (Fig. 2.11) gate terminals voltage and mirror the current to I_{cp}. And the circuit of OP_2 and OP_3 showing in Fig. 2.14 make sure V_a with V_b and V_c with V_d are equal and another avail is to increase current devices impedance about sourcing and sinking. The current I_p source to low pass filter when UP is high and the current I_n sink from low pass filter when DN is high. If UP and DN are high together then current of I_p drift into current of I_n. And the point V_{ctrl} connects to low pass filter. If the charge pump sourcing and sinking current are match then there are not any current to charge or discharge low pass filter. So, the structure of charge pump has perfect current match characteristic.

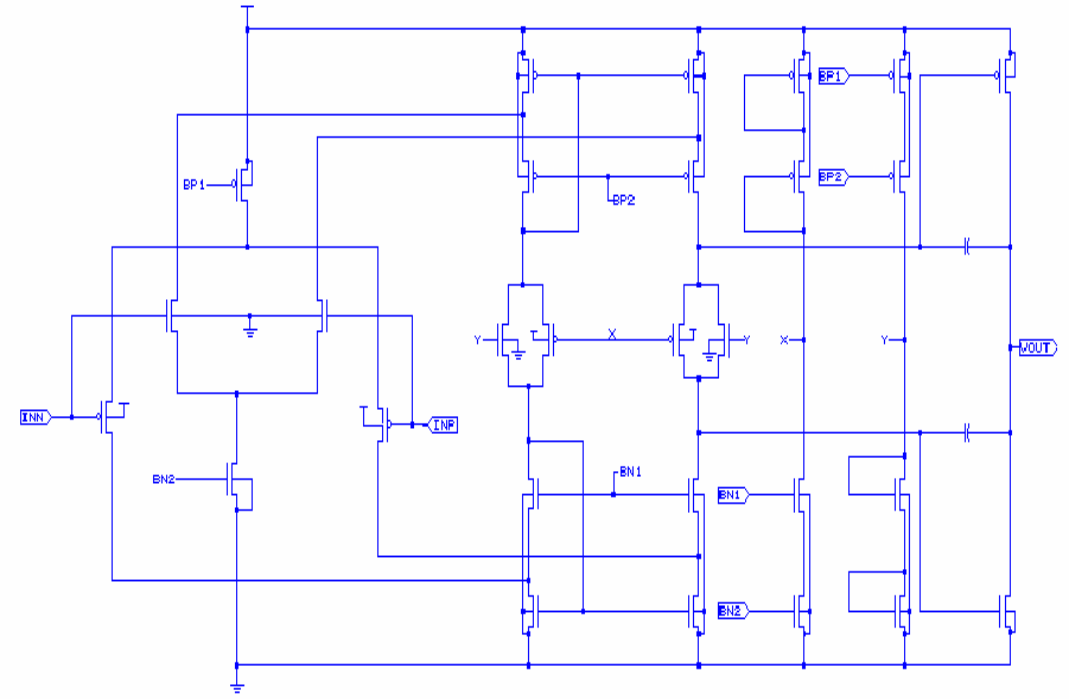


Fig. 2.12 Rail-to-rail OP circuit in charge pump type 2 (OP1)

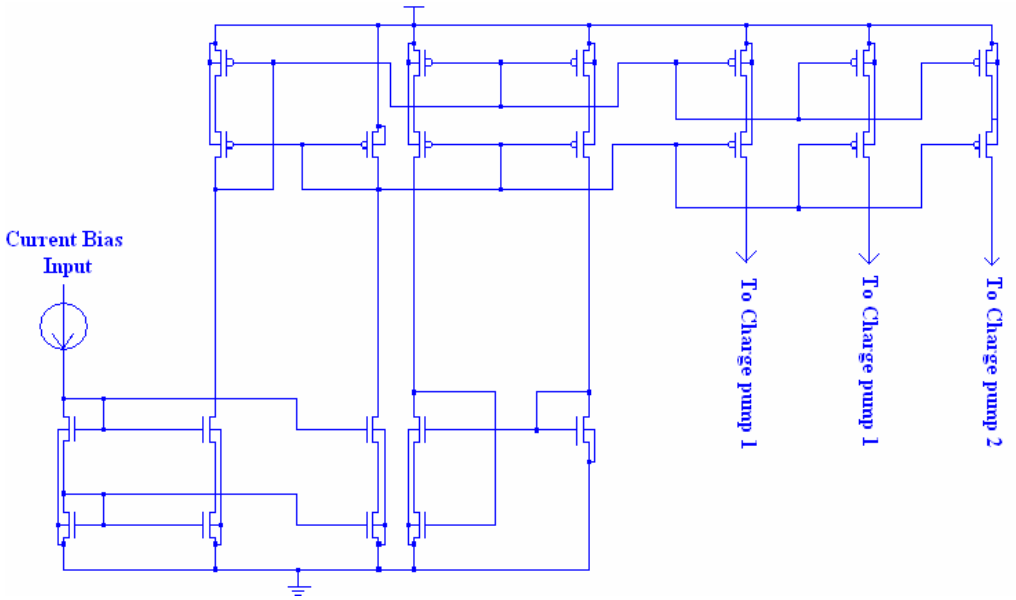
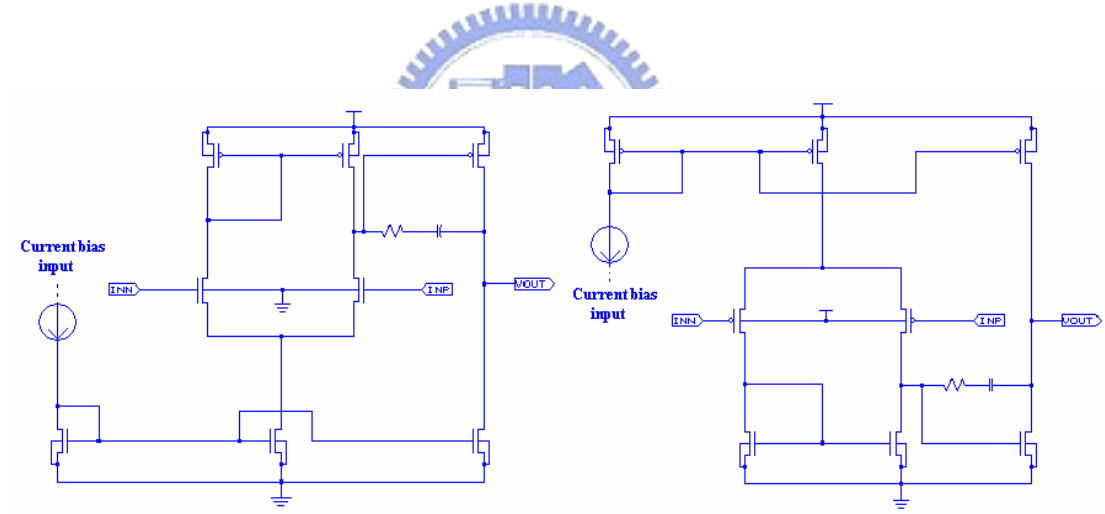


Fig. 2.13 Current bias of charge pump in this work



(a) OP2 circuit **(b) OP3 circuit**

Fig. 2.14 OP circuit of charge pump in this work

2.2.2 Low pass filter design

The loop filter in this work is a third-order passive filter that consists of two resistors and three capacitors. The resulting PLL is then a type-2 fourth-order loop which provides great noise suppression for the PLL output spurious level. The standard third-order passive loop filter configuration shown in Fig. 2.15 is utilized. The resisters R_1 and capacitors C_1, C_2 are off chip devices, the resister R_3 and capacitor C_3 are build in chip. Resistor R_1 and C_1 in the loop filter generate a pole at the origin and a zero at $1/(R_1C_1)$. Capacitor C_2 and combination of R_3 and C_3 are used to add extra poles at frequency higher than the PLL bandwidth to reduce reference feed-through and decrease the spurious sidebands at harmonics of the reference frequency. The capacitors and resistors of the loop filter should be properly chosen to perform the required filtering function and maintain the stability of the loop without introducing too much noise. The component values in the filter are calculated following the design flow.

(1) The average VCO gain in this work is about 480 *MHz/V*.

$$K_{vco} = 480\ MHz/V \tag{2-15}$$

(2) The input reference clock is 10MHz.

$$F_{ref} = 10\ MHz \tag{2-16}$$

(3) A 250 *kHz* open loop bandwidth is chosen.

$$K = 250\ KHz \tag{2-17}$$

(4) 67°phase margin is chosen. It corresponds to a γ of 5. In other words, the zero ω_z is placed a factor 5 below K, and the pole ω_{p1} is placed a factor 5 above K,

to obtain a phase margin of approximately 67°.

$$\omega_z = 2\pi \cdot 50\ kHz \tag{2-18}$$

$$\omega_{p1} = 2\pi \cdot 1.25\ MHz \tag{2-19}$$

(5) An equivalent charge pump current is 500u*A*.

$$I_{cp} = 500\ uA \tag{2-20}$$

(6) The average divider is 525. That includes program counter, prescaler divider (*M*) and dive-by-2.

$$N = 2 \cdot M = 525 \tag{2-21}$$

(7) Calculate R_1:

$$R_1 = N \cdot K \ / \ (I_{cp} \cdot K_{vco} (1 - 1 / \gamma^2)) \approx 3.9k\Omega \tag{2-22}$$

(8) Calculate C_1 and C_2:

$$C_1 = 1 \ / R_1 \cdot \omega_z \approx 820\ pF \tag{2-23}$$

$$C_2 = C_1 \ / \ (\gamma^2 - 1) \approx 33\ pF \tag{2-24}$$

(9) An additional attenuation value of the reference spur of 20 dB is chosen, thus

$$\omega_{p2} = 2\pi f_{ref} \Big/ \sqrt{10^{ATTEN/20} - 1} = 2\pi \cdot 3.33MHz \tag{2-25}$$

(10) Chosen R_2 and C_3:

$$\omega_{p2} = 1/R_2C_3\,, \tag{2-26}$$

R_2=24 $k\Omega$ and C_3=2 pF are chosen.

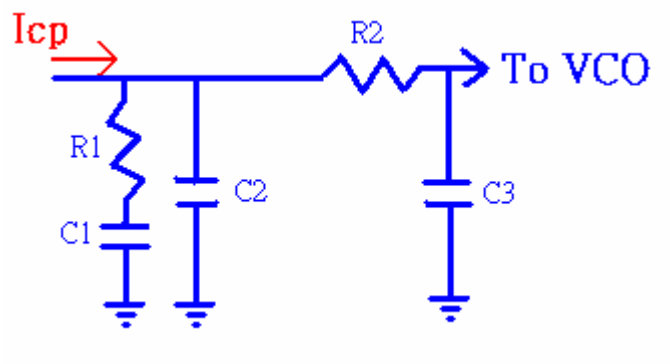


Fig. 2.15 Type 2 third-order low pass filter

However, since discrete resistors and capacitors are only available in standard values, components near the calculated values are used. Table 5 gives the selected component values. C_1 and C_2 are polyester film capacitor. Although the physical size is larger than the ceramic capacitor, film capacitors do not experience random voltage changes associated with the ceramic type [28]. C_3 is chosen somewhat smaller then the calculated value in consideration of the VCO tuning port parasitic capacitance.

Final PLL Parameters In This Work		
VCO gain	K_{vco}	480 MHz/V
Open loop gain bandwidth	K	250 kHz
Zero frequency	ω_z	50 kHz
First pole frequency	ω_{p1}	1.25 MHz
Second pole frequency	ω_{p2}	3.33 MHz
Passive elements	R_1	3.9 kΩ
	C_1	820 pF
	C_2	33 pF
	R_2	24 kΩ
	C_3	2 pF

Table 5 Final frequency synthesizer parameters

2.2.3 Circuit realization of quadrature VCO

Modern receiver architectures, such as the zero-IF receiver and the low-IF receiver, allow a high degree of integration and are therefore often utilized in wireless transceiver designs. In order to avoid loss of information, these architectures normally have an in-phase and quadrature signal processing path. Usually the receiver signal is split after the LNA and multiplied with a quadrature signal source.

Quadrature signal may also be needed at the transmit side of a wireless transceiver. Base band data streams are multiplied with a quadrature carrier signal, added, and transmitted. Quadrature LC oscillator usually has large layout area, especially on-chip inductors layout area. ‘Optimally Coupled 5-GHz Quadrature LC Oscillator [22]’ and ‘Super harmonic Coupling 5-GHz CMOS Quadrature VCO [23]’ also need four inductors in two close couple stage VCO. This work use two inductors in two close couple stage VCO to decrease layout area and keeps perfect performance, the circuit show in Fig. 2.16. The inductance is about 2.368nH and the varactors are about 2.92pF in ideal conditions.

Anyway, there are basically two types of VCO, tuned and un-tuned. Un-tuned oscillators have inferior spectral purity compared to tuned oscillator for the same power consumption. The performance of a tuned oscillator depends on the quality factor Q of the tuned element. A typical example of an un-tuned oscillator is a ring oscillator. It consists of n inverters in a ring and the end of the ring is 180° out of phase from the beginning of the ring.

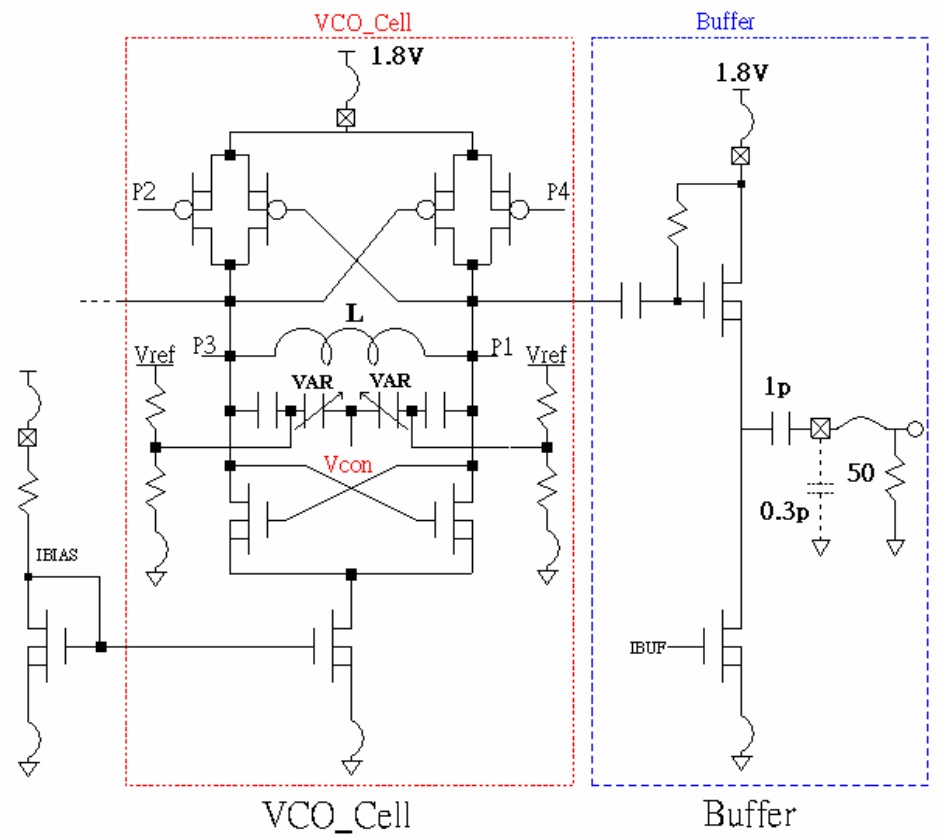


Fig. 2.16 VCO circuit in this work

However, when the VCO is integrated with other circuits, noise can be coupled through the substrate. The supply line might not be as clean as the supply in the stand-along VCO. The power supply rejection ratio becomes very important. If the output is differential, any variation in the control voltage or supply will result in variation in the effective capacitance in the tank. Hence the oscillation frequency will also fluctuate with the control voltage or supply.

And, if the inductors are the main source of noise, maximizing their quality factor would improve the phase noise significantly. However, in multi-GHz VCO's with short channel transistors, inductors are not the main source of noise and a better design strategy is not maximize the effective parallel impedance of the RLC tank at resonance. This choice increases the oscillation amplitude for a given power

consumption and hence reduces the phase noise caused by the noise injection from the active devices. Since inductors are the main source of loss in the tank, the LQ product should be maximized to maximize the effective parallel impedance of the tank at resonance, where L is the inductance and Q is the quality factor of the spiral inductors. It is important to realize that maximizing Q along does not necessarily maximize the LQ product, and it is the latter that matters here.

In a standard process, metal layers can be used to construct on-chip spiral inductors. Fig. 2.17 shows a square spiral inductor. Several issues associated with the on-chip inductor need to be mentioned. First, there is series resistance in the metal layers which reduces the quality factor of the inductor. Second, there is capacitive coupling from the metal to substrate which reduces the self-resonant frequency of the inductor. Third, there is resistance in the conducting substrate which also reduces the quality factor of the inductor. These non-idealities are modeled in the lumped π model.

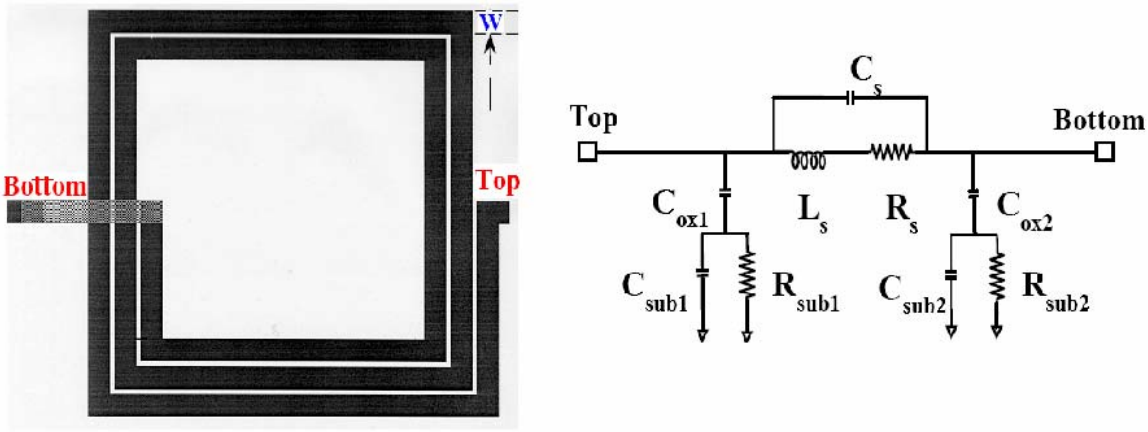


Fig. 2.17 On chip spiral inductors layout and equivalent circuit

In a standard process, the N+/Nwell junction can be used as a varactor. Fig. 2.18 shows the RF model about varactor. The distance between the N+ regions is the current path and it should be kept minimum or minimum series resistance associated with the varactor. Sidewall capacitance has a larger Q and less tuning range because of the higher doping profile. Bottom-plate capacitance has a lower Q and larger tuning because of the lower doping profile.

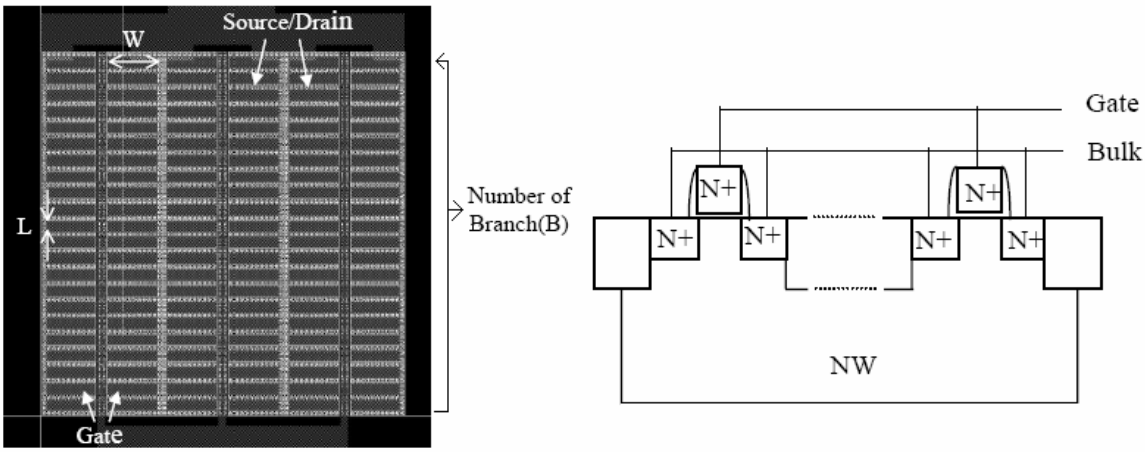


Fig. 2.18 An N+/Nwell junction varactor

The Q of the tank thus is dominated by the Q of inductor rather than Q of varactor. But when the operating frequency is high, the Q of varactor is reduced because the Q of varactor is inversely proportional to the operating frequency. In the mean time, the Q of the inductor is proportional to the operating frequency. This is, at higher frequencies, the Q of the varactor is more important. Fig. 2.19 shows the low Q and high Q structures of LC tank of VCO. That use varactor to replace the capacitor and switch to reach high Q.

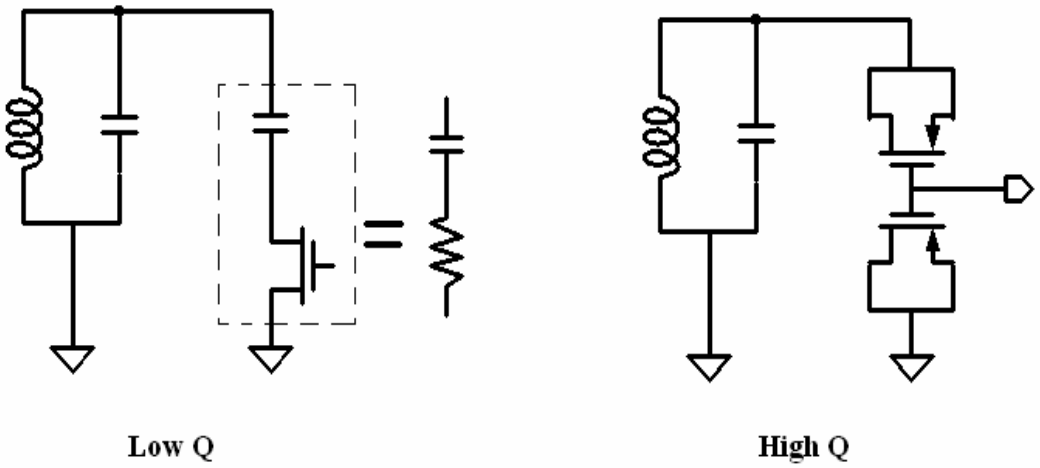


Fig. 2.19 High Q structure of LC tank VCO

A general LC-VCO can be symbolized as in Fig. 2.20. The oscillator consists of an inductor *L* and a capacitor *C*, building a parallel resonance tank R_{tank}! We need an active element $-R_{tank}$, compensating the losses of the inductor ($R_{tank}L$) and the losses of the capacitor ($R_{tank}C$). As the capacitance *C* is proportional to a tuning input voltage, the circuit results in a VCO with angular center frequency.

$$Wc = 1 / \sqrt{LC} \qquad (2\text{-}27)$$

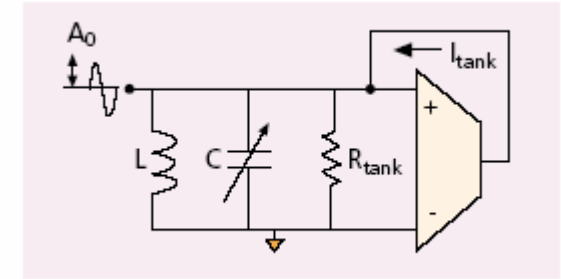
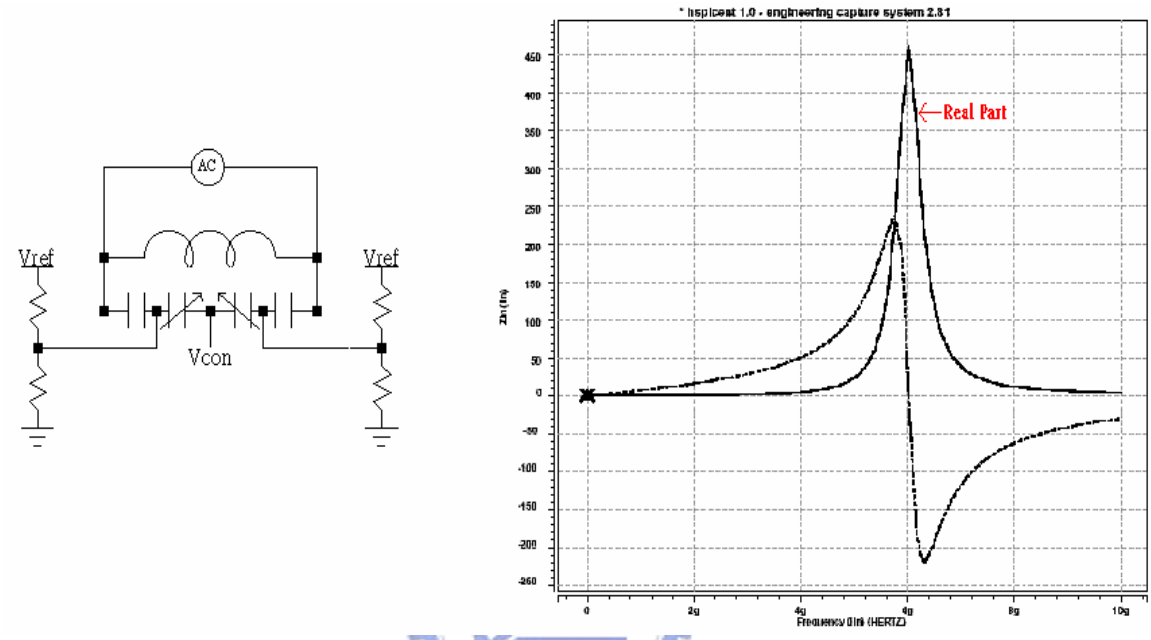


Fig. 2.20 LC tuned VCO model

The capacitor *C* in Fig. 20 not only consists of a variable capacitor to tune the oscillator, but it also includes the parasitic or fixed capacitances of the inductor, the active elements, and the load. Anyway, to get the LC tank resistance value was

important before to design the resistance $-R_{tank}$ value. Fig. 21, (a) show the LC tank simulation circuit of this work and Fig. 21, (b) show the real part and imaginary part about LC tank simulation resistance.



(a) Effect resistance of LC tank (b) Real part of LC tank resistance at 6GHz

Fig. 2.21 The resistance simulation of LC tank in tuned VCO

In Fig. 16 shows the schematic of the VCO. Two cross-coupled transistors generate the negative impedance ($-R_{tank}$) required to cancel the losses of the negative impedance required to cancel the losses of the RLC tank. On-chip spiral inductors with patterned ground shield are used in this design. The three main requirements for the VCO are low phase noise, low power consumption and small layout area. To improve the $1/f^3$ corner of the phase noise it is convenient to have a symmetric tank ($g_{m,n} = g_{m,p}$)[13][14]. For symmetric tanks, $g_{neg,tank}$ is given by the expression,

$$g_{neg,tank} = -(g_{m,n} + g_{m,p}) / 2 = -g_{m,n} \quad (2\text{-}28)$$

To make sure this VCO can oscillate normally, the loop gain must at least 3 hence,

$$g_{m,n} >= A * G_{tank,\ max} \quad and\ A>=3 \tag{2-29}$$

$$G_{tank,\ max} = R_{tank} = LC\ tank\ resistance \tag{2-30}$$

$$R_{tank} = Re(Z_{tank}),\ when\ Im(Z_{tank}) = 0 \tag{2-31}$$

The VCO, which is another dominant source of PLL power consumption, need to be carefully optimized in terms of dissipation, without degrading tuning range and phase noise performance. The power consumption of an oscillator is inversely proportional to its phase noise level. Therefore, the efficiency of an oscillator topology is typically quantified in terms of the noise power product. The structure had perfect characteristics about low power, low phase noise and high output swing. The simulation results describe in section 2.3.1.

The selection of VCO gain (K_{vco}) and VCO input range (V_{ctrl}) are tradeoff in PLL. Table 6 shows the influences in PLL about the tradeoff of K_{vco} and V_{ctrl}. The best choices about them are middleman values.

	Kvco ↓ and Vctrl ↑	Kvco ↑ and Vctrl ↓
VCO Output Sensitivity	Low	High
Loop Damping Effect	Low	High
Low-pass-filter Bandwidth	High Bandwidth	Narrow Bandwidth
Loop Settling Time	Small	Large
Low-pass-filter size	Small	Large
Charge pump output range	High	Low
Charge pump channel length modulation effect	High	Low

Table 6 The influences of K_{vco} and V_{ctrl} in PLL

2.2.4 Circuit realization of integer-N divider

In the block of integer-N include a divide-by-2 divider and pulse swallow frequency divider. The block most difficult to design is the first ÷2 stage, which should operate at 5.3 GHz or more, and the speed and power consumption be dominated at the block. Fig. 2.22 shows the divide-by-2 divider in this work. The structure has very small layout area and not bad power consumption. This structure worked at differential signals to improve low noise and low power characteristics. Using Pseudo-NMOS gates enables high-speed operation which providing large output swing. The ÷2 divider input signals come from phase 0° and phase 180° of quadrature VCO output which signals AC couple to an inverter whose input and output are tied together to get the correct dc level. The voltage of *VB* can control the output amplitude and common mode voltage of ÷2 divider.

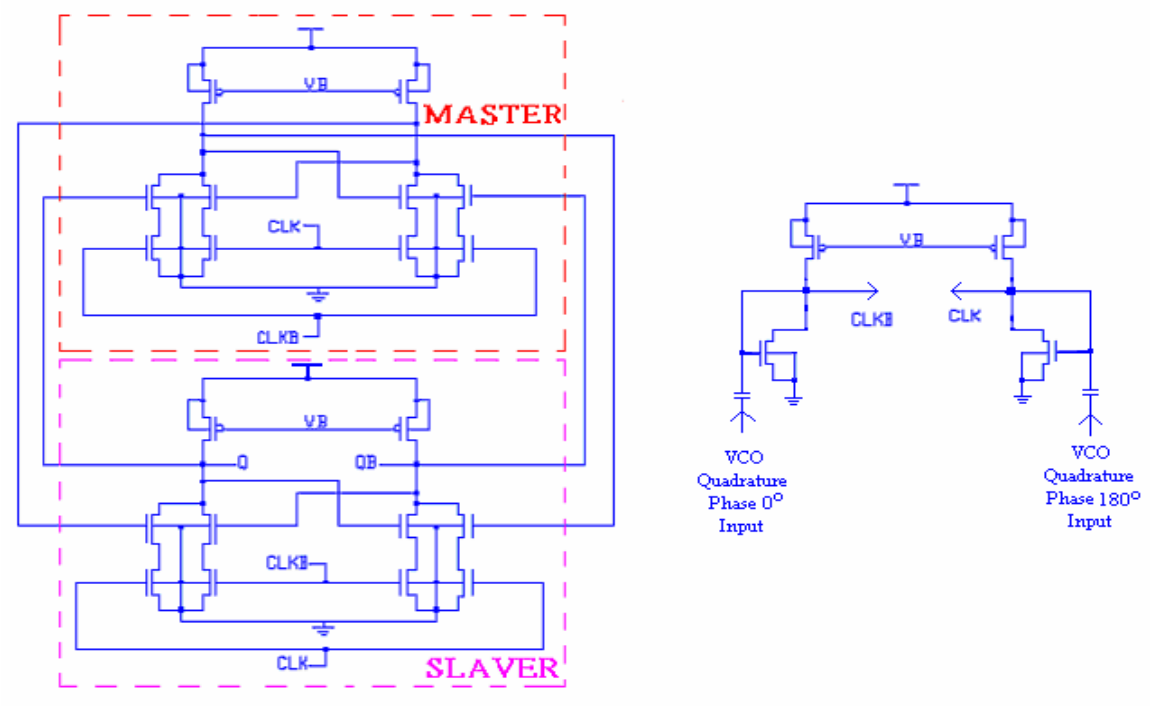


Fig. 2.22 Pseudo-NMOS divider-by-two circuit (HDIV2) and input ac coupling

The divider structure of SCL was found to work only up to the 4.8 GHz in post-simulation in the process and another the divider structure of TSMP has 25% duty cycle of the output signals is less convenient for phase switching. This led to our choice of pseudo-NMOS logic despite its high power consumption.

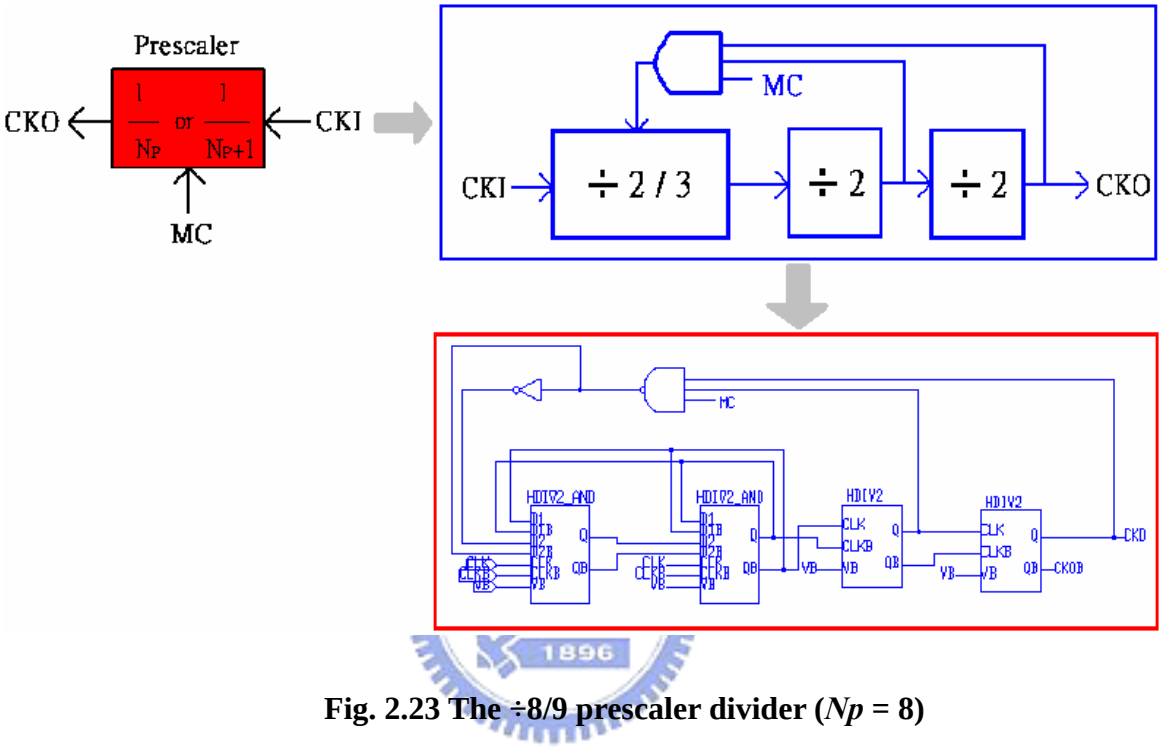
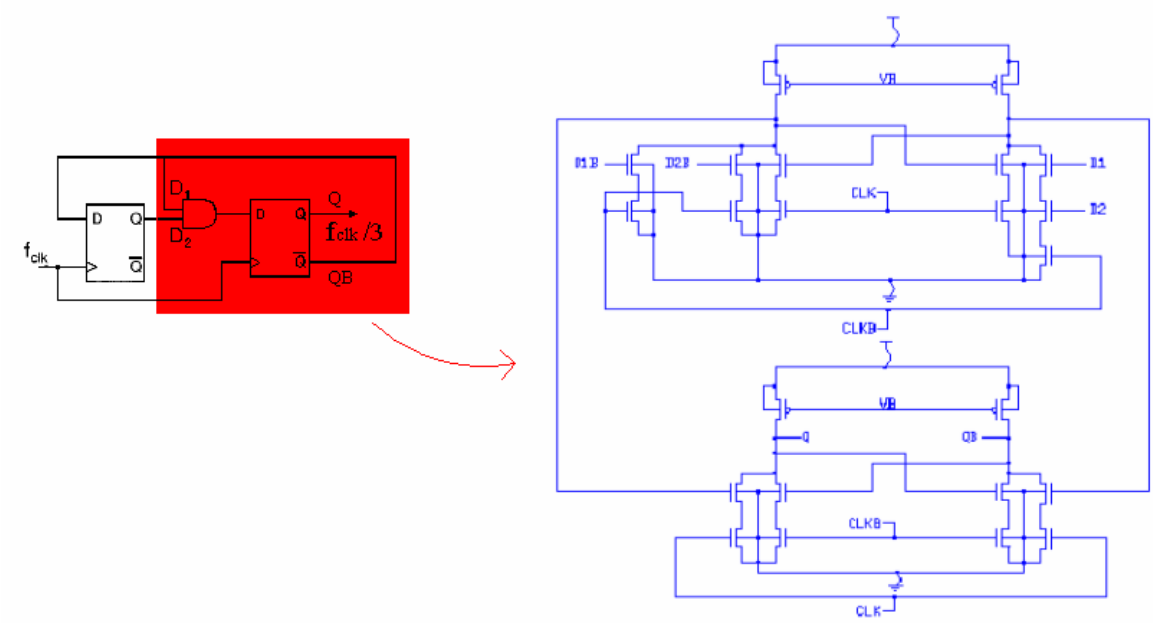


Fig. 2.23 The ÷8/9 prescaler divider (*Np* = 8)

The pulse swallow frequency divider (÷M) consists of a ÷8/9 prescaler followed by a program and pulse swallow counter. Fig. 2.23 shows the ÷8/9 prescaler divider and the prescaler consists of two dual-modulus divide-by-2/3 and two divide-by-2 frequency divider. The modulus control (MC) input selects between divide-by-8 and diide-by-9. A "÷2–AND" block circuit is a ÷3 stage and the logic diagram is shown in Fig. 2.24 (a). The combination of the AND gate and flip-flop is implemented as shown in Fig. 2.24 (b). The parallel branches implement the AND function.



(a) ÷3 stage logic diagram **(b) ÷3 stage circuit implement**

Fig. 2.24 The structure of divide-by-three stage

Only one CMOS logic ripple counter is used for both program and pulse swallow counters, which are shown in Fig. 2.25.

Total divide value is *N*, *S* is swallow counter value and *P* is program counter value.

$$M = Np \cdot S + P + 1 \tag{2-32}$$

$$N = 2 \cdot M \tag{2-33}$$

The overall division ratio is 259 ~ 266 (*M*) and the channel value with divide value has a mapping table likes table 7. The program counter generates one output pulse for every thirty input pulses and five bits to select one of the carriers in the swallow counter. Fig. 2.26 shows the program and swallow counters circuit which output of the pulse swallow counter is controlled by five channel select bits. And in table 8 describes swallow counter setup function.

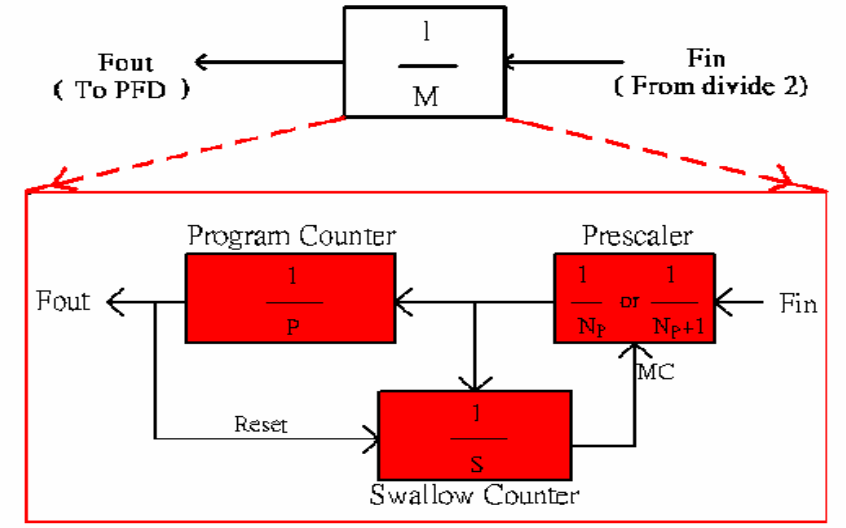


Fig. 2.25 The structure of program and swallow counters

Channel	Center Freq.	M	N_P	P	S
Carrier 1	5.18GHz	259	8	30	19
Carrier 2	5.20GHz	260	8	30	20
Carrier 3	5.22GHz	261	8	30	21
Carrier 4	5.24GHz	262	8	30	22
Carrier 5	5.26GHz	263	8	30	23
Carrier 6	5.28GHz	264	8	30	24
Carrier 7	5.30GHz	265	8	30	25
Carrier 8	5.32GHz	266	8	30	26

Table 7 Program and swallow counter channel select setup mapping

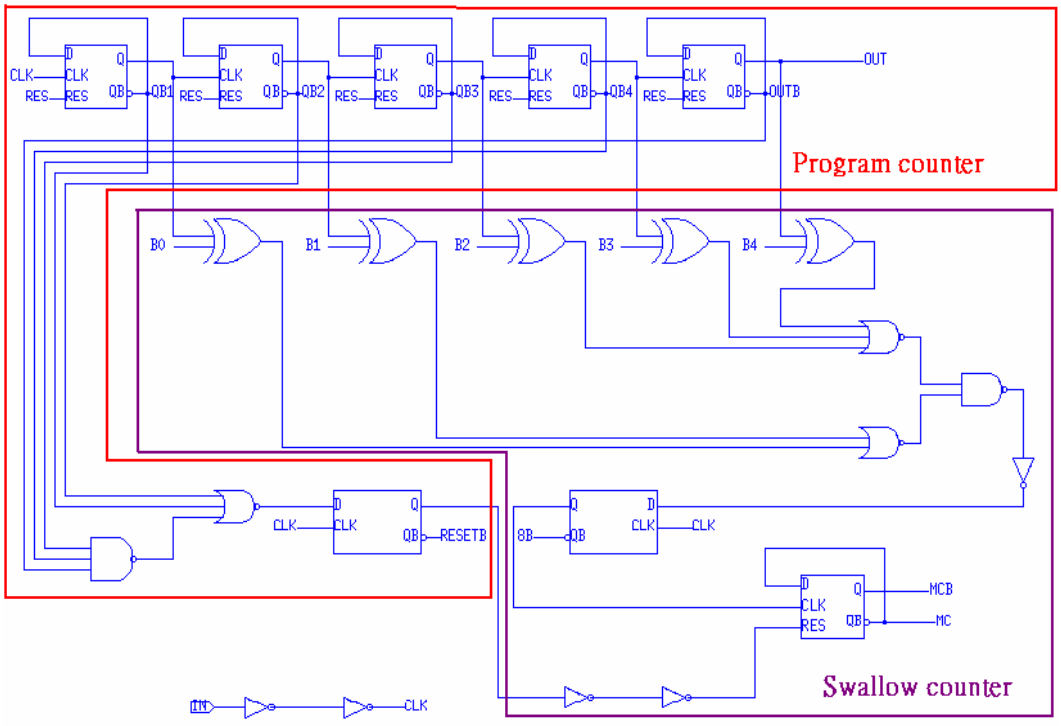


Fig. 2.26 The circuit of program and swallow counters

Swallow Counter Bit 4 – Bit 0 :

Data (S)	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17	0	1	1	1	1
18	0	1	1	1	0
19 (Carrier 1)	0	1	1	0	1
20 (Carrier 2)	0	1	1	0	0
21 (Carrier 3)	0	1	0	1	1
22 (Carrier 4)	0	1	0	1	0
23 (Carrier 5)	0	1	0	0	1
24 (Carrier 6)	0	1	0	0	0
25 (Carrier 7)	0	0	1	1	1
26 (Carrier 8)	0	0	1	1	0
27	0	0	1	0	1
28	0	0	1	0	0
29	0	0	0	1	1
30(Reset)	0	0	0	0	0

Table 8 Swallow counter setup mapping

2.2.5 Circuit realization of PFD

The control voltage of the VCO comes from the output of a loop filter, which contains the information of how much the VCO phase leads or lags that of the reference. The phase detector and loop filter are connected in order to generate the control voltage. A PFD is a sequential circuit which can not only detect the phase error between its two input signals but also provides a frequency-sensitive signal to aid acquisition when the loop is out of lock. In this work circuit implementation of the phase/frequency detector is shown in Fig. 2.27.

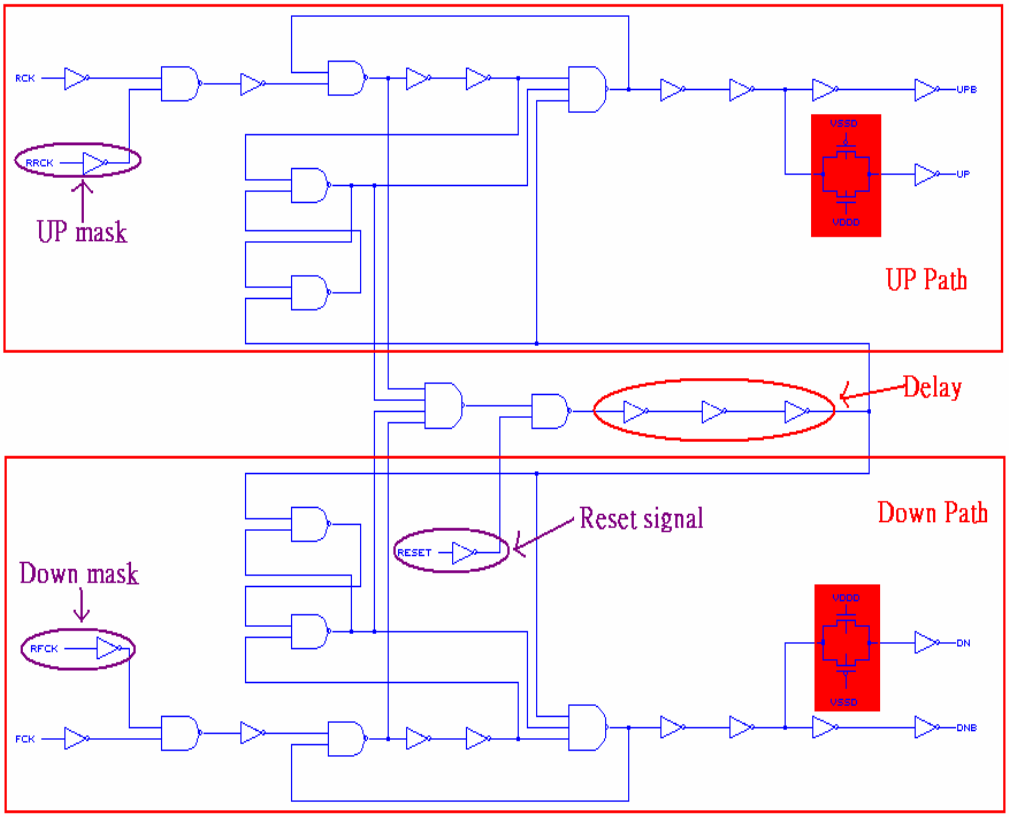


Fig. 2.27 The circuit of PFD in this work

In the circuit, if reference clock (*RCK*) fast than feedback clock (*FCK*) then PFD generate high pulse "*UP*" at "UP Path" On the other hand, if reference clock

(*RCK*) slow than feedback clock (*FCK*) then PFD generate high pulse "*DN*" at "Down Path". The two outputs, *UP* and *DN*, of the PFD control the charge pump circuit. *UP* and *DN* will never be active together. When *UP* is active, it will close the lower switch in the charge pump, and then a positive current will flow into the loop filter. The current will cause the output voltage of the loop filter to rise. On the other hand, when *DN* is active, it will close the upper lower switch in the charge pump, and then a negative current will flow into the loop filter. The current will cause the output voltage of the loop filter to drop. The third state of the PFD is when neither *UP* nor *DN* is active. At this time, the charge pump output current is zero and therefore charge pump output is in high-impedance state. Fig. 2.28 describes the fundamental of PFD stage diagram.

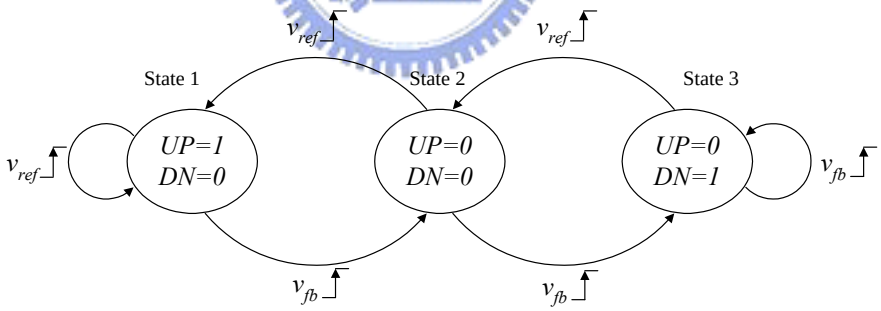


Fig. 2.28 The PFD state diagram

The *UP* and *DN* signal are full swing signals in order to minimize the leakage current in the switches in the charge pump. Because the charge pump also needs differential *UP* and *DN* signals for the four switches, the PFD should also uses a differential topology. And the "UP Path" and "Down Path need have equal delay time and devices layout.

In order to minimize the noise generated by the gate of charge pump, the ratio of PMOS size to NMOS size should be designed properly so that the output rising or falling edge is sufficiently fast. Assuming the rising slope is S_r and the reference waveform period is T, any voltage variation or noise V_{noise} at the zero crossing is translated to phase variation or noise Φ_{noise} as

$$\Phi_{nois}e = (2\pi / T) \cdot (Vnoise / S_r) \qquad (2\text{-}34)$$

So, minimum length device should be used for largest S_r to decrease Φ_{noise}.

And, there are several control signals to set PFD working state. One of the three stages, when "*RRCK*"is high, the PFD always output "*UP*" pulse. Opposite another state, when "*RFCK*"is high, the PFD always output "*DN*" pulse. Besides, the circuit added a "*RESET*" signal to make high-impedance state at the net of loop filter. Those control signals will help designer to test the frequency synthesizer detail. Next section shows the PFD simulation results, we could see those control signals to affect the PFD output waveform.

2.3 Simulation results

In this section, all the functional blocks have been simulated. And those simulation results have been described in sub-section from section 2.3.2 to section 2.3.5. A summary about simulation is described in section 2.3.5.

Anyway, all simulation conditions based on TSMC 0.18um CMOS process model to simulate and that include FF, TT, SS, SF and FS type model. The simulation results include temperature condition, too!

Some important characteristics about this simulation be focused at

(1) The tune range, gain and phase noise of VCO.

(2) The frequency range and output magnitude error of quadrature VCO

(3) The current match characteristic of charge pump is improved result.

(4) The function of PFD works correctly.

(5) The function of integer-N divider works correctly.

(6) The loop settling time of synthesizer in close loop.

(7) The locked state analysis in close loop.

(8) The power of whole chip is simulated.

, those characteristics and waveforms show in following subsection.

2.3.1 Simulation results of quadrature VCO

Fig. 2.29 show the four phase output waveforms of quadrature VCO. The VCO output works at 5.5GHz and P1 is phase 0˚, the P2 is phase 90˚, P3 is phase 180˚ and P4 is phase 270˚. In those waveforms, the output amplitude closes to 1.05 Volt. Fig. 2.30 show the magnitude error which is small than 3mV from 5GHz to 5.6GHz of the VCO.

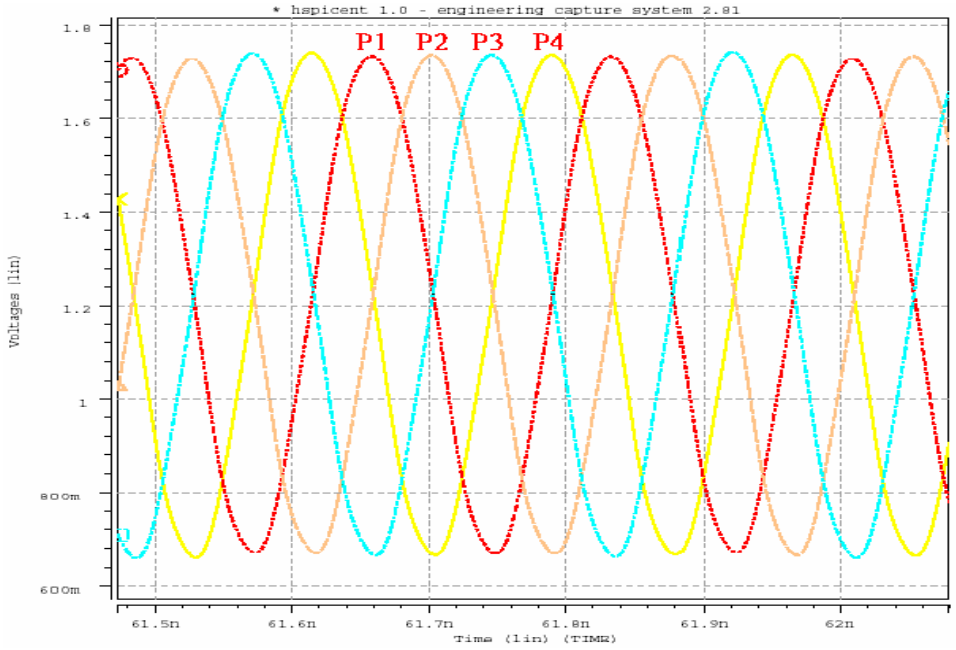


Fig. 2.29 Four phase output waveforms of quadrature VCO

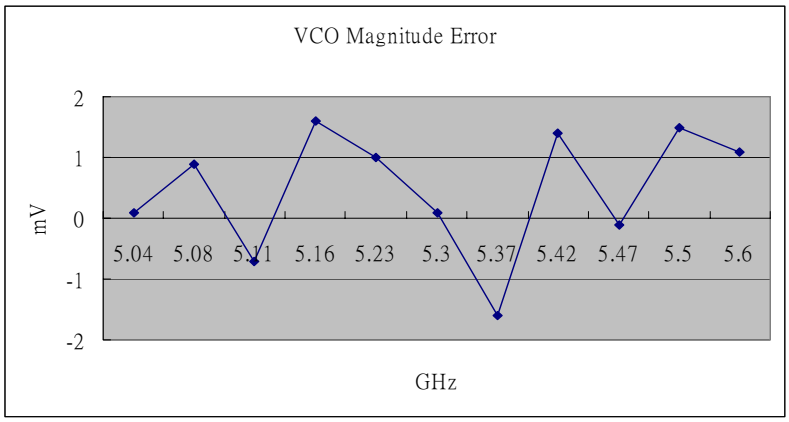


Fig. 2.30 The magnitude error of the quadrature VCO

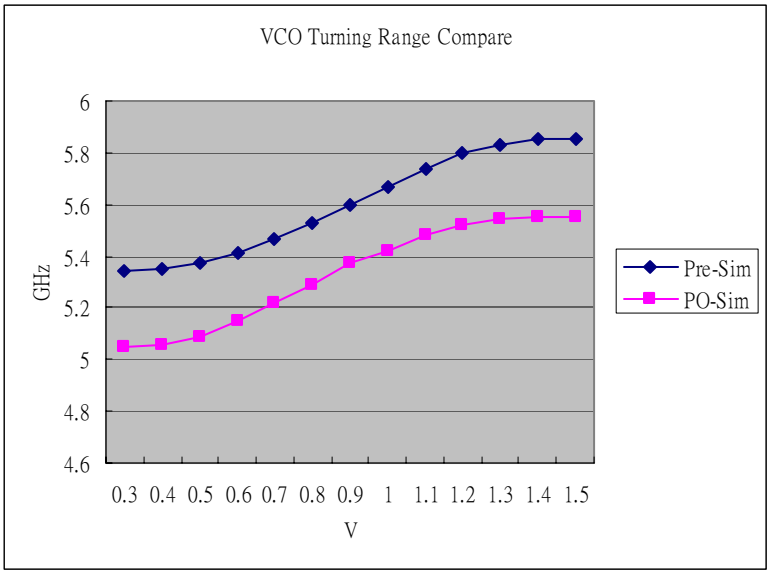


Fig. 2.31 The simulation of VCO turning range

Fig. 2.31 shows the frequency turning range of VCO. The gain of VCO at post-simulation is smaller than pre-simulation. And the VCO output frequency in post-simulation is smaller than pre-simulation be shown in Fig. 2.32

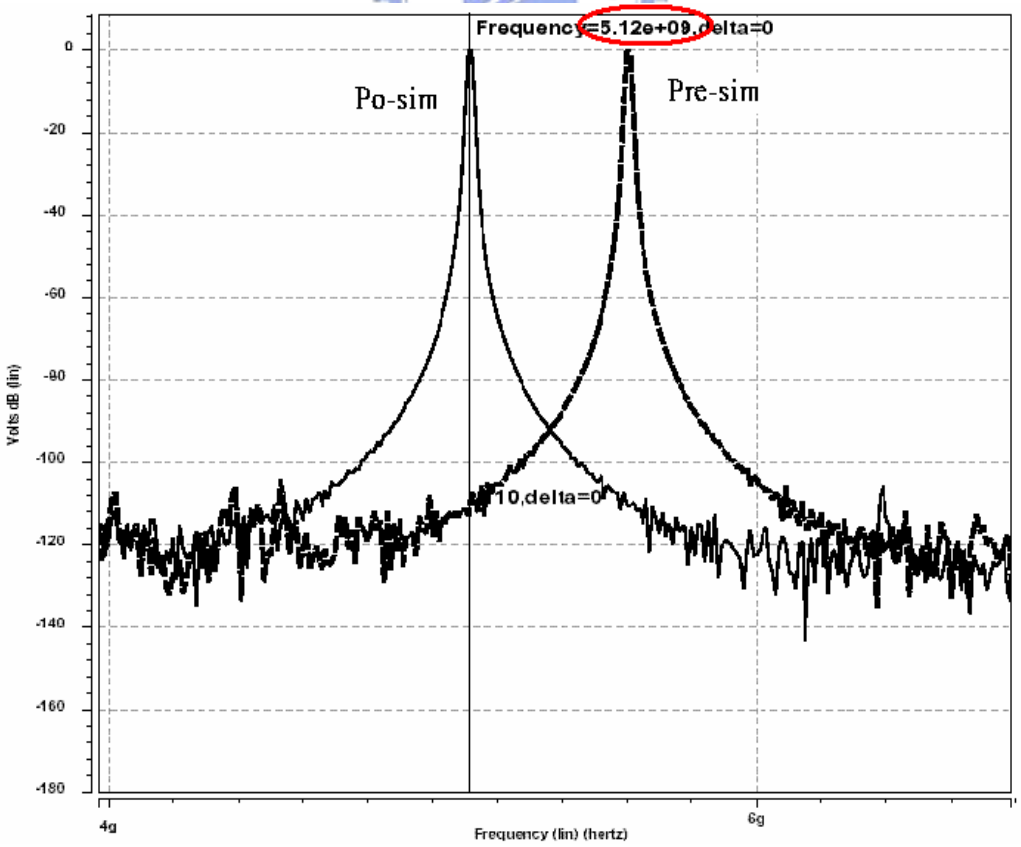


Fig. 2.32 The frequency domain simulation of VCO

Fig. 2.33 shows the phase noise of VCO. And the phase noise is -105.787dBc at 1 MHz offset.

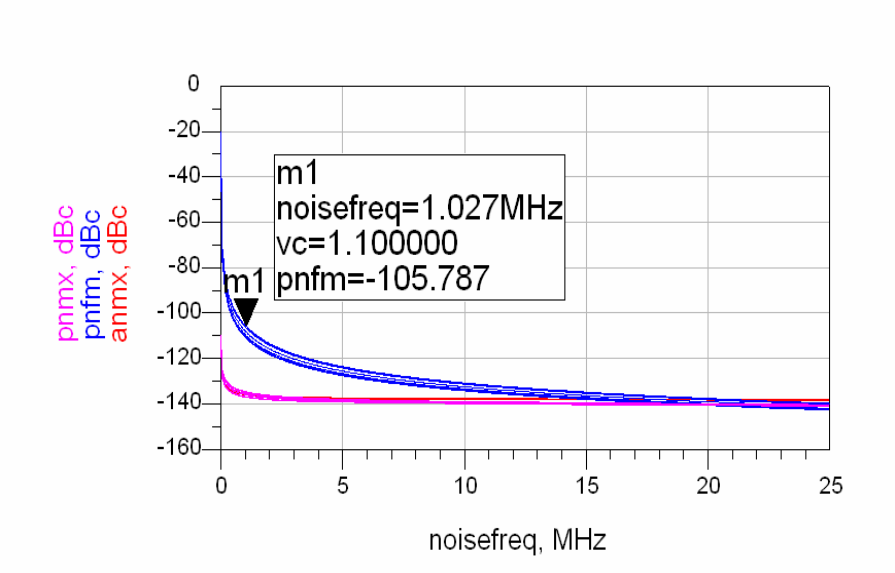


Fig. 2.33 The phase noise of VCO

In table 9, all characteristics are shown and compared after pre-simulation and post-simulation. We can see some characteristics in pre-simulation are better than post-simulation. Because some parasitic of resistances and capacitances are generated to cause the performance of VCO.

	Pre-Sim	Po-Sim
Technology	TSMC 0.18um	TSMC 0.18um
VCO Power Source	1.8V	1.8V
VCO Power Dissipation	3.8mW	3.6mW
VCO Tuning Range	5.38G ~ 5.82G (11%)	5.07G ~ 5.51G (9%)
VCO Input Voltage	0.3V ~ 1.5V	0.3V ~ 1.5V
Output Amplitude	1.1V	0.98V
Magnitude Error	3%	5%
Phase Noise	-109dBc@1MHz -118dBc@2MHz -126dBc@3MHz	-105dBc@1MHz -116dBc@1MHz -123dBc@1MHz
Kvco	500MHz/V	480MHz/V

Table 9 The summary of VCO simulation

2.3.2 Simulation results of current-match charge pump

The current matches of charge pump type 2 improved result which shows in Fig. 2.34. In the waveforms, we can see the tail current of PMOS is 500uA and the tail current of NMOS is 500uA, and they are mirrored from 1/10 time of original current source. Fig. 2.35 show the sourcing and sinking current of charge pump type 2. In the waveforms, we find the sourcing current is 506uA and sinking current is 505uA when “UP pulse” and “DOWN pulse” are on at same time, the current mismatch variation just only 1uA .

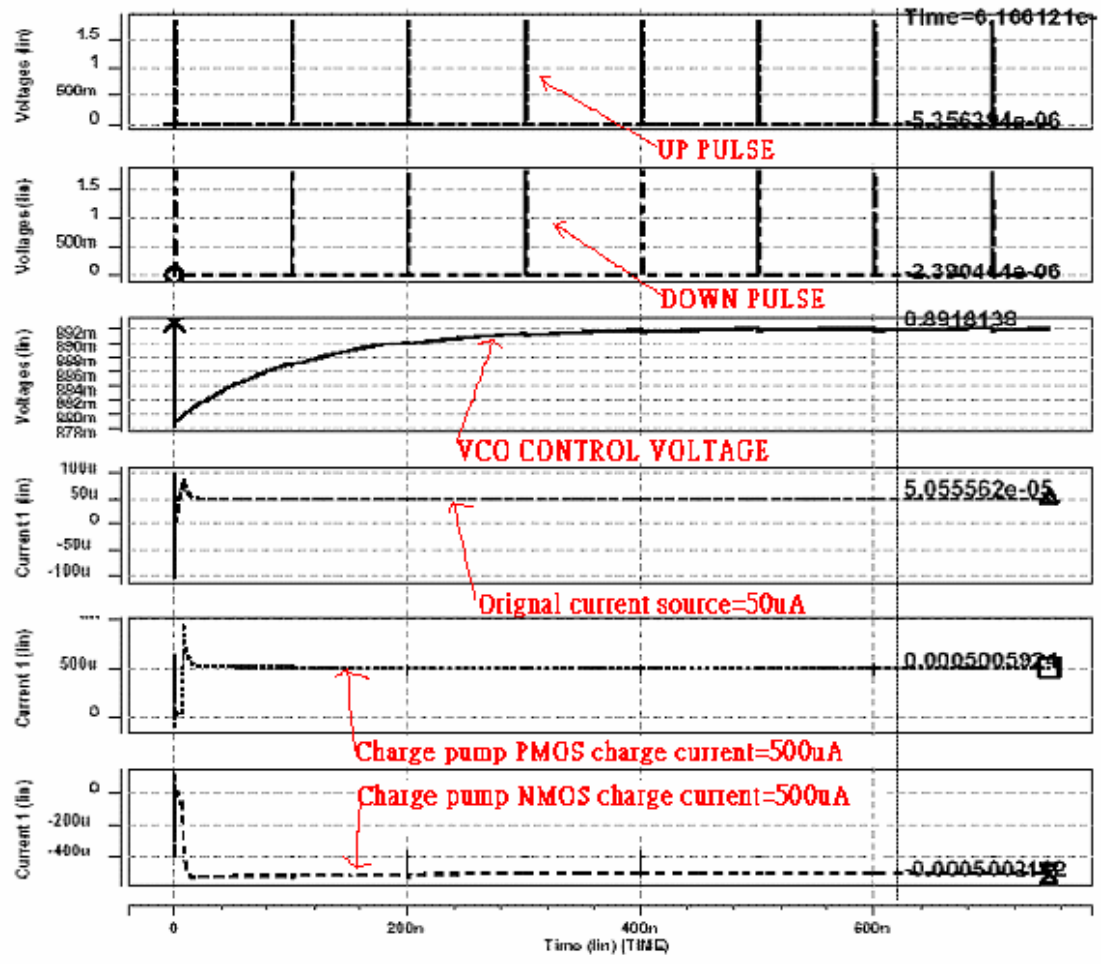


Fig. 2.34 The simulation result of charge pump 2 tail current match waveforms

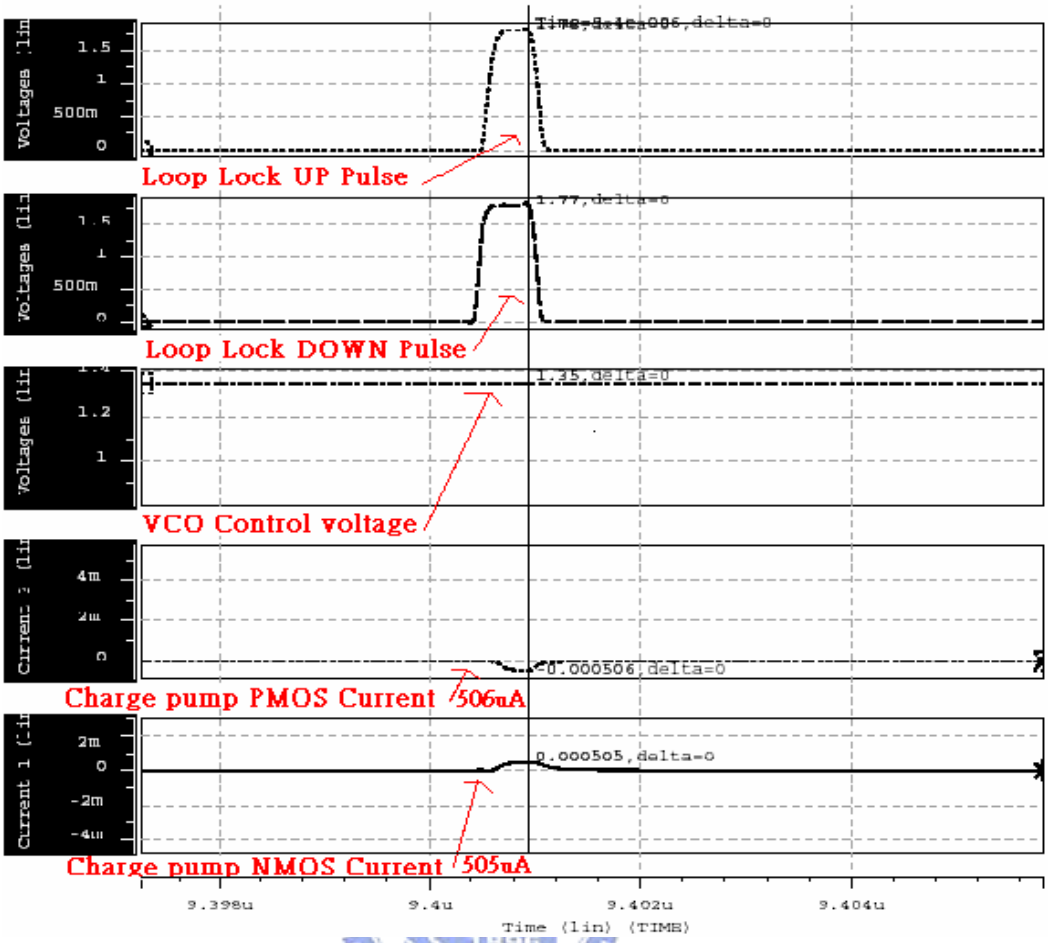


Fig. 2.35 The simulation result of current match charge pump type 2

Table 10 shows the simulation result of the rail-to-rail OP (OP1) for charge pump type 2. The results are to fit the application in charge pump type 2 output voltage with VCO input voltage. Fig. 2.36 show the distributed of gain and VCO input range.

Power Supply	1.8V
Gain	65dB
Bandwidth	85MHz
Input Range	1.6V ~ 0.2V
Output Range	1.6V ~ 0.2V
Phase Margin	68°
Power Consumption	0.7mW

Table 10 The simulation results of rail-to-rail OP for charge pump type 2

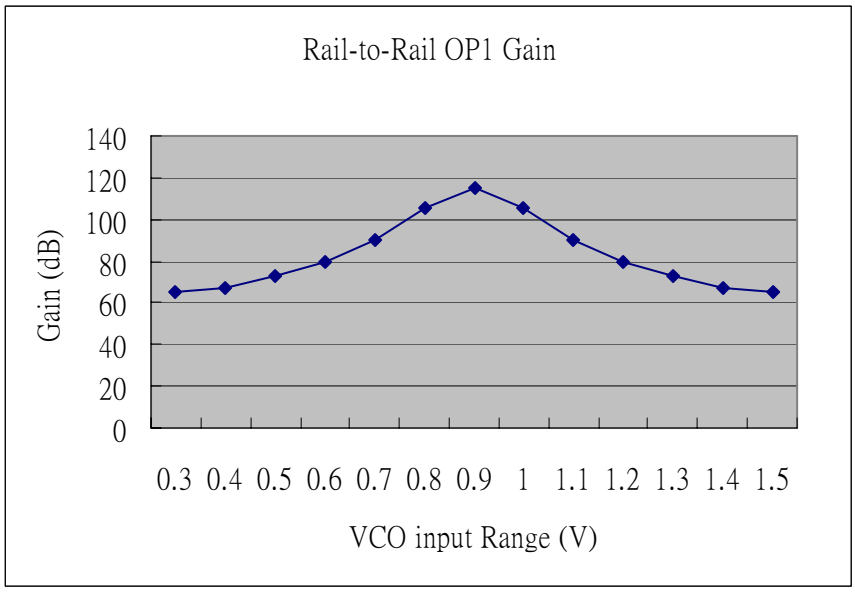


Fig. 2.36 The gain distributed of rail-to-rail OP

Following table 11 compared the simulation result and layout area about charge pump type1 and type 2. The current match characteristic of charge pump is type 2 better than type 1.

Structure	Charge Pump Type 1	Charge Pump Type 2
Power Supply	1.8V	1.8V
Control VCO Range	0.15V ~ 1.65V	0.25V ~ 1.55V
Current mismatch	< 1.6%	< 0.2%
Layout Area	0.082 mm²	0.1038mm²
Power Consumption	0.87mW	1.2mW

Table 11 Compare the simulation results of charge pump type1 and type 2

2.3.3 Simulation results of frequency divider

Fig. 2.37 shows the simulation result of divide-by-2 and prescaler divider. In the waveforms, the ÷8/9 function work correctly.

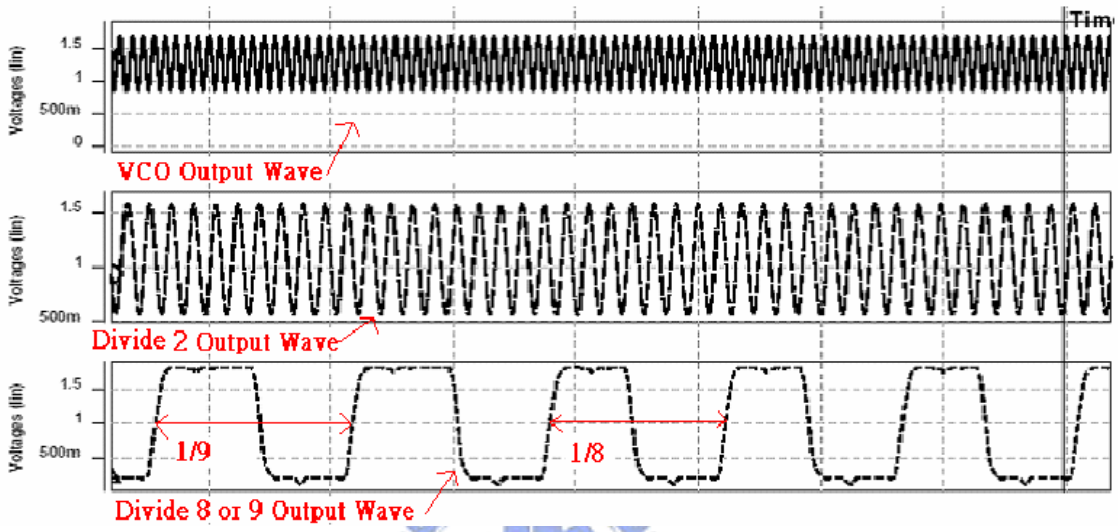


Fig. 2.37 Prescaler (÷8/9) and ÷2 simulated results.

Fig. 2.38 shows the program and swallow counters simulation results. Those functions work correctly in channel 5.

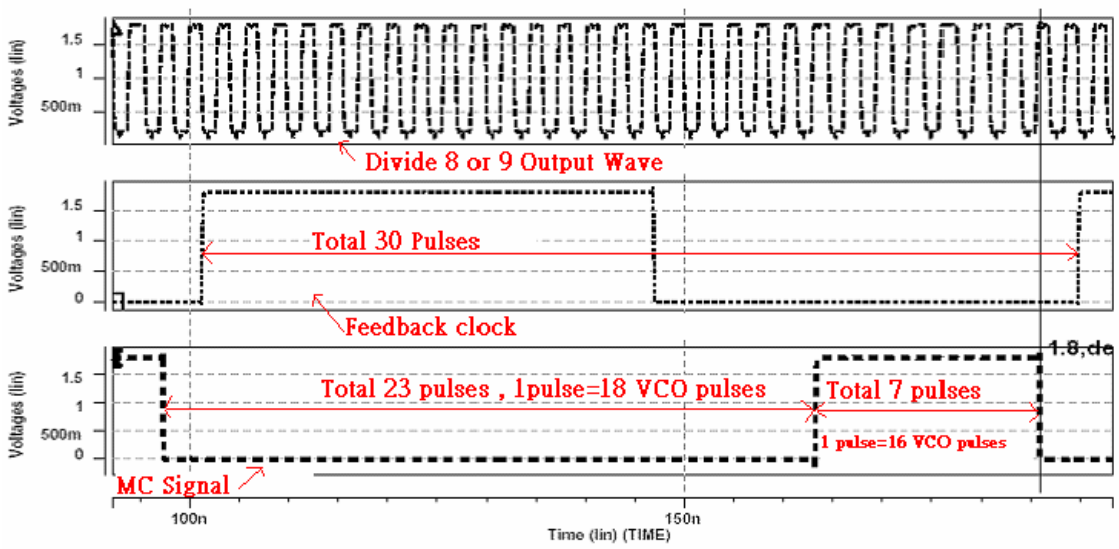


Fig. 2.38 Program and swallow counter simulation results (channel 5).

2.3.4 Simulation results of PFD

The PFD simulation result is shown in Fig. 2.39. We can see the waveforms of 3rd and 4th work correctly when input clock is fast than feedback clock which UP pulse is generated or input clock slower than feedback clock which DOWN pulse is generated. The 6th waveform is “RFCK” signal which if “RFCK” is high then make “up pulse” always low and “down pulse” always high. Opposite, the 7th waveform is “RRCK” which if “RRCK” is high then make “up pulse” always high and “down pulse” always low. Those functions applied to test charge pump current is usefully.

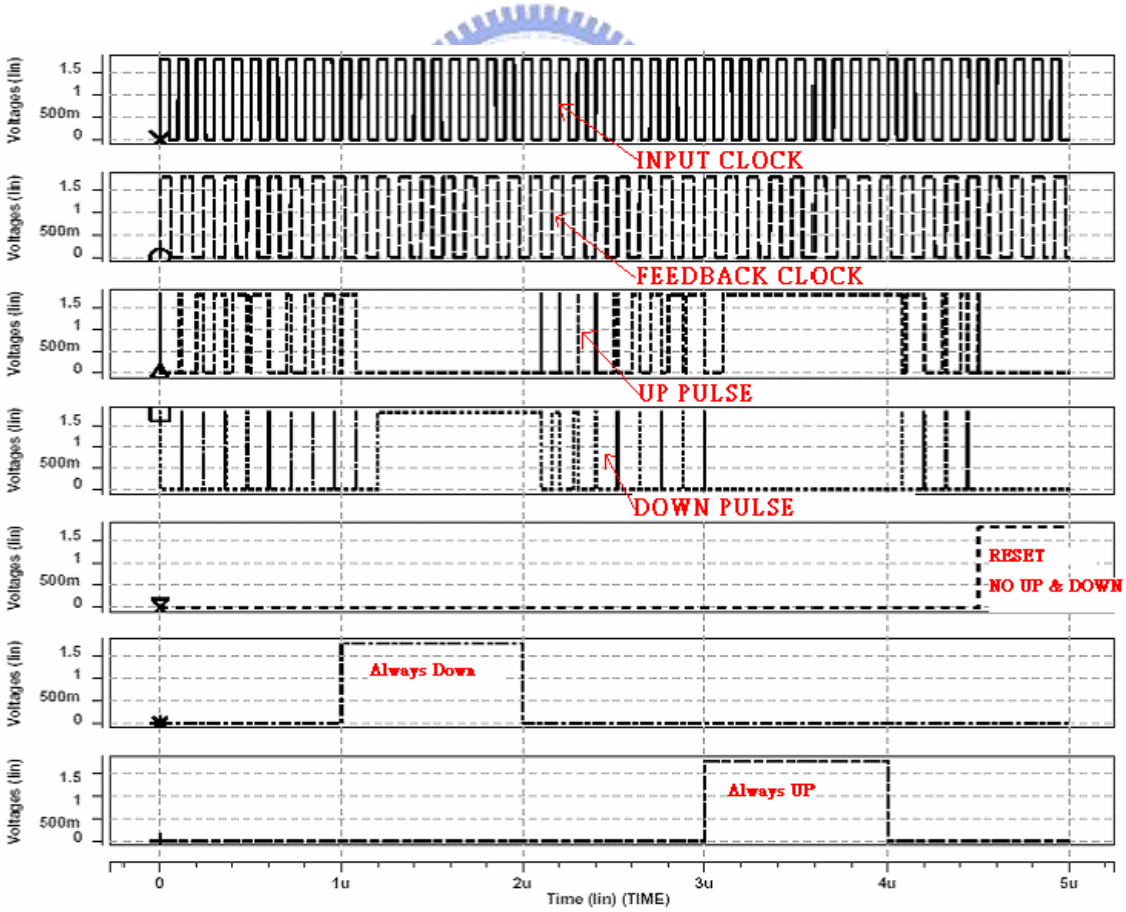


Fig. 2.39 The simulation result of PFD function

Fig. 2.40 showing the “UP” and “DOWN” pulses turn on at the same time which has perfect layout match of delay time at two paths after post-simulation. And the zero dead zone delay is 0.5nS.

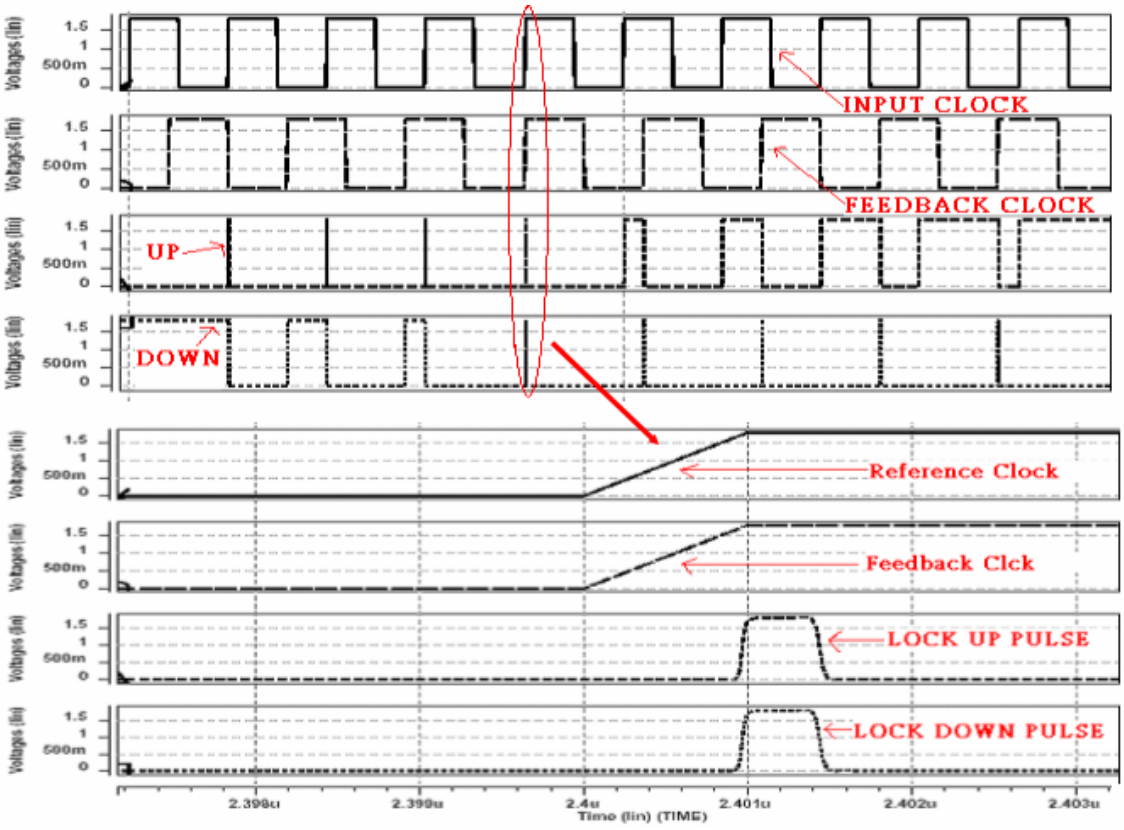


Fig. 2.40 The simulation result of PFD locks state

2.3.5 Simulation results of close loop synthesizer

Fig. 2.41 shows the settling time of close loop 1 (include charge pump type 1) of frequency synthesizer is smaller than 16uS (802.11a). Fig. 2.42 shows the synthesizer worked at channel 8, frequency is 5.32GHz.

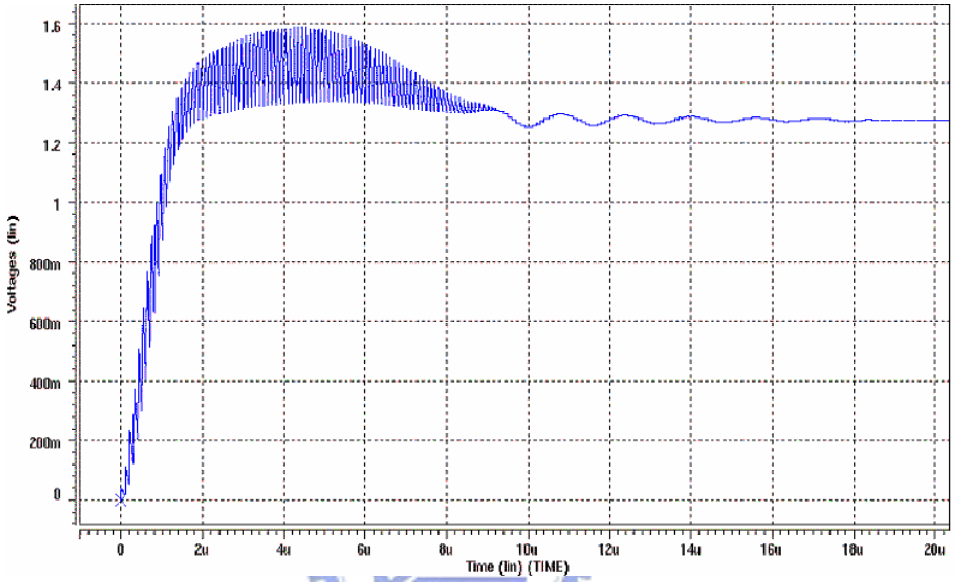


Fig. 2.41 Settling time of close loop 1 simulation of the synthesizer

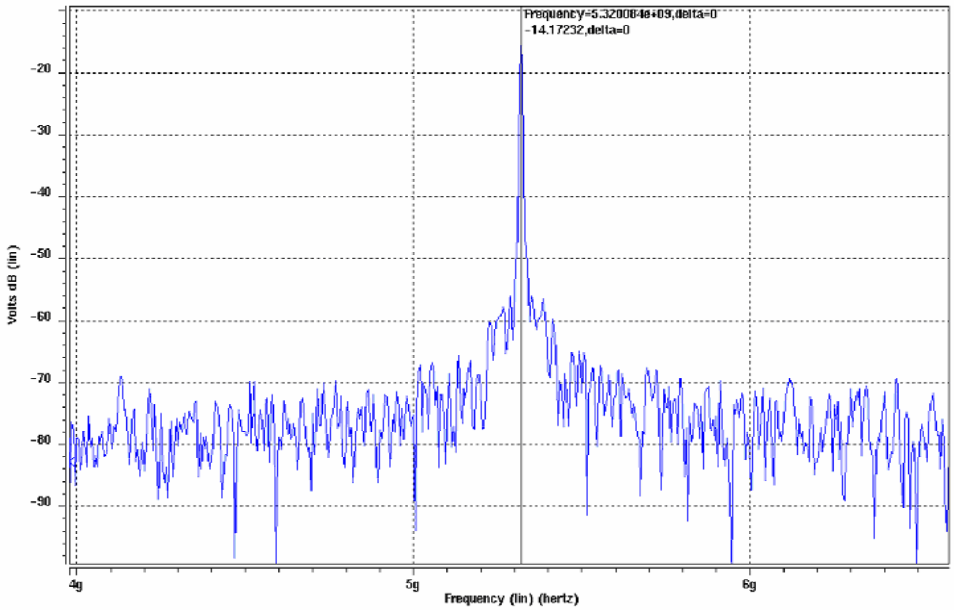


Fig. 2.42 Synthesizer loop 1 works at channel 8 that frequency is 5.32GHz.

Fig. 2.43 shows the settling time of close loop 2 (include charge pump type 2) of frequency synthesizer is small than 16uS (802.11a). Fig. 2.44 shows the synthesizer worked at channel 8, frequency is 5.32GHz.

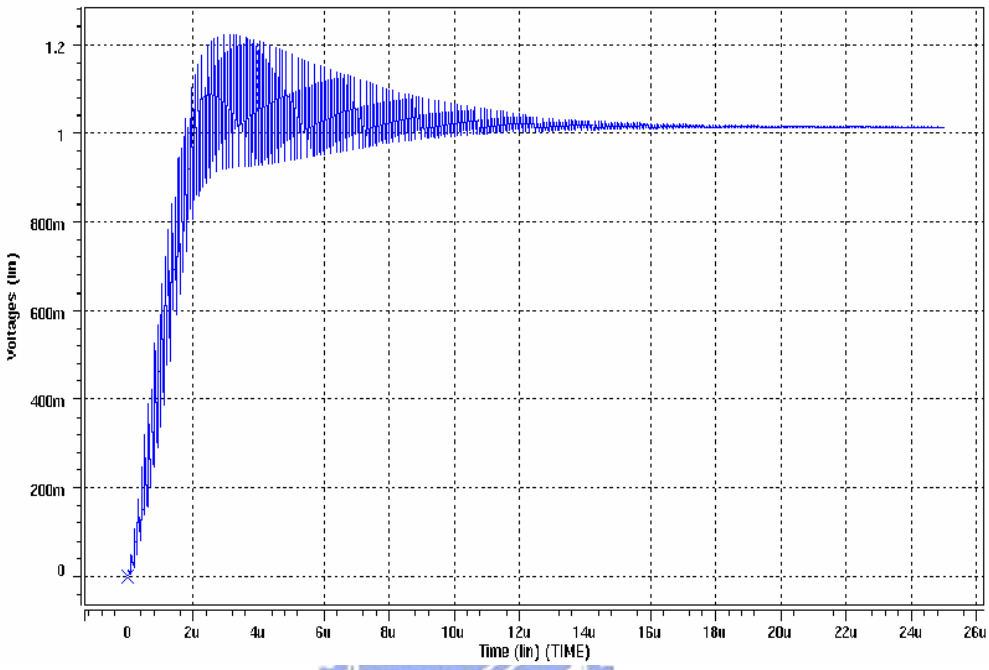


Fig. 2.43 Settling time of close loop 2 simulation of the synthesizer

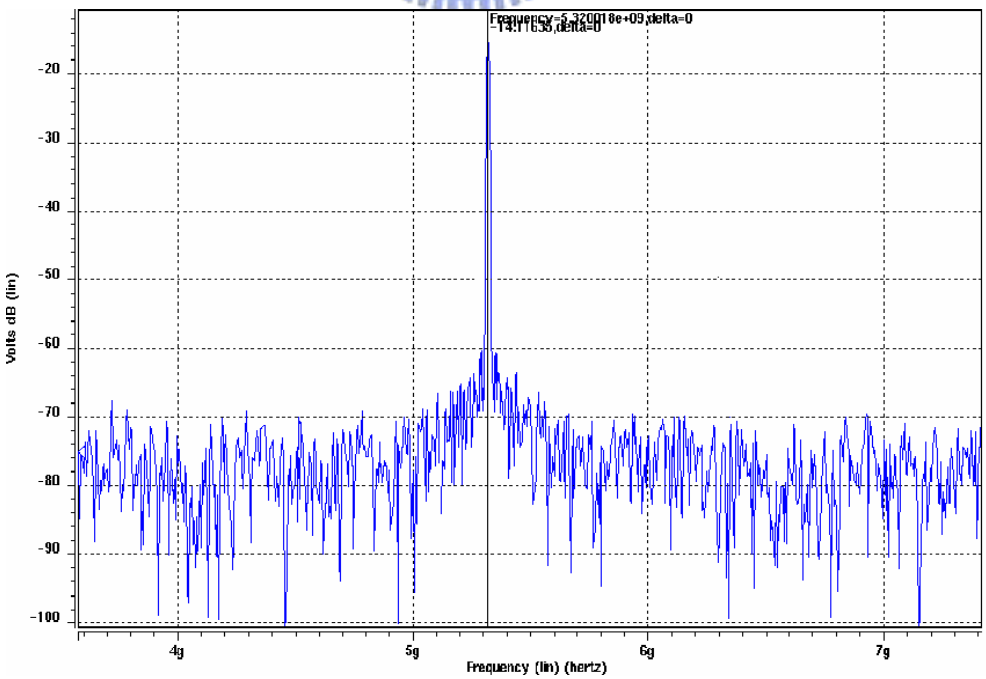


Fig. 2.44 Synthesizer loop 2 works at channel 8 that frequency is 5.32GHz.

2.4 Summary

Table 12 lists all characteristics about the simulation of frequency synthesizer in this work after added parasitical devices. Those data are measured after post-simulation. All properties close to IEEE 802.11a and have some perfect characteristics more than other structure of frequency synthesizer. The total chip area is smaller then 1 mm^2.

Synthesizer (charge pump 2) Performance:	
Synthesizer Frequency	5.07GHz ~ 5.51GHz
Reference Frequency	10MHz
LO Spacing	20MHz
Number Of Channels	8
Spur @ 10MHz	-60dBc
VCO Phase noise	-105dBc/Hz @ 1MHz
Loop Bandwidth	250KHz
Charge Pump Current	505uA
Current mismatch	<2%
Phase Margin	67°
Settling Time	< 16us
Power Dissipation:	
Supply voltage	1.8V
VCO	3.6mW
Charge Pump type 2	1.2mW
Divide-by-2 divider	9.22mW
PFD + Prescaler + Program Counter	7.4mW
Total Power	21.42mW
Implementation:	
Chip area	0.97mm²
Technology	TSMC 0.18um

Table 12 The simulation results summary of frequency synthesizer

CHAPTER 3

EXPERIMENTAL RESULTS

This frequency synthesizer has been fabricated in TSMC 0.18um 1P6M RF CMOS process. There are two loops of synthesizer be measured, one loop collocated charge pump type 1 and another loop collocated charge pump type 2. External low pass filter connected different charge pump output point to make different loop. In this measurement results, all characteristics be compared about two different loops.

Anyways, the best performance of synthesizer apply with charge pump type 2 of loop, and the phase noise is -107.36dBc @ 1MHz offset, and spurious tones is -69.52dBc @ 10MHz. Whole chip power is 18.85mW for PFD, program and swallow counter work at 1.4V power supply and another block work at 1.8V. Total layout area is 0.97mm^2. The loop settling time is smaller than 16uS.

3.1 Chip on board testing and setup

Fig. 3.1 shows the testing board that includes one chip on main board and two DC boards. The main board includes main die, four phases of VCO output and low pass filter. One of the DC board includes low path filter for power supply, channel select of jumpers, band pass filter for input reference clock and variable resisters for bias current. And another DC board includes 1.8V regulators and batteries.

Fig. 3.2 shows the testing board function block. The battery and regulator can decrease the power noise and decrease the spurious tones effectively. In the testing function block which use an AWG to generate square waveform to input to the chip and use a spectrum analyzer to measure the chip output signals. Further to test the settling time and feedback clock use two scopes to do it.

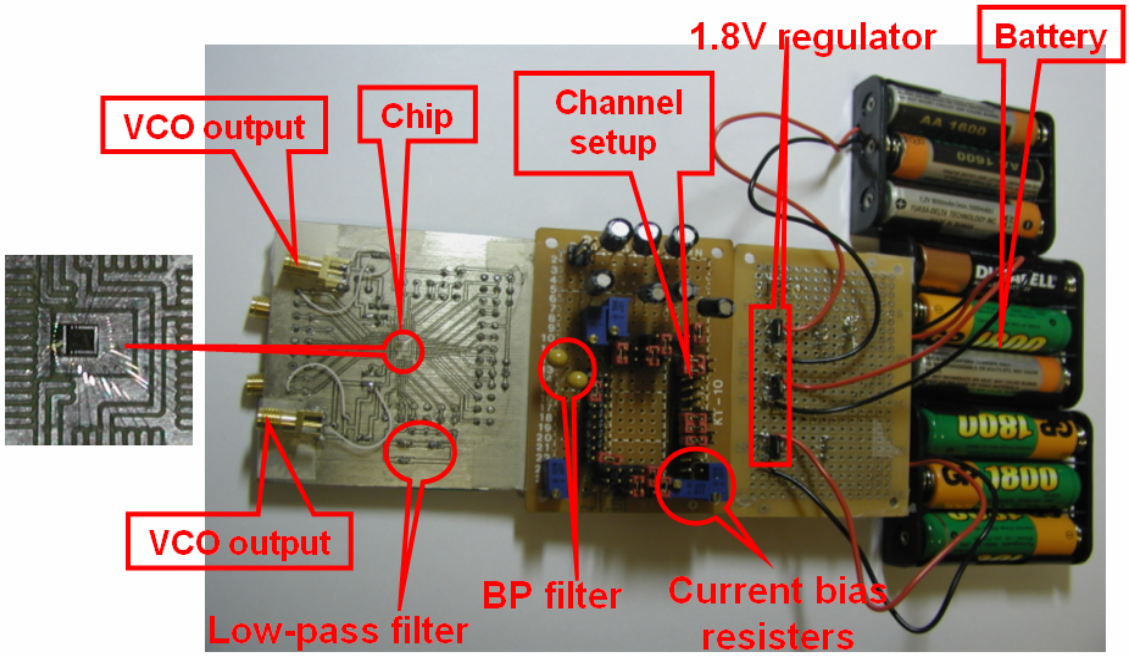


Fig. 3.1 The photo of the testing board in this work

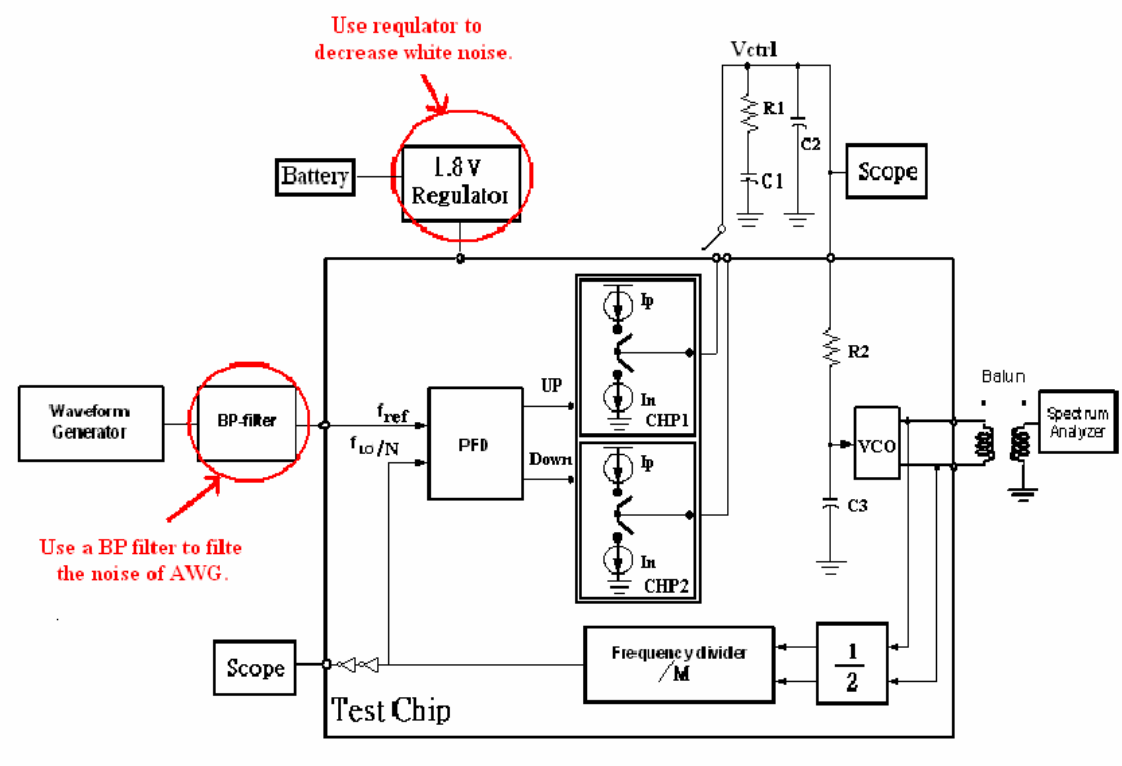


Fig. 3.2 The function block of the frequency synthesizer and testing environment

Fig. 3.3 shows the photo of main die and describes all sub-block layout places. In the photo, the main layout area consume at inductors of VCO.

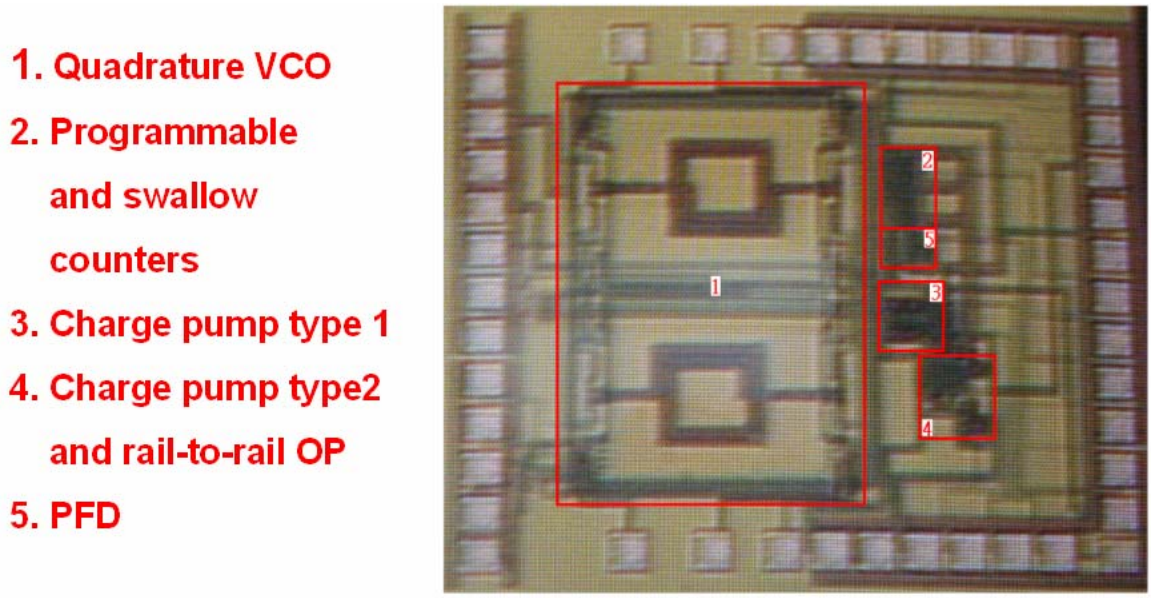


Fig. 3.3 The photo of main die in this work

3.1.1 Measure result of VCO

Fig. 3.4 shows the turning range and output frequency of the VCO. There are three gain curves variation to describe the “pre-simulation”, “post-simulation” and “measurement”. The testing curve of VCO gain is smaller then pre-simulation and post-simulation. From the testing curve to see the frequency is higher than post-simulation and frequency range is smaller than other. The K_{vco} decreases from 480 MHz in post-simulation to 450 MHz and the frequency range is 5.17 GHz ~ 5.62 GHz in measurement.

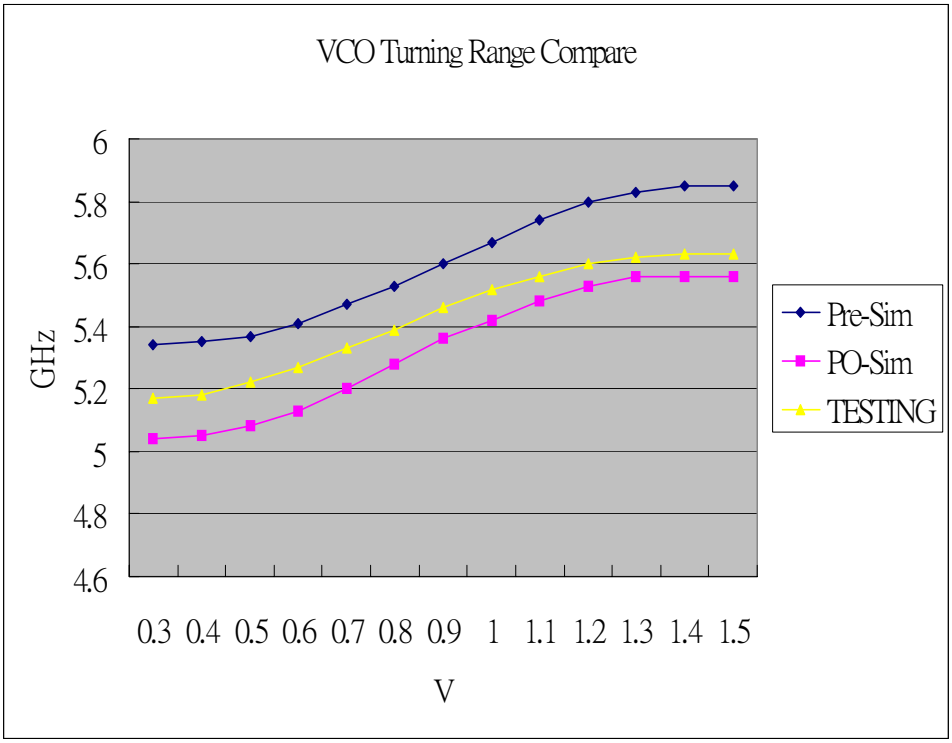


Fig. 3.4 The frequency and input turning range curves of VCO

3.1.2 Measure result of frequency synthesizer

In this work, many factors make the spurious tones had large power level. The power supply generated while noise to effect power level of spurious tones is very serious. Another noise effect power level of spurious tones is charge pump current mismatch. So, we selected three dies to measure and compare the spurious tones of power level base on different charge pump type and different power source. In table 13, that shows the measurement results of the three chips. From those chips to see that chip 1 performance bad than other chips. Maybe chip 1 is a bad die in the edge of a wafer. But the three chips have same variation for different type of charge pump and different power supply source. Summary the results, the spurious tones power level of charge pump type 2 is smaller then charge pump type1 about 1.32dBc and the spurious tones power level of using battery added regulator is smaller then only using regulator about 0.81dBc. Fig. 3.5 shows frequency response of chip 3, which use charge pump type 2 and regulator with battery of power source. The power level of spurious tones is -69.52 dBc @ 10MHz

	The Spur @ 10MHz					
	Charge Pump type1			Charge Pump type 2		
	Normal Power Supply	Regulator	Regulator + Battery	Normal Power Supply	Regulator	Regulator + Battery
Chip 1	-49.77dBc	-57.84dBc	-58.97dBc	-51.83dBc	-60.28dBc	-63.17dBc
Chip 2	-57.62dBc	-66.21dBc	-67.11dBc	-59.16dBc	-67.75dBc	-68.83dBc
Chip 3	-58.31dBc	-67.72dBc	-68.32dBc	-60.05dBc	-68.86dBc	-69.52dBc

Table 13 The measurement results of spurious tones

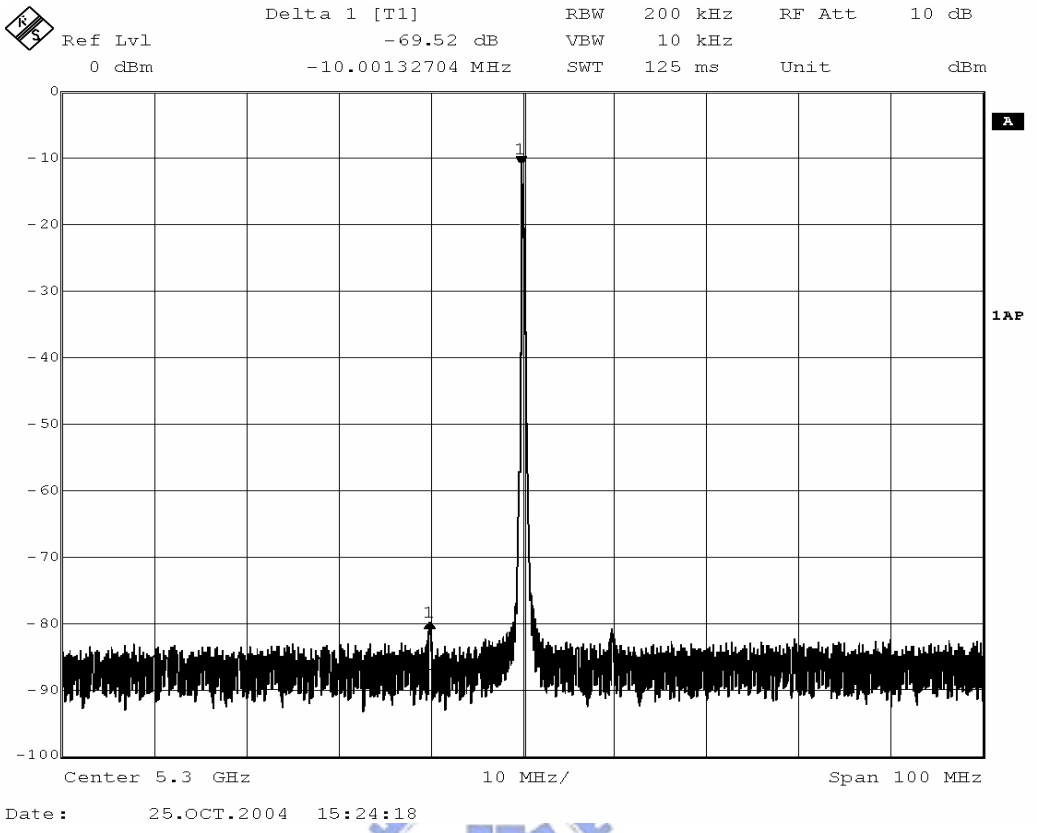


Fig. 3.5 The power level of spurious tones is channel 7 for charge pump2 and the power source is battery with regulator

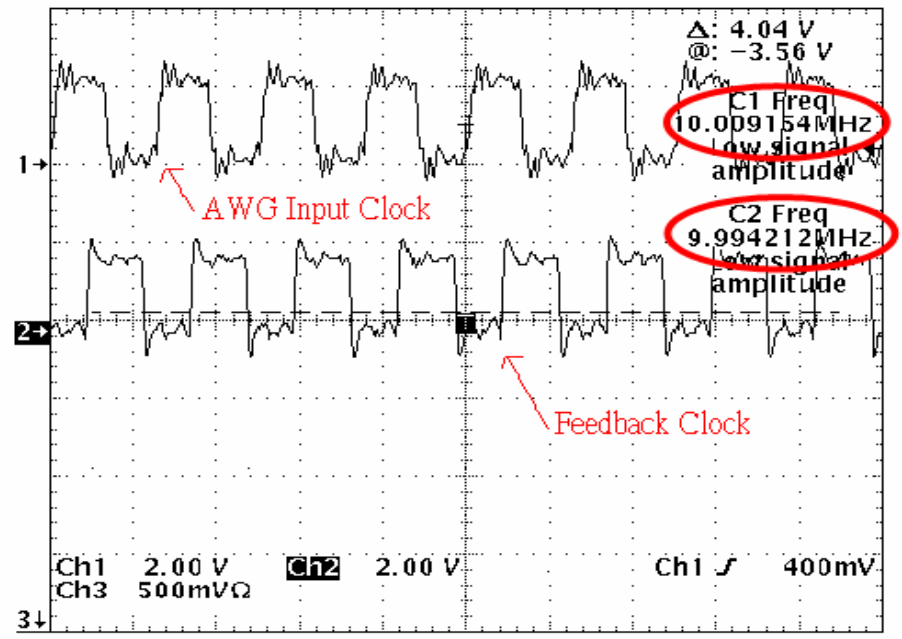


Fig. 3.6 The measurement result of feedback clock

Fig. 3.6 shows the reference clock and feedback clock in PLL locked state. Ideally, the rising edge of reference clock with the rising edge of feedback clock active at same time in locked state, but the waveforms in Fig. 3.6 have some delay time between reference clock (AWG input) and feedback clock. Why? Because the feedback clock close to 10 MHz which need some buffer to drive the testing PAD for easy to test. In Fig. 3.6, the measurement results of reference clock and feedback clock are the same which close to 10 MHz. So, the loop is locked.

Table 14 shows the output range and current variation of charge pump type 1 and type 2. The charge pump type 2 has perfect current match but that has small output range and large power consumption and layout area.

Fig. 3.7 shows the settling time of synthesizer in close loop for charge pump type 2. The measurement probe of scope needs an active probe. The measurement result of the settling time is 13.5uS that use active probe to test. It meets the specification of IEEE 802.11a which is smaller than 16uS.

Fig. 3.8 shows the frequency synthesizer phase noise for charge pump type 2. The measurement result of phase noise is -107.36 dBc @ 1MHz offset.

	Simulation	Measurement	Simulation	Measurement
Structure	Charge Pump Type 1	Charge Pump Type 1	Charge Pump Type 2	Charge Pump Type 2
Control VCO Range	0.15V ~ 1.65V	0.2V~1.6V	0.25V~1.55V	0.4V~1.4V
Channel Select Range	1 ~ 8	1 ~ 8	1 ~ 8	2 ~ 8
Current Mismatch	< 1.6%	< 2.1%	< 0.2%	< 0.5%
Layout Area	0.082mm^2	0.082mm^2	0.1038mm^2	0.1038mm^2
Power Consumption	0.87mW	1.01mW	1.2mW	1.5mW

Table 14 The measurement results of charge pump type 1 and type 2

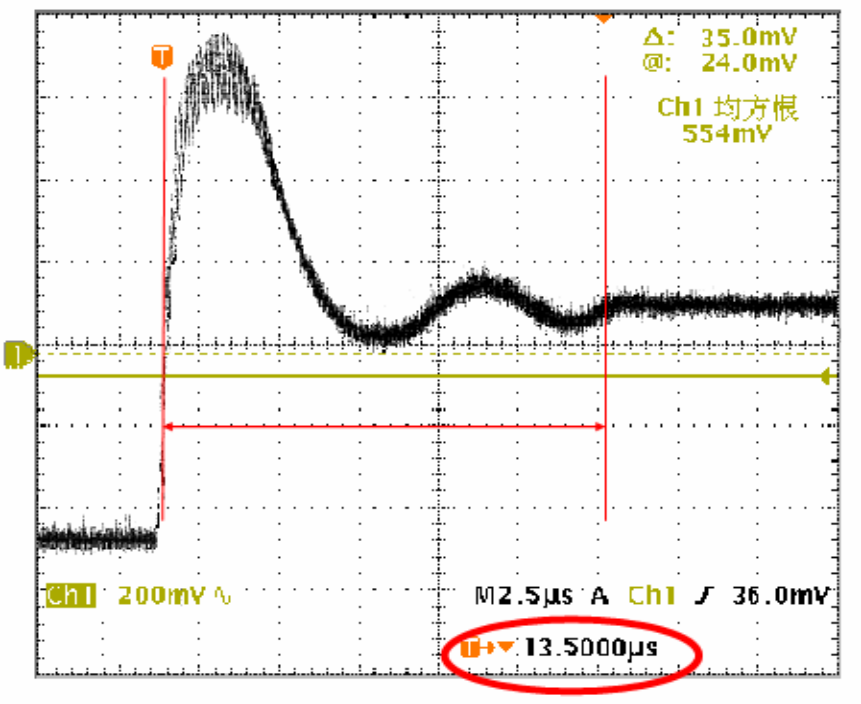


Fig. 3.7 The measurement result of settling time in close loop (charge pump type 2)

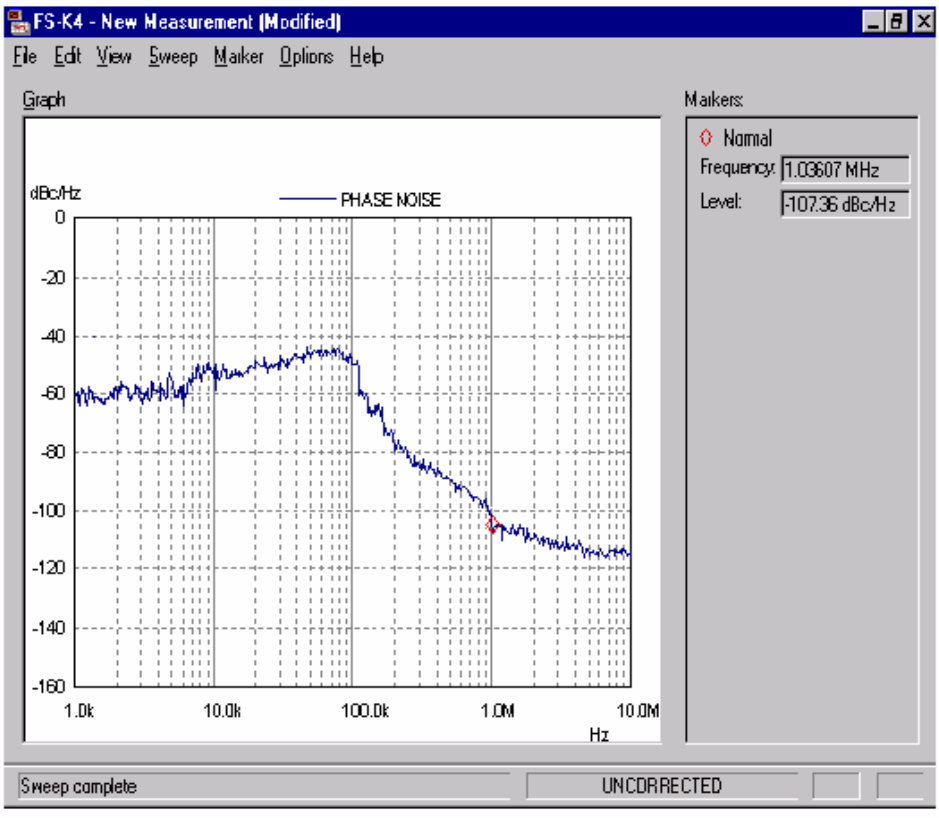


Fig. 3.8 The measurement result of phase noise in 1 MHz offset (charge pump type 2)

3.2 Comparison

Table 15 compares all characteristics in this work with another three papers of 5 GHz frequency synthesizer. In this work, the charge pump current is larger than other 10 time to get fast settling time in wide loop bandwidth. In [2], the loop bandwidth design in narrow band to get low spur power level, but it's settling was too slow. In [1], the synthesizer never used current match charge pump and the spur power level was highest. Another to bring up in [1] is large layout area which used ILFD divider. In [4], the synthesizer applied a current match charge pump to get low power level of spur. Anyway, this work performance meets IEEE.802.11a and has perfect current match structure of charge pump.

Synthesizer Performance:							
	This Work (Charge pump type 1)		This Work (Charge pump type 2)		[1]	[2]	[4]
Synthesizer Frequency	5.15 ~ 5.62GHz		5.19 ~ 5.62GHz		4.84 ~ 4.994GHz	5.14 ~ 5.7GHz	5.5GHz
Reference Frequency	10MHz		10MHz		11MHz	10MHz	43MHz
LO Spacing	20MHz		20MHz		22MHz	20MHz	N.A.
Phase Margin	67°		67°		46°	N.A.	55°
Phase noise (@ 1MHz)	-106.84dBc/Hz		-107.36dBc/Hz		-101dBc/Hz	-110dBc/Hz	-116dBc/Hz
Loop Bandwidth	250KHz		250KHz		280KHz	30K.	<140K.
Charge Pump Current	501uA ± 8.1uA		503uA ± 2.5uA		50uA	50uA	50uA
Current mismatch	1.6%		0.5%		--	--	--
Spur @ Fref	-68.32dBc		-69.52dBc		-45dBc	-70dBc	-69dBc
Settling Time	14.8us		13.5us		N.A.	100us	N.A.
Power Dissipation:							
Supply voltage	1.8V	1.8V / 1.4V	1.8V	1.8V / 1.4V	Analog 1.5V/ Digital 2V	2.5V	1.5V
VCO	3.3mW		3.3mW		3mW	6.25mW	6.9mW
Charge Pump	1.01mW		1.5mW		N.A.	N.A.	N.A.
Divide-by-2 stage	8.9mW		8.9mW		0.8mW	6.25mW	10.5mW
PFD + Swallow and Program Counter	6.6mW (1.8V)	5.1mW (1.4V)	6.6mW (1.8V)	5.1mW (1.4V)	19mW	1mW	>5.6mW
Total Power	19.8mW	18.3mW	20.3mW	18.8mW	25mW	13.5mW	23mW
Implementation:							
Die area	0.948mm²		0.97mm²		1.6mm²	0.55mm²	>1mm²
Technology	TSMC CMOS 0.18um		TSMC CMOS 0.18um		CMOS 0.24um	CMOS 0.25um	CMOS 0.25um
Structure							
Current match CHP	Yes		Yes		No	N.A.	Yes
Divide-by-2 divider	Pseudo-NMOS DFF		Pseudo-NMOS DFF		ILFD	TSCP	SCL

Table 15 Compare all characteristics of frequency synthesizer

3.3 Discussion

After designed and measured the frequency synthesizer, there are some functions which need to improve even more batter. So, in this section have some discussions to bring up.

(1) How does the synthesizer to solve the variation of the output range in charge pump type 2?

(2) In this work, the performance of spur level is smaller than [2]. Why?

(3) The power consumption still larger than [2].

(4) The charge pump type 2 still has some different about current mismatch in simulation and measurement.

In discussion (1), the charge pump type 2 could not work at wide output range for VCO. Because the MOS *Vt* has some variation which makes the NMOS working at triode region and lets output range of charge pump type 2 smaller than simulation results. The current mismatch makes the spur level increasing when output voltage is below 0.4V which shows in table 14. Using an active low pass filter can solve the problem [24], but the active low pass filter has larger layout size and power computation, so it need be design in off-chip. Fig. 3.9 shows the active low pass filter circuit. Anyway, the output voltage of charge pump has not varied, and the positive terminal is fixed at half of *VDD* or other optimum voltage for lower affect of channel length modulation about PMOS and NMOS. This way need an OP and passive devices of resisters and capacitors to combine an active low pass filter. In this application, using a National Semiconductor's rail-to-rail OP "LMV931" can

prove the active low pass filter which let $V_b = V_{op}$ to reduce the effect of channel length modulation. The measurement results are showing in table 16.

In discussion (2), the loop bandwidth was designed in 0.12 time of this work. So, the [2] had perfect characteristic of spur level. But the design of [2] lost the settling time of condition which it can not apply in specification of IEEE.802.11a. If the circuit of low pass filter be merged in the chip, than it will need large layout area.

In discussion (3), the structure of divide-by-2 of TSPC is good chaise in application of high speed and low power consumption in [2]. But the structure has high/low duty cycle unbalance that duty cycle is 25% in worse case, and the single signal of structure difficult to work in quadrature phase output of VCO for low noise issue. Other brings up problem of TSPC structure could not work to 5.5 GHz at simulation in TSMC process. So, this work chooses another structure of divide-by-2 is Pseudo-NMOS gate.

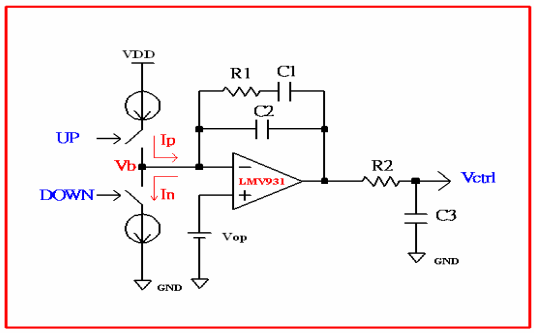


Fig. 3.9 The active low pass filter apply in charge pump output

	Measurement	Measurement
Structure	Charge Pump Type 2	Charge Pump Type 2
Low Pass Filter Type	Passive	Active
Control VCO Range	0.4V~1.4V	0.2V~1.6V
Channel Select Range	2 ~ 8	1 ~ 8

Table 16 Measurement results of synthesizer using active low pass filter

In discussion (4), the process variation makes a little current mismatch in charge pump type 2 UP/DOWN current at simulation and measurement. In Fig. 3.10 and Fig. 3.11 show the simulation results of process variation makes threshold voltage *Vt* has some variation which makes current mismatch in charge pump type 2. If *Vt* has variation -4% then current has variation from 500uA to 502.5uA and current mismatch is 0.49%. But the current mismatch effect the spur level is too small which can ignore it.

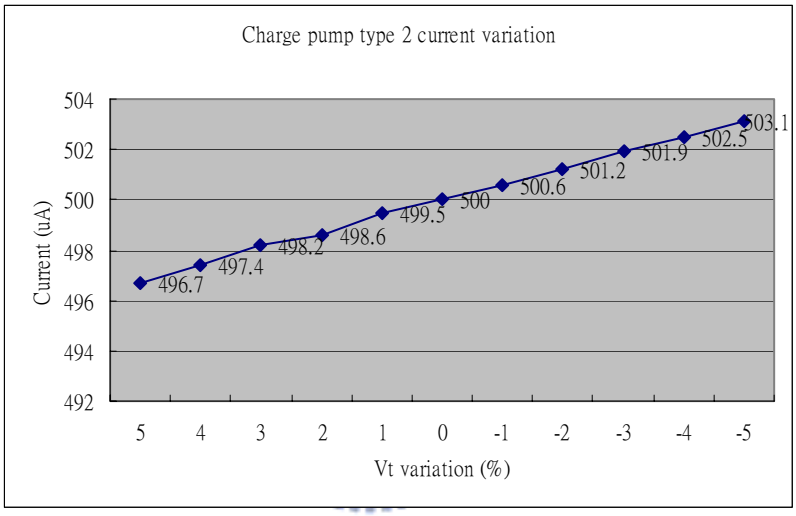


Fig. 3.10 The variations of charge pump current and *Vt*

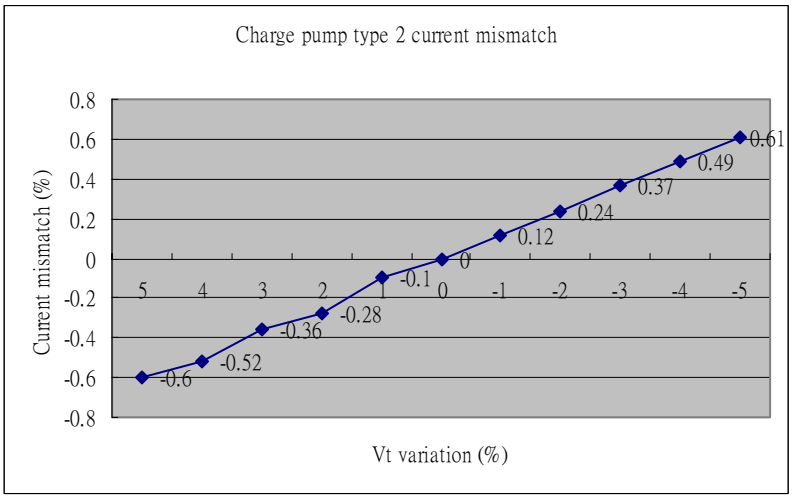


Fig. 3.11 The current mismatch with *Vt* variation

CHAPTER 4

CONCLUSIONS AND FURTURE WORKS

4.1 Conclusions

A low spurious tone of 5 GHz CMOS frequency synthesizer for wireless LAN transceivers has been presented. The synthesizer integrated in a 0.18um CMOS technology consumes only 18.8mW in 1.8V/1.4V power supply. This work includes a quadrature VCO and Pseudo-NMOS of divide-by-two latch. All chip layout area smaller than 1mm^2. The PLL working frequency reaches 5.628GHz and loop phase noise is -107dBc at 1 MHz offset. The close loop of settling time is 13.5uS to meet specification of IEEE.802.11A.

Two perfect current matches of charge pump circuits are implemented and compared in this work. One is a current-steering of charge pump and another is a new current-switching of charge pump. Compare the measurement results of those two types of charge pump circuits to found the new current-switching has perfect current match characteristic more than current-switching charge pump. The spurious tones of new current-switching charge pump circuit can be suppressed to -69.52 dBc at 10 MHz offset. The new charge pump circuit can effectively suppress the spurious tones successfully.

4.2 Future works

Although the new charge pump can suppress the spurious tones effectively. But some application of wide input range of VCO can not work correctly. And the total power consumption still large more, because large part of power dominate at divide-by-two block. Another bring up problem is chip integration of SOC; this work could not merge low pass filter circuit in chip. So, some future works is list following:

(1) Re-design the chip working on low power supply to reach low power consumption; maybe the power supply is lower than 1V.

(2) Use active low pass filter to apply in wide input range of VCO to decrease the effect of channel length modulation.

(3) Develop another structure of divider for lower power and high speed application.

(4) Merge low pass filter circuit to reach real SOC.

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簡　歷

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