High-Performance InGaZnO Thin-Film Transistors Using HfLaO Gate Dielectric

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***Abstract*—In this letter, we report a low-voltage-driven amorphous indium–gallium–zinc oxide thin-film transistor with a high-κ-value HfLaO gate dielectric. Good characteristics were achieved including a low V_T of 0.22 V, small subthreshold swing of 76 mV/dec, high mobility of 25 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, and large $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of 5×10^7. These good performances are obtained at an operation voltage as low as 2 V. These characteristics are attractive for high-switching-speed and low-power applications.**

***Index Terms*—Amorphous indium–gallium–zinc oxide (a-IGZO), equivalent oxide thickness, HfLaO, high-κ, thin-film transistors.**

I. Introduction

After Nomura *et al.* [1], [2] demonstrated the transparent and flexible TFTs using novel amorphous indium–gallium–zinc oxide (a-IGZO), the a-IGZO TFTs [2]–[15] have attracted lots of attention for potential application in high drive current and large-area display with a low cost. This high transistor current is particularly required to drive high-resolution active-matrix organic light-emitting-diode displays [3], [4]. Compared to the Si-based counterpart, a-IGZO TFTs can provide the merits of both amorphous-Si and polycrystalline-Si TFTs, i.e., even in the amorphous phase, a-IGZO TFTs still exhibit high mobility comparable with polycrystalline-Si TFTs, and the amorphous property of IGZO channel also helps to reduce the nonuniformity of mobility and threshold voltage (V_T). Moreover, a-IGZO TFTs can be processed with a significantly low thermal budget, and therefore, they can be used in emerging applications such as flexible displays and low-cost flexible ICs [2]–[15].

To improve the device performance, low V_T and small subthreshold swing (SS) are required. These can be achieved by controlling the device process, such as oxygen partial pressure, deposition pressure, IGZO composition, channel thickness, and anneal temperature [5]. Incorporating high-κ gate dielectric into TFT provides alternative solution to reach these goals [16]–[18]. In this letter, we report the high-performance a-IGZO TFT using high-κ HfLaO gate dielectric. The HfLaO also shows less Fermi-level pining than $\mathrm{HfO_2}$ [19]–[21], owing to unique negative flatband voltage of $\mathrm{La_2O_3}$ [22] for low V_T n-MOS devices. Our HfLaO IGZO TFT also permits low-voltage operation with low power consumption for portable display application.

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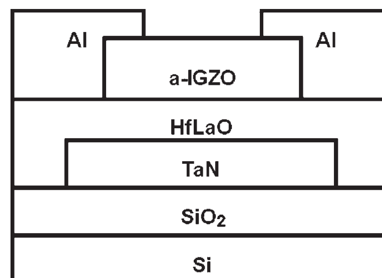

Fig. 1. Schematic diagram of the a-IGZO TFT with HfLaO gate dielectric.

II. Experiments

The devices were fabricated on the insulated $\mathrm{SiO_2/Si}$ substrate. A 50-nm TaN was first deposited by reactive sputtering. After gate patterning, the TaN surface was treated by $\mathrm{NH_3^+}$ plasma that is important to reduce gate leakage current [17], [18], [23]. Then, a 300-nm HfLaO gate dielectric was deposited by PVD at room temperature, followed by a 400 °C $\mathrm{O_2}$ annealing for 5 min. The gate dielectric is preferred to form by PVD for its low process temperature, particularly when a plastic substrate is used [2], [18], [24]. Next, 40-nm IGZO channel layer was deposited by sputtering from a ceramic IGZO target $(\mathrm{Ga_2O_3 : In_2O_3 : ZnO} = 1:1:1)$ in a gas mixture with a 5% $\mathrm{O_2}$ in Ar. Then, Al source/drain electrodes of 300 nm were deposited and annealed at 300 °C under $\mathrm{N_2}$ ambient. Here, metal masks were used to pattern the device. The metal–insulator–metal capacitors were also fabricated side-by-side to characterize the gate capacitance and leakage current. The devices were characterized by current–voltage $(I–V)$ and capacitance–voltage $(C–V)$ measurements using HP4156C semiconductor parameter analyzer and HP4284A precision LCR meter, respectively.

III. Results and Discussion

Fig. 1 shows the schematic cross-sectional view of the a-IGZO TFT, where bottom gate device structure is used. The $C–V$ and $J–V$ characteristics of the TaN/HfLaO/Al gate capacitors are shown in Fig. 2(a) and (b), respectively. The measured high capacitance density of 5.1 $\mathrm{fF}/\mu\mathrm{m}^2$ gives an equivalent oxide thickness of 7 nm and a high-κ value of 25

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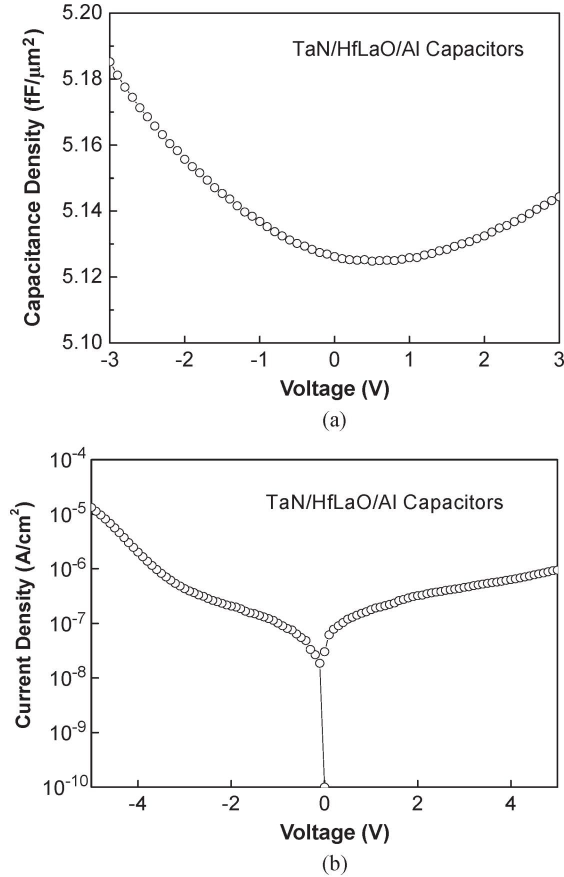

Fig. 2. (a) C–V and (b) J–V characteristics of TaN/HfLaO/Al capacitors.

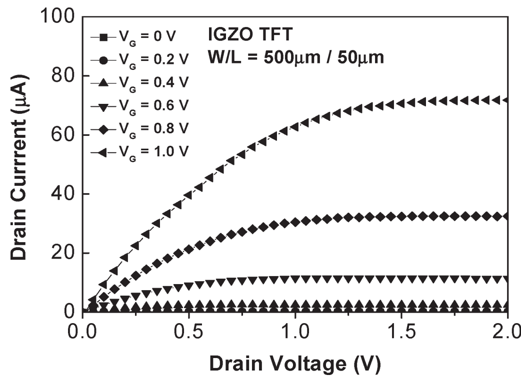

Fig. 3. Output characteristics of an a-IGZO TFT with HfLaO gate dielectric. The device size is 50 μm $\times$ 500 μm.

in HfLaO dielectric. Such large gate capacitance density can benefit the transistor drive current, lower down the operation voltage, and improve the $I_{\mathrm{on}}/I_{\mathrm{off}}$. A low leakage current of 5.7×10^{-7} A/cm^2 at 2 V was also measured due to the large 30-nm thickness.

The output I_D–V_D characteristics of the high-κ HfLaO/a-IGZO TFT is shown in Fig. 3. Well-behaved transistor characteristics were observed even under a low operation voltage of 2 V, which is important for low-power application.

Fig. 4 shows the transfer I_D–V_G characteristics of the high-κ HfLaO/a-IGZO TFT. The μ_{FE} and V_T were determined from the linear $I_D^{1/2}$ versus V_G plot. Excellent low SS of

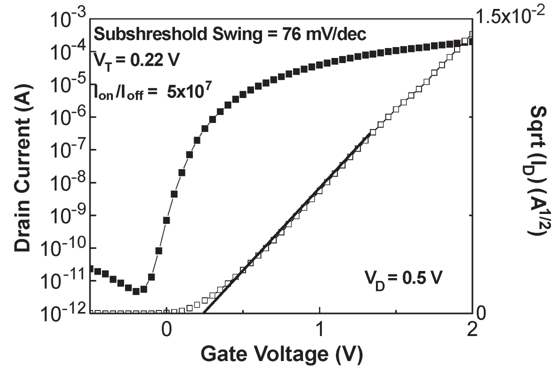

Fig. 4. Transfer characteristics of an a-IGZO TFT with HfLaO gate dielectric. The device size is 50 μm $\times$ 500 μm.

TABLE I
COMPARISON OF IGZO TFTS WITH VARIOUS GATE DIELECTRICS

Gate dielectric	Operating voltage (V)	V_T (V)	μ_{FE} (cm^2/Vs)	SS (V/decade)	I_{on}/I_{off}	μCi (μA/V^2)
HfLaO [This work]	2	0.22	25	0.076	5×10^7	12.6
[a]SiO_2 [5]	30	1.01	51.7	0.25	1.88×10^8	1.2
SiO_2 [6]	1.5	~0.11	3.1	0.063	$>10^8$	0.16
AlTiO [7]	20	1~2	11~15	0.2~0.25	$>10^7$	0.6
[b]SiO_2 [8]	10	0.5	104	0.25	$>10^8$	10.2
[c]Si_3N_4 [9]	20	3.25	5.1	0.68	3×10^7	0.12
Si_3N_4 [10]	20	5	10	0.23	$>10^8$	0.52
SiO_2 [11]	30	2	24.5	-	6×10^7	0.56
SiO_2 [12]	30	5.9	35.8	0.59	4.9×10^6	0.82
[d]Si_3N_4/TiO_2 [13]	30	5	9.9~1.8	0.22	3×10^7	0.16
$Ba_{0.5}Sr_{0.5}TiO_3$[14]	3	0.5±0.1	10±1	0.06±0.01	8×10^7	1.12
Y_2O_3 [15]	6	1.4	12	0.2	~10^8	1.24

[a]GIZO=1:2:2, P_{dep}=0.7 Pa, d_s=40nm, P_{O2}=1.5mbar, anneal at 150°C, [b]ITO/IGZO channel, [c]IGZO/Cu-doped IGZO channel, [d]for TiO_2 = 8 nm

76 mV/dec is reached, which is even comparable with submicrometer single-crystalline Si MOSFET.

Such small SS is essential to turn on the transistor fast at low voltage. This small SS is attributed to both good high-κ–a-IGZO interface charge density (D_{it}) and the high gate capacitance density [17]

$$SS = \frac{KT}{q} \times \ln 10 \times \left(1 + \frac{C_{\mathrm{dep}} + C_{\mathrm{it}}}{C_i}\right) \qquad (1)$$

where C_{dep} is the depletion capacitance density of a-IGZO, C_{it} is the capacitance density from charged interface traps, and C_i is the gate capacitance density. The very high C_i of 5.1 fF/μm^2 using HfLaO results in the good SS. Aside from a large 5×10^7 for $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, a low V_T of 0.22 V and high μ_{FE} mobility of 25 cm^2/V $\cdot$ s are obtained simultaneously. The good mobility is also related to the amorphous structure of HfLaO after 400 °C anneal [19] with small surface roughness of only 0.57 nm.

In Table I, we compare important device parameters of a-IGZO TFTs with various gate dielectrics of SiO_2, AlTiO,

Si_3N_4/TiO_2, Si_3N_4, $Ba_{0.5}Sr_{0.5}TiO_3$, and Y_2O_3. The performance of our HfLaO IGZO TFTs is comparable with other devices, with additional merit of the best normalized drive current (μC_i) [17], [18] under a low voltage of 2 V. Therefore, the high gate capacitance density C_i is as important as mobility for the needed high transistor drive current.

IV. Conclusion

A high-κ HfLaO dielectric was successfully integrated into a-IGZO TFTs. The HfLaO/a-IGZO TFTs showed a low V_T of 0.22 V, small SS of 0.76 mV/dec, large μ_{FE} mobility of 25 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ under a low operation voltage, and a high $I_{\mathrm{on}}/I_{\mathrm{off}}$ of 5×10^7. This device is suitable for high-speed low-power ICs on glass panel.

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