Analysis and Design of a Single-Stage Parallel AC-to-DC Converter

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***Abstract*—In this paper, a single-stage (S^2) parallel ac-to-dc converter based on single-switch two-output boost–flyback converter is presented. The converter contains two semistages. One is the boost–flyback semistage, which transfers partial input power transferred to load directly through one power flow path and has excellent self-power factor correction property when operating in discontinuous conduction mode even though the boost output is close to the peak value of the line voltage. The other one is the flyback dc-to-dc (dc/dc) semistage that provides the output regulation on another parallel power flow path. With this design, the power conversion efficiency is improved and the current stress of control switch is reduced. Furthermore, the calculation process of power distribution and bulk capacitor voltage, design equations, and design procedure for key parameters are also presented. By following the procedure, an 80 W prototype converter has been built and tested. The experimental results show that the measured line harmonic current at the worst condition complies with the IEC61000-3-2 class D limits, the maximum bulk capacitor voltage is about 415.4 V, and the maximum efficiency is about 85.8%. Hence, the proposed S^2 converter is suitable for universal input usage.**

***Index Terms*—AC/DC power conversion, fly back converter, power factor correction, single-stage, single-switch.**

I. Introduction

THE POWER factor correction (PFC) has been widely employed for improving the power quality of the power converters. In conventional converters design, a two-stage structure was usually employed for performing PFC and output regulation simultaneously, where the bulk capacitor C_B is in the power transfer path between the PFC stage and dc-to-dc (dc/dc) stage. This structure can give high power factor and high regulation simultaneously by using two independent controllers and power stages, but the cost of switching devices and the control circuitry is not easy to cut down especially in low-power application. Although unity power factor is the ideal objective, it is no longer an essential requirement. According to the regulation IEC61000-3-2 [1], the power supplies of low-power products such as computers, PC monitors, and television sets have to comply with class D limits. This fact promotes the development of the S^2 ac-to-dc converter, such as boost integrated/flyback rectifier/energy storage/dc-to-dc converter (BIFRED) [2] and boost input current shaper (ICS) [3]–[8], which comply with the regulations without achieving unity power factor. In those designs, two power stages were integrated into one stage by using only one controller and sharing the control switch so that the component count and cost could be reduced. However, these converters have the problems of high bulk capacitor voltage at high line and light load when PFC semistage is operated in discontinuous conduction mode (DCM) and dc/dc semistage in continuous conduction mode (CCM). Some alternative designs [5]–[8] using additional coupled feedback windings could reduce the bulk capacitor voltage, but they also result in dead angle in the input current so that the input current distortion is increasing. Furthermore, it can be seen that part of the power is repeatedly processed or recycled in both the conventional two-stage and S^2 ac-to-dc converters.

To improve the power processing, the concept of parallel PFC (PPFC) has been proposed in [9] and [10]. In those schemes, two parallel power flow paths are used and part of the input power is processed only once. Therefore, the converters could transfer power with higher efficiency. Since each path only transmits part of the whole conversion power, the components can be replaced with smaller ones. However, the PPFC design has complex circuit with special control scheme as mentioned in [11]. Another scheme of parallel power processing approach was presented on the base of two-output preregulator cascaded with two-input postregulator [12]. Although the output capacitor is smaller and the power conversion efficiency is high, some extra implementation prices exist, such as multiple switching devices and floating MOSFET driver. In addition, the output range of the postregulator is limited so as not suitable for universal input, and it is a two-stage structure by nature. The universal boost/forward converter presented in [14], [15] makes use of an auxiliary transformer to reduce link voltage stress without inducing the dead angle of the line current. Hence, it inspires the parallel idea for the universal S^2 converter in this paper.

For an ideal PFC converter, the input power ($p_{\rm in}$) is a sine square function biased by constant output power ($P_{\rm out}$). As mentioned in [9] and [10], there is 68% of line average input power that can be transferred to output directly through PFC stage, which is called the direct power (DP). Only the remaining 32% of line average input power needs to be stored in the bulk capacitor temporarily through PFC stage and taken off from the bulk capacitor through dc/dc stage. Since the processed powers are not directly transferred from ac input to dc output, they are

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TABLE I
RECENTLY PUBLISHED S^2 APPROACHES

	Diode	Control Switch	Magnetic components	Control	V_{CB} (V)	Switching frequency (kHz)	Input Voltage (V_{rms})	Output Voltage (V)	Output Power (W)	Maximum Efficiency (%)	PF (%) or compliance
[20] 2004	4	1	1 T with 3 windings + 1 L	Single controller	<375	96	90-264	5	60	73.2	IEC 1000-3-2 CL.D
[21] 2005	7	1	1 T with 3 windings + 1 T + 1 L	Single controller UC3844	<260	100	85-265	28	150	83.2	>0.97
[13] 2007	2	2	1 T + 1 L	Single controller	<35	?	187-265	56	100	85.4	IEC 61000-3-2 CL.D
[22] 2008	4	2	1 T + 1 L	Two controllers and logic	400	50	100-240	24	100	87	0.93-0.96 IEC 61000-3-2 CL.D
[23] 2008	2	2	1 T with 6 windings	Single controller and logic	?	140	110-120	?	150	92	IEC 1000-3-2 CL.D
Proposed	5	1	2 T + 1 L	Single controller UC3844	<415.4	100	85-265	54	80	85.8	0.91-0.99 IEC 61000-3-2 CL.D

Letter T denotes transformer, letter L denotes inductor, V_{CB} denotes bulk capacitor voltage, mark "?" denotes that the item was not mentioned in the literature

called indirect powers (IDPs). Hence, based on the aforementioned concept, a new family of S^2 ac-to-dc (ac/dc) converter is proposed in this article to increase the DP content percentage on the input power. In the circuits, the front semistage is of single-switch two-output (SSTO) boost–flyback configuration that works as a power factor corrector. Part of input power is processed with the front flyback cell, and the remainder of input power is processed through the path along boost cell-C_B-dc/dc semistage.

To illustrate the circuit and control of the proposed converter, several recently published low-power S^2 approaches are tabulated in Table I. Only the proposed converter and those in [20], [21] are implemented with single-switch and single-loop controller. However, the efficiency of [20] is significantly lower than the proposed one and the component count of [21] is more than the proposed one. From Table I, the circuits in [20], [21], and [13] have relatively small capacitor voltages. However, the circuit of [20] has the shortcoming of low efficiency. The circuit of [21] employs two bulk capacitors and multiwinding transformer to get low voltage. The circuit in [13] puts bulk capacitor on the secondary side of flyback transformer, which results in the low capacitor voltage. However, it also has the shortcomings of extra control switch and that the efficiency would decrease when universal voltage is applied. Though the bulk capacitor voltage in proposed converter is higher than those in [13], [20], and [21], it is not higher than 450 V, the voltage limitation of commercial capacitors. Additionally, the use of single switch with small current stress, two parallel power streams with small components, and single-loop controller is a competitive advantage in the low-power universal applications.

Besides the S^2 parallel topologies, the detailed operation principle and design procedure for universal application is also presented in this article. With the procedure, an 80 W prototype is constructed, which is a specific demonstration case used

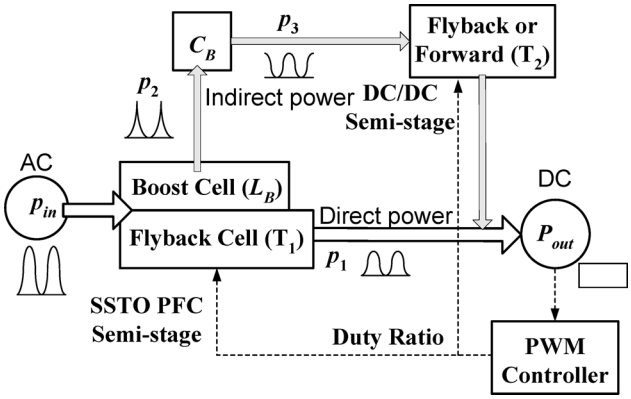


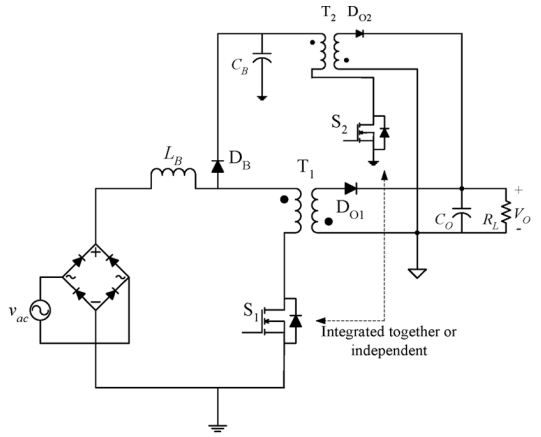
Fig. 1. Proposed S^2 PPFC scheme.

for clear demonstration. Its experimental results have shown that input current has no dead angle and its harmonics satisfies IEC61000 class D at low line with full load and the maximum bulk capacitor voltage is under 450 V at high line with light load. It is suggested that the proposed S^2 converter could be used for 50–150 W with universal input voltage range and up to 200 W with European voltage range. Therefore, the potential applications could be PC monitors, ac/dc adapters, and small television sets.

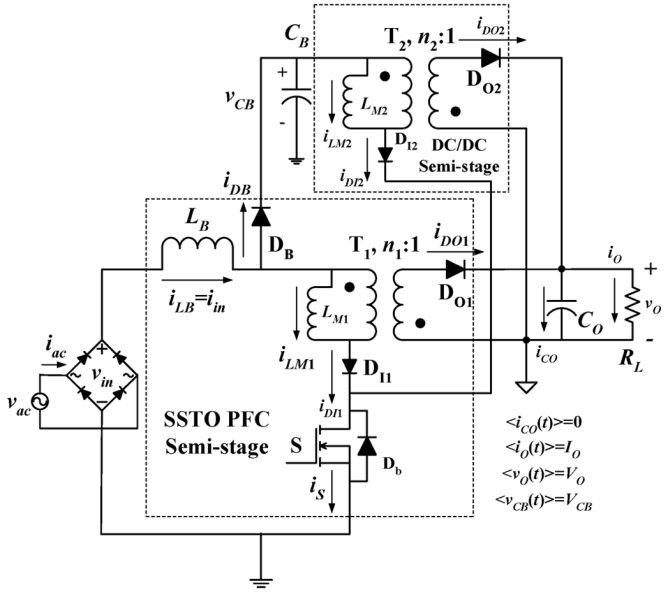
II. Operation Principles

A. S^2 Parallel Boost–Flyback Converter

The new design power flow scheme of a S^2 PPFC is shown in Fig. 1. In Fig. 1, the line power $p_{\rm in}$ is fed to SSTO boost–flyback semistage and split to two power flow streams p_1 and p_2. The power flow stream p_1 is processed only by flyback cell and transferred to output directly, and hence it is DP. Since the instantaneous $p_{\rm in}$ is always different from output power $P_{\rm out}$, the remaining input power, p_2, is buffered to bulk capacitor C_B through the boost function of boost cell to regulate power flow. To fulfill a better output power regulation, a dc/dc semistage is employed to transfer the power, denoted by p_3, from C_B to the output when $p_{\rm in}$ is low, especially smaller than $P_{\rm out}$. The power series p_2 and p_3 are processed twice from ac input to dc output, and hence they are IDPs. Furthermore, to obtain high power factor, the boost and flyback cells both had to better operate in DCM, whereas the dc/dc semistage can be implemented with forward or flyback configuration and operate either in CCM or DCM. A S^2 implemented circuit of Fig. 1 is shown in Fig. 2(a). The circuit has been simplified so as to use only one common power control switch for SSTO boost–flyback and dc/dc semistages as shown in Fig. 2(b). In Fig. 2(b), PFC and output regulation are performed with one feedback controller as shown in Fig. 2(c). More topologies variations had been shown in [15]. The practical realization circuit in Fig. 2(b) is composed of a SSTO boost–flyback semistage, which is constructed by $L_B, D_B, T_1, D_{O1}, D_{I1}$, S, D_b, and a bulk capacitor C_B, and a dc/dc semistage, which is implemented by a flyback circuit and constructed by T_2, D_{O2}, D_{I2}, S, and D_b. In Fig. 2(a) and (b), the two transformers T_1 and T_2 share the load current, so their size could be small. Furthermore, the boost inductor L_B



(a)



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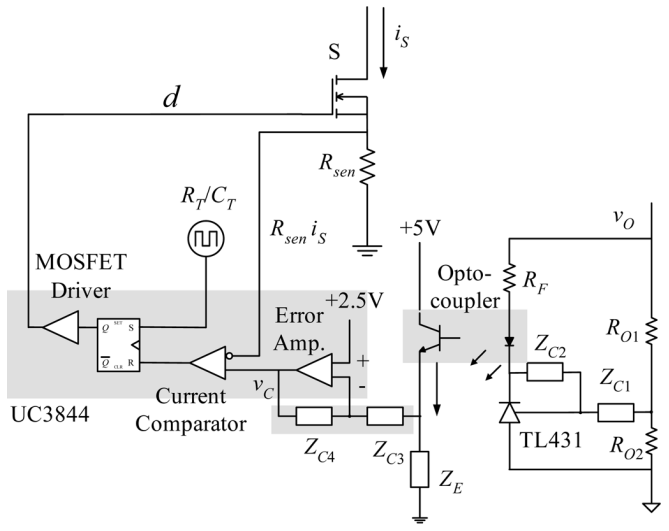

(c)

Fig. 2. S^2 Implementation circuit of parallel boost–flyback–flyback converter. (a) Two-switch circuit. (b) Single-switch circuit. (c) Feedback controller circuit.

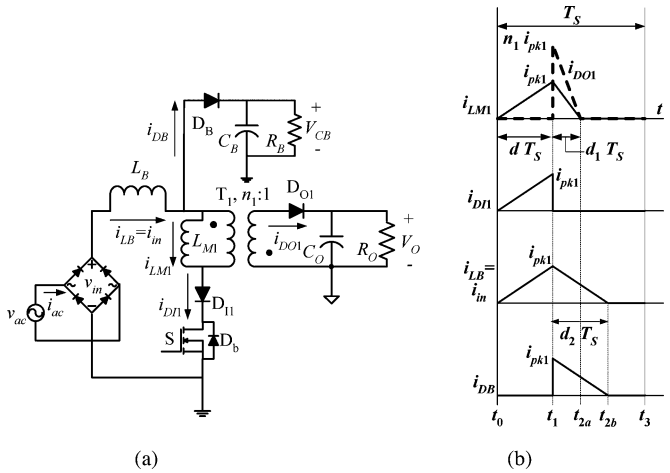

Fig. 3. SSTO boost–flyback converter. (a) Circuit. (b) Main waveforms.

and transformers T_1 distribute the input power together when switch S is ON, so the size of L_B could be of smaller one. Therefore, the sizes of L_B, T_1, and T_2 can be chosen as smaller ones in this design.

B. SSTO Boost–Flyback Circuit

In order to clearly build the primary operation concepts and theories of the proposed S^2 parallel ac-to-dc converter depicted in Figs. 1 and 2, the operation of a SSTO boost–flyback converter depicted in Fig. 3(a) will be introduced in advance. In SSTO boost–flyback converter, $T_1 - D_{O1} - D_{I1} - C_O - R_O - S$ is the flyback cell and $L_B - D_B - C_B - R_B - S$ is the boost cell. This converter has PFC function that will be demonstrated later. In the converter, the boost inductance L_B and the flyback transformer T_1 both operate in DCM. When control switch S is turned on, T_1 and L_B are charged serially. When S is turned off, T_1 and L_B are discharged to $R_O - C_O$ and $R_B - C_B$, respectively. The main current waveforms of SSTO boost–flyback converter operating in one switching period are shown in Fig. 3(b). To demonstrate the operation theory of the converter, the moving average notation $\langle x(t)\rangle$ of a waveform $x(t)$ over a switching period T_S is employed and defined as follows [16]:

$$\langle x(t)\rangle \equiv \langle x(t)\rangle_{T_{\rm S}} = \frac{1}{T_{\rm S}}\int_t^{t+T_{\rm S}} x(\tau)\,d\tau. \tag{1}$$

To focus on the primary analyses, some assumptions are made as follows.

1) All components are ideal.
2) Since switching frequency $f_{\rm S}$ is far greater than line frequency $f_{\rm L} = 1/T_{\rm L}$, where $T_{\rm L}$ is line period. The input voltage $v_{\rm in}(t)$, regarded as the rectified line voltage $V_{\rm inpk}\left|\sin(\omega_{\rm L}\cdot t)\right|$, is approximated to a constant over one switching period, where $V_{\rm inpk}$ is the ac voltage amplitude and $\omega_{\rm L} = 2\cdot\pi/T_{\rm L}$.
3) Since bulk capacitor C_B and output capacitor C_O are sufficiently large, flyback output voltage V_O and boost output voltage V_{CB} are regarded as constants within one half line cycle.

From Fig. 3(a), it can be seen that the average input current $\langle i_{\rm in}(t)\rangle$ is equal to the sum of average flyback input diode current $\langle i_{DI1}(t)\rangle$ and average boost output diode current $\langle i_{DB}(t)\rangle$. Therefore, by summing the current waveforms of $\langle i_{DI1}(t)\rangle$ and $\langle i_{DB}(t)\rangle$ shown in Fig. 3(b), $\langle i_{\rm in}(t)\rangle$ can be obtained as

$$\langle i_{\rm in}(t)\rangle = \langle i_{DI1}(t)\rangle + \langle i_{DB}(t)\rangle = \frac{i_{\rm pk1}\times(d+d_2)}{2} \tag{2a}$$

where d is the duty ratio of S, d_2 is the boost cell diode conduction time ratio, and the current peak value can be obtained from

$$i_{\rm pk1} = \frac{d\cdot v_{\rm in}(t)}{f_{\rm S}(L_B+L_{M1})} = \frac{d_2\cdot(V_{CB}-v_{\rm in}(t))}{f_{\rm S}L_B} = \frac{d_1\cdot n_1\cdot V_O}{f_{\rm S}L_{M1}} \tag{2b}$$

where L_{M1} is the primary magnetizing inductance of T_1, n_1 is the primary turns ratio of T_1, and d_1 is the flyback cell output diode conduction time ratio. From (2b), d_2 can be obtained as

$$d_2 = \frac{d\cdot v_{\rm in}(t)}{(V_{CB}-v_{\rm in}(t))}\left(\frac{L_B}{L_B+L_{M1}}\right). \tag{2c}$$

With substituting (2b) and (2c) into (2a),$\langle i_{\rm in}(t)\rangle$can be found as

$$\langle i_{\rm in}(t)\rangle = \frac{d^2 v_{\rm in}(t)}{2f_{\rm S}(L_B+L_{M1})} \times\left(1+\frac{v_{\rm in}(t)}{(V_{CB}-v_{\rm in}(t))}\left(\frac{L_B}{L_B+L_{M1}}\right)\right). \tag{2d}$$

Since the average current of C_O over a half line cycle is zero at steady state, the half line average current of i_{DO1} is equal to the average output current. Thus

$$\frac{2}{T_{\rm L}}\int_0^{\frac{\pi}{\omega_{\rm L}}}\langle i_{DO1}(t)\rangle\,dt = \frac{V_O}{R_O}. \tag{3a}$$

From Fig. 3(b), average current over one switching period $\langle i_{DO1}(t)\rangle$ in (3a) can be obtained as follows:

$$\langle i_{DO1}(t)\rangle = \frac{n_1\cdot i_{\rm pk1}\cdot d_1}{2} \tag{3b}$$

where the magnetism discharging time ratio of T_1 transformer, d_1, can be found from (2b) as

$$d_1 = \frac{d\cdot v_{\rm in}(t)}{n_1\cdot V_O}\left(\frac{L_{M1}}{L_B+L_{M1}}\right). \tag{3c}$$

With substituting (2b) and (3c) into (3b),$\langle i_{DO1}(t)\rangle$can be obtained as

$$\langle i_{DO1}(t)\rangle = \frac{L_{M1}d^2 v_{\rm in}^2(t)}{2f_{\rm S}(L_B+L_{M1})^2 V_O}. \tag{3d}$$

Substituting (3d) into (3a), the voltage gain of flyback cell M_O can be obtained as

$$M_O = \frac{V_O}{V_{\rm inpk}} = d\cdot\sqrt{\frac{L_{M1}\cdot R_O}{4f_{\rm S}(L_B+L_{M1})^2}} \tag{3e}$$

where R_O is the load resistance of flyback cell.

TABLE II
VARIOUS OPERATION MODES IN THE PROPOSED CIRCUIT

Mode	M_1	M_2	M_3	M_4	$M_5 \ldots M_8$
L_B	DCM	DCM	CCM	CCM	CCM/DCM
T_1	DCM	DCM	DCM	DCM	CCM
T_2	CCM	DCM	CCM	DCM	CCM/DCM
	Self PFC	Self PFC	Allowed under CL. D	Allowed under CL. D	Not happen

Similarly, since C_B has zero average current over a half line cycle in steady state, the average current relation can be obtained as

$$\frac{2}{T_{\rm L}}\int_0^{\frac{\pi}{\omega_{\rm L}}} \langle i_{DB}(t)\rangle\, dt = \frac{V_{CB}}{R_B} \tag{4a}$$

where $\langle i_{DB}(t)\rangle$can be obtained from Fig. 3(b) as

$$\langle i_{DB}(t)\rangle = \frac{i_{\rm pk1}\cdot d_2}{2} = \frac{L_B d^2 v_{\rm in}^2(t)}{2f_{\rm S}\left(L_B+L_{M1}\right)^2\left(V_{CB}-v_{\rm in}(t)\right)}. \tag{4b}$$

The voltage gain of boost cell M_{CB} is defined and obtained with substituting (4b) into (4a) as

$$M_{CB}=\frac{V_{CB}}{V_{\rm inpk}} = \frac{d^2\cdot R_B\cdot L_B}{2\pi\cdot f_{\rm S}\left(L_B+L_{M1}\right)^2}\int_0^{\pi}\frac{\sin^2\theta}{M_{CB}-|\sin\theta|}d\theta \tag{4c}$$

where R_B is the load resistance of boost semistage.

It can be seen from (2d) that while d and f_S are regarded as constants, the arrangement of smaller ratio of $L_B/(L_B+L_{M1})$ can result in higher linear relation between $\langle i_{\rm in}(t)\rangle$ and $v_{\rm in}(t)$, in other words, lower input harmonic distortion. Furthermore, (3e) and (4c) show that voltage gain rises as load resistance increases. In particular, V_{CB} in (4c) can be very high at light load and high line. Therefore, the method to keep it under commonly accepted limit would be presented in Section III.

C. S^4 Parallel Boost–Flyback–Flyback Converter

The proposed S^2 boost–flyback–flyback PPFC that has two semistages is shown in Figs. 1 and 2. The boost–flyback semistage has PFC function and simultaneously gives two energy-processing paths. Being the remaining semistage, the flyback dc/dc converter circuit has fast output regulation ability. The proposed circuit has three magnetic elements, and each element has two operation modes (i.e., CCM and DCM). Hence, there are eight modes that may happen in the circuit as shown Table II. In order to obtain good power factor, the boost and flyback cells are designed to operate in DCM, whereas the flyback dc/dc semistage operates in either CCM or DCM in a line cycle. Thus, the converter has two operating modes. The operation mode while the flyback dc/dc semistage operates in CCM is defined as the M_1 mode. Contrarily, the operation mode while the flyback dc/dc semistage operates in DCM is defined as the M_2 mode. As mentioned latter in Section III-C, it is not easy to make L_B operate in DCM throughout universal range, and CCM offers higher efficiency and lower current stress than DCM. M_3 and M_4 modes are allowed under harmonic limitation

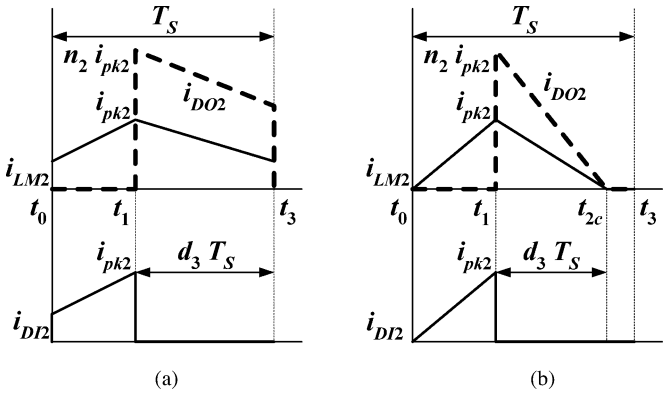

Fig. 4. Main waveforms of flyback dc/dc semistage in a switching period. (a) M_1 mode. (b) M_2 mode.

of IEC61000-3-2 class D and not discussed in this paper. With properly selected n_1, it is easy to control T_1 in DCM, so M_5–M_8 modes would not happen. The main current waveforms of the boost–flyback semistage in a switching period are the same as Fig. 3(b), and the waveforms of flyback dc/dc semistage in both modes are shown in Fig. 4. The circuit operations of the single-switch implemented circuit shown in Fig. 2(b) are demonstrated as follows:

In $t_0 \le t \le t_1$control switch S is switched on, flyback input diode D_{I1} conducts, and D_B, D_{O1}, and D_{O2} are cutoff. Because the boost inductor L_B and the flyback transformer primary inductance L_{M1} both are connected in series, they are charged by the input power at the same time. The current i_{LB}, which is equal to i_{DI1} and also the magnetizing current of T_1, i_{LM1}, increases linearly from zero. Meanwhile, the currents i_{DI2}, which is equal to the magnetizing current of T_2, i_{LM2}, also increases linearly from its initial value while in M_1 mode and from zero while in M_2 mode. At the moment t_1, S is turned off. The currents i_{LB}, i_{DI1}, and i_{LM1} reach the same peak value $i_{\rm pk1}$ and the currents i_{DI2} and i_{LM2} reach another peak value $i_{\rm pk2}$.

In $t_1 \le t \le t_3$, the main switch S is OFF, the diode D_{I1} and D_{I2} are OFF, and D_B, D_{O1} and D_{O2} are ON. The magnetic energy of inductor L_B is transferred to C_B and the magnetic energies of the transformers T_1 and T_2 are transferred to the same output load R_L simultaneously. Consequently, the energy discharging in T_1 produces the result that i_{LM1} and i_{DO1} $(= n_1\cdot i_{LM1})$ both decrease linearly to zero at t_{2a} and keep zero until t_3, and i_{LB} and i_{DB} decrease linearly to zero at t_{2b}. The energy discharging in T_2 gives the result that both i_{LM2} and i_{DO2} $(= n_2\cdot i_{LM2})$ decrease linearly to nonzero final values at t_3 for M_1 mode and to zero at t_{2c} for M_2 mode.

TABLE III
VARIOUS CASES IN THE PROPOSED CIRCUIT

Case	Mode	v_{ac}	P_{out}
I	M_1	Low	High
II	M_1+ M_2	Medium	Medium
III	M_2	High	Low

Since M_1 and M_2 modes are to be discussed, three kinds of the combination of operation modes may be yielded within a half line cycle as shown in Table III. The major current waveforms and the corresponding duty ratio waveforms are depicted and shown in Fig. 5. Case I normally happens in low input voltage and high output power condition, whereas case III normally happens at high input voltage and low output power.

For transient current balance of C_O, the transient load current can be expressed as

$$i_O(t) = i_{DO1}(t) + i_{DO2}(t) - i_{CO}(t) \tag{5a}$$

where $i_{DO1}(t)$, $i_{DO2}(t)$, and $i_{CO}(t)$ represent the transient current of D_{O1}, D_{O2}, and C_O. By an ideal output voltage feedback control, the duty-cycle of control switch is varied in order to set output voltage on reference value. As shown in Figs. 3(b) and 4, the input current $(i_{DO1}(t) + i_{DO2}(t))$ of C_O is regulated to balance with output current (i_O) in T_S so that $\langle i_O(t)\rangle = I_O, \langle i_{CO}(t)\rangle = 0, \langle v_O(t)\rangle = V_O$, and (5a) can be expressed as

$$I_O = \frac{V_O}{R_{\rm L}} = \frac{P_{\rm out}}{V_O} = \langle i_{DO1}(t)\rangle + \langle i_{DO2}(t)\rangle \tag{5b}$$

where V_O is the average output voltage, R_L is the load resistance, $\langle i_{DO1}(t)\rangle$ represents the averaging current of D_{O1} as expressed in (3d), and $\langle i_{DO2}(t)\rangle$ represents the averaging current of D_{O2}. Although the input voltage varies in a half line cycle, the output power will be kept constant through the output feedback control. To make (5b) come true, the ideal output voltage feedback controller should have superior transient response and robust stability. The structure of controller is implemented with current-mode controller with optically isolated feedback as shown in Fig. 2(c). In the circuit of Fig. 2(c), output voltage signal V_O is transferred to UC3844 via TL431 and optcoupler, the switch current i_S is sensed and fed back to comparator, and then the duty ratio d of control switch S is well controlled.

For the M_1 mode, consider the bulk capacitance is a large one. Then the duty ratio d in M_1 mode will be kept nearly constant D_{m1} and yield a high regulation output, which is given by

$$V_O = \left.\frac{V_{CB}\cdot d}{n_2(1-d)}\right|_{d=D_{m1}} \tag{6}$$

where n_2 is the turns ratio of T_2. From (6), D_{m1} can be found as

$$d = D_{m1} = \frac{n_2 V_O}{n_2 V_O + V_{CB}}. \tag{7}$$

From (5b), $\langle i_{DO2}(t)\rangle$ can be obtained as

$$\langle i_{DO2}(t)\rangle = I_O - \langle i_{DO1}(t)\rangle|_{d=D_{m1}}. \tag{8}$$

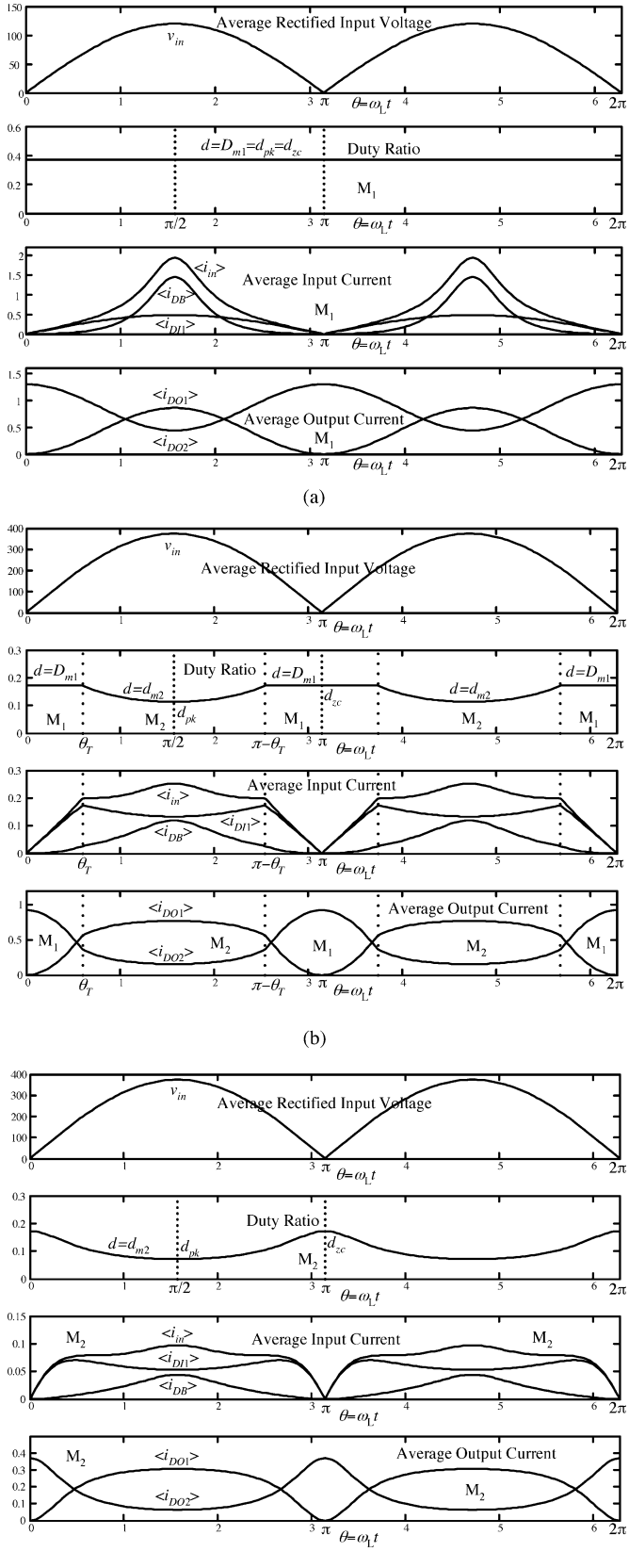

Fig. 5. Main waveforms of parallel boost–flyback–flyback converter in a line cycle. (a) Case I (M_1 mode only). (b) Case II (both M_1 and M_2 modes). (c) Case III (M_2 mode only).

TABLE IV
THE CORRESPONDING PARAMETERS OF CASES I–III ILLUSTRATION EXAMPLE

Case	L_B	L_{M1}	n_1	L_{M2}	n_2	v_{ac}	V_O	P_{out}	f_S	f_L	V_{CB}
I	35 μ H	135 μ H	1.2	4 mH	1.4	85 V_{rms}	54 V	70 W	100 kHz	60 Hz	128.5 V
II	30 μ H	150 μ H	1.6	1.5 mH	1.9	265 V_{rms}	54 V	50 W	100 kHz	60 Hz	444.5 V
III	30 μ H	150 μ H	1.6	1.5 mH	1.9	265 V_{rms}	54 V	20 W	100 kHz	60 Hz	449.9 V

While in M_2 mode, T_2 operates in DCM. From Fig. 4(b) by following the similar deriving procedure of (3d), $\langle i_{DO2}(t)\rangle$ can be obtained as

$$\langle i_{DO2}(t)\rangle = \frac{n_2 \cdot i_{\mathrm{pk}2} \cdot d_3}{2} = \left.\frac{d^2 \cdot V_{CB}^2}{2 f_S L_{M2} V_O}\right|_{d=d_{m2}} \tag{9}$$

where d_{m2} is the instant duty ratio in M_2 mode. Substituting (3d) and (9) into (5b), it can be obtained as

$$d = d_{m2}(\theta) = \sqrt{\frac{2 f_{\mathrm{S}} P_{\mathrm{out}}}{\left(\frac{L_{M1} V_{\mathrm{inpk}}^2 \sin^2\theta}{(L_B + L_{M1})^2} + \frac{V_{CB}^2}{L_{M2}}\right)}} \tag{10}$$

where $\theta = \omega_{\mathrm{L}} \cdot t$ is the phase of sinusoidal line voltage, and P_{out} is the output power. In order to generate the complex duty d_{m2}, the compensator in the current-mode control had been optimized to possess superior transient responses such as small rising time, low overshoot, and zero steady-state error. Additionally, the compensator also can generate the correct duty d_{m2} with different operation modes due to its superior performances.

From (3d) and (5b), $\langle i_{DO1}(t)\rangle$ reaches maximum and $\langle i_{DO2}(t)\rangle$ reaches minimum at $\omega_{\mathrm{L}} \cdot t = \pi/2$. For case I, the converter operates only in M_1 mode (T_2 operates in CCM), I_O must be greater than the boundary value$I_{DO1PK} + I_{DO2B}$

$$I_O \geq I_{DO1PK} + I_{DO2B} \tag{11}$$

where I_{DO1PK} is the peak value of $\langle i_{DO1}(t)\rangle$ and I_{DO2B} is the boundary value of i_{DO2} between CCM and DCM. The former can be obtained by replacing d with D_{m1} and $v_{\mathrm{in}}(t)$ with $V_{\mathrm{inpk}} \sin(\pi/2)$ in (3d), and expressed as

$$I_{DO1PK} = \frac{L_{M1} D_{m1}^2 V_{\mathrm{inpk}}^2}{2 f_{\mathrm{S}} (L_B + L_{M1})^2 V_O} \tag{12}$$

and the latter can be obtained by replacing d with D_{m1} in (9) and expressed as

$$I_{DO2B} = \frac{D_{m1}^2 \cdot V_{CB}^2}{2 f_{\mathrm{S}} L_{M2} V_O}. \tag{13}$$

Furthermore, as I_O is smaller than the boundary value in (11), M_2 mode shows in the operation of the proposed converter as plotted in Fig. 5(b). From the equality $I_{DO2} = I_{DO2B}$ and (5b), the transition angle θ_T from M_1 to M_2 mode can be expressed as

$$\theta_T = \omega_{\mathrm{L}} \cdot t_T = \sin^{-1}\left[\sqrt{\frac{2 f_{\mathrm{S}} (L_B + L_{M1})^2 V_O}{L_{M1} D_{m1}^2 V_{\mathrm{inpk}}^2} (I_O - I_{DO2B})}\right]. \tag{14}$$

As I_O gets smaller, the interval of M_2 becomes wider and M_1 becomes narrower. It can also be seen from (3d) that $\langle i_{DO1}(t)\rangle$ reaches zero at line voltage phase being 0 and π and from (5b) that $\langle i_{DO2}(t)\rangle$ reaches maximum at the same time. Thus, as I_O gets smaller than the boundary value of (13), the converter would work in M_2 mode only during a half line cycle. Consequently, for case II operation that the converter works in both M_1 and M_2 modes in a half line cycle, I_O will be in the range of

$$I_{DO1B} + I_{DO2B} \geq I_O \geq I_{DO2B}. \tag{15}$$

Besides, for case III operation that the converter works only in M_2 mode in a half of a line cycle, I_O is smaller than the boundary value

$$I_{DO2B} \geq I_O. \tag{16}$$

Based on the earlier discussion, the theoretical currents and voltage waveforms for the cases I–III examples are illustrated in Fig. 5(a)–(c), and the corresponding parameters used are shown in Table IV. For the case I operation, the value of L_{M2} in (13) intentionally selected a large one so that (11) can be satisfied and case I operation can present. For the other parameters, $L_B, L_{M1}, n_1,$ and n_2, they are selected according to the equations described in Section III so that cases II and III can be activated.

From Figs. 2 and 5(a)–(c), it can be seen that the average input current $\langle i_{\mathrm{in}}(t)\rangle$ is divided into $\langle i_{DI1}(t)\rangle$ and $\langle i_{DB}(t)\rangle$ through the operation of boost–flyback semistage. Among these two currents, $\langle i_{DO1}(t)\rangle$ is transformed to $\langle i_{DO1}(t)\rangle$ by the flyback cell, and then transferred to R_{L} directly. Alternatively, $\langle i_{DB}(t)\rangle$ is mainly buffered in C_B during v_{in} peak, then transformed to $\langle i_{DO2}(t)\rangle$ by the flyback dc/dc semistage, and then transferred to R_{L} for output regulation. The output current I_O is primarily supplied by $\langle i_{DO2}(t)\rangle$ in low line voltage duration.

The switch current of conventional cascade S^4 converter like [3] mainly composed of inductor current of the boost-ICS semistage and the transformer primary current of the flyback semistage. Both semistages have to handle the whole input power. Hence, the peak switch current is doubled and reaches peak value when input power is the maximum and occurs at $\theta = \pi/2$. In Fig. 2, the average switch current $\langle i_{\mathrm{S}}(t)\rangle$ of the proposed converter is the sum of $\langle i_{DI1}(t)\rangle$ and $\langle i_{DI2}(t)\rangle$ and can be expressed as

$$\langle i_{\mathrm{S}}(t)\rangle = \langle i_{DI1}(t)\rangle + \langle i_{DI2}(t)\rangle. \tag{17a}$$

Both $\langle i_{DI1}(t)\rangle$ and $\langle i_{DI2}(t)\rangle$ represent the charged current of the first semistage from line input and the transformer primary current of second semistage from bulk capacitor and can be

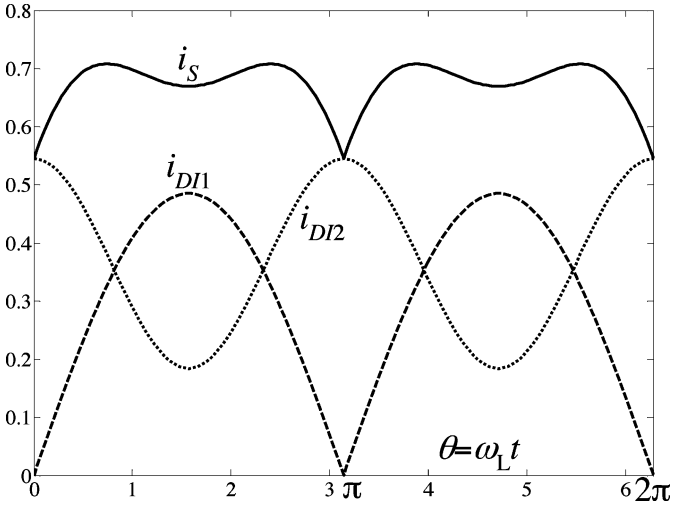

Fig. 6. Average switch current for case I.

obtained from Fig. 3(b) as

$$\langle i_{DI1}(t)\rangle = \langle i_{LB}(t)\rangle - \langle i_{DB}(t)\rangle \tag{17b}$$

and

$$\langle i_{DI2}(t)\rangle = \frac{V_O}{V_{CB}}\langle i_{DO2}(t)\rangle = \frac{V_O}{V_{CB}}\left(I_O - \langle i_{DO1}(t)\rangle\right). \tag{17c}$$

It can be seen from (17a) and (17c) that if $\langle i_{DO1}(t)\rangle$ increases, more output current will be provided by flyback cell, and $\langle i_S(t)\rangle$ will be reduced. Contrarily, if flyback cell is absent (i.e., $\langle i_{DO1}(t)\rangle = 0$), the circuit in Fig. 2(b) will be reduced to a conventional S^2 converter [3]. Furthermore, from Fig. 3(b), $\langle i_{DI1}(t)\rangle$ can be further obtained as

$$\langle i_{DI1}(t)\rangle = \frac{i_{\mathrm{pk1}}\cdot d}{2} = \frac{d^2 V_{\mathrm{inpk}}\sin(\omega_L\cdot t)}{2f_S(L_B+L_{M1})}. \tag{17d}$$

Substituting (3d) into (8) and the result is substituted into (17c), $\langle i_{DI2}(t)\rangle$ for M_1 mode can be further expressed as

$$\langle i_{DI2}(t)\rangle = \frac{V_O}{V_{CB}}\left(I_O - \frac{L_{M1}D_{m1}^2 V_{\mathrm{inpk}}^2\sin^2(\omega_L\cdot t)}{2f_S(L_B+L_{M1})^2 V_O}\right). \tag{17e}$$

Substituting (9) into (17c), $\langle i_{DI2}(t)\rangle$ for M_2 mode can be further obtained as

$$\langle i_{DI2}(t)\rangle = \left.\frac{d^2\cdot V_{CB}}{2f_S L_{M2}}\right|_{d=d_{m2}} \tag{17f}$$

where d_{m2} can be obtained from (10). It can be seen from (17d)–(17f) and Fig. 6 that $\langle i_{DI1}(t)\rangle$ reaches local maximum at $\theta=\pi/2$ while $\langle i_{DI2}(t)\rangle$ is minimum, and $\langle i_{DI2}(t)\rangle$ reaches local maximum at $\theta=\pi/2$ or π while $\langle i_{DI1}(t)\rangle$ is zero. Therefore, the power processed by flyback cell is transferred to load directly and would not be processed by the switch again, the local maximum current stresses due to DP and IDP do not appear at the same time during half line cycle, so the overall current stress of main switch was small compared with that of conventional S^4 converter.

III. Analysis and Design

A. Power Distribution and Bulk Capacitor Voltage

In the proposed S^2 PPFC scheme shown in Fig. 1, the power distribution between the DP (p_1) and IDP (p_2 or p_3) processing paths is one of the important design considerations since it affects not only the converter efficiency but also the power ratings required to the components in each processing power path. Besides, in the IDP path, the energy balance between the power flow into (p_2) and out (p_3) of bulk capacitor determines the bulk capacitor voltage, which can be very high if not properly designed. Based on the earlier design considerations, the power distribution will be analyzed according to the implementation circuit shown in Fig. 2(b), and hence the formula related to power distribution and bulk capacitance voltage can be derived. They are formulated as follows.

The input power p_{in} is composed of p_1 and p_2

$$p_{\mathrm{in}}(\theta) = v_{\mathrm{in}}(t)\langle i_{LB}(t)\rangle = p_1(\theta) + p_2(\theta). \tag{18}$$

The DP processed by flyback semistage is given by

$$p_1(\theta) = v_{\mathrm{in}}(t)\frac{L_{M1}}{L_B+L_{M1}}\langle i_{DI1}(t)\rangle = V_O\langle i_{DO1}(t)\rangle. \tag{19a}$$

Substitution of $\langle i_{DO1}(t)\rangle$ given by (3d) into (19a) gives

$$p_1(\theta) = 2k_p P_{\mathrm{out}}\sin^2\theta \tag{19b}$$

where k_P is defined as the DP ratio and can be obtained as

$$k_p \equiv \frac{P_{1,\mathrm{pk}}(d)}{P_{\mathrm{out}}} = \frac{L_{M1}d^2V_{\mathrm{inpk}}^2}{4f_S(L_B+L_{M1})^2 P_{\mathrm{out}}} \tag{20}$$

and $P_{1,\mathrm{pk}}$ is given by

$$P_{1,\mathrm{pk}}(d) = \frac{L_{M1}d^2V_{\mathrm{inpk}}^2}{4f_S(L_B+L_{M1})^2}. \tag{21}$$

In M_1 mode, k_p is a constant and can be found by

$$k_p = k_p|_{d=D_{m1}} = K_{P1}. \tag{22}$$

In M_2 mode, k_p is a function of θ and obtained by

$$k_p = k_p|_{d=d_{m2}(\theta)} = k_{p2}(\theta) = \frac{L_{M1}\cdot V_{\mathrm{inpk}}^2}{2\left[L_{M1}V_{\mathrm{inpk}}^2\sin^2\theta + \frac{V_{CB}^2}{L_{M2}}(L_B+L_{M1})^2\right]}. \tag{23}$$

It can be seen from (23) that k_{p2} is independent of P_{out}. The values of D_{m1} and d_{m2} can be obtained from (7) and (10).

The IDP processed by boost semistage from L_B to C_B is given by

$$p_2(\theta) = V_{CB}\langle i_{DB}(t)\rangle. \tag{24a}$$

Substitution of $\langle i_{DB}(t)\rangle$ given by (4b) into (24a) gives

$$p_2(\theta) = \frac{M_{CB}\sin^2\theta}{M_{CB}-|\sin\theta|}\frac{2k_pP_{\mathrm{out}}}{K_{M1}} \tag{24b}$$

where K_{M1} is called inductance ratio and expressed as

$$K_{M1} = \frac{L_{M1}}{L_B}. \tag{25}$$

TABLE V
$K_{\rm IDP}$ INDIRECT POWER RATIO

Case	$P_{2,ave}/P_{out}$	$P_{3,ave}/P_{out}$
I	$\frac{2K_{P1}}{\pi \cdot K_{M1}} \int_0^{\pi} \frac{M_{CB}\sin^2\theta}{M_{CB}-\lvert\sin\theta\rvert} d\theta$	$1-K_{P1}$
II	$\frac{4}{\pi \cdot K_{M1}}\left[\int_0^{\vartheta_T} \frac{M_{CB}\sin^2\theta \cdot K_{P1}}{\left(M_{CB}-\lvert\sin\theta\rvert\right)} d\theta + \int_{\vartheta_T}^{\frac{\pi}{2}} \frac{M_{CB}\sin^2\theta \cdot k_{p2}(\theta)}{\left(M_{CB}-\lvert\sin\theta\rvert\right)} d\theta\right]$	$\frac{2}{\pi}\left[\int_0^{\vartheta_T}\left(1-2K_{P1}\sin^2\theta\right)d\theta + \int_{\vartheta_T}^{\frac{\pi}{2}}\left(1-2k_{p2}(\theta)\sin^2\theta\right)d\theta\right]$
III	$\frac{2}{\pi \cdot K_{M1}} \int_0^{\pi} \frac{M_{CB}\sin^2\theta \cdot k_{p2}(\theta)}{\left(M_{CB}-\lvert\sin\theta\rvert\right)} d\theta$	$\frac{1}{\pi}\int_0^{\pi}\left(1-2k_{p2}(\theta)\sin^2\theta\right)d\theta$

The dimensionless variable M_{CB} in (4c) and (24b) can be regarded as the normalized V_{CB} with respect to $V_{\rm inpk}$. In practice, the true value of V_{CB} is lower than the theoretical value because of presence of the equivalent series resistance (ESR) of inductance and capacitor. Thus, in order to avoid the bulk capacitor voltage V_{CB} from exceeding the limitation voltage, 450 V, of the commercial capacitor, it is suggested that M_{CB} had better been controlled below or just equal to 1.2 for $v_{\rm ac} = 265V_{\rm rms}$. Furthermore, the IDP processed by flyback dc/dc semistage from C_B can be expressed as

$$p_3(\theta) = V_O \langle i_{DO2}(t)\rangle = P_{\rm out} - p_1(\theta) = P_{\rm out}\left(1-2k_p\sin^2\theta\right). \tag{26a}$$

Substituting (9) into (26a), p_3 for M_2 mode can be expressed as

$$p_3(\theta) = \left.\frac{d^2\cdot V_{CB}^2}{2f_{\rm S}L_{M2}}\right|_{d=d_{m2}} = \left.\frac{d^2\cdot\left(M_{CB}\cdot V_{\rm inpk}\right)^2}{2f_{\rm S}L_{M2}}\right|_{d=d_{m2}}. \tag{26b}$$

Since p_1 and p_2 (or p_3) vary with θ, they would be expressed as

$$\left.P_{x,\rm ave}\right|_{x=1,2,3} = \left.\frac{1}{\pi}\int_0^{\pi} p_x(\theta)\,d\theta\right|_{x=1,2,3}. \tag{27}$$

Therefore, DP ratio $K_{\rm DP}$ is defined as

$$K_{\rm DP} = \frac{P_{1,\rm ave}}{P_{\rm out}}. \tag{28}$$

In this equation, high $K_{\rm DP}$ implies high efficiency and large utilization performance of T_1. Because the average power sent to and out from C_B are equal for a half line cycle, the IDP ratio $K_{\rm IDP}$ can be defined as

$$K_{\rm IDP} = \frac{P_{2,\rm ave}}{P_{\rm out}} = \frac{P_{3,\rm ave}}{P_{\rm out}} = 1 - K_{\rm DP}. \tag{29}$$

The more detailed IDP ratio expressions defined in (29) for three cases can be derived as shown in Table V by substituting (24b) and (26a) into (27) and normalizing with $P_{\rm out}$. By using iterative approaching methodology for obtaining accurate M_{CB}, the detailed expressions in Table V are calculated repeatedly until (29) is satisfied, and $K_{\rm DP}$, $K_{\rm IDP}$, and M_{CB} can be solved consequently. Following the iterative calculation process, the curves of DP ratio $K_{\rm DP}$ versus output power $P_{\rm out}$ for different line input voltage $v_{\rm ac}$ and operation cases are obtained and shown in Fig. 7, and the curves are obtained by taking the converter parameters in Table IV–case I as an example. It can be seen from Fig. 7 that the relation between $K_{\rm DP}$ and case is $(K_{\rm DP})_{\rm III} > (K_{\rm DP})_{\rm II} > (K_{\rm DP})_{\rm I}$. $K_{\rm DP}$ increases as $P_{\rm out}$ is low or $v_{\rm ac}$ is high.

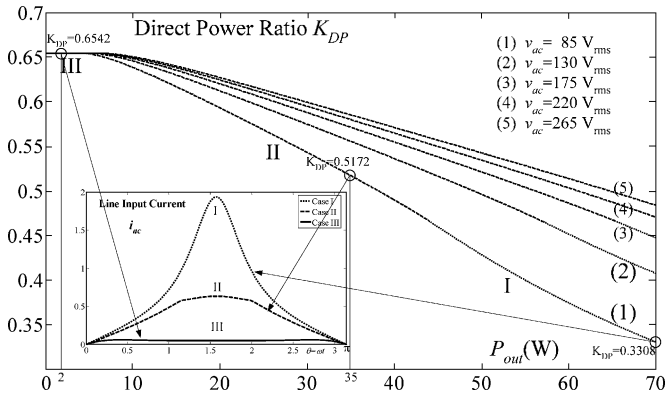

Fig. 7. $K_{\rm DP}$ versus output power for different $v_{\rm ac}$ and cases at the condition of Table IV-case I.

The curves of $K_{\rm DP}$ and M_{CB} versus $P_{\rm out}$ for different K_{M1} and L_{M2} at the assigned conditions of the converter, $L_{M1} = 150$ μH, $n_2 = 1.7$, $V_{\rm ac} = 265$ $V_{\rm rms}$, and $V_{\rm O} = 54$ V, are shown in Fig. 8. Substituting (23) into case III of Table V, M_{CB} obtained from (29) is independent of $P_{\rm out}$. Hence, each M_{CB} curve in Fig. 8(b) is horizontal when converter operates in case III. From Fig. 8(a), it can be seen that $K_{\rm DP}$ is greater at low output power. That is to say, $K_{\rm IDP}$ rises as output power increases. This implies that the DP is the main portion providing the load and the IDP is regarded as energy reservoir used for regulating the power flow to load. Besides, it can be seen from Fig. 8(b) that M_{CB} increases as $P_{\rm out}$ decreases and approaches and holds to the maximum value at lighter load. This phenomenon shows that high bulk capacitor voltage will be resulted at high line and case III. However, from Fig. 8, it also can be seen that $K_{\rm DP}$ goes up and M_{CB} slides down as K_{M1} increases. This is because more input power goes through flyback cell without being buffered by C_B. Hence, for the purpose of obtaining high efficiency and low V_{CB} it is better to select K_{M1} as large as possible. Furthermore, the decrease of L_{M2} can lower both $K_{\rm DP}$ and M_{CB} since it can be seen from (9) that low L_{M2} will result in large current $i_{\rm DO2}$ for M_2 mode or equivalently to say that the output power ratio provided by C_B will be increased. In other words, more output power comes from buffered energy and less input power passes through

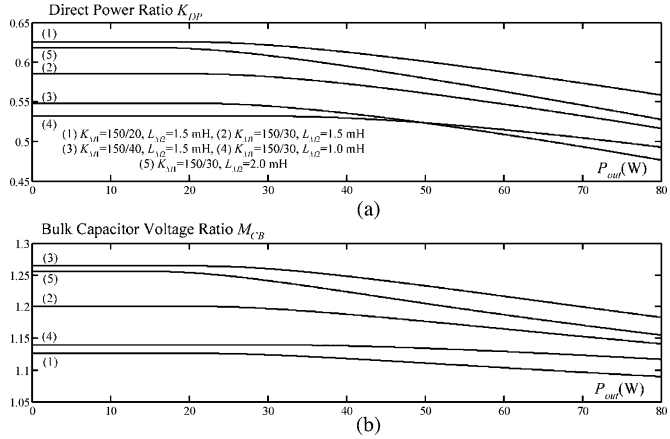

Fig. 8. (a) $K_{\rm DP}$. (b) M_{CB} versus output power for different K_{M1} and L_{M2}, at $L_{M1} = 150\ \mu$H, $n_2 = 1.7$, $V_{\rm ac} = 265\ {\rm V_{rms}}$, $V_O = 54$ V.

flyback cell, so this will result in lower efficiency. However, it is good for reducing the maximum value of M_{CB} since more power is continuously sent out from C_B. Therefore, M_{CB} has to be lower to achieve half line cycle average IDP balance in (29) as can be seen from (24b) and (26b). Besides, decreasing L_{M2} would cause flyback dc/dc semistage closer to DCM but make worse output voltage regulation. A compromise is suggested for selecting proper value of L_{M2} in considering of the proper values of V_{CB}, $K_{\rm DP}$, and output voltage regulation. It can be seen from Fig. 8 that curves (1) and (2) have high $K_{\rm DP}$ and the maximum values of M_{CB} are below or close to 1.2 among all curves. Thus, with the consideration of obtaining high efficiency and low V_{CB}, curves (1) and (2) are better choices.

B. Design Equations

The design equations are going to be derived for the objectives of obtaining proper PFC and output voltage regulation. The DCM operation design of boost–flyback semistage is essential for obtaining good PFC. It can be seen from i_{LM1} waveform in Fig. 3(b) that to guarantee $\rm T_1$ operating in DCM, $d_1\,T_{\rm S}$ should be smaller than $(1-d)T_{\rm S}$. Thus, n_1 should be designed to satisfy the following equation derived from (3c)

$$n_1 \geq \frac{K_{M1}}{(K_{M1}+1)}\frac{V_{\rm inpk}}{V_O}\frac{d_{\rm pk}}{(1-d_{\rm pk})} \tag{30a}$$

where $d_{\rm pk}$ is the duty ratio occurring at $\theta = \frac{\pi}{2}$ as shown in Fig. 5. From (30a), the minimum turns ratio for $\rm T_1$ to operate in DCM is obtained as

$$n_1 \geq n_{1,\min} = \frac{K_{M1}}{(K_{M1}+1)}\frac{V_{\rm inpk,min}}{V_O}\frac{d_{\rm pk,max}}{(1-d_{\rm pk,max})} \tag{30b}$$

where $d_{\rm pk,max}$ is the maximum of $d_{\rm pk}$ and occurs at the lowest rectified line input voltage $v_{\rm in}(t) = V_{\rm inpk,min}|\sin(\pi/2)|$ and the largest output power. With conservative design, $d_{\rm pk,max}$ can be replaced with the acceptable maximum value.

Similarly, to guarantee L_B operating in DCM, $d_2\,T_{\rm S}$ should be smaller than $(1-d)T_{\rm S}$. Thus, L_B and L_{M1} should be designed to satisfy the following equation derived from (2c):

$$(1-d_{\rm pk}) \geq \frac{L_B}{(L_B+L_{M1})}\frac{d_{\rm pk}}{(M_{CB}-1)} \tag{31a}$$

where M_{CB} can be solved from (29) and Table V. From previous section, it can be known that M_{CB} will slide down and $d_{\rm pk}$ thus rises as output power is increasing. Thus, the worst DCM condition occurs at the low input voltage and the large output power for universal application. From (31a), the minimum time ratio needed for i_{LB} to decay to zero before the end of switch OFF time duration can be obtained as

$$D_{dz} = \frac{L_B}{(L_B+L_{M1})}\frac{d_{\rm pk,max}}{(M_{CB,\min}-1)} \tag{31b}$$

where $M_{CB,\min} = V_{CB,\min}/V_{\rm inpk,min}$, and $V_{CB,\min}$ is the minimum bulk capacitor voltage occurring at the lowest rectified line input voltage and the largest output power. However, the converter needs sufficient secondary open voltage of dc/dc semistage transformer $\rm T_2$, V_{CB}/n_2, to guarantee the output regulation operation all the time even at $v_{\rm in}\,(t) = 0$. Hence, for flyblack dc/dc semistage, the following relation must be satisfied

$$\frac{V_{CB}}{n_2}\frac{d_{zc}}{(1-d_{zc})} = V_O \tag{32a}$$

where d_{zc} is the duty ratio at $v_{\rm in}\,(t) = 0$ as denoted in Fig. 5. It can be seen from (32a) that V_O is decreasing as n_2 increases. Thus, after rearranging (32a), the turns ratio limitation of $\rm T_2$ is obtained as

$$n_2 < \frac{V_{CB,\min}}{V_O}\frac{d_{zc,\max}}{(1-d_{zc,\max})} = n_{2,\max} \tag{32b}$$

where $d_{zc,\max}$ is the maximum d_{zc} while occurring at the lowest rectified line input voltage and the largest output power, and $n_{2,\max}$ is the upper bound of n_2 to satisfy output voltage requirement shown in (32a).

C. Example and Design Procedure

To verify the proposed boost–flyback–flyback converter, a prototype converter with the following specifications was designed:

1) ac input voltage ($v_{\rm ac}$): 85–265 $\rm V_{rms}$;
2) output voltage (V_O): 54 V;
3) maximum output power ($P_{\rm out,max}$): 80 W;
4) switching frequency ($f_{\rm S}$): 100 kHz;
5) maximum duty ratio ($D_{\rm max}$) at $v_{\rm ac}$ = 85 $\rm V_{rms}$: 0.44.

As the suggested criterion [17] for universal input voltage $\rm S^2$ converter, the main design objective is to comply with the line current harmonic standards such as IEC61000-3-2 class D, to keep bulk capacitor voltage below 450 V, and to filter output ripple as small as possible.

From the previous section, it can be known that L_B tends to operate in CCM as input voltage decreases and load increases, thus at this condition the harmonic current will get large. Furthermore, the bulk capacitor voltage will be high and may increase over 450 V at high line and light load. While considering the object of input current, the DCM operation gives a better

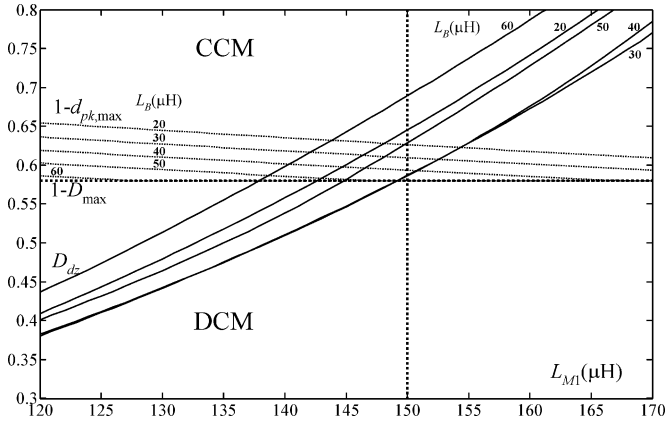

Fig. 9. D_{dz} and $(1-d_{\mathrm{pk,max}})$ versus L_{M1} for different $L_B, L_{M2} = 1.5$ mH, at $D_{\max} = 0.42, v_{\mathrm{ac}} = 85\ \mathrm{V_{rms}}, V_O = 54$ V, and $P_{\mathrm{out}} = 60$ W.

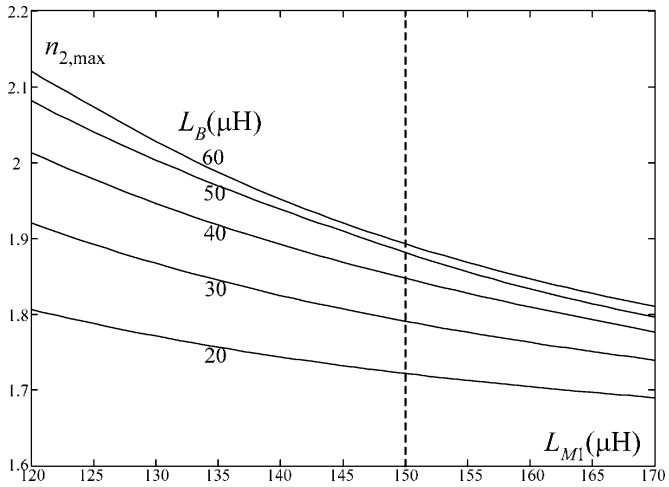

Fig. 10. $M_{CB,\min}$ and $n_{2,\max}$ versus L_{M1} for different $L_B, L_{M2} = 1.5$ mH, at $D_{\max} = 0.42, v_{\mathrm{ac}} = 85\ \mathrm{V_{rms}}, \mathrm{V}_O = 54$ V, and $P_{\mathrm{out}} = 60$ W.

TABLE VI
PARAMETERS OF CRITICAL COMPONENTS

L_B	35 μ H
T_1	L_{M1}=145 μ H; n_1=1.6
T_2	L_{M2}=1.4 mH; n_2=1.8
S	K2968
C_B	470 μ F/450 V
C_O	220 μ F/100 V

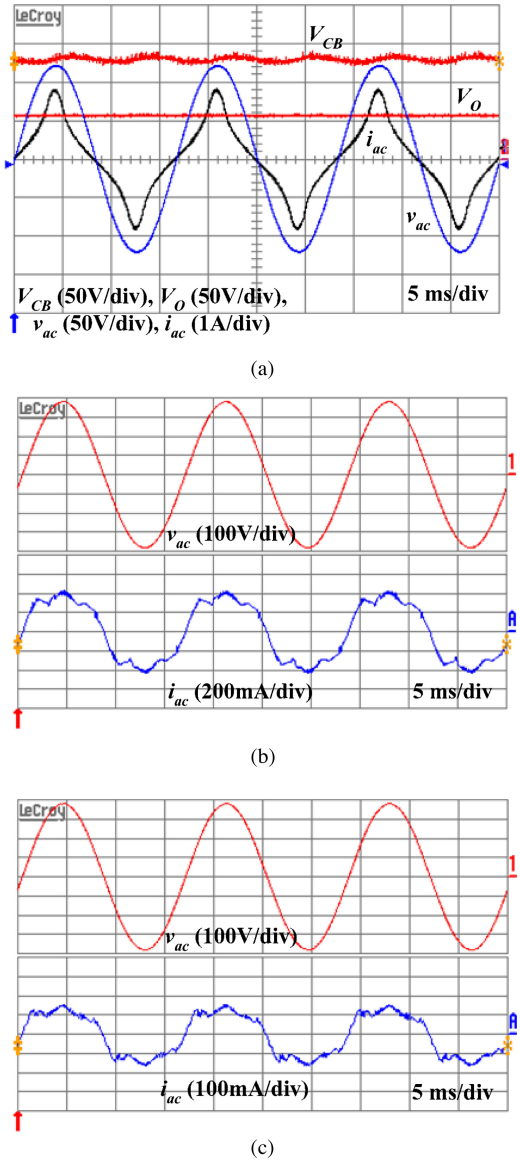

Fig. 11. Measured line voltage, bulk capacitor voltage, line current, output voltage. (a) $v_{\mathrm{ac}} = 85\ \mathrm{V_{rms}}, P_{\mathrm{out}} = 60$ W. (b) $v_{\mathrm{ac}} = 265\ \mathrm{V_{rms}}, P_{\mathrm{out}} = 60$ W. (c) $v_{\mathrm{ac}} = 265\ \mathrm{V_{rms}}, P_{\mathrm{out}} = 20$ W.

PF in comparing with that given by the CCM operation. However, the CCM operation offers higher conversion efficiency and lower switch current stress than those given by the DCM operation. For the regular design, it is not easy to be realized in practice that L_B operates in DCM under the lowest line and the fullest load condition. Hence, it is not necessary for L_B to operate in DCM during the whole half cycle, and the worst DCM condition for L_B in this example is set at $v_{\mathrm{ac}} = 85\ \mathrm{V_{rms}}$, and $P_{\mathrm{out}} = 60$ W. It is permissible that L_B operates in CCM during a small interval within a half line cycle, that is also called semi-continuous conduction mode (SCM) [17] while $v_{\mathrm{ac}} = 85\ \mathrm{V_{rms}}$ and $P_{\mathrm{out}} > 60$ W, as long as the IEC regulation can be satisfied. With the substitution of the earlier specifications to (30b), DCM condition for T_1 could be reached as long as n_1 and K_{M_1} were properly selected. However, L_{M1} and L_B cannot be determined by (31b) directly since L_{M2} must be assigned in advance, and further, $M_{CB,\min}$ and $d_{\mathrm{pk,max}}$ have to be calculated. For the object of low bulk capacitor voltage, M_{CB} had better no more than 1.2 at high line and light load condition in order to guarantee V_{CB} below 450 V by properly selecting K_{M1} and L_{M2}. The critical parameters L_B, L_{M1}, n_1, L_{M2}, and n_2 are interrelated and designed from the following procedure.

1) Assign L_{M2} at first, and calculate $M_{CB,\min}$ and $d_{\mathrm{pk,max}}$ by following the iterative calculating process in

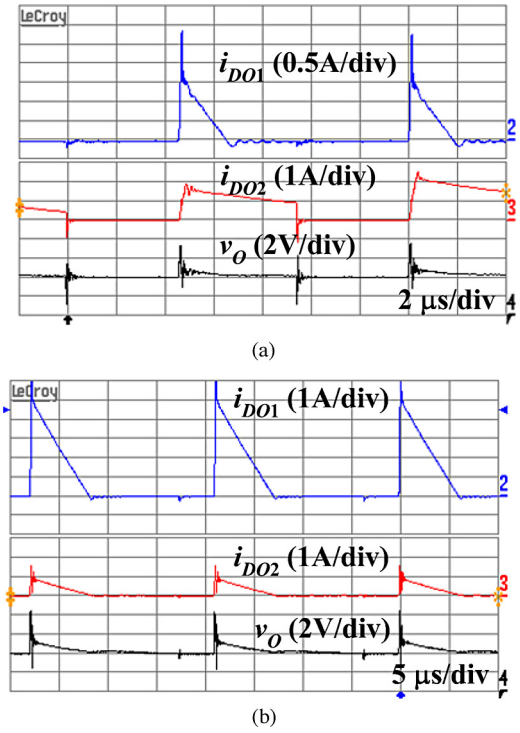

Fig. 12. Measured switching waveforms. (a) M_1 mode. (b) M_2 mode at $v_{\rm ac} = 130\ {\rm V_{rms}}, R_L = 60.24\ \Omega$.

Section III-A at the preset worst DCM condition of L_B, $v_{\rm ac} = 85\ {\rm V_{rms}}$, and $P_{\rm out} = 60$ W.

2) Generate the curves of $(1 - d_{\rm pk,max})$ and $D_{\rm dz}$ versus L_{M1} for different L_B by using equation (31b) with the calculated $M_{CB,\rm min}$ and $d_{\rm pk,max}$ in step 1.
3) Generate the curves of $n_{2,\rm max}$ versus L_{M1} for different $L_{\rm B}$ with substituting $M_{CB,\rm min}$ and $d_{zc,\rm max}$ in (32b), and set $d_{zc,\rm max}$ to 0.42 while $P_{\rm out} = 60$ W to prevent from over 0.44 when $P_{\rm out} = 80$ W.
4) Select L_{M1} and L_B from the curves of $(1 - d_{\rm pk,max})$ and $D_{\rm dz}$ provided from step 2 such that L_B can operate in DCM at the preset worst DCM condition, and hence $K_{M1} = L_{M1}/L_B$ is determined.
5) Select n_2 with selected L_{M1} and L_B from $n_{2,\rm max}$ curves given by step 3 such that flyback dc/dc semistage can correctly fulfill output regulation.
6) Select n_1 with the selected K_{M1} from step 4 substituted to (30b) such that T_1 can operate in DCM.
7) Calculate M_{CB} at high line and light load with the selected L_B, L_{M1}, n_1, L_{M2}, and n_2 by following the iterative calculating process in Section III-A.
8) Check M_{CB} whether it is below 1.2 at high line and light load or not. If not, reduce L_{M2} and repeat steps 1–7 until M_{CB} is equal to or smaller than 1.2 at high line and light load.

Following these procedures, the final curves of $(1 - d_{\rm pk,max})$ and $D_{\rm dz}$ are shown in Fig. 9, the curves of $n_{2,\rm max}$ are shown in Fig. 10, and the designed parameters of key components are obtained as $L_B = 30\ \mu$H, $L_{M1} = 150\ \mu$H, $n_1 = 1.6$, $L_{M2} = 1.5$ mH, $n_2 = 1.7$.

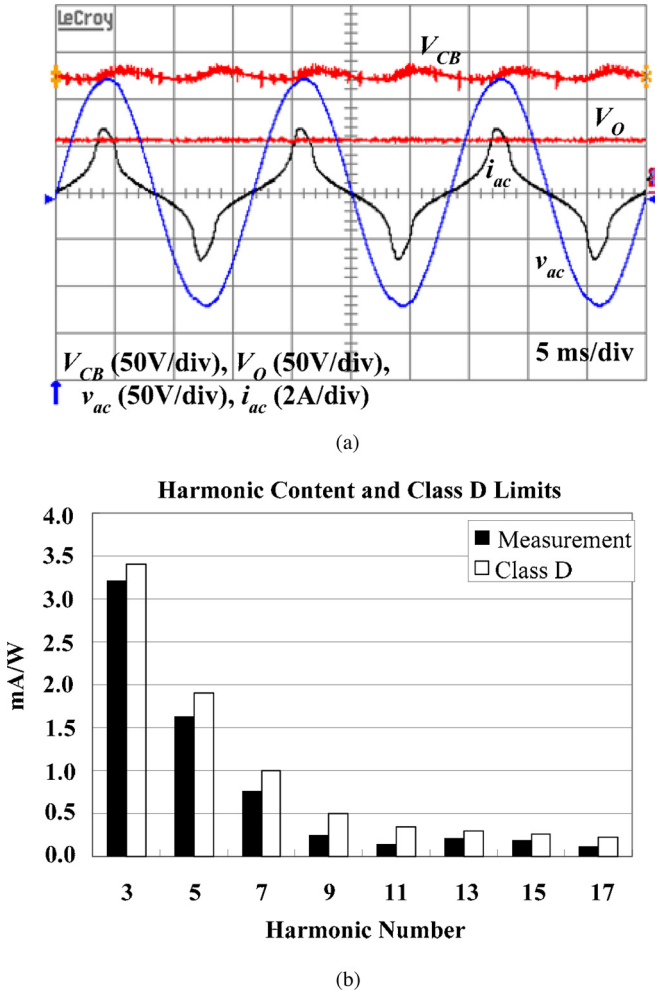

Fig. 13. (a) Line voltage and line current measured at worst condition. (b) Harmonic content and class D limits.

IV. Experimental Results

For presenting the performance of the prototype based on the proposed topology, the circuit of Fig. 2(b) and (c) has been built and tested in the specifications described in Section III-C. The parameters of the critical components are given in Table VI. Because the input current $i_{\rm in} = i_{LB}$ of the proposed converter is pulsating when $L_{\rm B}$ operates in DCM, the electromagnetic interference (EMI) level would be above the limits of standard such as Federal Communications Commission (FCC) or International Special Committee on Radio Interference (CISPR). Hence, an input filter with low input displacement angle between input voltage and current, minimum interaction with the converter and system stability are designed to attenuate EMI to meet regulatory specifications and get smooth waveform of line input current $i_{\rm ac}$ in Figs. 11 and 13(a). The detailed design and analysis about input filter could be referred to [18] and [19]. The key waveforms at $v_{\rm ac} = 85\ {\rm V_{rms}}/P_{\rm out} = 60$ W, $v_{\rm ac} = 265\ {\rm V_{rms}}/P_{\rm out} = 60$ W, and $v_{\rm ac} = 265\ {\rm V_{rms}}/P_{\rm out} = 20$ W are presented in Fig. 11, and the switching waveforms for M_1 mode and M_2 mode at $v_{\rm ac} = 130\ {\rm V_{rms}}/R_{\rm L} = 60.24\ \Omega$ are presented in Fig. 12. As can be seen, the shapes of line input current $i_{\rm ac}$ are approaching to the average input currents shown in Fig. 5. The

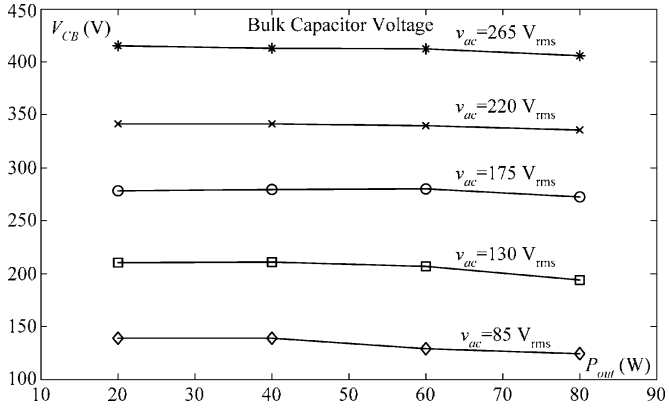

Fig. 14. Measured bulk capacitor voltage under line and load variations.

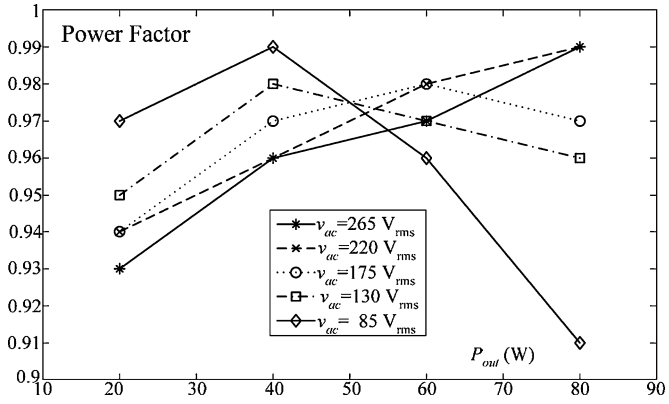

Fig. 15. Measured power factor under line and load variations.

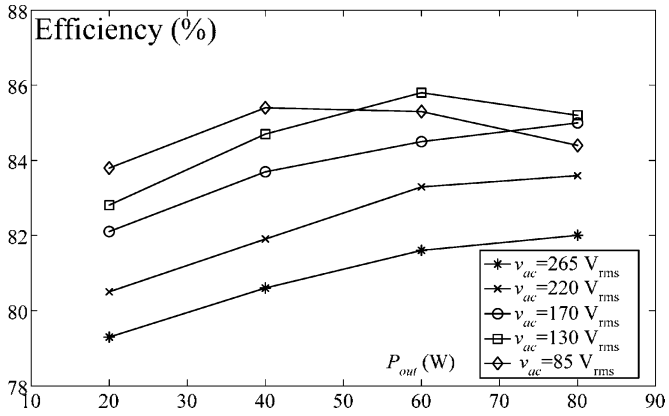

Fig. 16. Measured efficiency under line and load variations.

measured key waveforms at the worst condition ($v_{\rm ac} = 85\ {\rm V_{rms}}$ and $P_{\rm out} = 80$ W) are shown in Fig. 13(a). Although the line input current is distorted due to the SCM operation of L_B, its harmonic contents still comply with the class D limits as shown in Fig. 13(b). Fig. 14 shows the measured bulk capacitor voltage under line and load variations. The maximum bulk capacitor voltage is 415.4 V, which is below the commercial size 450 V and occurs at $v_{\rm ac} = 265\ {\rm V_{rms}}$ with $P_{\rm out} = 20$ W. Fig. 15 shows measured power factor under line and load variations. It can be seen that the lowest power factor is 0.91 and occurs at the worst condition. The power factors at most conditions are above 0.95 and some even reach 0.99. As described in Sections III-B and III-C, L_B tends to operate in CCM as input voltage decreases and load increases, and the worst DCM condition for L_B is set at $v_{\rm ac} = 85\ {\rm V_{rms}}$ and $P_{\rm out} = 60$ W. Hence, L_B begins to operate in SCM when $P_{\rm out}$ is greater or equal to 60 W. Consequently, $i_{\rm ac}$ is distorted and PF degrades as can be seen $v_{\rm ac} = 85\ {\rm V_{rms}}$ curve in Fig. 15. Fig. 16 shows efficiency under line and load variations. The efficiency is greater than 80% in most operating range, and the maximum value is 85.8% at $v_{\rm ac} = 130\ {\rm V_{rms}}$ with $P_{\rm out} = 60$ W.

V. Conclusion

The SSTO boost–flyback converter and corresponding S^2 parallel converter were introduced in this paper. The SSTO boost–flyback converter has appreciable self-PFC property when operates in DCM. By cascading dc/dc semistage to the boost cell output of boost–flyback converter, the S^2 parallel converter can achieve input line current shaping and tight output voltage regulation with single-loop feedback control. Since partial of input power is processed only once by flyback cell, so the conversion efficiency is improved and the switch current stress is small compared with the conventional S^2 converter. The proposed circuit has two parallel power streams so that the components could be small. Furthermore, the analysis of the implemented circuit and the design procedure for universal application are also presented. With this procedure, an 80 W prototype was built and tested. The experimental results show that the voltage across bulk capacitor is kept under 415.4 V for full range operation (85–265 $\rm V_{rms}$) and load (20–80 W). The maximum power factor is 0.99 and the measured line current harmonic contents at the worst condition comply with the IEC61000-3-2 class D limits. The maximum efficiency is 85.8%. This new circuit structure also can be extended to more alternative parallel combinations. Therefore, the proposed parallel converter presents an overall good performance in the main aspects of universal S^2 PFC converters.

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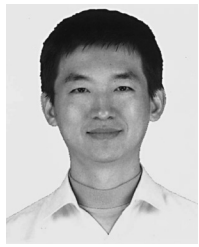

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