國立交通大學

電機資訊學院 電信學程

碩 士 論 文

低相位雜訊架構之 ku 頻段鎖相震盪器

Low Phase Noise Architecture Study of a Ku Band Phase Locked Oscillator

研 究 生：李建志

指導教授：周復芳 博士

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學生：李建志　　指導教授：周復芳 博士

國立交通大學電機資訊學院 電信學程（研究所）碩士班

摘　　要

本論文研製低相位雜訊之 Ku 頻段鎖相震盪器。主要分為兩部份，第一部份使用一般直接除頻架構之鎖相迴路來實現鎖相震盪器。第二部份使用混波器取代直接除頻架構中之除頻器來實現鎖相震盪器。利用混波器相位雜訊之特性來取代除頻器以降低整個迴路的除頻比例，藉此來改善輸出端之相位雜訊。兩種架構之電路同時被分析並實現。本論文測試結果顯示使用混波器取代直接除頻架構中之除頻器之架構於 15.2 GHz 距離載波 100KHz 之相位雜訊為-106.33 dBc/Hz，此結果優於直接除頻架構，以本論文所測試結果，相位雜訊能夠改善 8.84 dB。

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student：Chien-Chih Lee　　Advisors：Dr. Christina F. Jou

Degree Program of Electrical Engineering Computer Science
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ABSTRACT

The thesis is low phase noise architecture study of a Ku band phase locked oscillator. The content is divided into two parts. In section 1, the general direct division architecture is used to implement phase locked oscillator (PLO). In section 2, mixer is used to replace frequency divider in general architecture. Using mixer to replace frequency divider can reduce the frequency division ratio and improve output phase noise performance. Two kinds of architectures are analyzed and produced. The test results show that using mixer to replace frequency divider can improve the output phase noise. The phase noise at 15.2 GHz offset carrier 100 KHz is –106.33 dBc/Hz. It is 8.84 dB better than the direct division architecture.

誌　　謝

本論文得順利完成，首先感謝周復芳教授於在學期間給予之指導。同時感謝在學期間所有幫助過我的教授、同學及同事。謝謝我的父母李泰山先生和李郭秀琴女士三十多年來的辛苦栽培及支持，在此獻上個人最崇高的敬意與謝意。也感謝老婆佳娥及家人這麼多年來的陪伴，謝謝你們使我能夠順利完成學業。

李建志　2005/6 於交通大學

目　　錄

Chapter 1 Introduction

1.1 Objective of this thesis

The phase noise performance [1][2] of different structures phase-locked oscillators is studied in this thesis. A mixer replaces a frequency divider [3] in a direct division structure phase-locked oscillator in order to gain better phase noise performance. The concept of the structure is to use mixer's phase noise characteristics to reduce phase noise degradation at frequency divider of loop path. Two types of PLO are designed. One is direct division structure, and another is used mixer to replace divider structure. Two types of PLO are design at X-band and multiplied to Ku-band.

1.2 Motivation

In digital communication system, BER (bit error rate) is a parameter to evaluate the system performance. Phase noise is one of the critical parameters

that can affect the system BER test result. On the other hand, for higher data rates, higher transmitting frequencies have to be used due to the limited available bandwidth. Higher transmitting frequency and lower phase noise performance are required in modern digital communication systems. It is critical to generate a high frequency, low phase noise local oscillator for up-conversion and down-conversion. In this thesis, two types of PLO's phase noise performances are measured and compared. The phase noise performance of mixer structure is at least 2dB better than the direct division structure.

1.3 Overview

This paper consists of five chapters.

Chapter 1 introduces of the motivation of this thesis.

Chapter 2 describes the phase noise definition and its effect in practical system.

Chapter 3 presents the general structure of PLL and its performance.

Chapter 4 introduces the architecture to improve phase noise.

Chapter 5, propose some topics for future study.

Chapter 2 Phase noise

2.1 Noise in oscillator systems [4]

Frequency stability is a critical specification of oscillators. We are both interested in long-term and short-term frequency stability. In communication systems, long-term stability is also called central frequency tolerance or frequency accuracy. It is concerned with the frequency varies over a time interval (hours, months, or years). It is usually specified as the ratio, △f/f for a given period of time, expressed as PPM or in dB.

On the other hand, short-term stability can be easy to understand. These variations can be random or periodic. A spectrum analyzer can be used to measure the short-term stability of a signal. Fig. 2-1 shows a typical spectrum, with random and discrete frequency components causing a broad skirt and

spurious peaks. The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to *phase noise*. It can be the result of thermal noise, shot noise and/or flicker noise in active and passive devices.

2.2 Phase noise in voltage-controlled oscillators

Before we look at phase noise in a PLL system, it is worth considering the phase noise in a voltage-controlled oscillator (VCO). An ideal VCO would have no phase noise. Its output as seen on a spectrum analyzer would be a single spectral line. In practice, of course, this is not the case. There will be jitter on the output, and a spectrum analyzer would show phase noise. To help understand phase noise, consider a phasor representation, such as that shown

in Fig. 2-2. ω_0 represents an output signal of angular velocity, ω_0. Superimposed on this is an error signal represented by ω_m. To quantify this error, it is possible to take the rms value of the phase fluctuations and express them as $\Delta\theta$. This then is the phase error or jitter and may be express in rms picoseconds (ps rms) or rms degrees (θ_{rms}).

In many radio systems, an overall integrated phase error specification must be met. This overall phase error is made up of the PLL phase error, the modulator phase error and the phase error due to base band components. In GSM, for example, the total allowed is 5 degrees rms [5].

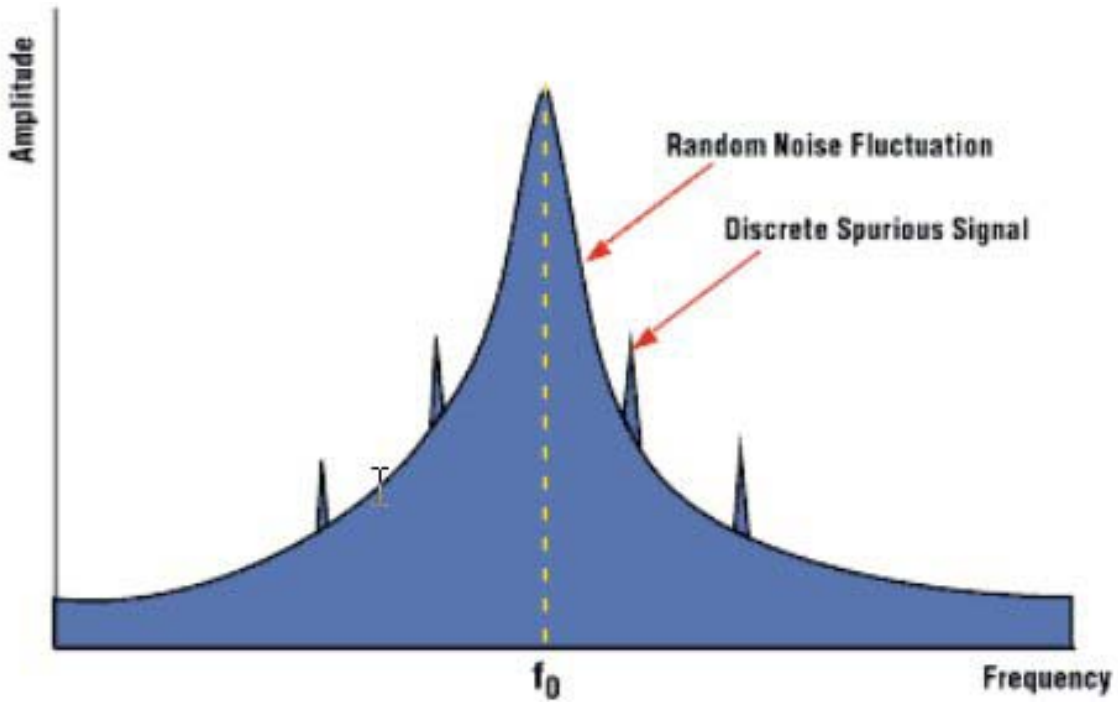

Fig 2-1 Short-term stability in oscillators

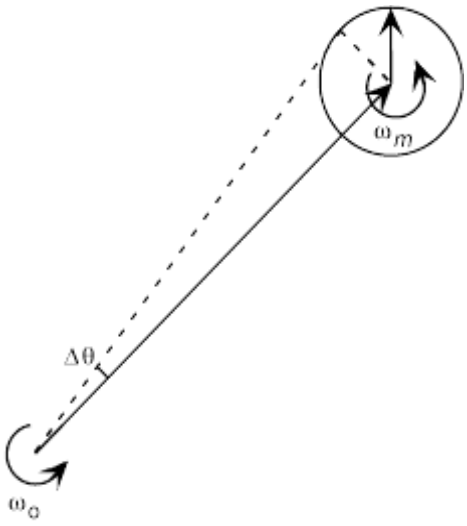

Fig 2-2 Phasor representation of phase noise

2.3 Lesson's oscillator model [6]

An oscillator can be modeled as an amplifier with positive feedback. If the phase noise is added to an amplifier that has a noise figure F, with F defined by

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} = \frac{N_{out}}{N_{in}G} = \frac{N_{out}}{GkTB} \tag{2-1}$$

$$N_{out} = FGkTB \tag{2-2}$$

$$N_{in} = kTB \tag{2-3}$$

where N_{in} is the total input noise power to a ideal noise-free amplifier.

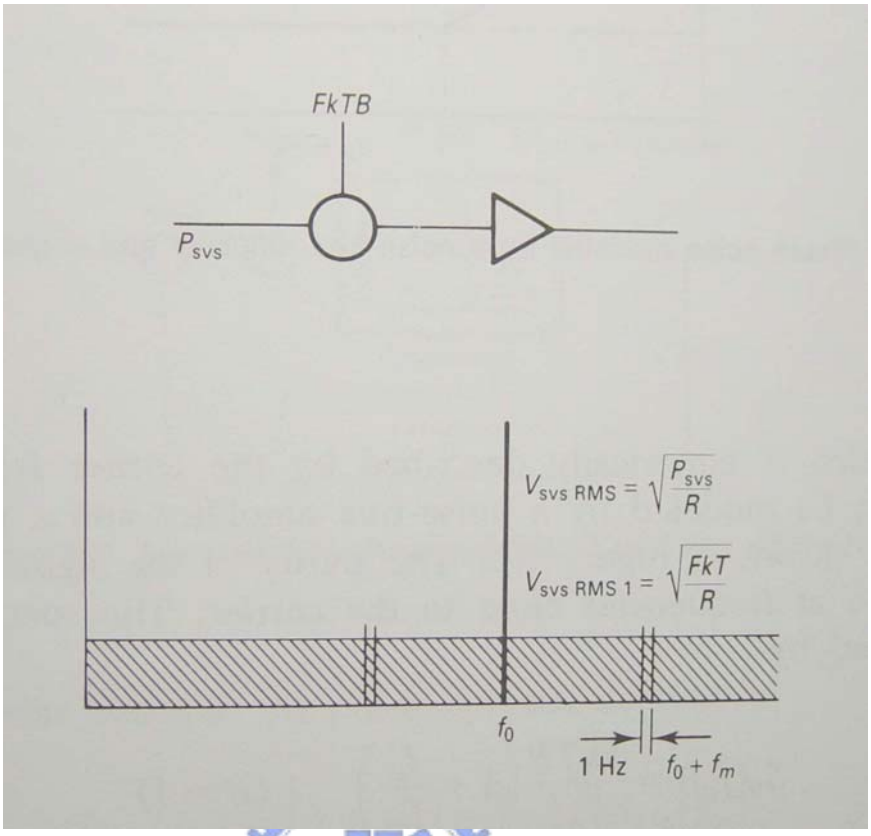

Fig 2-3 Phase noise added to carrier [6]

The input phase noise in a 1-Hz bandwidth at any frequency f_0+f_m from the carrier produces a phase deviation given by (Fig. 2-3)

$$\Delta\theta_{peak} = \frac{V_{nRMS\ 1}}{V_{avsRMS}} = \sqrt{\frac{FkT}{P_{avs}}} \tag{2-4}$$

$$\Delta\theta_{RMS} = \frac{1}{\sqrt{2}}\sqrt{\frac{FkT}{P_{avs}}} \tag{2-5}$$

From the Eq.2-5, the total phase deviation is

$$\Delta\theta_{RMStotal} = \sqrt{FkT/P_{avs}} \tag{2-6}$$

The phase noise spectrum density becomes

$$S_\theta(f_m) = \Delta\theta^2_{RMS} = FkTB/P_{avs} \tag{2-7}$$

For a modulation frequency close to the carrier, $S_\theta(f_m)$ shows a flicker or 1/f component. The phase noise model can use a noise-free amplifier and a phase modulator combination as shown in Fig 2-4. The spectral density of purity signal add flicker noise can be represent by

$$S_\theta(f_m) = \frac{FktB}{P_{avs}}(1 + \frac{f_c}{f_m}) \tag{B=1}$$

(2-8)

The oscillator may be modeled as an amplifier with feedback as shown in Fig. 2-5. The phase noise at the input of the amplifier is affected by the resonator bandwidth in the oscillator circuit. The tank circuit has a low pass transfer function

$$L(\omega_m) = \frac{1}{1 + j(2Q_L\,\omega_m/\omega_0)}$$

(2-9)

where $\omega_0/2Q_L = B/2$ is the half bandwidth of resonator.

The close loop response of the phase feedback loop is given by

$$\Delta\theta_{out}(f_m) = \left(1 + \frac{\omega_0}{j2Q_L\omega_m}\right)\Delta\theta_{in}(f_m)$$

(2-10)

The power transfer becomes the phase spectral density

$$S_{\theta\,out}(f_m) = \left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right]S_{\theta in}(f_m)$$

(2-11)

So the phase noise at the output of amplifier is

$$L(f_m) = \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right]S_{\theta in}(f_m)$$

(2-12)

From Eq. (2-8) and Eq. (2-12), the overall phase noise is

$$L(f_m) = \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{f}{2Q_L}\right)^2\right]\frac{FkT}{P_{avs}}\left(1 + \frac{f_c}{f_m}\right)$$
$$= \frac{FkTB}{2P_{avs}}\left[\frac{1}{f_m^3}\frac{f^2 f_c}{4Q_L^2} + \frac{1}{f_m^2}\left(\frac{f}{2Q_L}\right)^2 + \frac{f_c}{f_m} + 1\right] \text{ dBc/Hz} \qquad (2\text{-}13)$$

2.4 Phase noise characteristics of divider

In this article, it is important to know the phase noise characteristics of dividers for estimating the overall PLL phase noise performance. Let us assume an instantaneous phase $\theta_i(t)$ of a carrier frequency modulated by a sine wave of frequency f_m is given by

$$\theta_i(t) = \omega_0 t + \frac{\Delta f}{f_m}\sin\omega_m t \qquad (2\text{-}14)$$

Instantaneous frequency is defined as the time rate of change of phase

$$\omega(t) = \frac{d\theta_i(t)}{dt} = \omega_0 + \frac{\Delta f}{f_m}\omega_m \cos\omega_m t \qquad (2\text{-}15)$$

If this signal passes through a frequency divider that divides the frequency by N, the output frequency ω' will be given by

$$\omega' = \frac{\omega_0}{N} + \frac{\Delta\omega}{N} \qquad (2\text{-}16)$$

and the out phase by

$$\theta_i(t) = \frac{\omega_0 t}{N} + \frac{\Delta f}{N f_m} \sin \omega_m t \qquad (2\text{-}17)$$

The fundamental frequency at the divider output is

$$S(t) = V \cos\left(\frac{\omega_0 t}{N} + \frac{\Delta f}{N f_m} \sin \omega_m t \right) \qquad (2\text{-}18)$$

where V is the input peak voltage. The divider reduces the carrier frequency by N but does not change the frequency of the modulation signal. The peak phase deviation θ_p is reduced by the division ratio N. Since it is shown that the ratio of the noise power to carrier power is

$$\frac{V_n^2}{V^2} = \frac{\theta_p^2}{4} \qquad (2\text{-}19)$$

Frequency divide by N reduces the noise power by N^2 for a perfect divider.

2.5 Phase noise calculation of mixer

Mixers are unique with respect to phase noise analysis because they

have typically two or more input frequencies. This does not affect the phase noise analysis. However, we need to know the operation of mixer in order to apply a heuristic formulation of analysis. The essence of mixer operation is linear in the in the sense that a sum or difference signal is the final output, even if the actual operation is nonlinear. Remember, the output signal from a resistive mixer is the result of the spectral product of a signal with a conductance that is changing at the local oscillator frequency.

An ideal mixer, that is, a mixer that adds no noise, would degrade the input noise to carrier ratio only if the conversion loss is 0 dB and the corner frequency of the mixer diode is 0 Hz. Further, because the output signal is the sum or difference frequency, the cumulative effect of mixer is the root-mean-square (rms) sum of the noise to carrier ratios of the input signals. Fig. 2-4 shows the structure of the mixer phase noise to carrier model prediction. The added noise of mixer is represented by the factor FkT , and the

mixer conversion loss is represented by the output attenuator having a value L_c , i.e., the mixer conversion loss. The input signal noise to carrier ratio at the R-port is $(N_i/C_i)|_R$ while the noise to carrier ratio at the L-port of mixer is $(N_i/C_i)|_L$. With this understanding, the noise to carrier ratio degradation may be written as

$$L_o(f_m)_{dB} = 10\log\times\left[10^{\left[\frac{L_{iR}(f_m)_{dB}}{10}\right]}+10^{\left[\frac{L_{iL}(f_m)_{dB}}{10}\right]}+\left(1+\frac{f_c}{f_m}\right)\times 10^{\left(\frac{F_0+kT-C_{iR}}{10}\right)_{dB}}+10^{\left(\frac{kT-C_o}{10}\right)_{dB}}\right] \quad (2\text{-}20)$$

The following definitions are applicable to this equation.

- $L_o(f_m)_{dB}$ is the output noise-to carrier ratio in dBc/Hz at a carrier offset frequency of f_m.
- $L_{iR}(f_m)_{dB}$ is the input noise-to-carrier ratio in dBc/Hz at a carrier offset frequency of f_m at the R-port of the mixer.

- $L_{iL}(f_m)_{dB}$ is the input noise-to-carrier ratio in dBc/Hz at a carrier offset frequency of f_m at the L-port of the mixer.
- kT=-174dBm/Hz
- C_i is the carrier input power in dBm at the R-Port.
- C_o is the carrier output power in dBm at the X-Port.
- F_0 is the noise figure floor of the active element in dB.
- The numeric factor $\left[1+(f_c/f_m)\right]$ accounts for the active element, i.e., mixer diode flicker noise.

If the mixer uses silicon Schottky diodes, the parameters of Table 5.1 may be used for the noise figure and flicker noise corner frequency. GaAs Schottky diodes, typically used for millimeter wave mixers, have significantly higher flicker noise corner frequency [14].

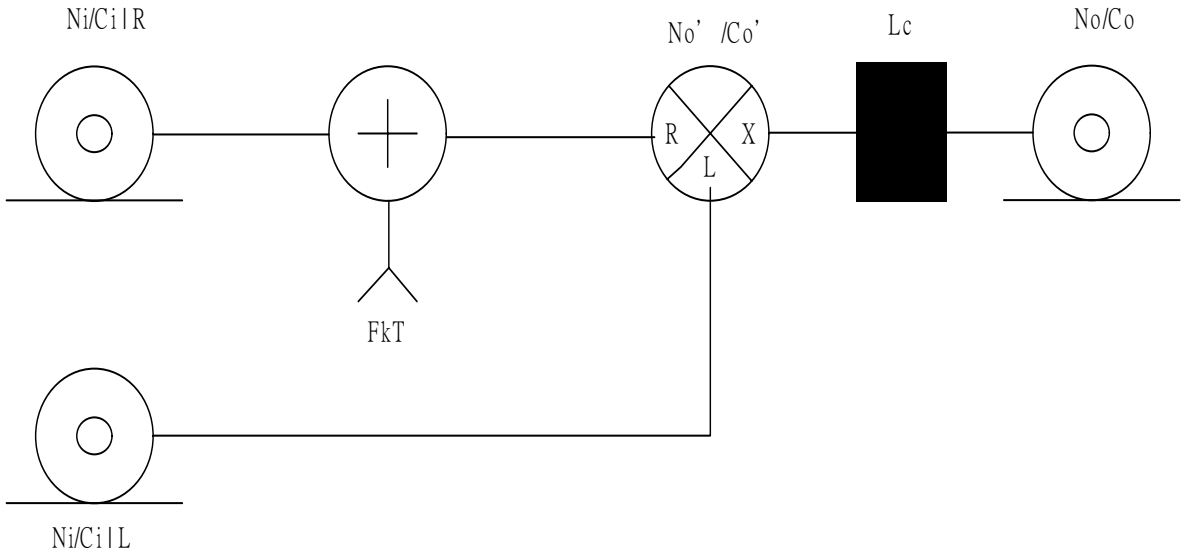

Fig. 2-4 Mixer added phase noise model

Diode Type	F_0 -noise figure (dB)	f_C -corner Frequency (KHz)
Schottky (Silicon)	0.0	25.0
Step recovery(0 Vdc)	0.0	50.0

Table 4-1 Diode residual phase noise data

2.6 Practical example of phase noise effect

Fig.2-5 is an ideal 16-QAM constellation diagram. If we include the phase noise effect, the constellation diagram will become to Fig.2-6. You can

see that phase jitter will affect the digital symbol decision. In this situation, the phase noise performance will impact the communication quality especially in the higher order modulation scheme. Fig.2-7 shows the 16-QAM [17] and 64-QAM scatter plots. We can see that 16-QAM the constellation points are well within the decision regions, whereas, the 64-QAM case clearly shows that decision errors would be caused by only small noise excursions. [7]

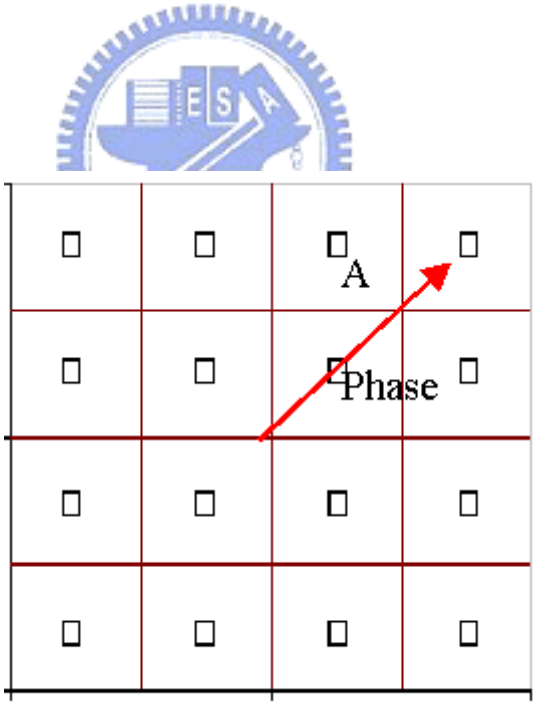

Fig 2-5 Ideal 16 QAM constellation diagram

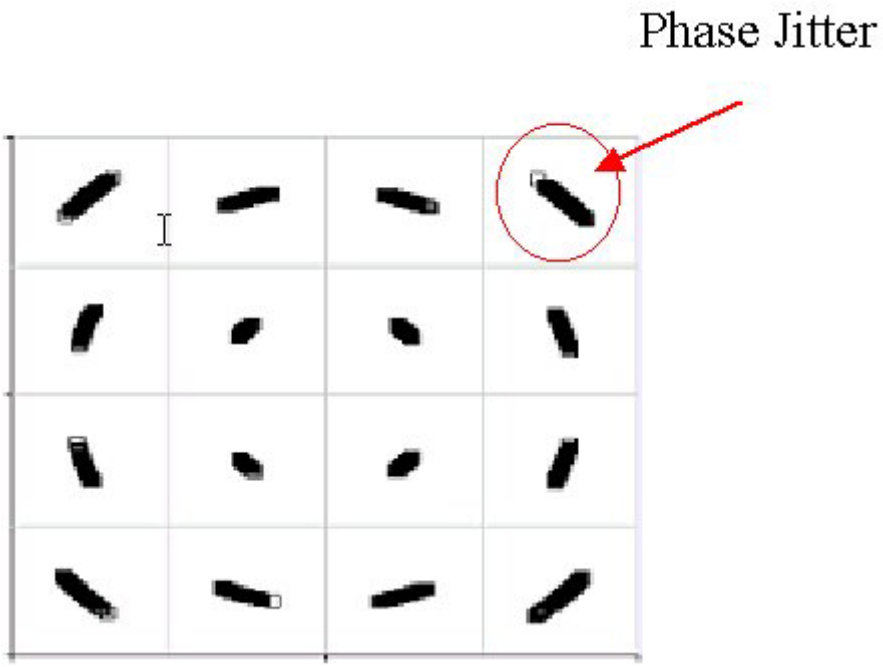

Fig 2-6 Practical 16 QAM constellation diagram

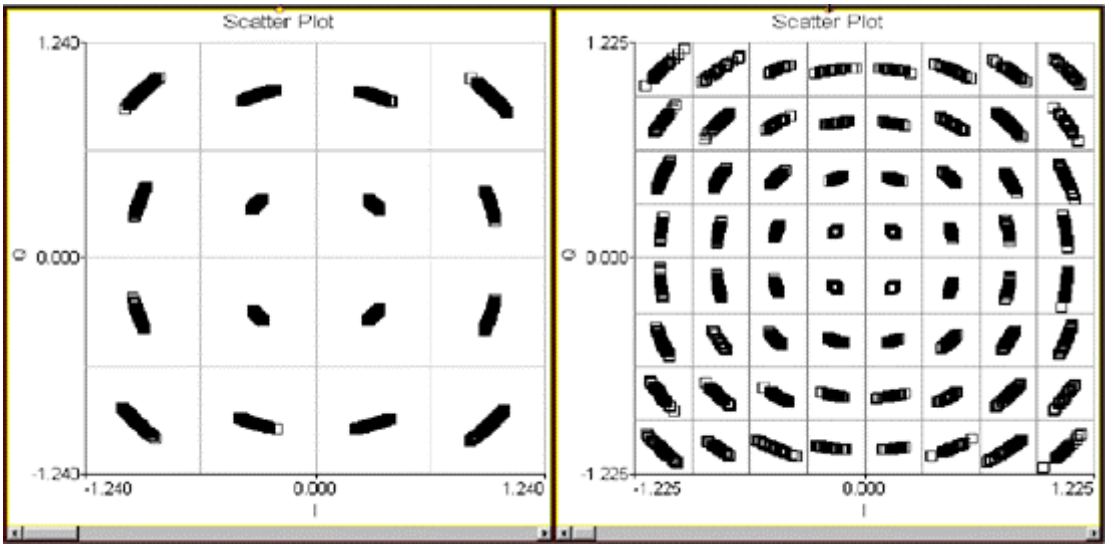

Fig 2-7 Practical 16 QAM and 64 QAM constellation diagram

Chapter 3 General architecture of PLL

3.1 Phase-locked loop basics

Fig. 3-1 shows a basic Phase-locked loop block diagram. It consists of six components [11].

1. Crystal reference
2. Reference divider
3. Loop filter
4. VCO
5. Main divider
6. Phase detector

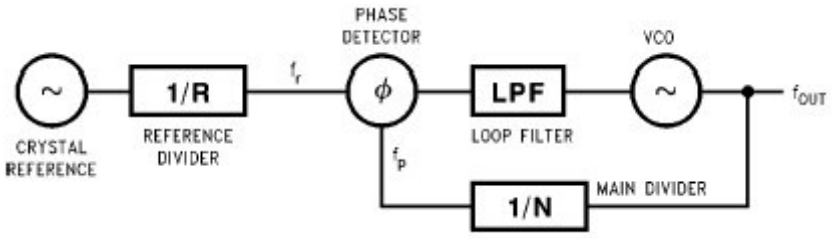

Fig. 3-1 Basic Phase locked-loop block diagram

The six blocks are introduced briefly. It is clear that crystal reference is a reference signal source for VCO locked to it. Reference divider and main divider are frequency dividers. These two dividers output two signals (f_r and f_p) into phase detector. Phase detector will compare two signals' frequency and phase, to generate an error signal into Loop filter. Loop filter is a low pass filter. The output of loop filter is a control voltage to control VCO output frequency f_{out}. Then VCO output signal feed-in the main divider form a closed loop. This structure is a negative feedback loop. Finally, the f_p and f_r will have the same frequency and phase. It is so-called the loop is locked.

3.2 7.6 GHz VCO design

Oscillator can be designed by controlling the reflection coefficient or the loop gain of the transistor [8]. One of the critical components of PLO is VCO. In this thesis, a VCO which frequency covers 7.6 GHz needs to be designed. Negative impedance oscillator [9] method is used to design this VCO [10].

First, transistor BFG425W's stability factor was simulated. Fig. 3-2 shows BFG425W's K factor between 3 to 9 GHz. It can be seen that K>1 at the frequency between 3 GHz to 9 GHz.

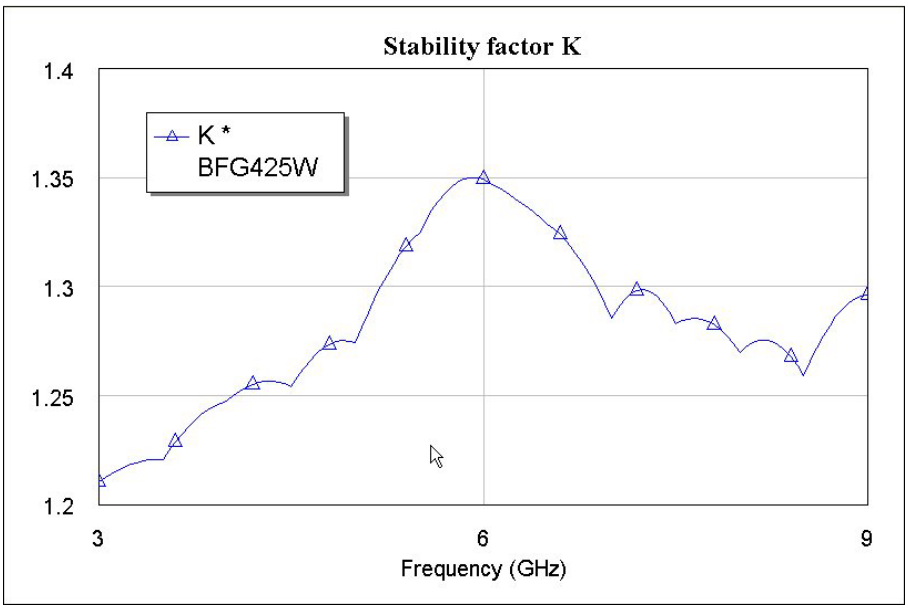

Fig 3-2 Philips NPN transistor BFG425W K factor

To design the oscillator at 7.6 GHz, K<1 is needed. An open stub feedback is added at the emitter of BFG425W for getting K<1. In Fig.3-3, it can be seen the K=0.38409<1 at 7.6 GHz after added the open stub. A section of microstrip line and a varactor diode MA46H200-1088 are used as resonator at BFG425W's base. Resonate the input port by adjust the microstrip line's width and length to get the negative resistor at the desired frequency. Fig. 3-4 shows the output negative resistance simulation result of VCO.

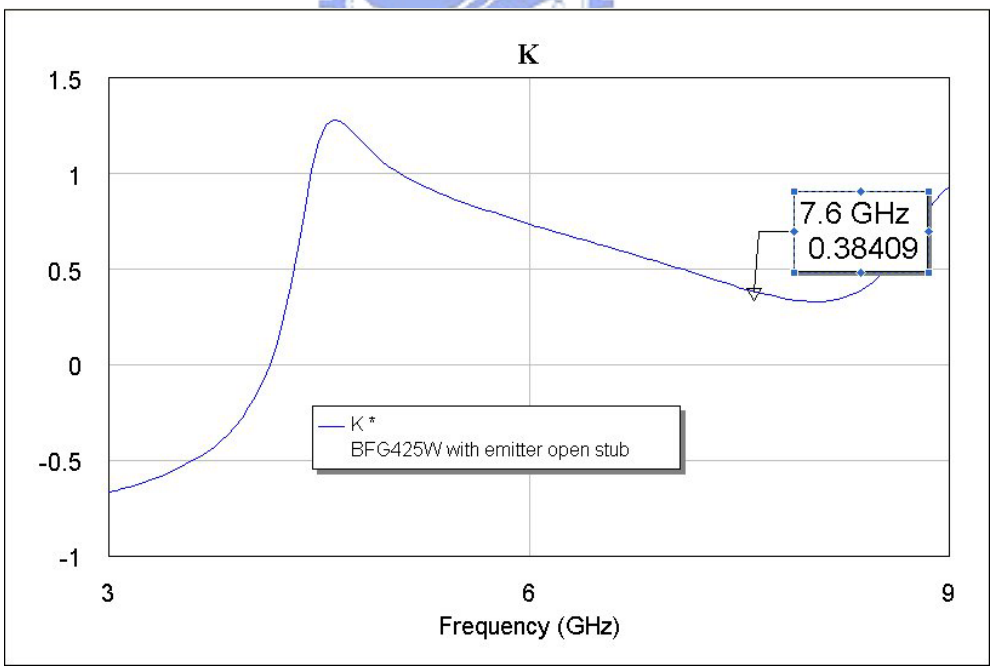

Fig 3-3 Philips NPN transistor BFG425W with Emitter open stub K factor

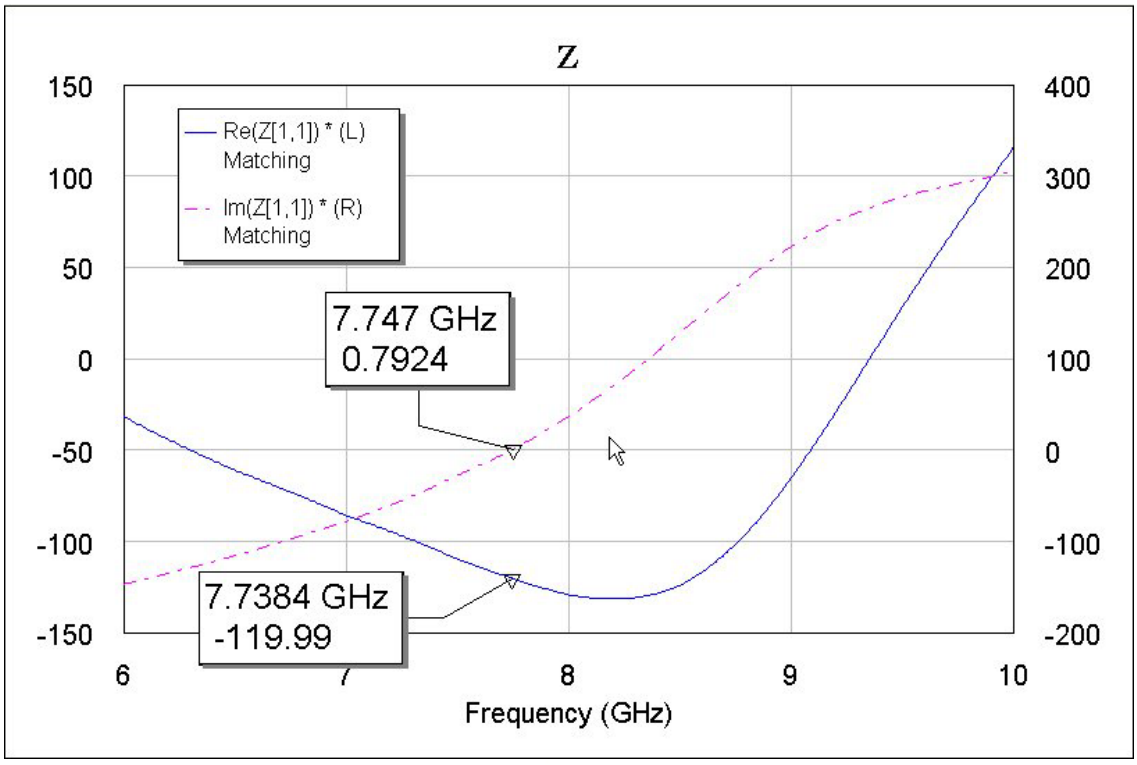

Fig 3-4 7.37~8.07 GHz VCO negative resistance simulation result

Fig. 3-5 shows the VCO circuit schematic. The VCO's tuning voltage vs. frequency test data can be seen in Fig. 3-6 and Table 3-1. The sensitivity is flat enough for PLO to operate between a wide bandwidth with a similar loop bandwidth.

Fig 3-7 shows the VCO output spectrum. Fig. 3-8 is the output phase noise performance at 7.6 GHz, the phase noise value is –103.7dBc/Hz at offset carrier 100 KHz.

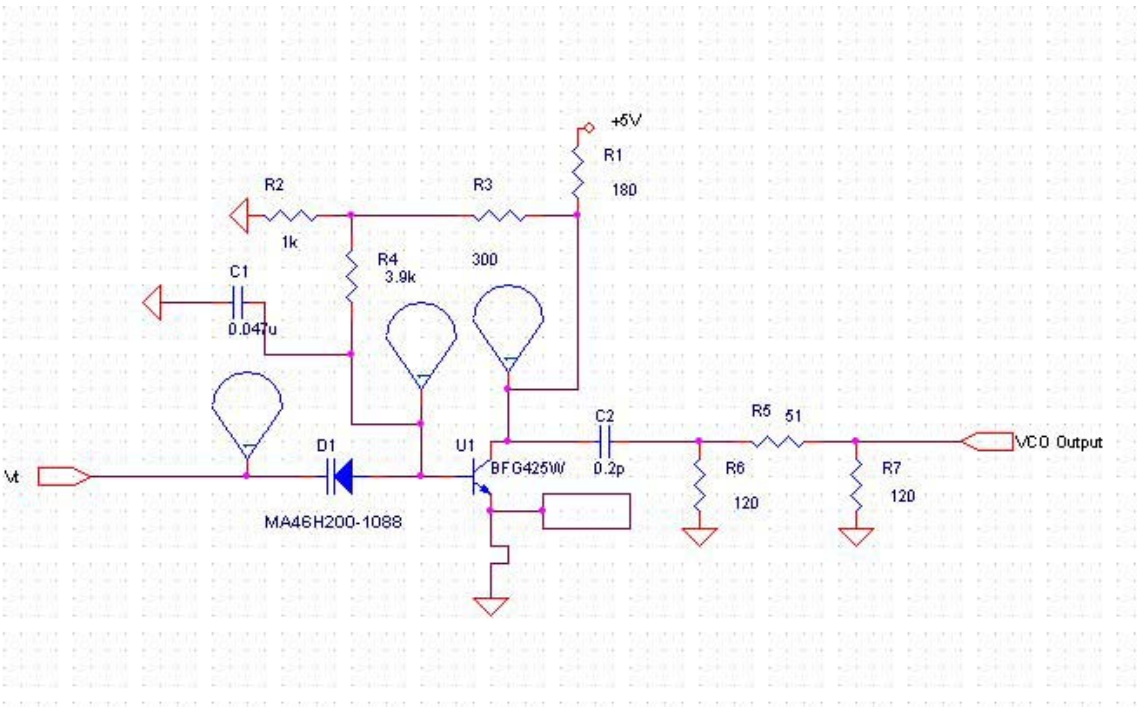

Fig 3-5 7.37~8.07 GHz VCO circuit schematic

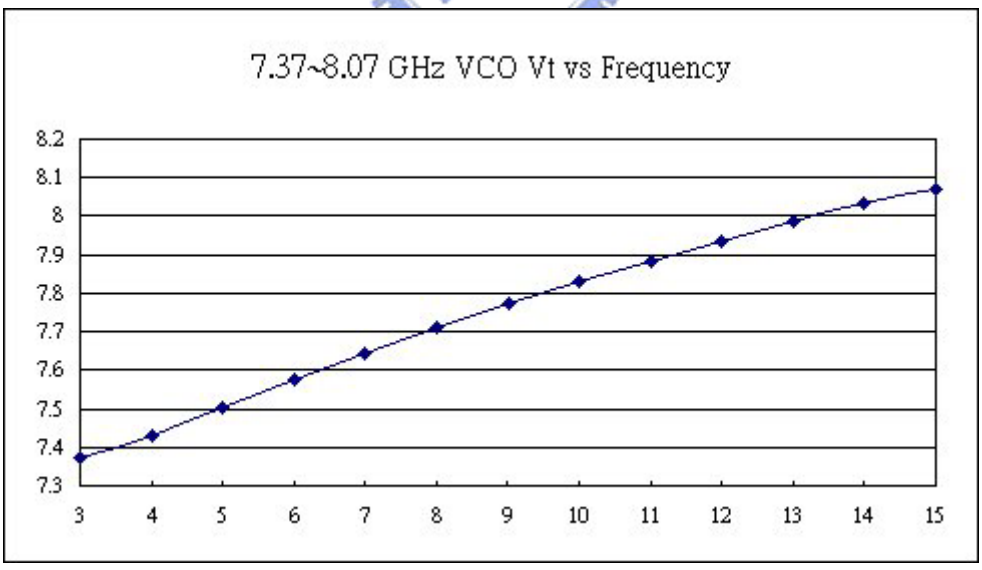

Fig 3-6 7.37~8.07 GHz VCO Tuning Voltage vs. Frequency Curve

V_T(Volts)	Frequency(GHz)	Sensitivity(MHz/V)
3	7.3721	-
4	7.4291	57
5	7.5038	74.7
6	7.5781	74.3
7	7.645	66.9
8	7.7106	65.6
9	7.773	62.4
10	7.8286	55.6
11	7.881	52.4
12	7.9346	53.6
13	7.9865	51.9
14	8.0331	46.6
15	8.0703	37.2

Table 3-1 7.37~8.07 GHz VCO Test results

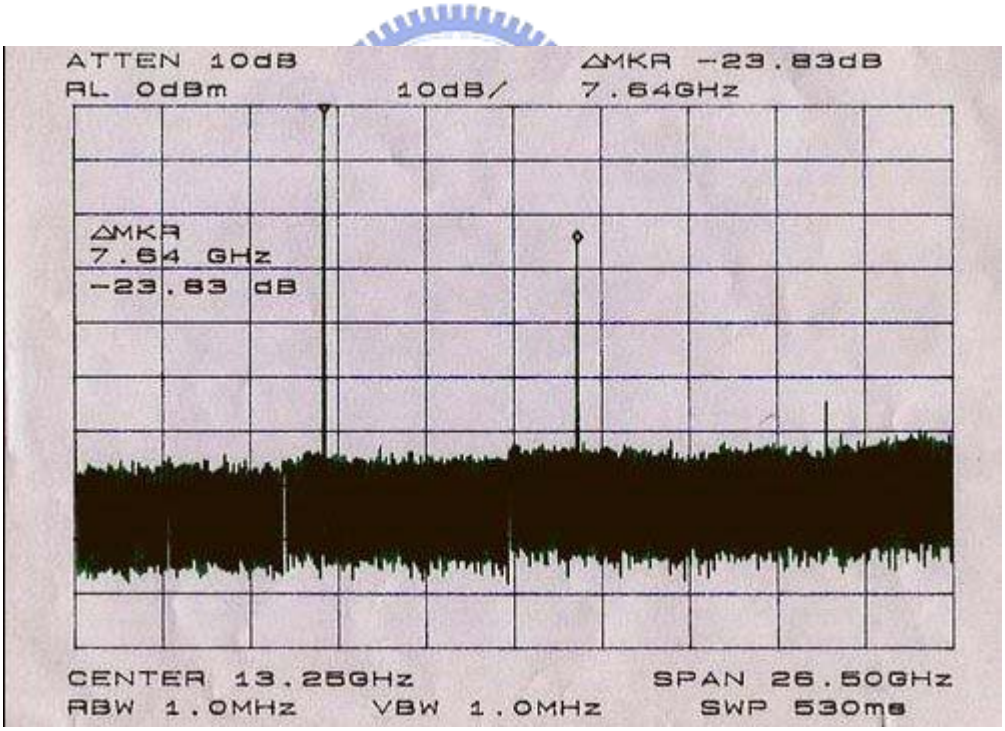

Fig 3-7 7.6 GHz VCO output spectrum

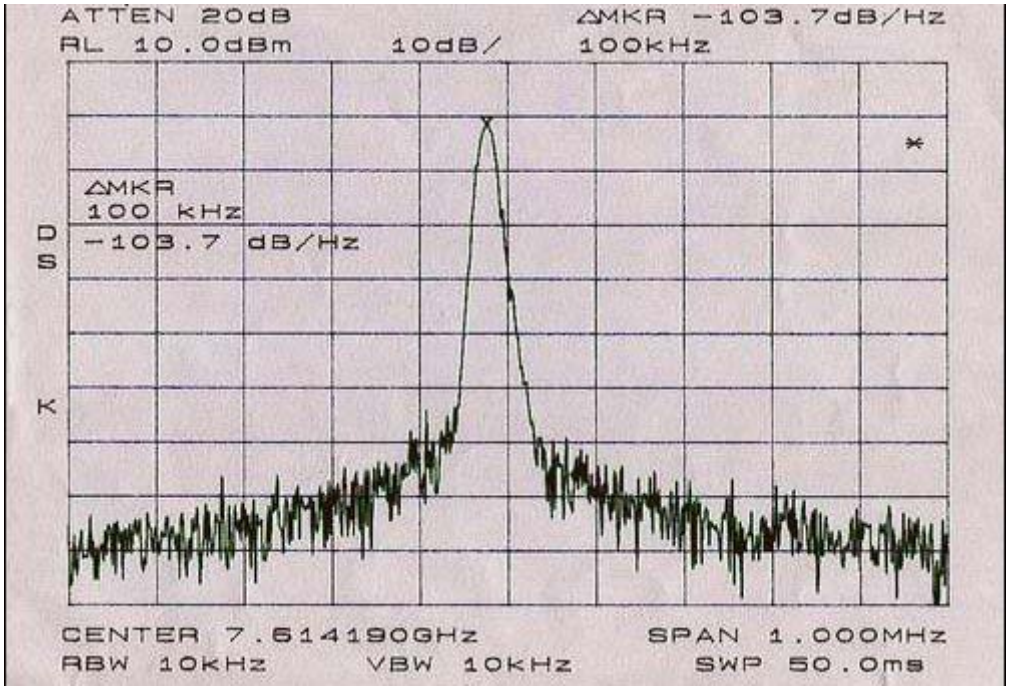

Fig 3-8 7.6 GHz VCO's output phase noise

3.3 General architecture of phase-locked oscillator

In practical microwave transceiver design, local oscillator is one of the critical parts in whole system. There are many structures to design a local oscillator. First, a general direct division structure was used to design a 7.6 GHz phase-locked oscillator (PLO). Fig. 3-9 is the general architecture of the PLO [12].

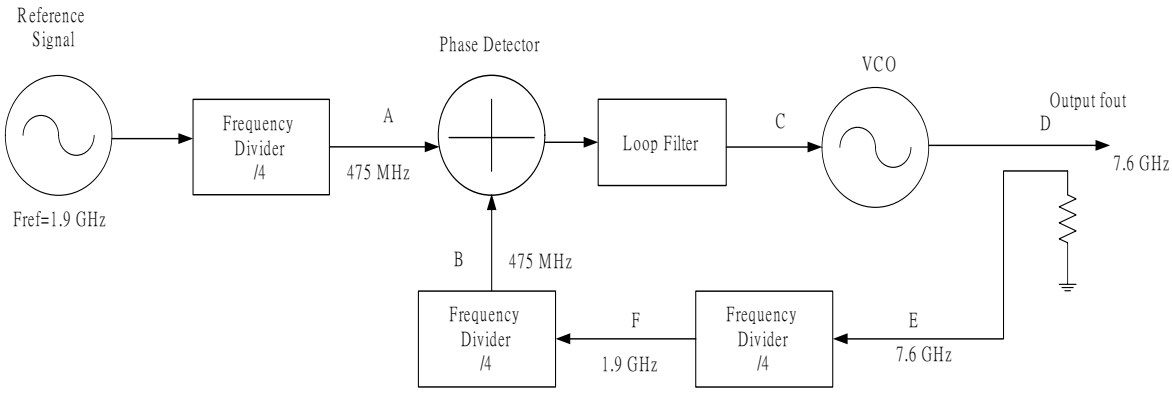

Fig 3-9 Typical Structure of 7.6 GHz Phase-Locked Oscillator

The PLO works at 7.6 GHz. A high frequency reference is chosen to minimize the phase noise degradation by high multiplication factor. All components are realized using commercial available, low cost devices. The components are built discretely for measuring phase noise and replacing component easily.

In practical application, the purpose of design a wider loop bandwidth is to gain the lower phase noise inside the loop bandwidth. In this study, the loop bandwidth is designed about 300 KHz [13], and all the measurements are focused on the phase noise value at offset carrier frequency 100 KHz.

The equipment Agilent 83732B is used as reference signal. Its phase noise performance is shown in Fig. 3-10. In the measurement data, Agilent 83732B phase noise at offset carrier f_0=1.9 GHz 100 KHz is -118.67dBc/Hz. The phase noise at output is only determined by the basic PLL phase detector and frequency divider.

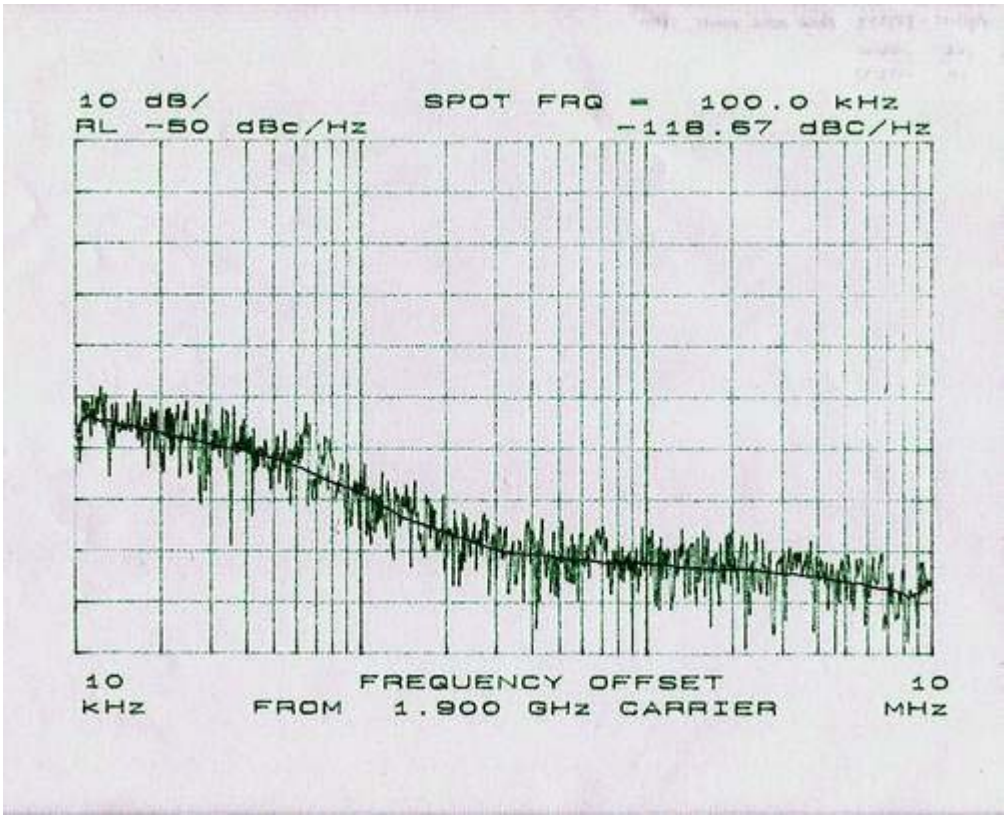

Fig 3-10 Agilent 83732B Phase noise measurement data f_0=1.9GHz

The output frequency is reference frequency multiply by 4. So the phase

noise will degrade 12dB from the phase noise at point F. In the ideal situation, we suppose that phase detector, frequency divider don't degrade the phase noise performance. The phase noise at the point F will be the same value as the reference inside the loop bandwidth. The output phase noise at the point D can be calculated as -106.63dBc/Hz.

But in fact, the phase detector and frequency divider will have some phase noise degradation. Fig. 3-11 is the phase noise measurement data at the point F.

It can be seen that the phase noise at the point F is -115.17dBc/Hz. The phase noise at the point D can be calculated as -103.13dBc/Hz. Fig. 3-12 shows the measurement data of phase noise at the point E. It is close to the calculated value.

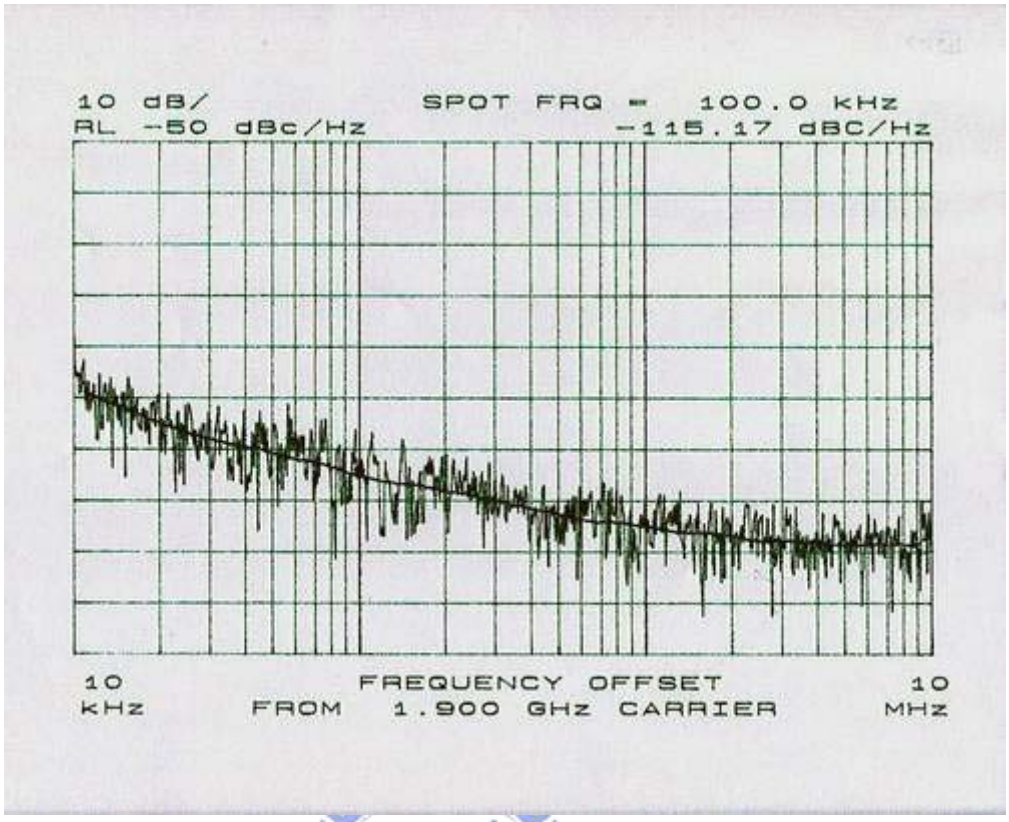

Fig 3-11 Phase noise @ Point F of Fig.3-9 ($f_0 = 1.9\,GHz$)

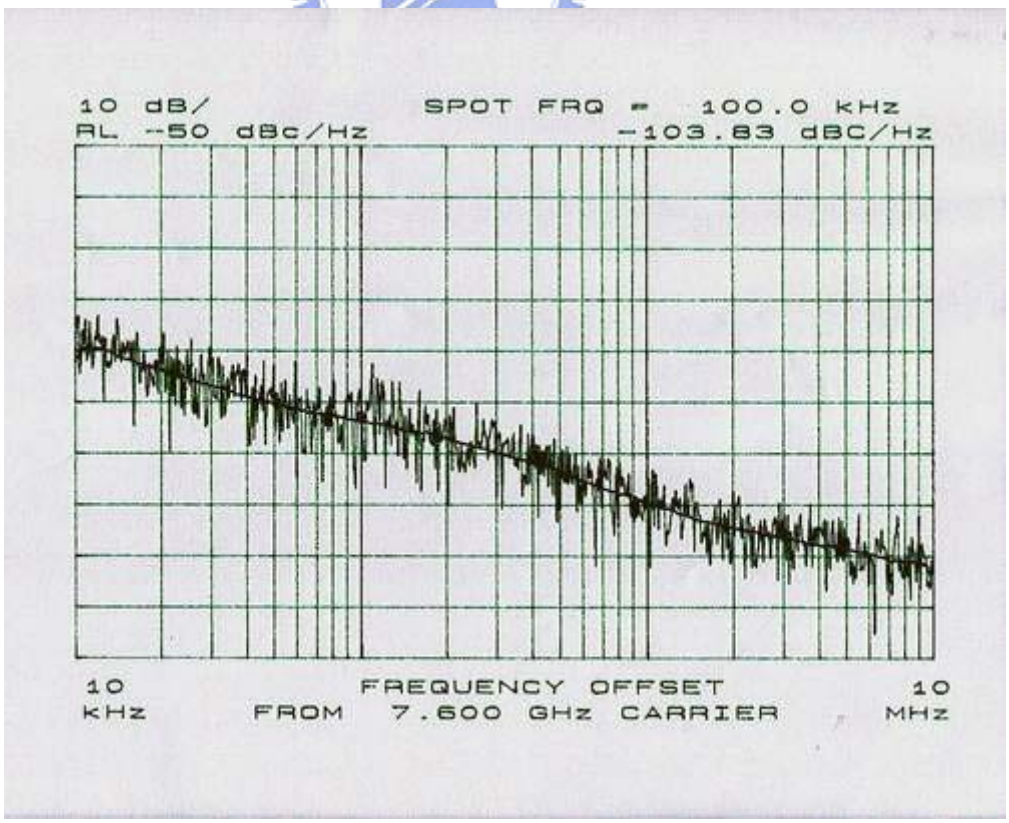

Fig 3-12 Phase noise @ Point D 0f Fig. 3-9 ($f_0 = 7.6\,GHz$)

From results in above analysis and test results, the phase noise performance uses this type of architecture determined by the total multiplication factor from the reference frequency to the output frequency.

Base on this result, I will introduce a different structure for phase noise improvement in the below chapter.

Chapter 4 Architecture to improve phase noise

4.1 Using mixer to replace frequency divider

In the discussion of previous chapter, the output phase noise of PLO is depended on total division ratio of f_{out} to f_{in}. So, in the previous architecture, the higher divide ratio, the worse phase noise. In this chapter, I will introduce a different architecture [15]. This architecture can improve phase noise performance.

Fig. 4-1 shows the architecture that will be introduced in this chapter.

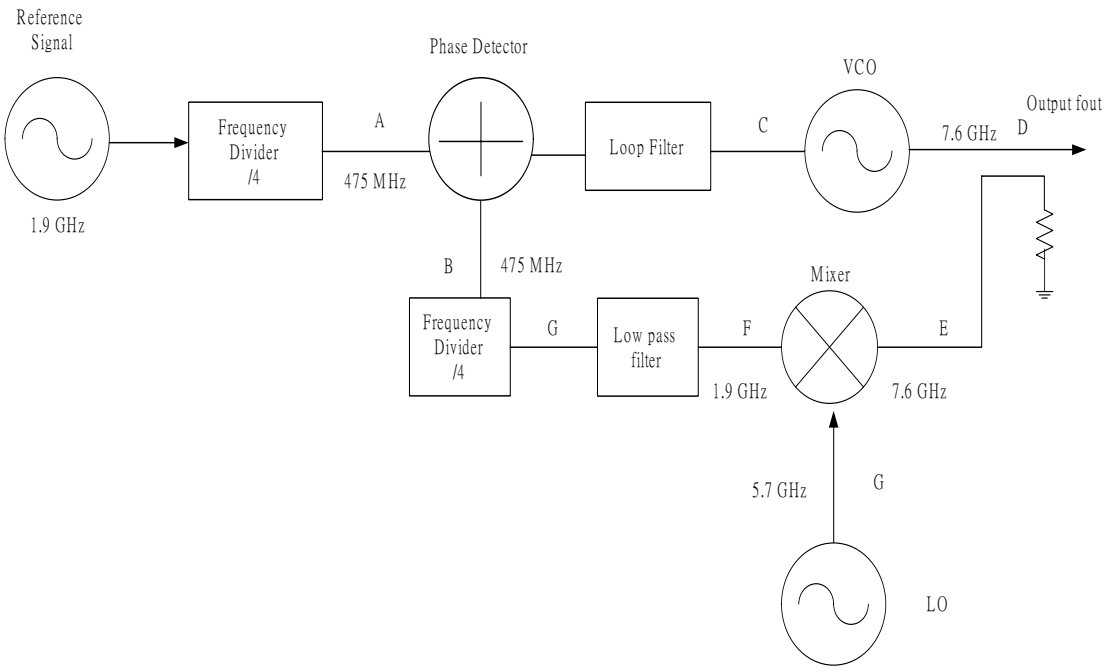

Fig 4-1 PLO use mixer to replace frequency divider

From Eq. 2-20, if the phase noise at the local port is lower enough than the phase noise at the input port, the output phase noise will be similar to the input. Base on this concept, we use a mixer [13] to replace frequency divider. The mixer's LO use a signal with frequency equal to 3* f_{ref} (f_{LO} =5.7 GHz). When PLO is locked, the frequency at mixer output will equal to the f_{ref} (1.9GHz).

In the Fig. 4-1, if the phase noise of the mixer's LO is good enough, the phase noise at point E will similar to the phase noise at point F when PLO is locked. Compare to the architecture of Fig. 3-9, this architecture will decrease the division ratio and will improve phase noise performance.

4.2 Practical experiments

In this section, the PLO which frequency is 7.6 GHz is realized using the architecture of Fig. 4-1. The purpose is to compare the phase noise performance between the architectures in Fig. 3-9 and Fig. 4-1. Equipment Agilent 83732B is used as the reference signal the same as in previous chapter. The reference signal's frequency is 1.9GHz and its performance is shown in Fig.3-10.

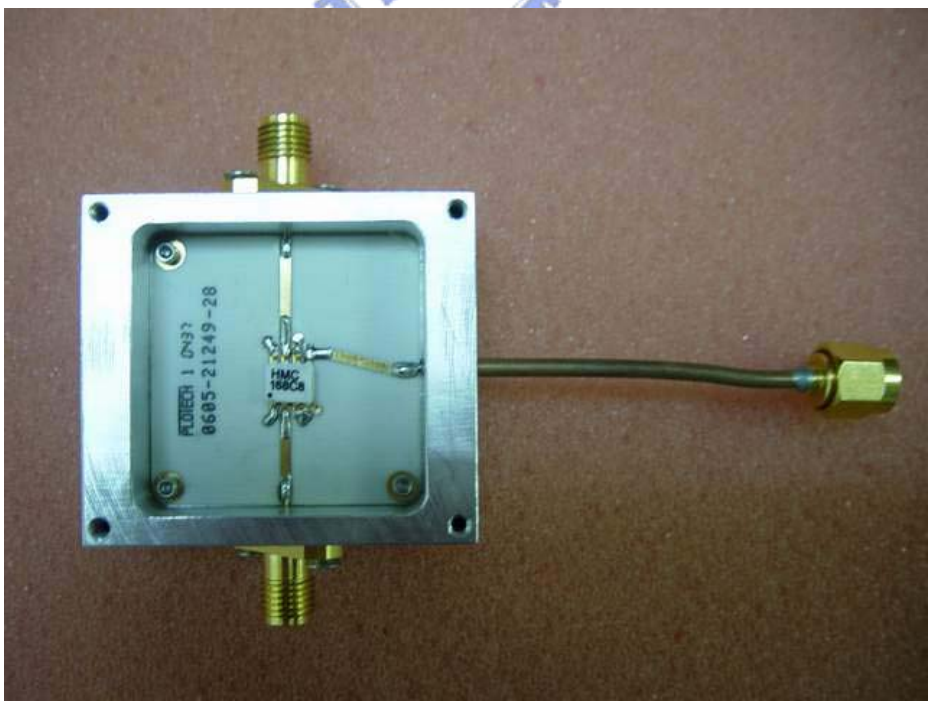

Fig. 4-2 GaAs MMIC SMT Double-balance mixer 4.5-8 GHz (Hittite Microwave corporation)

MMIC mixer HMC168C8 (Fig 4-2) is used in this architecture[16]. The mixer's LO will use two kind of equipments, which have different phase noise performance to compare the LO effect in this structure. Fig. 4-3 is the photo of practical PLO.

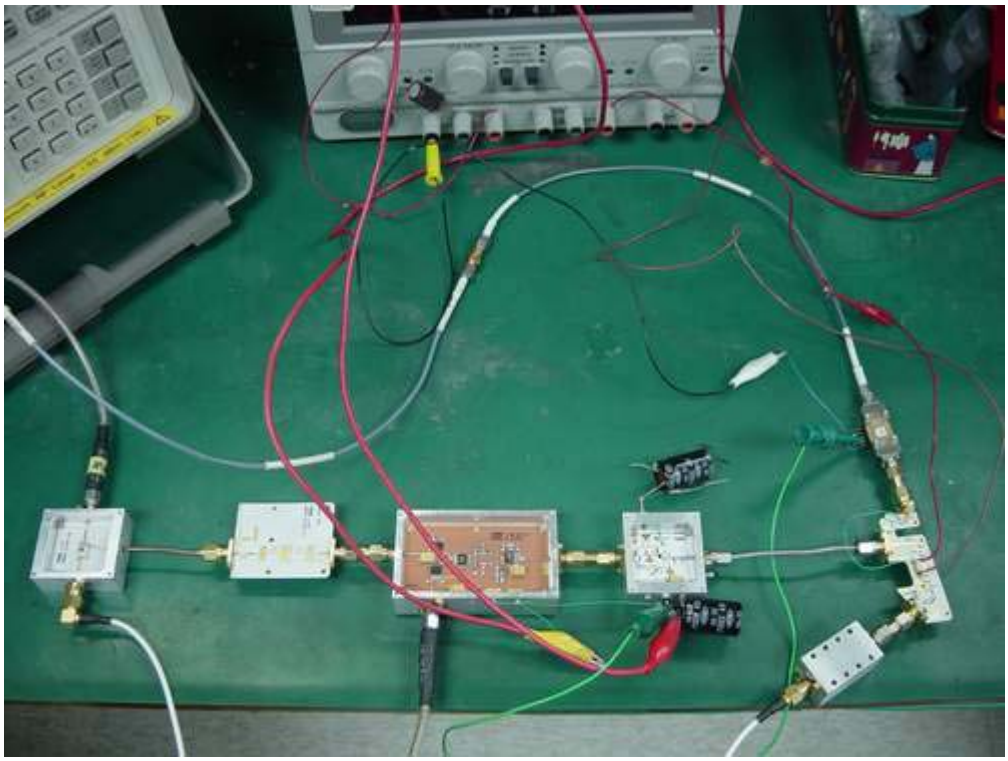

Fig.4-3 Photo of the PLO

Fig.4-4 Agilent signal generator and synthesizer sweeper

4.2.1. Mixer's LO use Agilent 83640B

First, Agilent 83640B is used as the LO signal to analyze 7.6 GHz PLO phase noise performance. Fig. 4-5 shows the Agilent 83640B phase noise performance @. $f_0 = 5.7GHz$. The phase noise value is -116dBc/Hz.

In this article, the phase noise performance inside the loop bandwidth is observed. All the phase noise test data are at offset carrier frequency 100 KHz. It can be roughly estimate the loop bandwidth by seeing the phase noise shape in spectrum analyzer. Fig. 4-6 shows the output signal of 7.6 GHz PLO, its loop bandwidth is about 330 KHz.

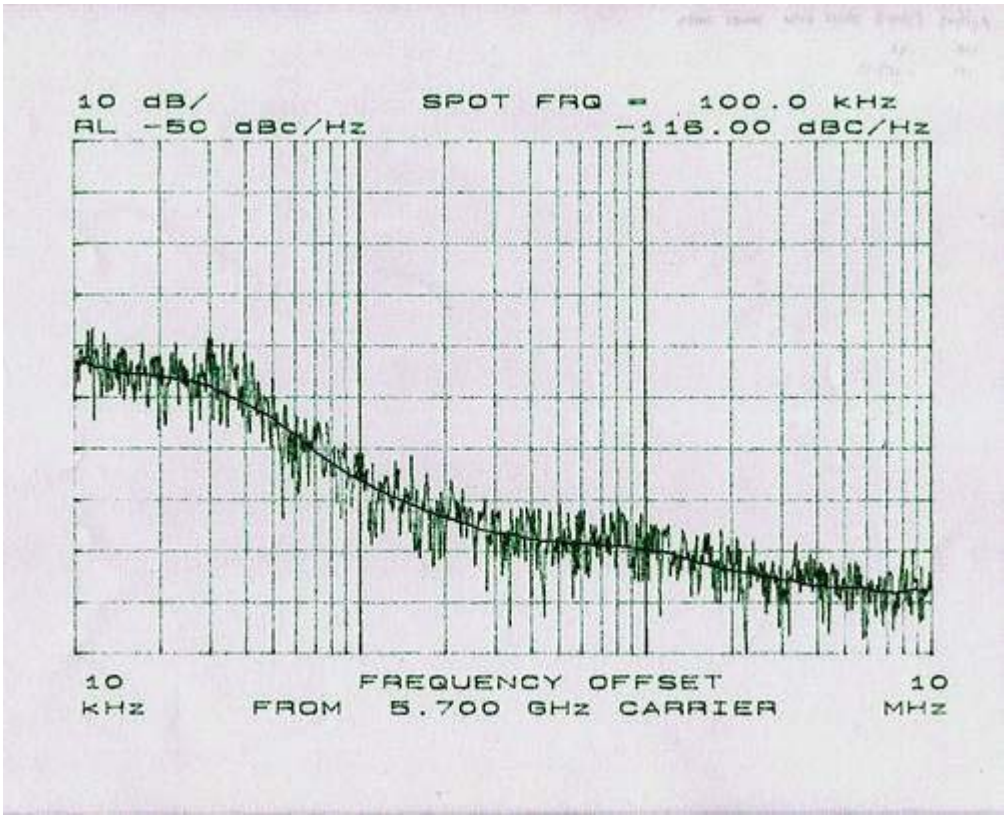

Fig.4-5 Agilent 83640B Phase noise measurement data f_0=5.7GHz

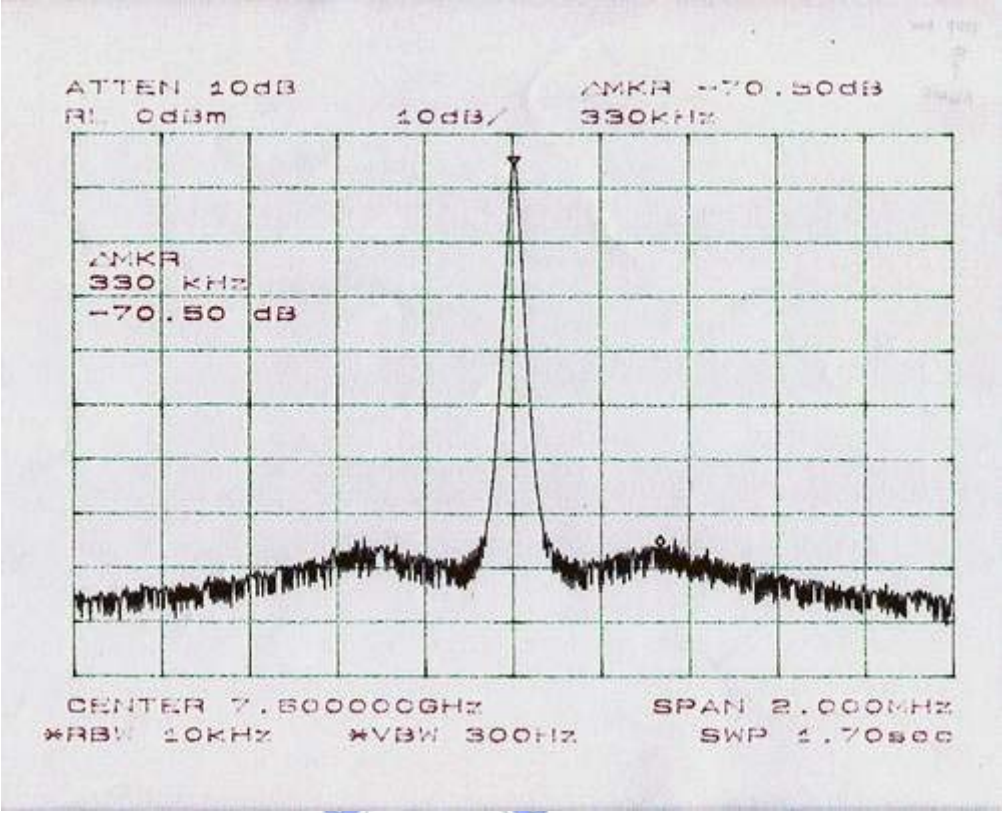

Fig. 4-6 Loop Bandwidth (Mixer LO use Agilent 83640B)

The measure result of the phase noise at point F of Fig. 4-1 is showed on Fig.4-7. The phase noise value is -114.5dBc/Hz. It's a little worse than the reference signal's phase noise -118.67dBc/Hz. But It's similar to the phase noise that use general architecture (-115.17dBc/Hz) at point F.

Fig.4-8 shows the PLO output phase noise at offset carrier 100KHz. The value is -112.67 dBc/Hz.

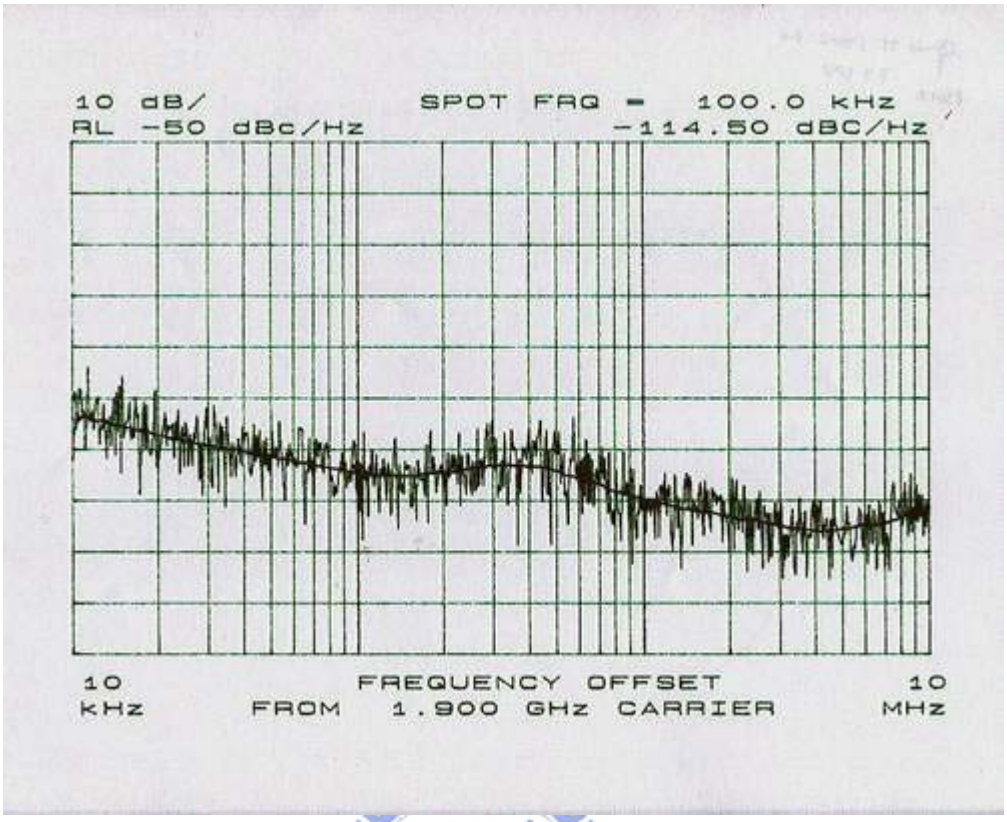

Fig. 4-7 Phase noise @ Point F of Fig. 4-1

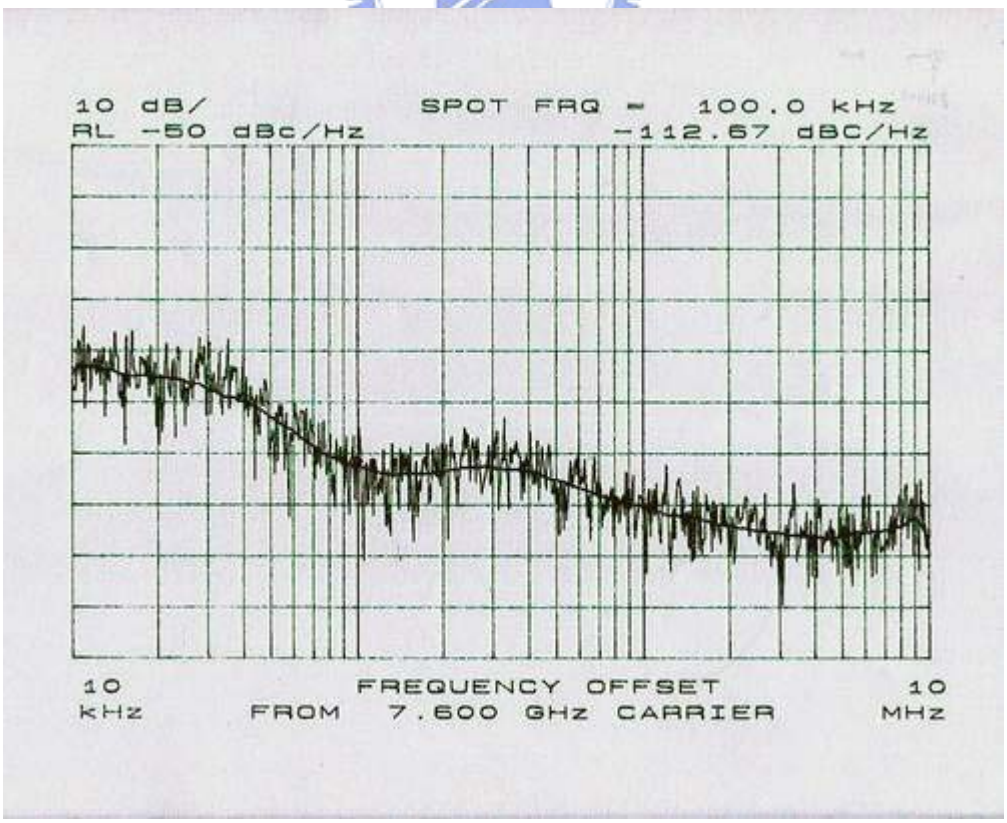

Fig4-8 Phase noise @ Point D 0f Fig. 4-1 ($f_0 = 7.6\,GHz$) (mixer LO use Agilent 83640B)

4.2.2. Mixer's LO use Agilent 83752B

In this section, the only different with 4.2.1 is the mixer LO. Agilent 83752B is used as the LO signal to analyze 7.6 GHz PLO phase noise performance again. Fig. 4-9 shows the Agilent 83640B phase noise performance @. $f_0 = 5.7GHz$. The phase noise value is -106.67dBc/Hz. It is 9.33dB worse than Agilent 83640B.

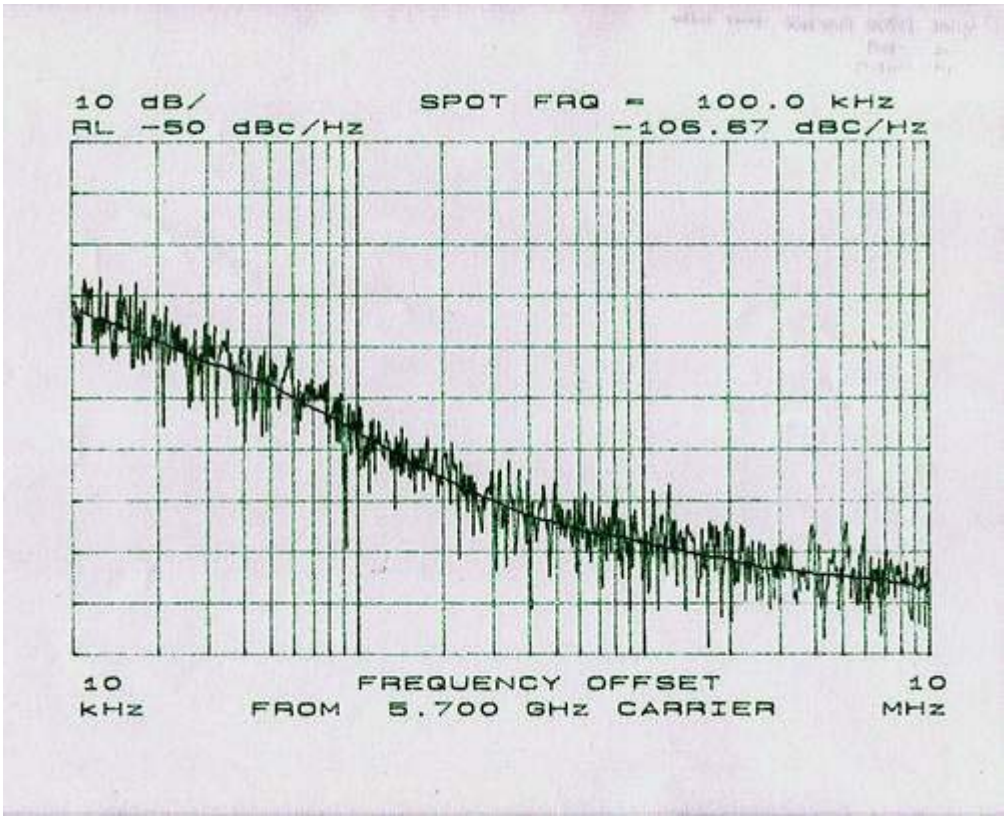

Fig 4-9 Agilent 83752B Phase noise measurement data f_0=5.7GHz

Fig. 4-10 shows the output signal of 7.6 GHz PLO, its loop bandwidth is about 330 KHz.

The measure result of the phase noise at point F of Fig. 4-1 is showed in

Fig.4-11. The phase noise value is -114.33dBc/Hz. It's similar with mixer LO use Agilent 83640B.

Fig.4-12 is PLO output phase noise at offset carrier 100KHz. The value is -105.83 dBc/Hz. The phase noise value is 6.84dB worse than mixer LO uses Agilent 83640B. But It's still 2dB better than the structure that use divider.

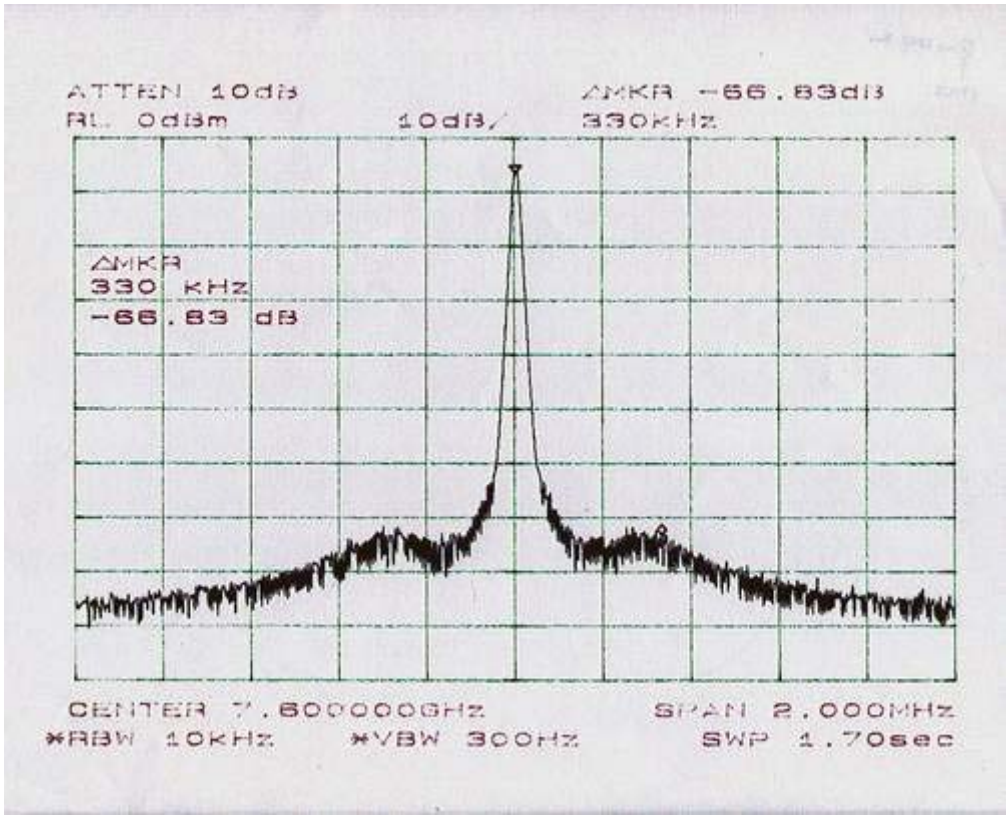

Fig 4-10 Loop Bandwidth (Mixer LO use Agilent 83752B)

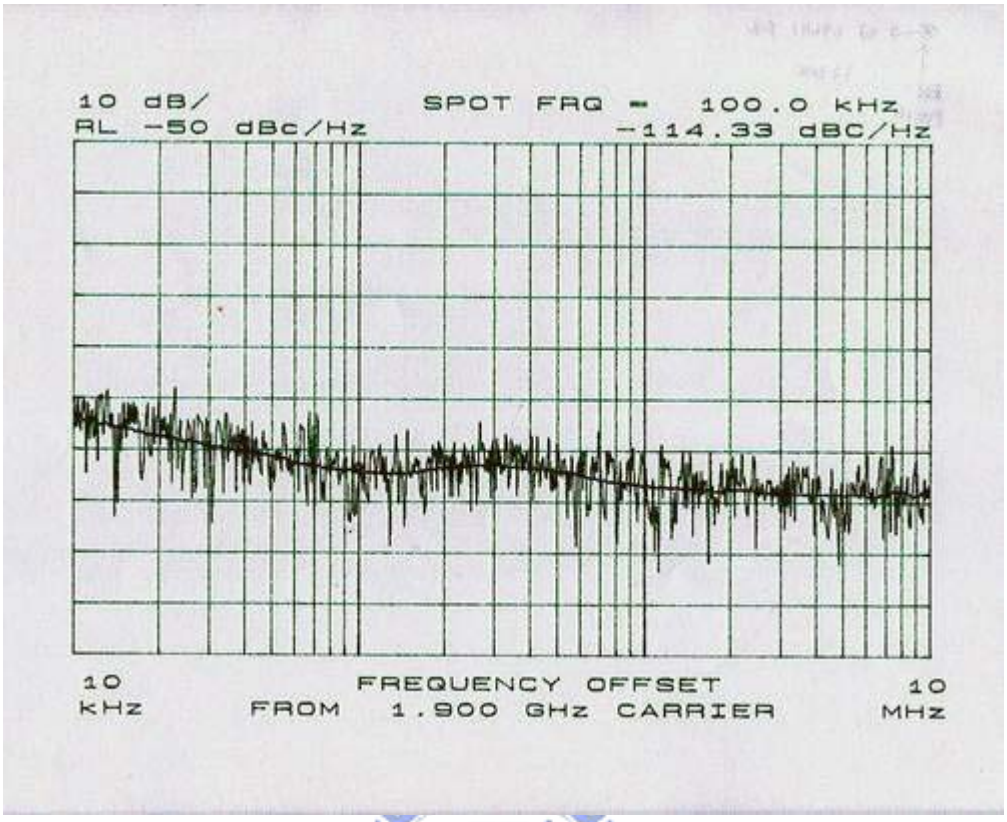

Fig.4-11 Phase noise @ Point F of Fig. 4-1

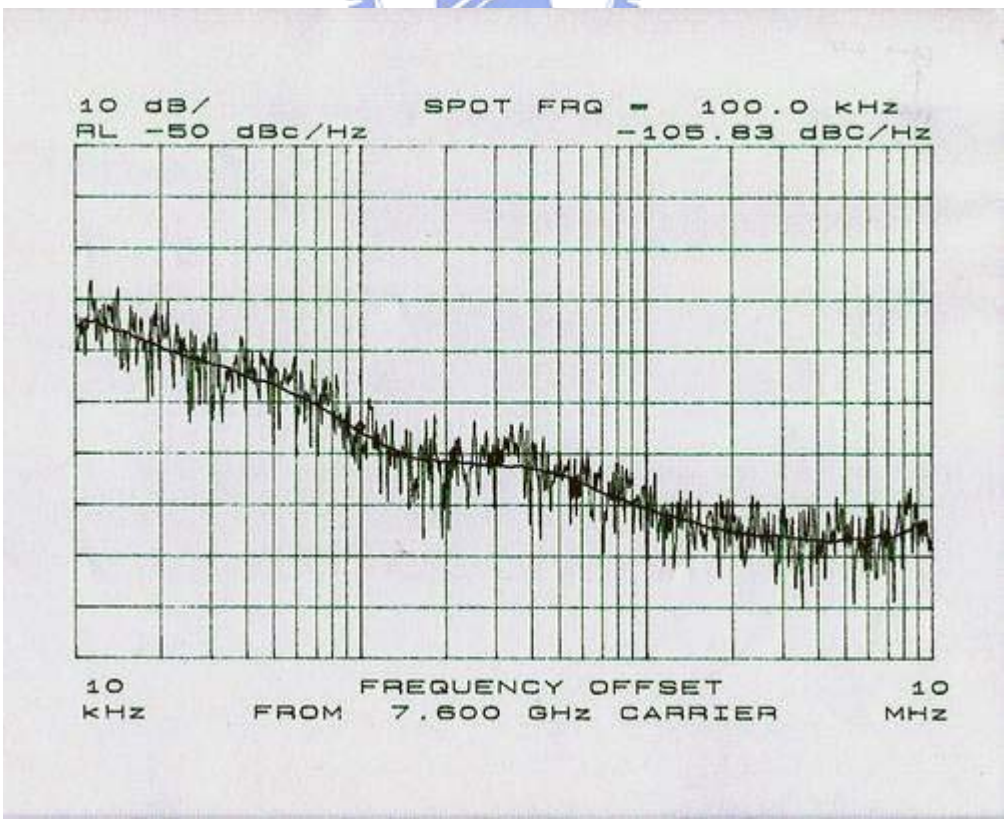

Fig.4-12 Phase noise @ Point D 0f Fig. 4-1 ($f_0 = 7.6\,GHz$) (mixer LO use Agilent 83752B)

4.4. Frequency multiplier

Generally, in a multiplier the reverse result of that found in a frequency divider is encountered: the sideband noise and spurious response are increased by the multiplication.[6] For example, when a signal input to a multiplier ($f_{out} = N \times f_{in}$), the phase noise at multiplier's output will degrade by $20 * \log N$.

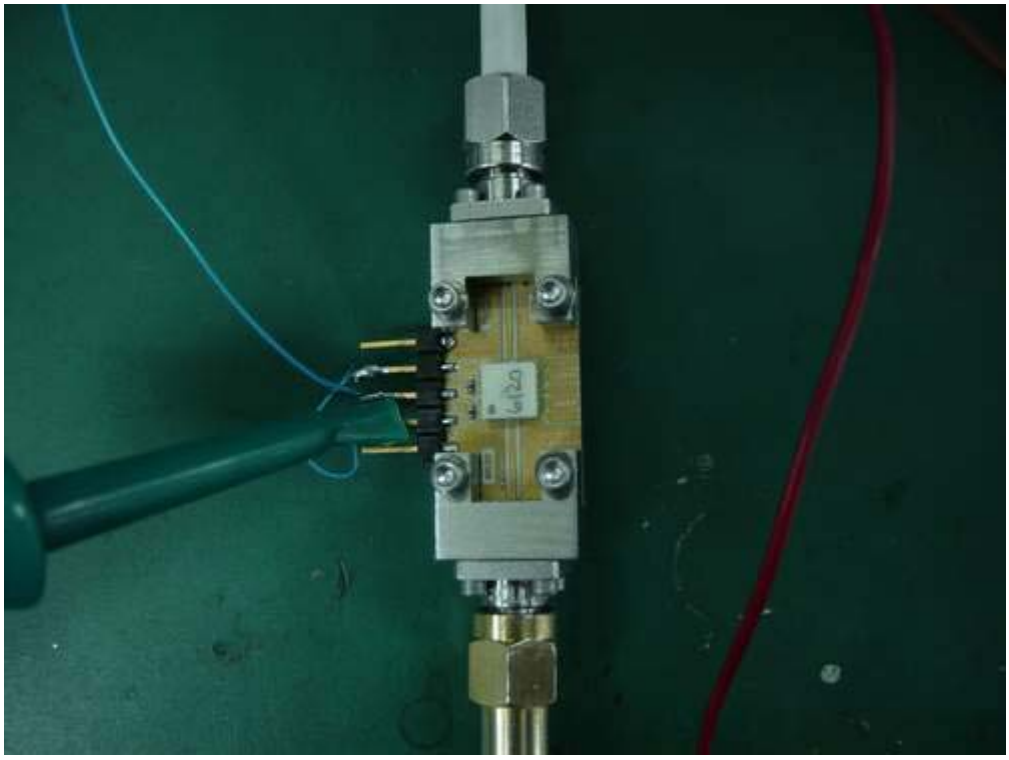

Fig 4-13 Agilent Frequency Doubler AMMC-6120

Fig. 4-13 shows the Agilent frequency doubler. The device is connected at the output of 7.6 GHz PLO. The output frequency of the doubler will be 15.2GHz.

Fig. 4-14 and Fig.4-15 show the phase noise test results at the output of

the frequency doubler. Fig. 4-14 show the phase noise is -106.33dBc/Hz at offset carrier(15.2GHz) 100KHz. Compare to the phase noise value at the input of frequency doubler(Fig.4-8,-112.67dBc/Hz), the degradation is 6dB. The same situation, the value difference between Fig.4-15 and Fig.4-12 is about 6dB.

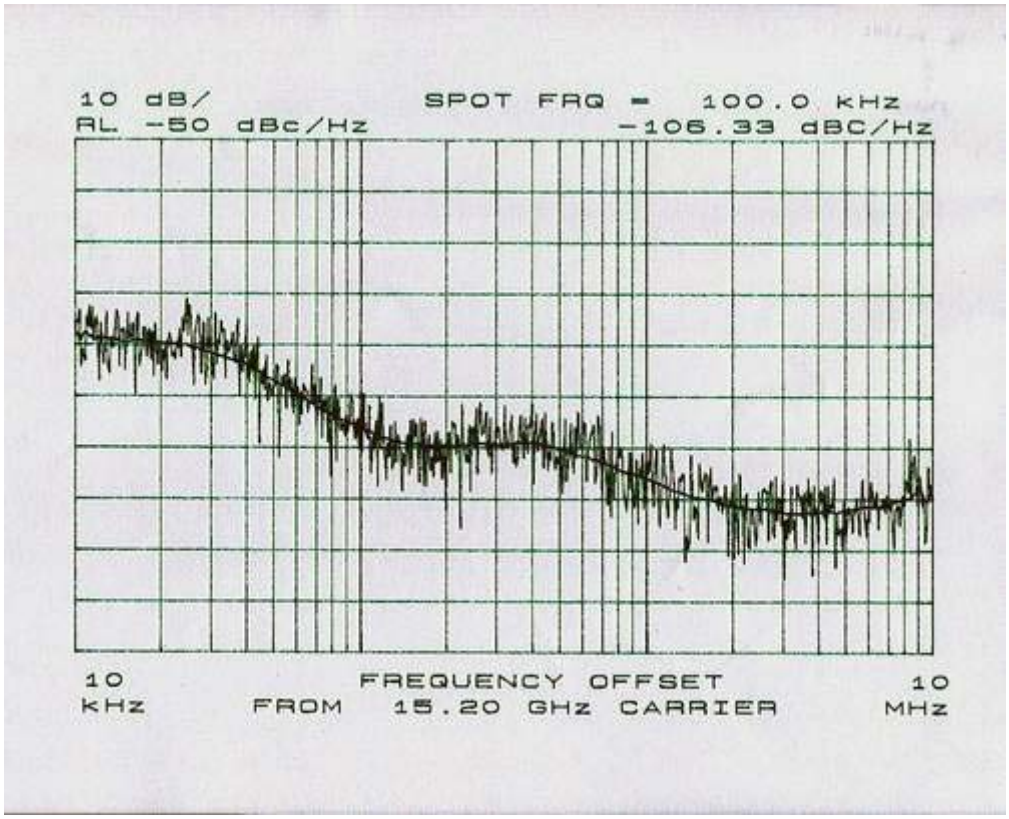

Fig 4-14 Phase noise of 15.2GHz (mixer LO use Agilent 83640B)

These results meet our expectation. The phase noise will be degraded 6dB when we use a frequency doubler at the LO path.

Fig.4-16 shows the output spectrum of the frequency output.

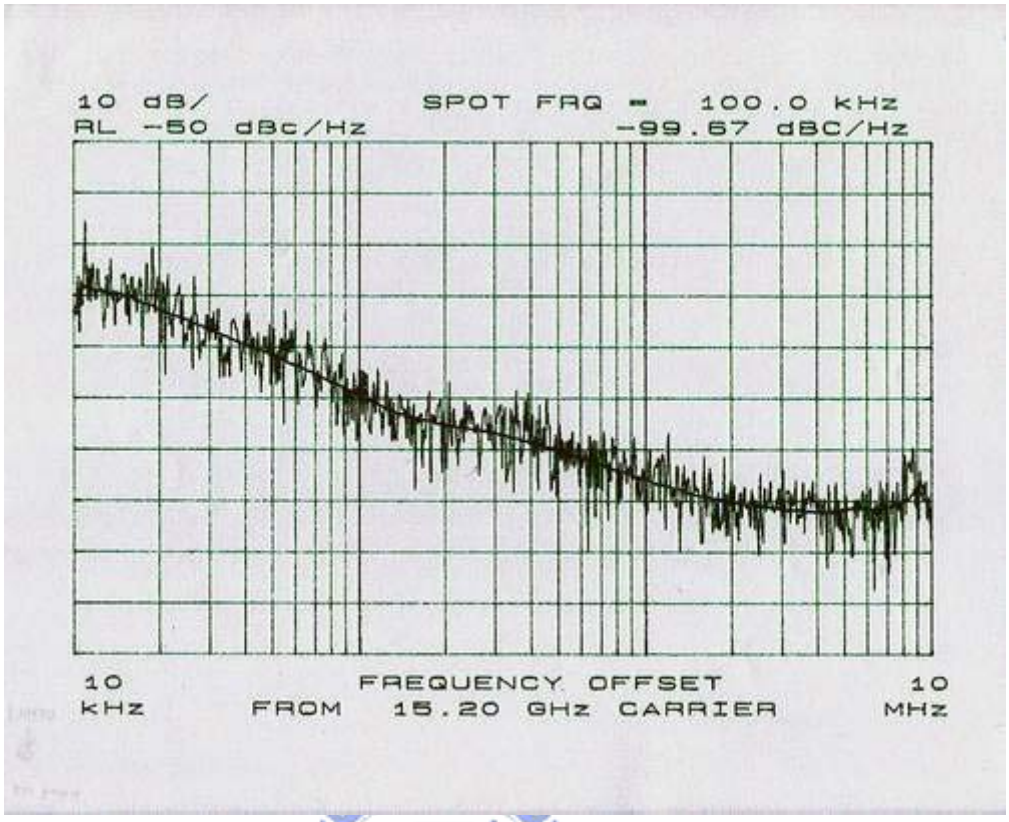

Fig 4-15 Phase noise of 15.2GHz (mixer LO use Agilent 83752B)

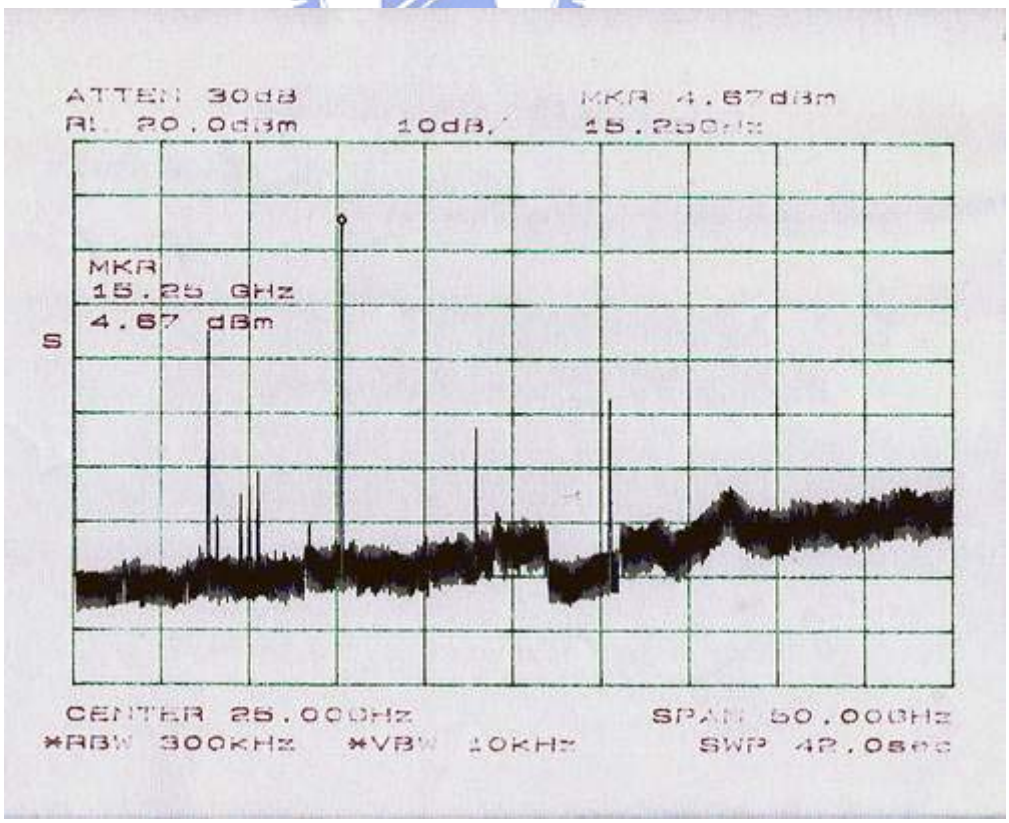

Fig 4-16 Frequency doubler spectrum

Chapter 5 Conclusion and Future study

The phase locked oscillator with mixer to improve phase noise performance has been developed and measured. The direct division structure has also been designed and the phase noise performance has been measured. From what has been discussed above, we can reasonable to conclude that use mixer to replace frequency divider in PLO can improve the output phase noise performance.

In this thesis, the frequency of mixer's local oscillator's was chosen $3 * f_{REF}$. Two Agilent equipment were selected as mixer's LO. Table 5-1 lists the summary of the output phase noise test results at offset 100 KHz of 7.6 GHz. There was the only one equipment used as reference signal. The phase noise at offset 100 KHz of 1.9 GHz is -118.67dBc/Hz. If the reference signal input a multiplier and the multiplicator is three. The output signal can be used as the LO signal in mixer's PLO structure. It's phase noise will be -109.12dBc/Hz.

It’s better than the Agilent 83752B. The result indicated that we can design a multiplier for this new structure. As direct division structure, we use single loop but different structure to improve the output phase noise.

	PLO Structure		
	Frequency divider	Mixer	Mixer
Reference signal phase noise@1.9GHz	-118.67	-118.67	-118.67
Mixer' LO	-	Agilent 83640B	Agilent 83752B
Phase noise@5.7GHz	-	-116	-106.67
Output Phase noise@7.6GHz	-103.83	-112.67	-105.83

Table 5-1 Summary of 7.6 GHz output phase noise test results

Reference

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