Chapter 2

Power Control and Linear Transmitter Fundamental Theory

2.1 Typical power control architecture

The digital wireless communications standard requires accurate control of a unit`s transmitted power over a wide dynamic range. Accurate power control is required to meet system specifications under operating conditions like supply voltage variation.

Today, The most common solution today is a power-control loop based on a directional coupler with a peak detector and a comparator.

2.1.1 RF attenuator power control architecture

With RF attenuator power control, the attenuator is inserted into two stages (is shown in Figure 2.1) before the power amplifier. Figure.2.2 shows the RF attenuator.

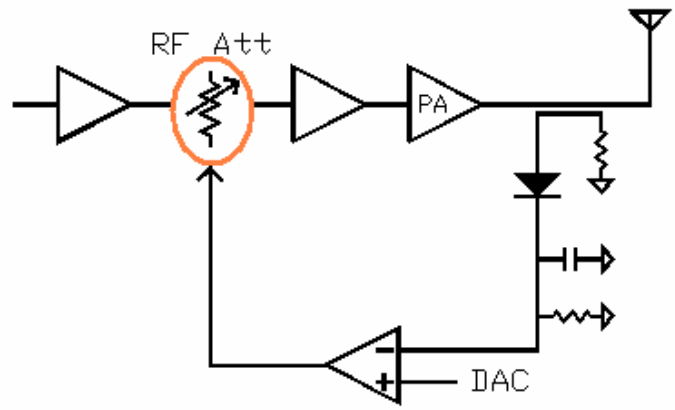


Figure 2.1 RF attenuator power control

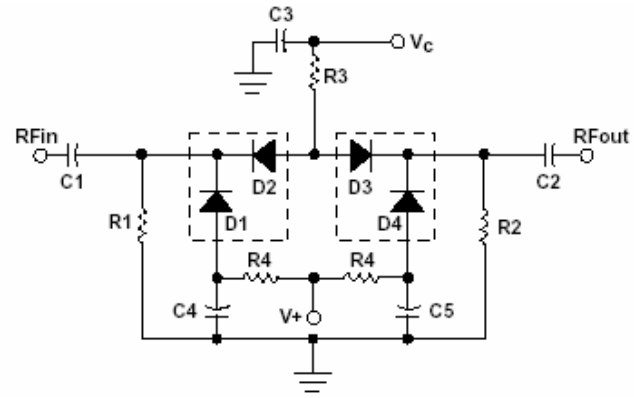


Figure 2.2 A four diode attenuator

This decreasing the RF power into the power transistors, hence reducing the RF output power, as long as the amplifier is not driven into saturation.

The output power in the RF attenuator control is related to the linear attenuation of input power. The fact that there is a simple linear relation between control signal and RF output power provides three disadvantages:

1. It is too small that the dynamic range of the RF attenuator is 20 dB.

2. The diode is saturated when large signal into the pin diode of RF attenuator.

3. The mismatch between the two stages is caused by the reflecting attenuator.

2.1.2 A variable gain of pre-amplifier power control architecture

The amplifier is designed to a variable gain device. Figure2.3 shows the architecture. The different gain control is based on a attenuation relation between the power of the amplifier.

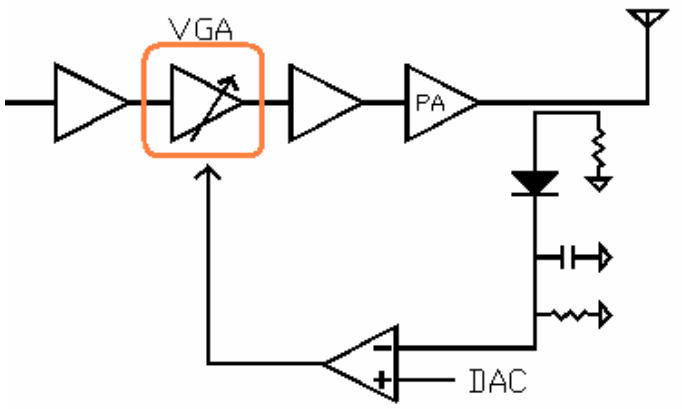


Figure 2.3 Pre-amp variable gain power control

If the output power versus gain characteristic is known for a given amplifier, the output power can accurately set. The advantage of this configuration is the possibility to achieve the wide dynamic range of power control. But there are the following disadvantages to this method:

1. The consideration of the power consumption of the other amplifiers.
2. A linear power amplifier is demand.

2.1.3 A variable gain of output power amplifier power control architecture

The power control architecture of my propose is a variable gain output power amplifier as shown in Figure 2.4. The principle of power controlling is the closed loop approach. Under this approach, the RF output power is sensed via a directional coupler and is detected across a fast Schottky diode. The resulting voltage signal is directly proportional to the RF peak voltage and is compared with a reference voltage in an error amplifier. The loop controls the power amplifier gain via a control line to

force the detected voltage and the reference voltage to be equal. Power control is accomplished by setting the reference voltage. Figure2.5 shows the PA bias circuit.

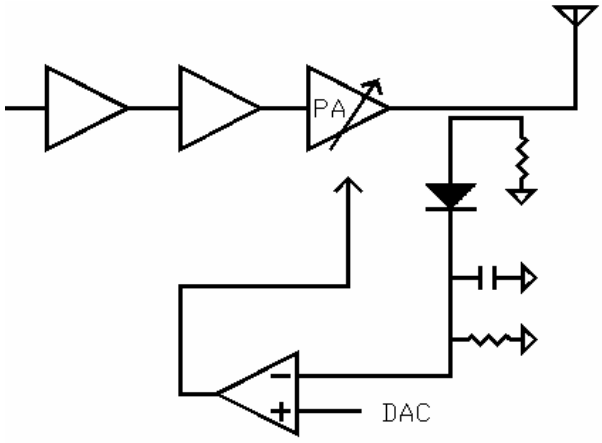


Figure 2.4A variable gain of output power amplifier power control

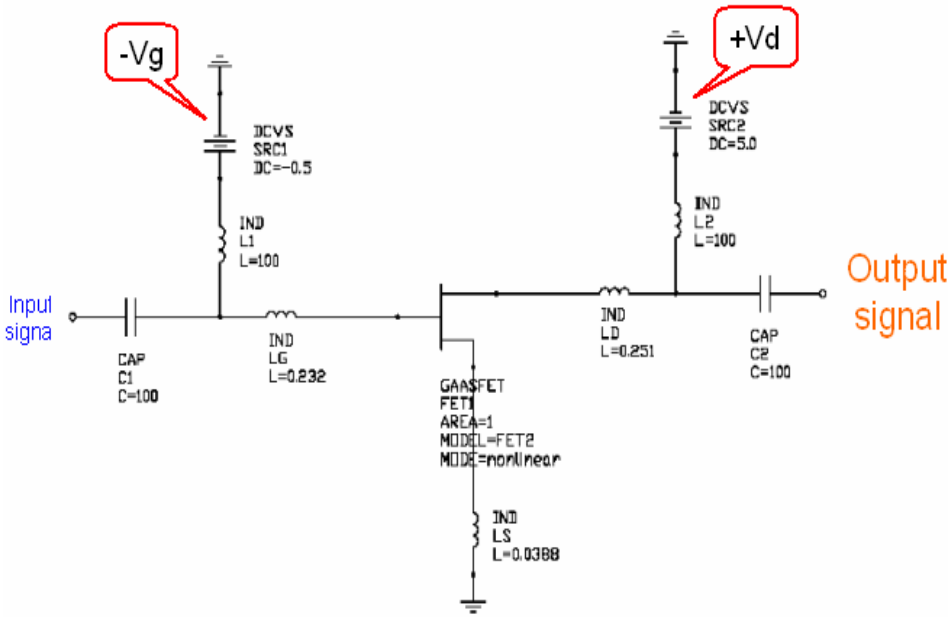


Figure 2.5 PA bias circuit

The advantage of the closed-loop power control method is an excellent behavior under mismatched conditions. This method performs well under mismatch because the directional coupler can distinguish between incident and reflected power. The attenuation of the variable gain amplifier is mach than the RF attenuation. And the input and output signal are separated by the amplifier.

In the linear region, I set the gate DC voltage to control the RF attenuation value from positive gain to the negative gain. A variable gain amplifier is made use to achieve wide power control range.

I control the gate DC voltage of the power amplifier to compensate the movement of bias point when large AC signal input the device. We utilize the different gate bias voltage to change the gain of device to achieve power gain linearizer.

Both the power control and linearizer can be accomplished. Figure 2.6 shows the attenuation v.s. the gate Vg bias. The power gain is decreasing from 10.67 dB to –29.33dB at different Vg bias voltage. Figure 2.7 shows the change of Vg bias depends on the different input power to compensate the non-linear power gain curve. When input –1dBm, the gate voltage should be set –0.725 V. And when input 11 dBm, the gate voltage should be set –0.880 V.

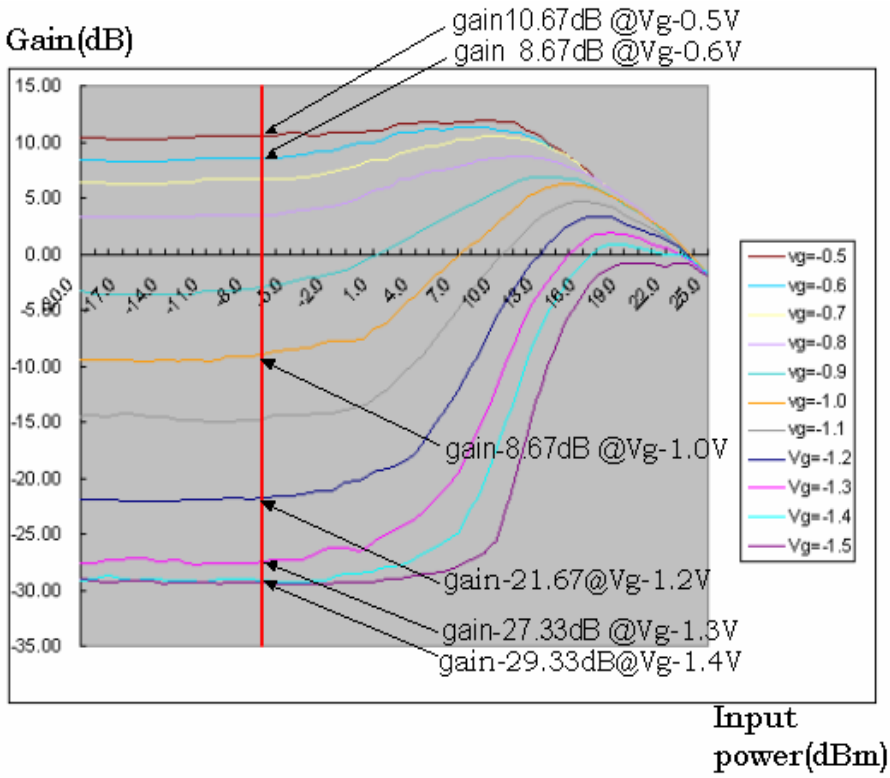


Figure 2.6 Attenuation V.S. gate Vg bias

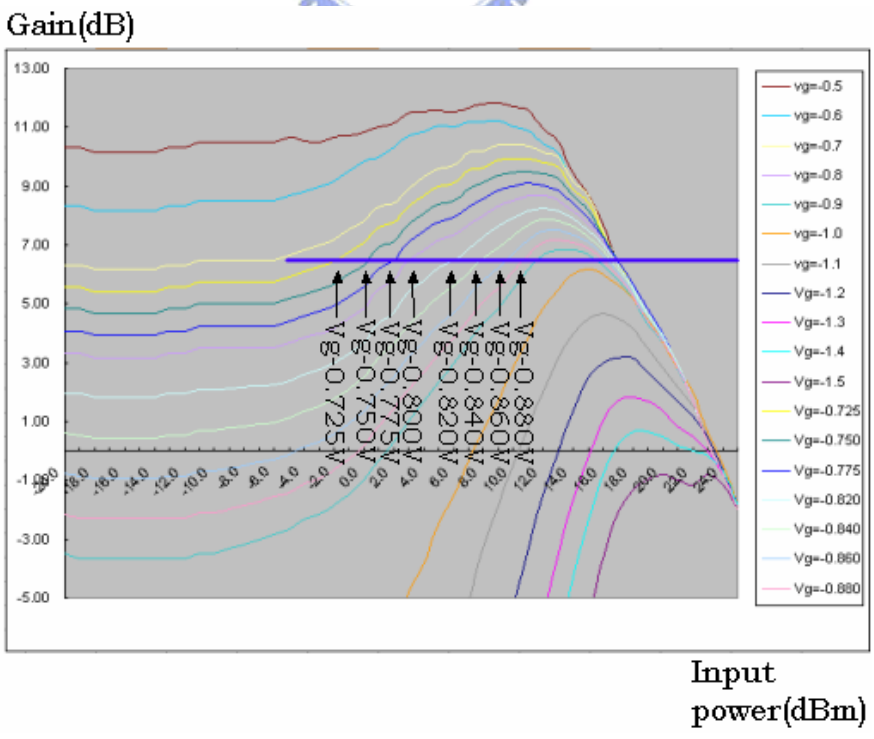


Figure 2.7 Input power V.S. power gain@gate Vg bias

2.2 The linearizer fundamental theory

2.2.1 A Microwave Miniaturized Linearizer Using a Parallel Diode with a Bias Feed Resistance

In this paper [3], a miniaturized linearizer using a parallel diode [4] with a bias feed resistance is proposed and its operation principle is investigated. Figure 2.8. shows a block diagram of the power amplifier with the linearizer. The linearizer achieves positive gain and negative phase deviations with the increase of input power because of a nonlinearity of the diode and movement of bias point caused by a voltage drop at the bias feed resistance. Moreover, the author make it clear that A.M./A.M and A.M./P.M. characteristics of the linearizer can be easily adjusted by controlling the anode supply voltage of the diode. They employ a variable gain amplifier between the linearizer and the power amplifier to control RF input power level of the power amplifier and achieve high isolation.

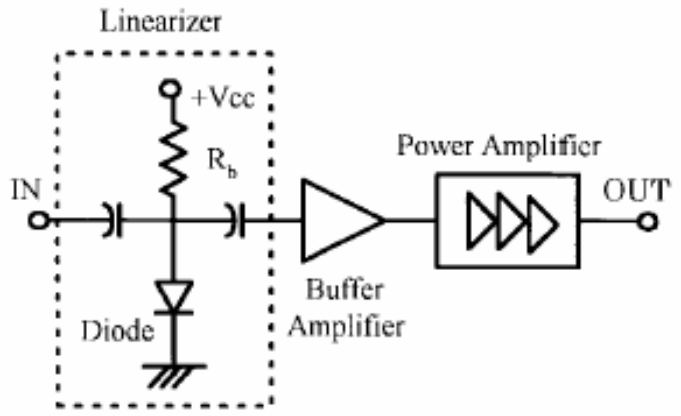


Figure 2.8 Block diagram of the power amplifier with the linearizer

The linearizer described above is used to compensate for the distortion of an S-band power amplifier.

To demonstrate the capability of this linearizer, the characteristics of the amplifier in the following condition.

Condition A: without the linearizer (idle current I_{do} = 1 A);

Condition B: without the linearizer in low current (idle current I_{do} = 0.52 A);

Condition C: with the linearizer in low current (idle current I_{do} = 0.52 A);

The gain and phase deviations of the power amplifier in condition-B become worse than those of the power amplifier in condition-A. We find the amplifier with the linearizer in condition-C achieves the improved A.M/A.M and A.M/P.M characteristics compared with the amplifier in condition-B. Figure2.9 shows the gain and phase deviations.

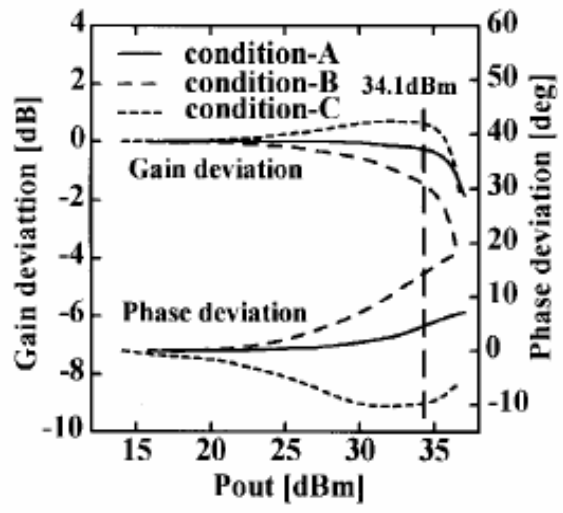


Figure 2.9 Gain and phase deviations of the power amplifier

2.2.2 Linearized High Efficient HBT Power Amplifier Module for L-Band Application

In this paper [5], a new on-chip linearizer that is applicable to L-band application is proposed as shown in Figure 2.10. It is composed of base-emitter diode of the active bias transistor and a capacitor for RF signal shorting to the base node of the active bias transistor [6-7], which improves the gain compression and phase advance of the power amplifier with no additional dc power consumption, and has negligible signal loss with almost no increase in die area.

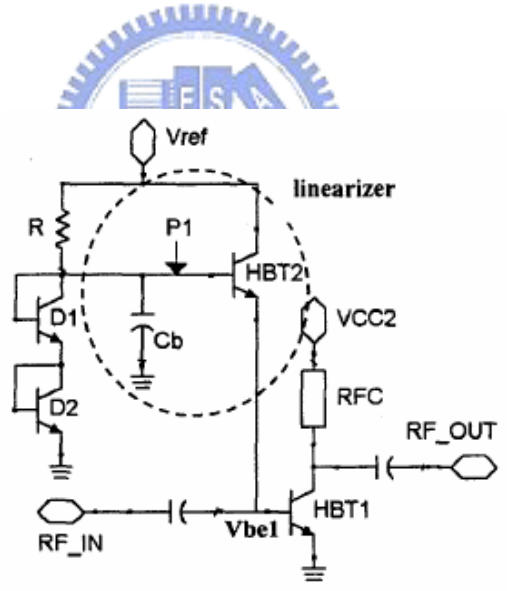


Figure 2.10 Circuit topology of the linearizer

Figure **2.11** describes the effect of the capacitance value on the Vbe1 of the RF amplifier (HBT1) simulated as a function of input power level. Capacitance of 6pF keeps the Vbe to the designed value upto the input power of 5 dBm, and shows 16dB improvement in input power stability of Vbe compared to the 0pF capacitance case.

The input impedance to the linearizer from the RF amplifier (HBT1) decreases with the increasing shunt capacitance, so there will be an increase of RF power loss to the linearizer. Figure 2.12 shows the simulated gain compressions and phase distortions of the power amplifier as a function of input power level for the different values of linearizing capacitance in the bias circuit.

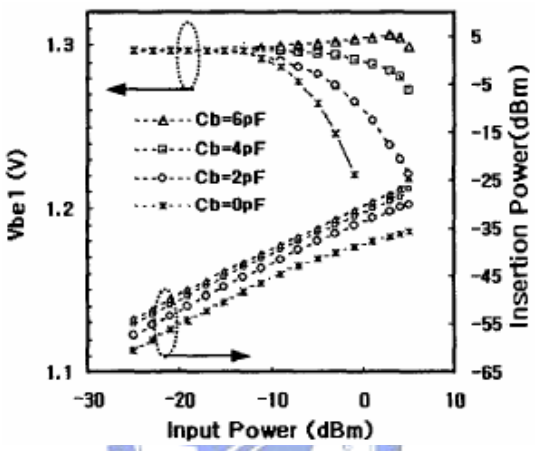


Figure 2.11 Vbe1 and insertion power loss V.S. linearizing capacitance as increasing input power

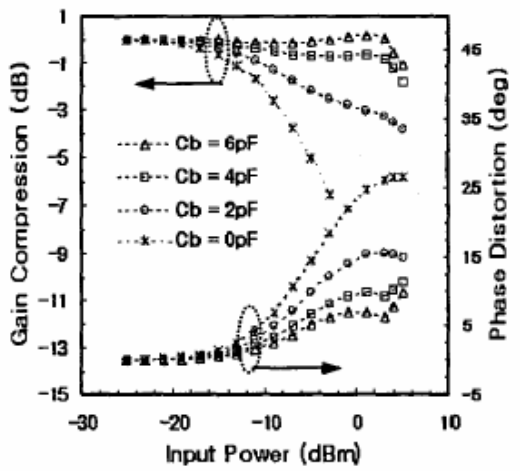


Figure 2.12 Gain compression and phase distortion for different value of linearizing capacitance

2.3 PHEMT device

An Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT) as shown in Figure2.13, Utilizing an Electron-Beam direct-write 0.25 um by 750 um schottky barrier gate [8]. The recessed “mushroom” gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for reliable high-power applications. Figure 2.14 2.15 2.16 show the performance specification. Figure 2.17 shows the libra model.

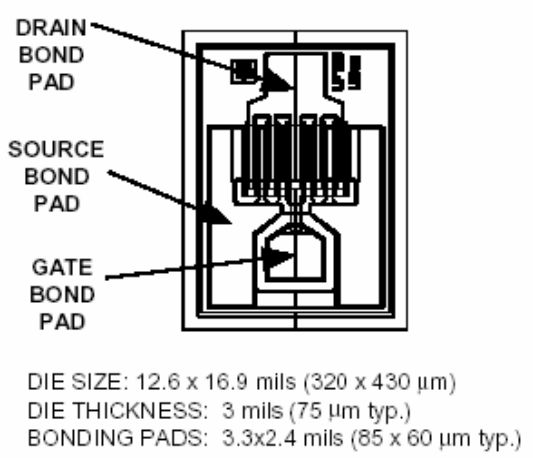


Figure 2.13 LP750 PHEMT 0.5W

SYMBOLS	PARAMETERS		MIN	TYP	MAX	UNITS
I_{DSS}	Saturated Drain-Source Current V_{DS} = 2V V_{GS} = 0V		190	225	265	mA
P_{1dB}	Output Power at 1dB Gain Compression V_{DS} = 8.0V, I_{DS} = 50% I_{DSS}	*f* = 18 GHz	26.5	28.0		dBm
G_{1dB}	Power Gain at 1dB Gain Compression V_{DS} = 8.0V, I_{DS} = 50% I_{DSS}	*f* = 18 GHz	8.0	10.0		dB
η_{ADD}	Power-Added Efficiency			55		%
I_{MAX}	Maximum Drain-Source Current	V_{DS} = 2V V_{GS} = +1V		400		mA
G_M	Transconductance	V_{DS} = 2V V_{GS} = 0V	180	230		mS
V_P	Pinch-Off Voltage	V_{DS} = 2V I_{DS} = 4mA	-0.25	-1.2	-2.0	V
I_{GSO}	Gate-Source Leakage Current	V_{GS} = -5V		5	40	µA
BV_{GS}	Gate-Source Breakdown Voltage	I_{GS} = 4mA	-12	-15		V
BV_{GD}	Gate-Drain Breakdown Voltage	I_{GD} = 4mA	-12	-16		V
Θ_J	Thermal Resistivity			65		°C/W

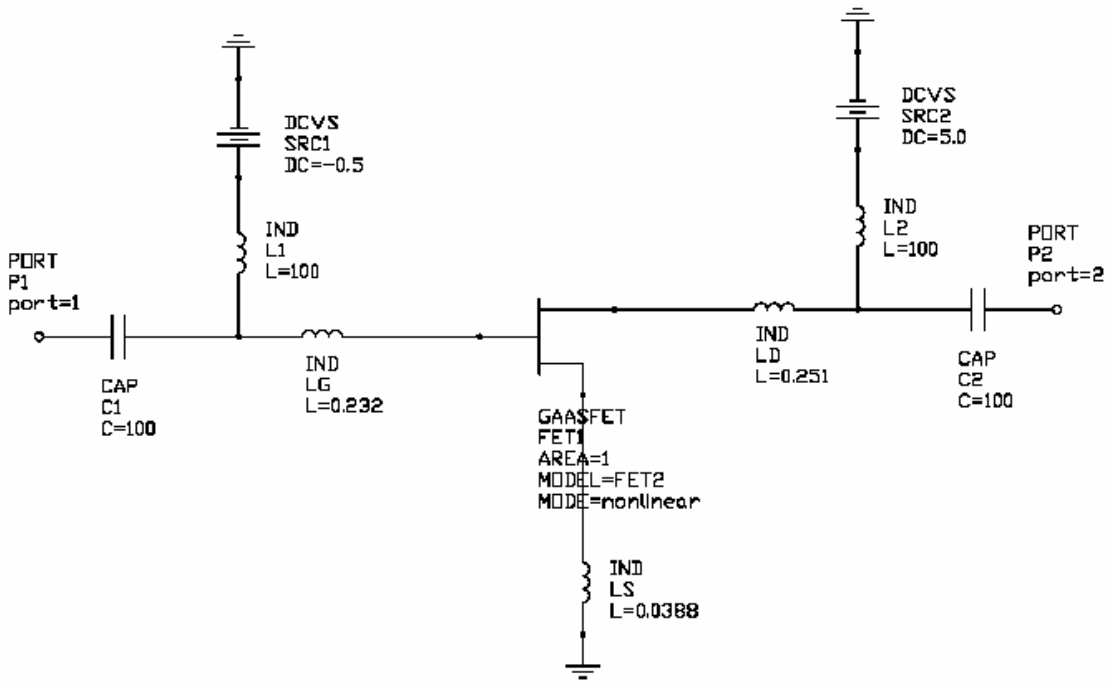
Figure 2.14 0.5W power PHEMT

RECOMMENDED CONTINUOUS OPERATING LIMITS		
SYMBOL	**PARAMETER**	**RATING[2]**
V_{DS}	Drain-Source Voltage	8V
V_{GS}	Gate-Source Voltage	-1V
I_{DS}	Drain-Source Current	0.8 x I_{DSS}
I_G	Gate Current	8 mA
P_{IN}	RF Input Power	150 mW
T_{CH}	Channel Temperature	150°C
T_{STG}	Storage Temperature	-20/50°C
P_T	Power Dissipation	2.0 W[3,4]
G_{XdB}	Gain Compression	8 dB

Figure 2.15 continuous operating limits

ABSOLUTE MAXIMUM RATINGS (25°C)		
SYMBOL	**PARAMETER**	**RATING[1]**
V_{DS}	Drain-Source Voltage	12V
V_{GS}	Gate-Source Voltage	-4V
I_{DS}	Drain-Source Current	2 x I_{DSS}
I_G	Gate Current	35 mA
P_{IN}	RF Input Power	300 mW
T_{CH}	Channel Temperature	175°C
T_{STG}	Storage Temperature	-65/175°C
P_T	Power Dissipation	2.2W[3,4]

Figure 2.16 Absolute maximum ratings



CURTICE3					
FET2					
BETA= 0.04647	A3= 0.00075	IS= 1.00E-14	RIN= 0	KF= 0	FFE1= 1
GAMMA=4.1457	TAU= 0.2709E-11	N= 1	CGS0= 0.13389E-11	AF= 1	
VOUTO= 7.4064	R1= 0	RDS= 379	CGD0= 0.11529E-12	TNOM= 27	
VTO= -1.0	R2= 0	CRF= 0.137E-10	FC= 0.50	XTI= 3	
A0=0.23189	VB0= 15	RD= 1.50	CDS= 0.1589E-12	EG= 1.11	
A1= 0.18564	VBI= 1.68	RG= 3.80	CGS= 0	VTOTC= 0	
A2= -0.0400	RF= 0	RS= 0.6446	CGD= 0	BETATCE= 0	

Figure 2.17 Libra model

2.4 Specification

2.4.1 Cascaded 2-Tone, 3rd-Order Compression Point (IP3)

When two or more tones are present in a nonlinear device, inter-modulation products are created as a result. A power series describes all of the possible combinations of generated frequencies, 3rd-order products lie near in frequency to the two input tones and are therefore very likely to fall in-band at the output. As a device

is driven farther into its nonlinear region, the amplitudes of the third order products increase while the powers of the input tones decrease. If the device was not limited in output power, then the powers of the inter-modulation products would increase in power until they were eventually equal in power with the input tones at the output.

Assuming a gain of 1(0dB) the slope of the fundamental gain line would be 1:1; the slope of the 3rd-order gain line would be 3:1. The slope of the 3rd-order gain line would 3:1. Figure 2.18 shows the IP3 point. The slope of the 3rd-order product line is 2:1 relative to the fundamental gain line. Accordingly, the 3rd-order products increase in power at twice the rate of the input tones and are always three times farther away from the IP3 than the input tones when not near saturation.

The power of the 3rd-order products can be predicted when the IP3 is know, or the IP3 can be predicted when the relative amplitudes of the 3rd-order tone and the input tones are know.

Equal Input Powers

$$P_{3rd\text{-}order\ products} = P_{input\ tones@output} - 2 \cdot (IP3 - P_{input\ tones@output}) \ \{dBm\}$$
$$P_{3rd\text{-}order\ products} = 3 \cdot P_{input\ tones@output} - 2 \cdot IP3 \ \{dBm\}$$
$$IP3 = 3/2 \cdot P_{input\ tones@output} - 1/2\ P_{3rd\text{-}order\ products} \ \{dBm\} \quad (2.1)$$

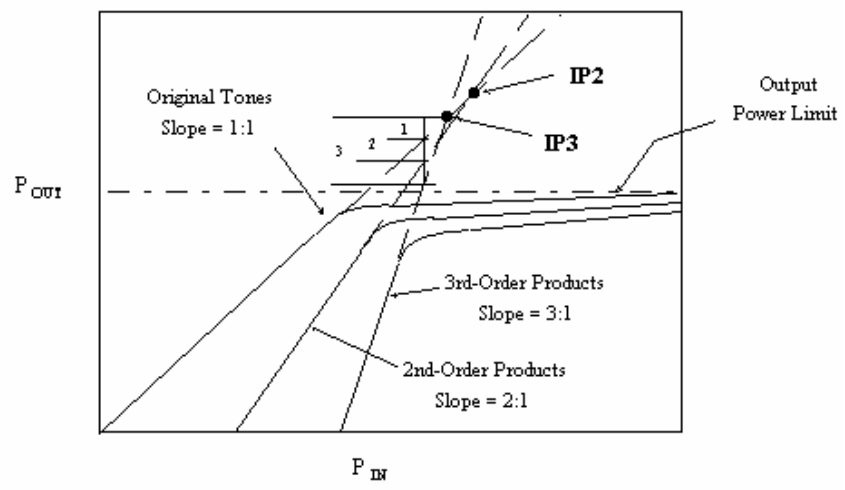


Figure 2.18 IP3

Calculating the cascaded values for IP3 requires the following operation base upon ratios for gain and IP3:

$$\frac{1}{ip3_N} = \sum_{i=1}^{N} \left[\frac{1}{ip3_i * \prod_{j=i+1}^{N} gain_j} \right]$$

convert to decibels

$$IP3 = 10 \cdot \log_{10}[ip3] \ \{dB\} \tag{2.2}$$

The following equation is a series expansion of the mixing of two pure tones:

$$P_{OUT} = a_1*(f_1) + a_2*(f_2) + a_3*(1*f_1 \pm 1*f_2) + a_4*(1*f_1 \pm 2*f_2) + a_5*(2*f_1 \pm 1*f_2) + \quad \Leftarrow \text{3rd-Order Products}$$
$$a_6*(2*f_1 \pm 2*f_2) + \ldots + a_\infty*(\infty*f_1 \pm \infty*f_2)$$

Conversion of the IP3 and IP2 reference may be accomplished with the following equations:

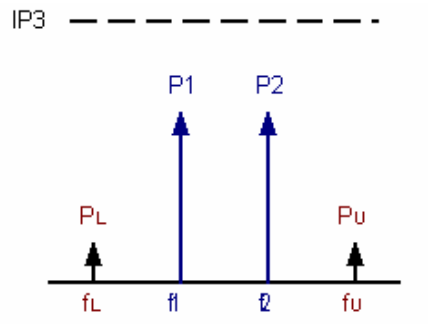
$$IP3/IP2_{OUTPUT} = (IP3/IP2_{INPUT} + Gain) \ \{dBm\} \quad (2.3)$$

$$IP3/IP2_{INPUT} = (IP3/IP2_{OUTPUT} - Gain) \ \{dBm\} \quad (2.4)$$

Unequal Input Powers

$$P_L = P_2 - 2*(IP3 - P_1)$$

$$P_U = P_1 - 2*(IP3 - P_2)$$



Where power units are kept constant in dBm

Figure 2.19 2-tone inter-modulation

2.4.2 1dB Compression Point (P_{1dB})

Active components are limited to the amount of power that can be provided. When operating within the linear region of the component, gain through the component is constant for a given frequency. As the input signal is increased in power, a point is reached where the power of the signal at the output is not amplified by the same amount as the smaller signal. At the point where the input signal is amplified by an amount 1 dB less than the small signal gain, the 1 dB compression point has been reached as shown in Figure 2.20. A rapid decrease in gain will be experienced after the 1 dB compression point is reached. If the input power is increased to an extreme value, the component will be destroyed.

Passive, nonlinear components such as diodes also exhibit 1 dB compression points. Indeed, it is the nonlinear active transistors that cause the 1 dB compression point to exist in amplifier. Of course, a power level can be reached in any device that will eventually destroy it.

$$G_{1dB}\,(dB) = G_0(dB) - 1 \tag{2.5}$$

$$P_{1dB}dBm) = G_{1dB}\,(dB) + P_{in}(dBm) \tag{2.6}$$

G_0 : linear gain

P_{1dB} : 1dB gain compress point

P_{in} : input signal 1dB compress point

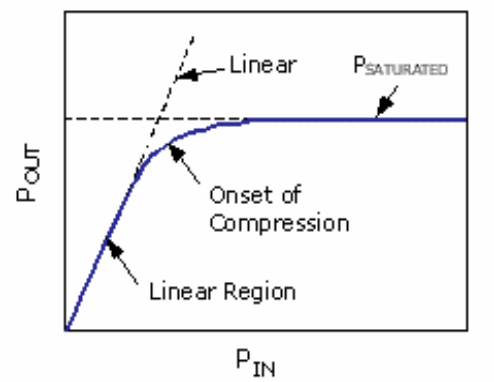


Figure 2.20 P_{1dB}

2.5 Budget

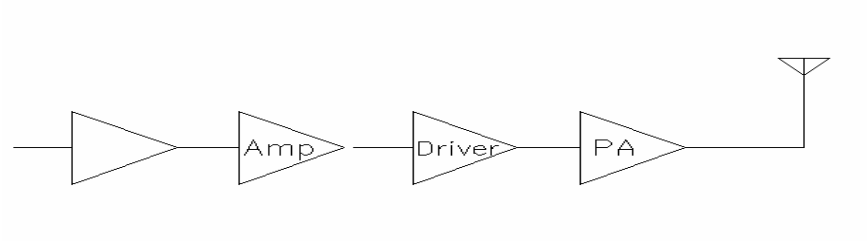


Figure 2.21 Stage cascade

IP3 of stage= P_{1dB} + constant (2.7)

2 Tone IMD of stage = 2* (P_{1dB} - P_{out}+ constant) (2.8)

2 Tone IMD of cascade = ROUND(-20*LOG(10^(- last stage IMD/20)+

10^(- stage IMD/20)) (2.9)