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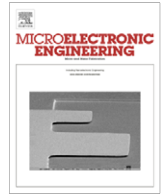

Accelarated Publication

Evaluation of Cu-bumps with lead-free solders for flip-chip package applications

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ABSTRACT

Low cost electroplated Cu-bump with environmental friendly Sn solder was developed for flip-chip applications. The seed layer used was Ti/WN_x/Ti/Cu where WN_x was used as the Cu diffusion barrier and Ti was used to enhance the adhesion between bump and the chip pad. Thick negative photoresist (THB JSR-151N) with a high aspect ratio of 2.4 was used for electroplating of copper bump and Sn solder. The Sn solder cap was reflowed at 225° for 6 min at N_2 atmosphere. No wetting phenomenon was observed for the Sn solder as evaluated by energy-dispersed spectroscopy (EDS). The Cu-bump with Ti/WN_x/Ti/Cu seed layer not only have higher shear force than the Cu-bump with Ti/Cu seed layer but also has higher resistance to fatigue failure than the Au, SnCu, SnAg bumps.

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1. Introduction

Flip-chip technology can dramatically reduce the packaging cost as compared to wire bonding for high frequency component assembly because their's no need for individual chip tuning for package. This technology provides a chip bonding process which meets the requirements of small dimensions, thin packages, low cost, and high reliability [1]. For the solder balls used in flip-chip technology, SnAg and SnCu are the most promising materials to replace the conventional SnPb solder which will be prohibited in the near future due to the toxicity of Pb. The European Union Waste in electrical and electronic equipment (WEEE) has proposed to ban Pb usage in electronic products by 2008 [2]. For flip-chip interconnections, bumps are required either on the substrate or on the chip side [3]. In high volume production, the bumps are usually formed either by photolithography combined with electroplating, or electroless deposition followed by solder printing. The development of advanced wireless communication system has increased the need of packaging applications at higher frequencies. For high frequency integrated circuits (RFIC), smaller bump cross section is required to improve the RF performance, however, the cross section is limited by the resolution and the aspect ratio of the photoresist used in the lithography. The bump shape also affects the performance [4], when the spacing between the chip and board is reduced, more field fringes into the substrate which will reduce the microwave line impedance. Simulations results show that when RFIC frequency is above 60 GHz, the bump height must be above 50 μm to reduce the electromagnetic (EM) interference between the RFIC on the chip and the substrate [5].

Low cost Cu-bump instead of Au bump with environment friendly lead-free Sn cap is developed with heights up to 85 μm for microwave flip-chip packaging in this study. The copper bumps developed contain Ti/WN_x/Ti/Cu diffusion barrier and are high enough (> to 50 μm) prevent the EM field fringe into the substrate and also to make the substrate surface less sensitive to the strains caused by the coefficient of thermal expansion (CTE) differences.

2. Experimental

The process flow of the flip-chip bumps in this study is shown in Fig. 1. An under bump metallization (UBM) layer was first sputtered on the bare 3 in. GaAs wafer substrate. The UBM consisted of sputtered Ti/WN_x/Ti/Cu metallization layers from bottom to top and their thicknesses were 30/60/30/100 nm, respectively. These UBM layer was used as seed layer for subsequent electroplating. The WN_x layer is an effective copper diffusion barrier layer [6]. After the UBM layer metallization, a negative photoresist (JSR THB-151N) was spun on the wafer, as the plating mask, the thickness of the photoresist was 120 μm and the diameter of the patterns was 50 μm. After the photoresist was patterned, copper bumps were electroplated using $CuSO_{4-}$-based electrolyte solution with the current density of 3.5 ASD (A/dm^2). Sn solder was electro plated on top of the Cu-bumps with $SnSO_4$-based solution. In order to enhance the wettability of the resist surface to the electrolyte solution and to activate the metallic seed layer, the wafer was dipped in the acid-based copper electrolyte solution shortly before electroplating. After electroplating, the photoresist was removed by stripper solution (JSR THB-S1) at 65 °C, and the WN_x and Ti layers were removed by wet etch. The reflow of the solder material was performed at 225 °C for 6 min. The reflow temperature and time were optimized to achieve optimum Sn–Cu-bump composi-

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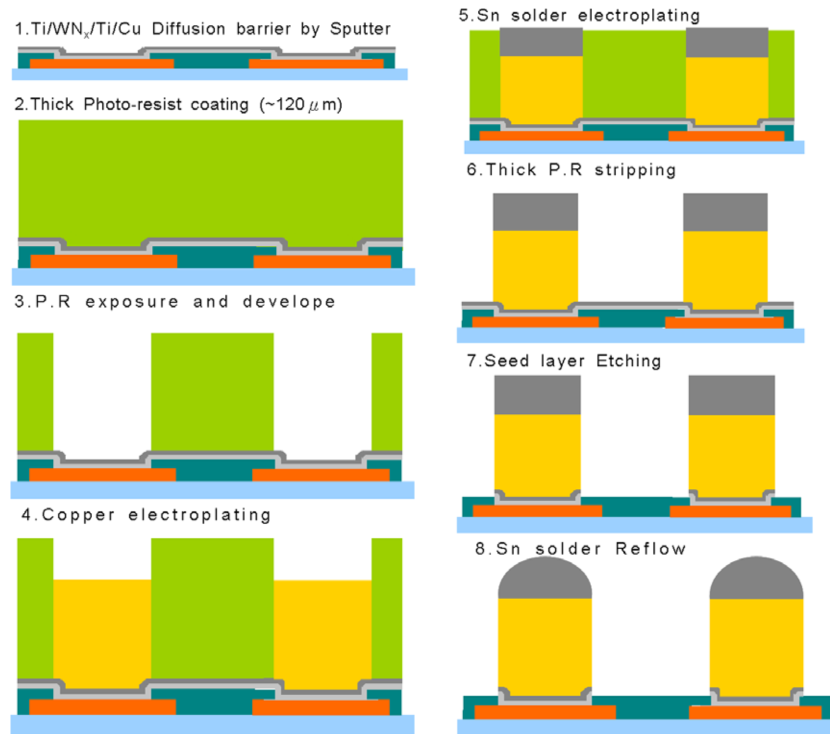


Fig. 1. Schematic of the process flow for the fabrication of the Cu-bump with lead-free solder.

tions. The total height of the Cu-bump and the Sn solder was measured by scanning electron microscopy (SEM). The shear strength of the bump was examined by commercial test apparatus (Dage-4000). The testing speed was 100 μm/s, test load was 100 g, and the shear height was set at 10 μm from the bottom of the bump. The solder voids were examined by X-ray (SMX-160 E-II after the solder reflow. Sn solder wettability was characterized by energy-dispersed spectroscopy (EDS) mapping.

3. Results and discussions

3.1. Copper bumps with plated Sn cap

Copper bumps were fabricated by electroplating process. The maximum aspect ratio achieved for the plated Cu-bumps using JSR THB-151N negative thick photoresist was up to 2.4. For thick photoresist coating, the resist thickness and uniformity mainly depend on the spin time and the spin speed. Non-uniform plating with partial filling of the plating via might occur during the electroplating process for the high aspect ratio photoresist. These problems can be solved by adding additives, controlling flow rate and using pulsed current plating. The uniformity of the height of the plated copper bumps can be improved by controlling the plating current density, the electrolyte flow rate and the electrolyte solution concentration [7]. In this study, the copper plating was performed using 3.5 ASD (A/dm^2) current density, 10 l/min electrolyte flow rate and 1/100 s pulse current. Due to the current crowding in the wafer edge, the plated bump around the edge of the wafer was 2–4 μm higher than the bumps at the wafer center.

The copper bump with Ti/WN$_x$/Ti/Cu UBM layer and the plated Sn solder on the top is as shown in Fig. 2. The plated copper bumps had a height of 65–70 μm. The height of copper bump in the structure is important in preventing of the EM interference between the chip and the lead-frame, it also determines the Sn solder thickness. Too thick plated solder could lead to solder bridging or solder spreading on the lead-frame at the reflow process. The Sn solder

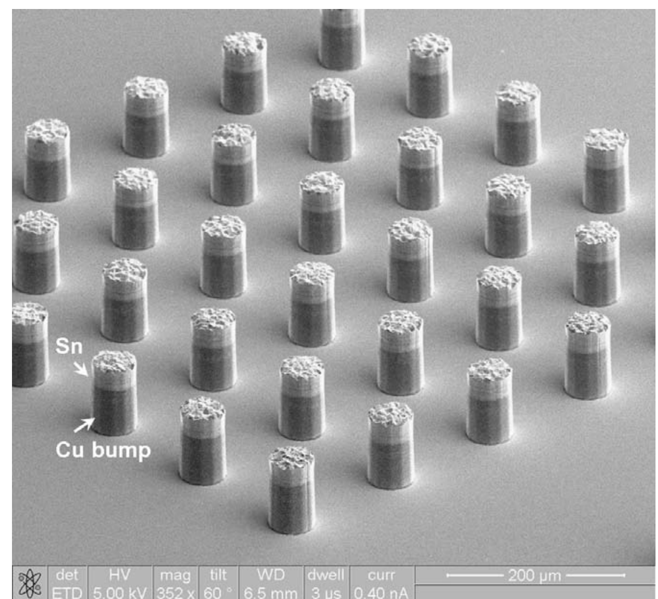


Fig. 2. SEM micrograph of the copper bump array with Sn cap.

plated on the copper bumps was between 25–30 μm in height, it provides a robust assembly process and the highest reliability [8].

3.2. Bump shear strength test results

For the solders used in the flip-chip package, bonding strength of the solder to the UBM on chip side is very important. In order to evaluate the shear strength of the copper bumps on the UBM with Cu diffusion barrier, copper bumps on different UBM layers including Ti/Cu and Ti/WN$_x$/Ti/Cu were tested and compared. Also the shear strength of different bump materials including Au, SnCu,

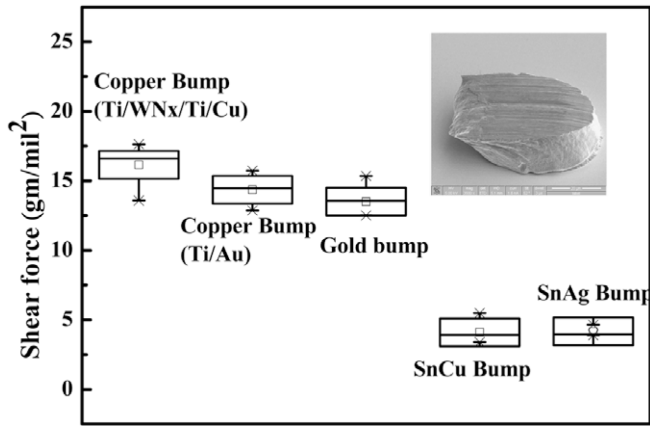


Fig. 3. Shear force test results for different types of bumps.

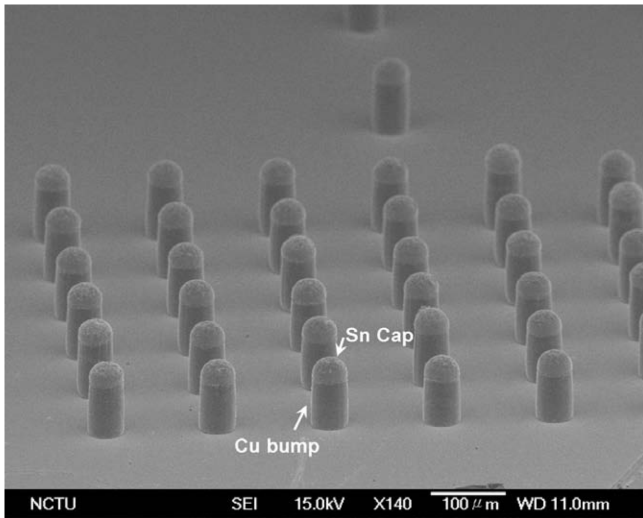


Fig. 4. SEM image of the Sn solder after reflow.

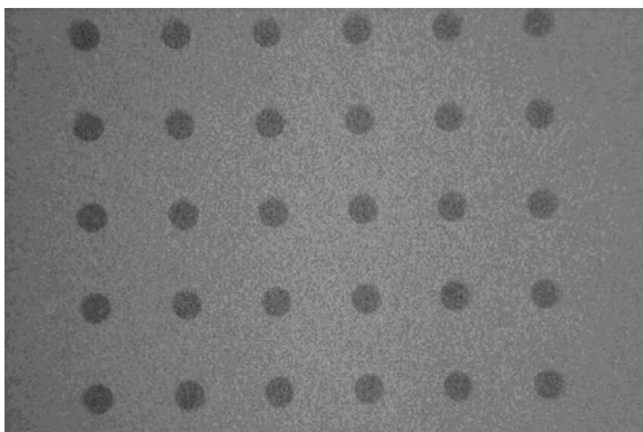
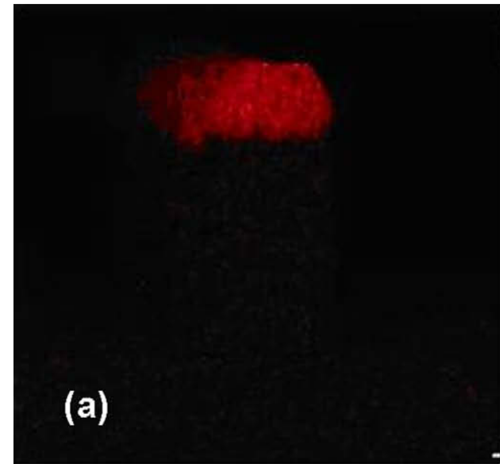
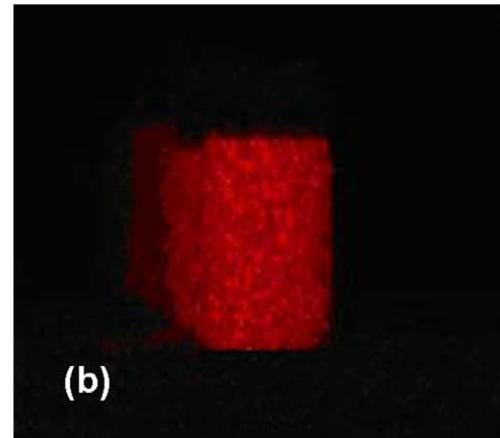


Fig. 5. X-ray image for the examination of the void in the solder after reflow.





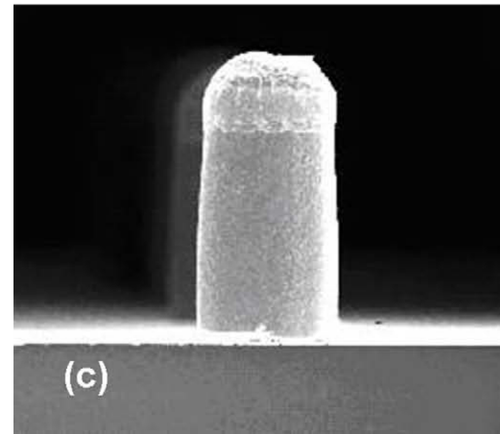


Fig. 6. Energy-dispersed spectroscopy (EDS) mapping of the copper bump with Sn cap: (a) Sn element mapping, (b) Cu element mapping, and (c) SEM image.

SnAg bumps were compared in this study. The shear force was conducted using global bond test (Dage-4000s, Richardson Electronics Ltd.). Shear blade height was set at 10 μm from the bottom of the bump. Shear force test results are shown in Fig. 3 with each material tested for 60 samples. Only two types of failure modes were observed. The failure occured either inside the solder as shown in the insert picture in Fig. 3 or between the UBM and the wafer interface (not shown here). For the copper bumps on Ti/WN_x/Ti/Cu UBM, the failure mode was inside the solder and it has higher shear strength than the bumps with Ti/Cu UBM. For the bumps with Ti/Cu UBM, the failure mode was at the interface of UBM and wafer. It indicates that the Ti/WN_x/Ti/Cu UBM can act as an effective Cu diffusion barrier and also provides a strong adhesion between the bump and the chip pad. The shear force of copper bumps is also stronger than Au, SnCu, SnAg bumps, this means that the copper bump fabricated by electroplating has acceptable mechanical properties for flip-chip package applications.

3.3. Sn soldering

After the electroplating process, resist was stripped and the Cu diffusion barrier layer beneath the resist was removed. The reflow process of the Sn solder was performed to form a solder ball on the top of the copper posts as shown in Fig. 4. The Sn solder reflow process was performed using horizontal furnace at 225 °C for 6 min at N_2 atmosphere to prevent the possible oxidation of the solder material. Oxidation on the surface of the solder material may effect the reliability of the solder joint to the substrate. No void or defect was found in the solder and the Cu-bump materials as analyzed by X-ray (SMX-160E-II) analysis. The X-ray mapping data after soldering is shown in Fig. 5.

Fig. 6 shows the EDS mapping results of the Sn solder after reflow process. There was no wetting phenomenon between Sn and Cu at the reflow temperature with the reflow time used. Fig. 6 (a–c) show the EDS analysis results which can be used to determine the composition of the elements around the bump and the solder. These figures indicate that after the reflow process, the Sn element in the solder and the Cu element in the bump were separated from each other, which means the Sn there was no wetting phenomenon during reflow process, it can provide a good solder ball for packaging applications.

4. Conclusions

In this study, high aspect ratio Cu-bumps with Sn solder cap were successfully fabricated by electroplating and thermal reflow process. The height of the bumps was higher than 85 μm, which is high enough to prevent the EM interference between the chip and the bonding substrate for high frequency flip-chip packaging. The fabricated copper bumps with Sn solder cap showed no voids or contamination on the solder. The shear test results showed that the UBM structure with Ti/WN_x/Ti/Cu had higher shear stress than the UBM with the Ti/Cu seed layer. The developed Cu-bumps with Ti/WN_x/Ti/Cu UBM layer also demonstrated higher shear force resistance and fatigue resistance than the Au, SnCu, SnAg bumps. Overall, the developed low cost, high aspect ratio Cu-bump structure with environmental friendly lead-free Sn solder cap demonstrated excellent material stability and mechanical stability and is suitable for high frequency flip-chip applications.

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