A Low-Power 2.4-GHz CMOS GFSK Transceiver With a Digital Demodulator Using Time-to-Digital Conversion

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***Abstract*—A technique of time-to-digital conversion is utilized in a digital demodulator for a low-power 2.4-GHz CMOS GFSK transceiver. The proposed time-to-digital converter (TDC) employs a self-sampling technique and an auto-calibration algorithm to avoid edge synchronization problems and the need of a delay-locked loop (DLL). With the TDC, a limiter and a digital demodulator can be employed simultaneously in the receiver to achieve low power consumption and high performance. Additionally, in the transmitter, the open-loop VCO modulation is adopted to save hardware and power consumption. The transmitter frequency drift in open-loop modulation and frequency offset between the receiver and the transmitter can be easily resolved by the proposed receiver architecture. All required building blocks of the proposed transceiver, except a RF matching network and a crystal, were implemented on a 4-mm^2 chip by a 0.18-μm CMOS process. The receiver achieves -89-dBm sensitivity at 0.1% BER with 1-Mb/s data rate, and the transmitter delivers up to 0-dBm output power. The receiver and transmitter consume 13.3 mA and 10.7 mA, respectively, from a 1.8-V power supply.**

***Index Terms*—Complex bandpass filter, demodulator, frequency synthesizer, low-noise amplifier (LNA), open-loop VCO modulation, time-to-digital converter (TDC).**

I. Introduction

THE wireless communication market has grown dramatically in recent years via the rapid development of new products and services. In addition to high-throughput applications, such as wireless local area networks (WLANs), demands have increased for low-rate and short-distance applications including wireless personal area networks (WPANs), short-range communications, sensor networks, remote control, and replacement for computer peripheral wires. Low power consumption, low cost, and small size are particularly important to such applications.

To achieve these goals of low power consumption, low cost, and small size, a number of GFSK receivers based on limiters followed by purely analog or mixed-signal demodulators have been reported [1]–[4]. The architecture of these receivers is shown in Fig. 1. However, most of the reported demodulators suffer from harmonic distortions produced by limiters and multipliers, which need to be eliminated by additional circuits. Moreover, these demodulators are usually more sensitive to process, voltage, and temperature (PVT) variations in comparison to digital demodulators.

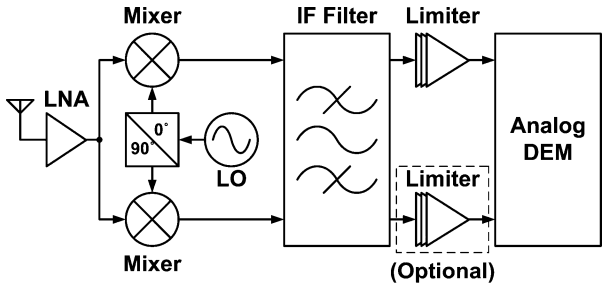

Fig. 1. A limiter-based receiver architecture employing an analog or mixed-signal demodulator.

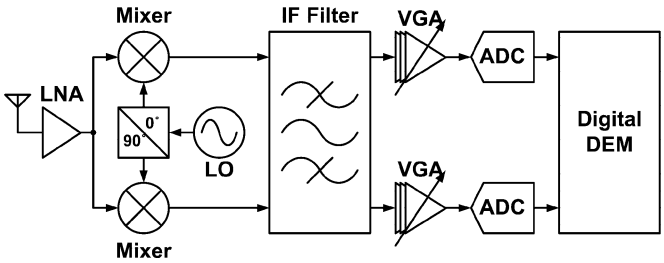

Fig. 2. A general receiver architecture employing a digital demodulator.

On the other hand, Fig. 2 shows the general architecture of a receiver employing conventional digital demodulators. Conventional digital demodulators exhibit advantages such as optimal performance and high tolerance to PVT variations. However, in order to employ digital demodulators, variable-gain amplifiers (VGAs), auto gain controllers (AGCs), and analog-to-digital converters (ADCs) are required. These circuits usually complicate the design and consume significant power. In addition, digital signal processing (DSP) functions following the ADCs are usually complex and, therefore, could result in a high gate count.

In order to achieve a low-power GFSK transceiver employing a limiter and a digital demodulator simultaneously in the receiver [5], this paper utilizes a technique of time-to-digital conversion in the digital demodulator [6]–[8] to permit using a preceding limiter. By this arrangement, the goals of low power consumption, low cost, and small size can be achieved while

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the advantages of the digital demodulator are kept. Moreover, since the time-to-digital conversion is performed by detecting the zero-crossings of the IF signal, the harmonic distortion problem in conventional analog or mixed-signal demodulators is inherently avoided in the proposed demodulator. Another advantage is that since large tolerance to the transmitter frequency drift and the frequency offset between the receiver and the transmitter can be achieved easily by the proposed demodulator, open-loop VCO modulation can be employed in the transmitter to save hardware and power consumption.

In Section II, the architecture of the proposed transceiver is presented. Section III describes the operation principle and implementation of the utilized time-to-digital conversion, and Section IV explains the circuit design of building blocks. The experimental results are shown in Section V. Section VI concludes a summary.

II. Transceiver Architecture

A. Receiver Architecture

In the design of a receiver, three commonly used architectures are high-IF, low-IF, and zero-IF. In this paper, the high-IF receiver architecture is not selected due to its low integration level and extra power consumption on I/O driving circuits for external components. Moreover, for a narrow-band GFSK-modulated signal, a substantial amount of signal power is confined in the low frequency range [1], [4]. If the zero-IF architecture is selected, the DC offset and flicker noise can significantly degrade the signal-to-noise ratio (SNR). Therefore, the low-IF architecture is employed in this receiver.

In addition, a dual-conversion structure with a careful frequency plan is employed for its several advantages. Fig. 3 shows the detailed frequency plan of the proposed receiver. The receiver employs a first LO (LO1) and a second LO (LO2) to perform dual conversion. The second IF signal (IF2) is selected as 6 MHz due to the reason described in Section III-A. The LO1 frequency is 2736–2831 MHz, which results in an image band located in the frequency range with less interference. According to the proposed frequency plan, the following equation can be derived:

$$f_{\mathrm{RF}} - \frac{7}{8} f_{\mathrm{LO1}} = f_{\mathrm{IF2}} \tag{1}$$

where f_{RF} is the RF frequency, f_{LO1} is the LO1 frequency, and f_{IF2} is the IF2 frequency. The advantages of this frequency plan are summarized as follows.

i) Quadrature LO2s are generated by using a divided-by-eight circuit. This approach avoids the use of poly-phase filters, which usually require power-hungry RF buffers at input and output terminals to compensate for their loss.

ii) Since the second down-conversion operation is performed with quadrature LO2s of 342–354 MHz, which is much lower than conventional quadrature LO frequencies, the accuracy in matching quadrature phases can be increased, and high image rejection ratio can be attained.

Fig. 4 shows the block diagram of the receiver. The input signal at 2400–2483.5 GHz is amplified by an LNA and, subsequently, is down-converted to the first IF (IF1) of 336–348 MHz by the first mixer. The I/Q mixers driven by the quadrature LO2s further down-convert the signal to a 6-MHz IF2. A complex bandpass filter with 6-MHz center frequency, acting as a channel-selection filter, selects the desired signals. After channel selection, the selected signal is amplified to a clipped level by a limiter, and received signal strength is also indicated. Finally, a digital demodulator extracts the digital bits.

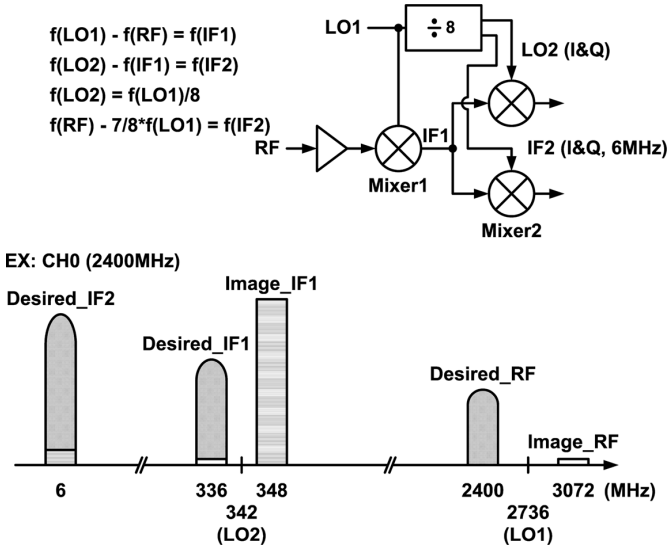

Fig. 3. Frequency plan of the proposed receiver.

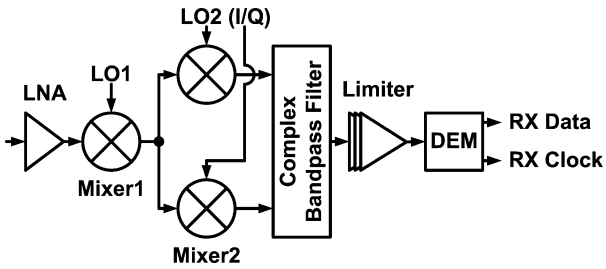

Fig. 4. Block diagram of the receiver.

B. Transmitter Architecture

In a transmitter, GFSK signals can be generated by various methods, such as the direct quadrature up-conversion of I/Q signals [1], [3], [9]–[11], the close-loop VCO modulation [12]–[18], and the open-loop VCO modulation [19]–[21]. The direct quadrature up-conversion is the most complex and power-hungry approach and, therefore, is not used in this paper. Applying the close loop VCO modulation might be suitable for achieving low power consumption. One of the most promising approaches is two-point sigma-delta modulation. However, a fractional-N PLL is required, increasing the circuit complexity and cost. Furthermore, a problem needs to be coped with is the mismatch between tuning gains of two modulation paths, which also complicates circuit designs [21]. The implementation of an open-loop VCO modulation is usually simpler and more efficient in power consumption. However, if this architecture is to be used, the most important factor needs to be considered is system tolerance to transmitter frequency drift. In our targeted applications, data throughput is typically low; transmitters do not have to work continuously for long duration. Moreover, the proposed receiver can provide sufficient tolerance to transmitter frequency drift. Therefore, the open-loop VCO modulation architecture is selected in this paper.

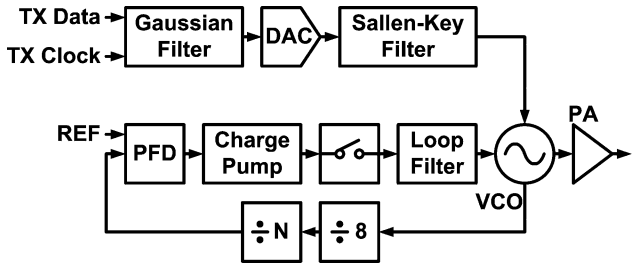

Fig. 5. Block diagram of the transmitter.

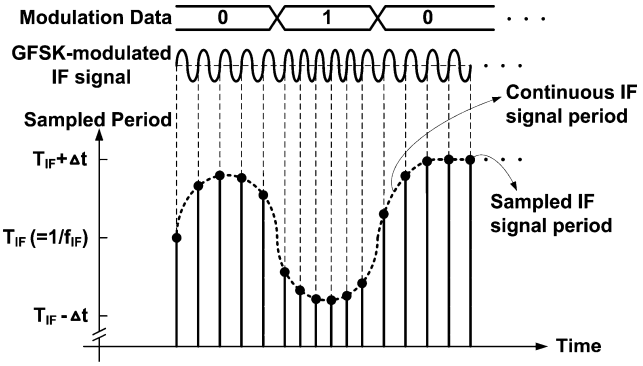

Fig. 6. Operation concept of sampling a GFSK-modulated IF signal with time-to-digital conversion.

Fig. 5 shows the block diagram of the transmitter. The transmitter consists of a Gaussian filter, a frequency synthesizer, and a power amplifier (PA). Data is fed into a lookup-table-based Gaussian filter and, then, converted to an analog frequency-controlling signal by a DAC and a Sallen-Key filter to modulate the VCO. A GFSK modulated signal output by the VCO is amplified to a desired power level by the PA. The frequency synthesizer employs the integer-N architecture and consists of a VCO, a frequency divider, a phase/frequency detector (PFD), and a loop filter. An auto-calibration circuit is also included to obtain low phase noise and good tolerance to PVT variations.

III. Utilized Time-to-Digital Conversion

A. Operation Principle

Fig. 6 depicts the operation concept of sampling a GFSK-modulated IF signal with time-to-digital conversion. For a GFSK-modulated IF signal, its frequency changes continuously according to Gaussian-shaped data. Therefore, it's important to estimate frequency change of a received GFSK-modulated IF signal during demodulation. In order to achieve this purpose, a technique of time-to-digital conversion is employed to detect zero-crossings, and, subsequently, to compute the period of the GFSK-modulated IF signal by measuring intervals between adjacent zero-crossings at rising or falling edges of the GFSK-modulated IF signal. This process can be regarded as sampling the period of the GFSK-modulated IF signal with a rate which approximately equals to the IF frequency $(f_{\rm IF})$. It is worth noting that since the IF carrier is eliminated after the time-to-digital conversion, the subsequent signal processing of demodulation can be simplified.

During the time-to-digital conversion, in addition to the desired signal, associated bandpass noise is also converted into the baseband. Shown in Fig. 7, the bandpass noise creates deviation of zero-crossing positions. This deviation results in variation of the IF period and is the main source of baseband noise. In order to explore the effect of the time-to-digital conversion to baseband SNR, the power of converted baseband noise is quantitatively analyzed in the following. Note that in the analysis, an un-modulated IF signal associated with bandpass noise with much lower power level than that of the IF signal is assumed to simplify the analysis.

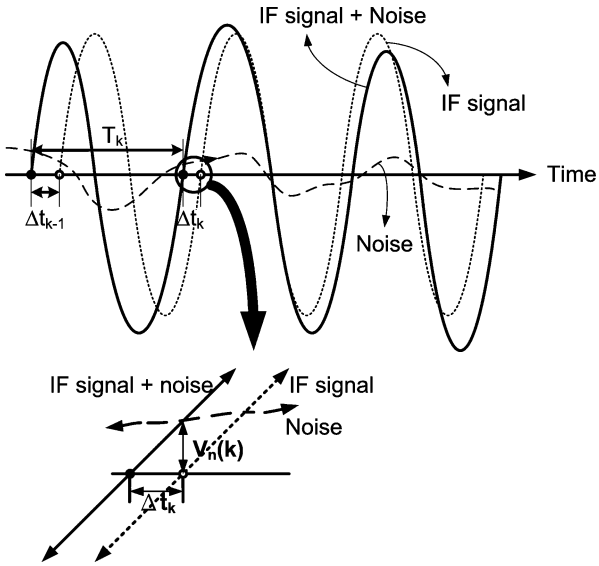

Fig. 7. Deviation of zero-crossings of IF signal due to bandpass noise.

Firstly, the power spectral density (PSD) of noise is determined. In Fig. 7, the variation of the kth period caused by bandpass noise can be represented as

$$\Delta T_k = -(\Delta t_k - \Delta t_{k-1}) = \frac{1}{R}v_n(t_{k-1}) - \frac{1}{R}v_n(t_k) \quad (2)$$

where R is the time derivative of the IF signal at zero-crossings; $v_n(t_{k-1})$ and $v_n(t_k)$ are voltage levels of the bandpass noise at times t_{k-1} and t_k, respectively. Equation (2) can be regarded as the result of another equivalent process: The original bandpass noise is delayed by a time of $1/f_{\rm IF}$, and, subsequently, the delayed bandpass noise is subtracted by the original bandpass noise and multiplied by a scaling factor, $1/R$; then, the delayed-subtracted-scaled bandpass noise is ideally sampled with a rate of $f_{\rm IF}$. Based on this alternative process, the PSD of the delayed-subtracted-scaled bandpass noise is

$$\begin{aligned} S_{n,o}(f) &= \frac{1}{R^2}S_n(f)\left|\mathrm{e}^{-\mathrm{j}2\pi f/f_{\rm IF}} - 1\right|^2 \\ &= \frac{1}{A_{\rm IF}^2(2\pi f_{\rm IF})^2}S_n(f) \\ &\quad \times \left|2\sin\left(\pi\frac{f}{f_{\rm IF}}\right)\mathrm{e}^{-\mathrm{j}\pi(f/f_{\rm IF}-1/2)}\right|^2 \\ &= \frac{1}{A_{\rm IF}^2(2\pi f_{\rm IF})^2}\left(2\sin\left(\pi\frac{f}{f_{\rm IF}}\right)\right)^2 S_n(f) \end{aligned} \quad (3)$$

where $S_n(f)$ is the PSD of the original bandpass noise in V^2/Hz, and A_{IF} is the IF signal amplitude in V. Note that

$S_{n,o}(f)$ has unit of s^2/Hz. Equation (3) shows a band-rejection shaping around $f_{\rm IF}$. Fig. 8 illustrates conversion of the noise PSD. Shown in Fig. 8(a), the original bandpass noise is assumed white, and its PSD is centered at $\pm f_{\rm IF}$. Fig. 8(b) shows the PSD of the delayed-subtracted-scaled bandpass noise, and Fig. 8(c) conceptually shows the PSD of the converted baseband noise. Note that the bandpass noise frequency bandwidth is assumed to be smaller than $f_{\rm IF}$.

The power of the converted baseband noise can be directly calculated with (3) because the noise power remains unchanged after the sampling operation. Based on the assumption that the double-sided PSD of the bandpass noise is $N_0/2$, ranging from $f_{\rm IF} - f_{\rm BW}/2$ to $f_{\rm IF} + f_{\rm BW}/2$ and from $-f_{\rm IF} - f_{\rm BW}/2$ to $-f_{\rm IF} + f_{\rm BW}/2$, and $f_{\rm BW}$ is smaller than $f_{\rm IF}$, (3) becomes

$$S_{n,o}(f) = \begin{cases} \frac{\frac{1}{2}N_0}{A_{\rm IF}^2(2\pi f_{\rm IF})^2}\left(2\sin\left(\pi\frac{f}{f_{\rm IF}}\right)\right)^2, & |f \pm f_{\rm IF}| \le \frac{1}{2}f_{\rm BW} \\ 0, & \text{otherwise.} \end{cases} \tag{4}$$

Therefore, the power of the converted baseband noise is

$$P_{n,o} = 2\int_{f_{\rm IF}-\frac{1}{2}f_{\rm BW}}^{f_{\rm IF}+\frac{1}{2}f_{\rm BW}} \frac{\frac{1}{2}N_0}{A_{\rm IF}^2(2\pi f_{\rm IF})^2}\left(2\sin\left(\pi\frac{f}{f_{\rm IF}}\right)\right)^2 df = \frac{F_{\rm ns}}{2{\rm SNR}_{\rm BP}(2\pi f_{\rm IF})^2} \tag{5}$$

where $\rm SNR_{BP}$ is the bandpass SNR, and $F_{\rm ns}$ is a noise-shaping factor defined as

$$F_{\rm ns} = 2\left(1 - \frac{1}{\pi}\frac{f_{\rm IF}}{f_{\rm BW}}\sin\left(\pi\frac{f_{\rm BW}}{f_{\rm IF}}\right)\right). \tag{6}$$

Fig. 9 compares the power of the converted baseband noise computed by (5) with that simulated by Matlab. The values of $f_{\rm IF}$, $\rm SNR_{BP}$, and $f_{\rm BW}$ are assumed to be 6 MHz, 14 dB, and 1 MHz, respectively. The computed results are very consistent with the simulated results.

Finally, the baseband SNR is considered. In order to simplify the derivation, the degradation of the signal power caused by the Gaussian filtering and the limited channel bandwidth is ignored. If a narrow band modulation is assumed, the baseband signal power is

$$P_{s,\rm bb} = \left(\frac{1}{2}\left(\frac{1}{f_{\rm IF} - f_d} - \frac{1}{f_{\rm IF} + f_d}\right)\right)^2 \approx \frac{f_d^2}{f_{\rm IF}^4} \tag{7}$$

where f_d is frequency deviation. By combining (5) and (7), the baseband SNR can be derived to be

$${\rm SNR_{BB}} = \frac{8\pi^2 f_d^2 {\rm SNR_{BP}}}{F_{\rm ns} f_{\rm IF}^2}. \tag{8}$$

Fig. 10 shows the baseband SNR as a function of the noise bandwidth under different IF frequencies. The values of f_d and $\rm SNR_{BP}$ are assumed to be 160 kHz and 14 dB, respectively. It is interesting to observe that the baseband SNR decreases rapidly with respect to noise bandwidth around 1 MHz, which is the value we concerned. Typically, the noise bandwidth is set by the channel-selection filter bandwidth. However, the channel-selection filter bandwidth is usually designed with large margin (in addition to the required IF signal bandwidth) to tolerate the transmitter frequency drift and the frequency offset between the receiver and the transmitter. Therefore, lowpass filtering following the time-to-digital conversion is essential to eliminate

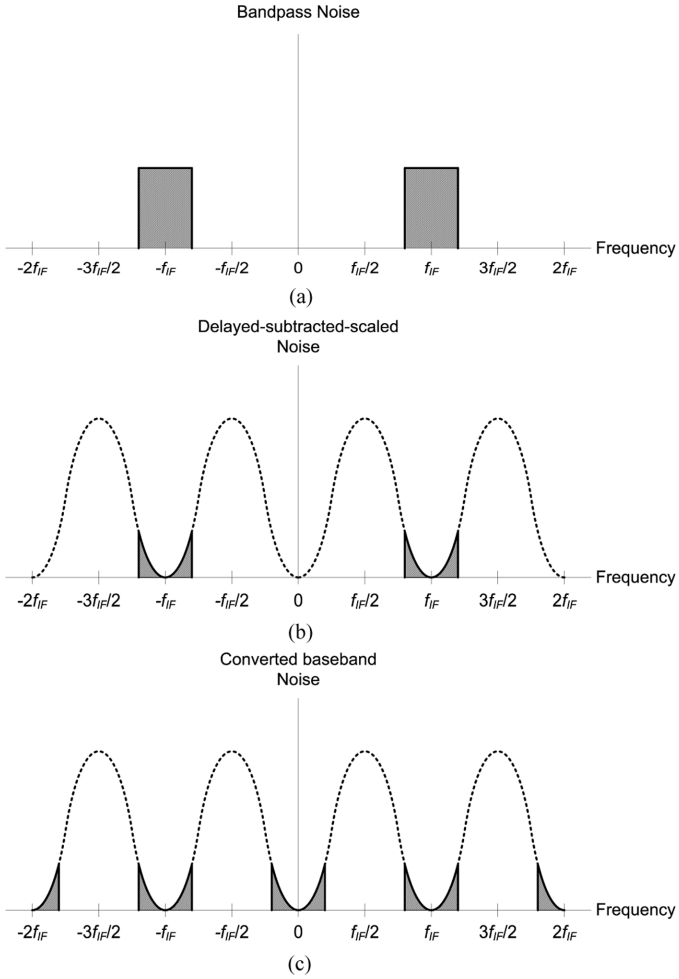

Fig. 8. PSD of: (a) original bandpass noise, (b) delayed-subtracted-scaled bandpass noise, and (c) converted baseband noise.

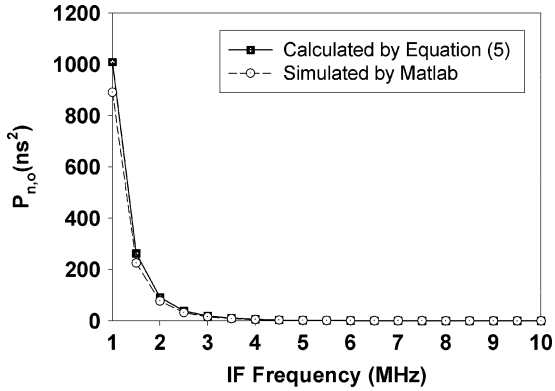

Fig. 9. Power of converted baseband noise.

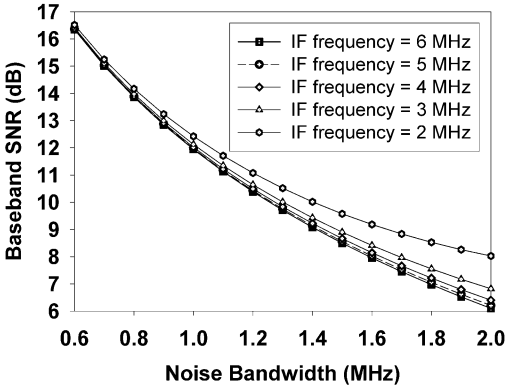

Fig. 10. Baseband SNR versus noise bandwidth.

the noise in the excess frequency band. Based on this consideration, the IF frequency needs to be selected to produce sufficient sampling rate of the baseband signal, and, therefore, an optimal digital lowpass filter can be designed. Furthermore, according to Fig. 10, since the converted baseband SNR degrades approximately only 0.5 dB when the IF frequency increases from 2 MHz to 6 MHz at around 1-MHz noise bandwidth, an IF frequency of 6 MHz is chosen to achieve a high sampling rate. This selection of the IF frequency can achieve much more robust receiver detection ability and smaller hardware implementation area at the cost of the slight increase of the power consumption.

B. Implementation

Numerous time-to-digital converters (TDCs) have been utilized in a variety of applications, such as space science, range finding, and digitally intensive PLLs [22]–[28]. In order to achieve fine resolution, most of them (excepting those used in digitally intensive PLLs) are complex and exhibit non-evitable measurement dead time. To utilize a TDC in a communication system, a long TDC measurement dead time is not allowed since the input signal period needs to be computed continuously. In our application, since a resolution of nanosecond is sufficient, techniques used to refine the TDC resolution can be avoided, so that the TDC measurement dead time can be eliminated, and the TDC complexity can be highly reduced.

Fig. 11 shows the block diagram and signal diagram of the employed TDC. The architecture is similar to the TDC employed in [25]. Zero-crossings of the input IF signal (IF2 in the presented receiver) are detected by its own delayed replicas. The delayed replicas are generated by a delay line which provides a coarse delay and several fine delays. Therefore, each replica is delayed by a period of

$$T_s(k) = \Delta T_1 + k \cdot \Delta T_2, \quad k = 0, 1, \ldots, N-1 \tag{9}$$

where ΔT_1 is a coarse delay; ΔT_2 is a fine delay; k is the index of each sampling signal; N is the number of the sampling signals. After sampling, the TDC generates a thermometer-coded $\mathrm{Q[N-1:0]}$ that represents the IF2 period. An encoder converts the thermometer code into the binary code $(\mathrm{S_{period}})$ for the following DSP circuits.

Fig. 12 shows the circuit of the auto-calibration delay line. The delay line is composed of several coarse delay cells $(\mathrm{D_C})$

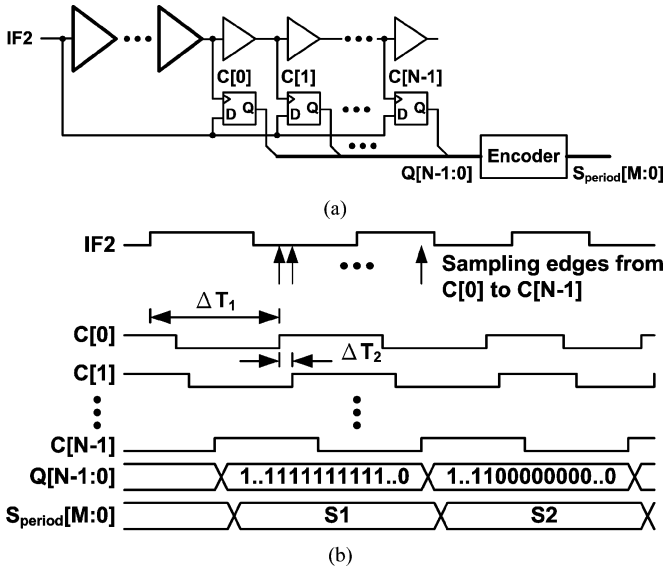

Fig. 11. (a) Block diagram and (b) signal diagram of the TDC.

and $N-1$ fine delay cells $(\mathrm{D_F})$. The utilization of the coarse delay cells helps to reduce the number of required delay cells. Therefore, a great amount of current consumption and chip area can be saved. The delay cells are constructed by source-coupled logic (SCL) gates. The first advantage provided by the SCL gates is that the differential scheme helps to mitigate delay variation caused by noise from the power supply, ground, and substrate. The second advantage is that the SCL gates allow tuning of their delays by trimming their bias currents.

In order to ensure the delay accuracy of the delay cells, an on-chip digital auto-calibration circuit is employed. The calibration is performed before the receiver starts up. During the calibration mode, a 6-MHz reference signal (FREF) is fed to the delay line through a MUX, and, at the same time, the IF2 is blocked. After a settling time, the digital TDC output $(\mathrm{S_{period}})$ is read and compared to a target value $(\mathrm{S_{target}})$. The bias currents of the delay cells are tuned according to the comparison result. After the calibration procedure is finished, the following equation can be satisfied:

$$\frac{1}{f_{\mathrm{ref}}} = \Delta T_1 + S_{\mathrm{target}} \cdot \Delta T_2 \tag{10}$$

where f_{ref} is the frequency of the reference signal. After the calibration mode, the MUX selects the IF2 and blocks the reference signal, and the demodulator starts to work at operation mode.

Advantages provided by this implementation are concluded as follows. First, the self-sampling technique performs the time-to-digital conversion by using its own delayed replicas. The advantage is that the self-sampling technique avoids edge synchronization problems [6] and exhibits low power consumption. Second, via the assistance of the auto-calibration circuit, the required delay line accuracy can be maintained under PVT variations. As a result, no analog intensive delay-locked loops (DLLs) are required, and, consequently, chip area can be significantly reduced. Third, the tolerance to IF frequency offset can be increased flexibly by extending the length of the delay line.

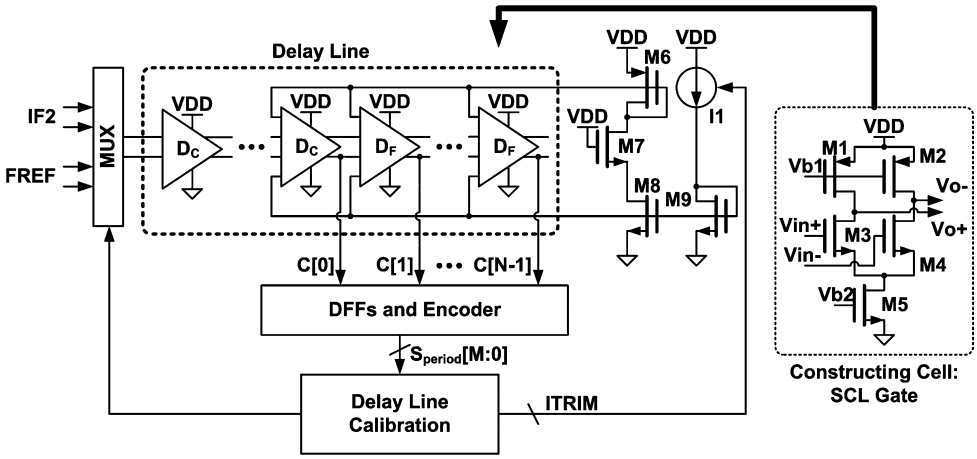

Fig. 12. Circuit of the implemented auto-calibration delay line.

C. Imperfections

The TDC quantization can contribute error to estimation of IF2 period. The quantization error of the proposed TDC is determined by the fine delay,ΔT_2. Therefore, the power of the quantization error is $\Delta T_2^2/12$. In this paper, the fine delay is designed to be 1.15 ns. This results in a SNR of 22.5 dB if (7) is used for signal power estimation, with the assumption that the values of f_d and $f_{\rm IF}$ are 160 kHz and 6 MHz, respectively. For a pulse-code modulation system, it requires 9-dB E_b/N_0 to achieve 10^{-5} error probability [29]. Therefore, the design margin can be sufficient even under serious PVT variations. Here, the criterion of 10^{-5} error probability is employed according to the BER performance floor defined by Bluetooth specification $\rm v2.0 + EDR$.

The TDC accuracy is primarily determined by the matching of the fine delays. The value of a fine delay depends on the device characteristics and the parasitic capacitances at the output of the delay cells. Due to the relaxed accuracy requirement, device mismatch set by process capability is acceptable. On the other hand, the matching of parasitic capacitances strongly depends on the layout style, which may leads to serious mismatch if an improper layout is employed. In order to reduce the parasitic capacitance mismatch, the layout has been considered carefully to ensure the same environment seen by each delay cell. Dummy cells and a layout shape of straight line are used to achieve this goal. The implementation size of all the fine delay cells is around 49 μm $\times$ 207 μm. In addition, in order to cover the possible IF2 frequency offset and PVT variation, the coarse delay is designed to be 141 ns and the number of fine delay cells is 63.

IV. Building Blocks

A. Receiver Front-End

The simplified schematic of the LNA is shown in Fig. 13. The differential scheme is selected to permit better rejection of the common-mode interference from the substrate, ground, and power supply. A constant-gm bias stabilizes the gain and input impedance over the fluctuations of the temperature and power supply. Two mixers are cascaded to perform the two-step down-conversion. The double-balanced Gilbert mixer is chosen for better LO-IF isolation and immunity of noise from the LO port. Two buffers are inserted between two mixers since the frequency of IF1 is higher than 300 MHz. The block diagram of the channel-selection filter is shown in Fig. 14. It comprises a complex bandpass filter and an automatic-tuning circuit. A fourth-order Chebyshev filter implemented by the transconductance-capacitor method is employed. In the automatic-tuning circuit, the VCO is composed of the replicas of the integrators in

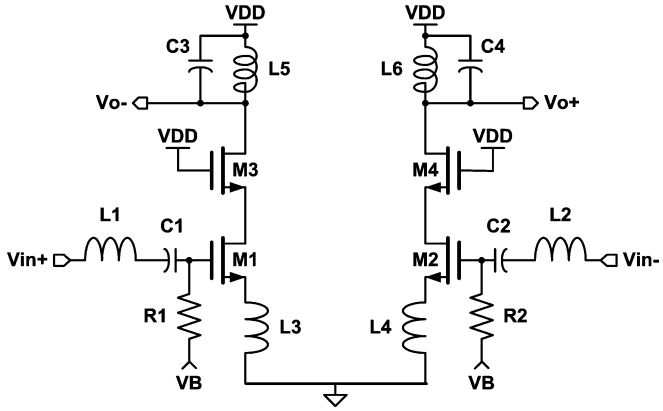

Fig. 13. Simplified schematic of the LNA.

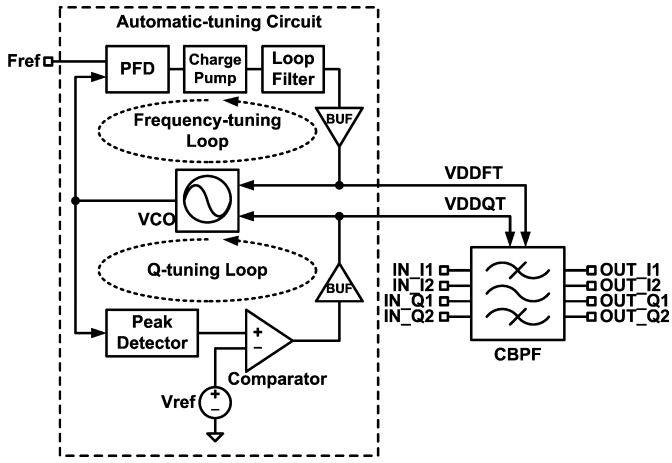

Fig. 14. Block diagram of the channel-selection filter with the automatic-tuning circuit.

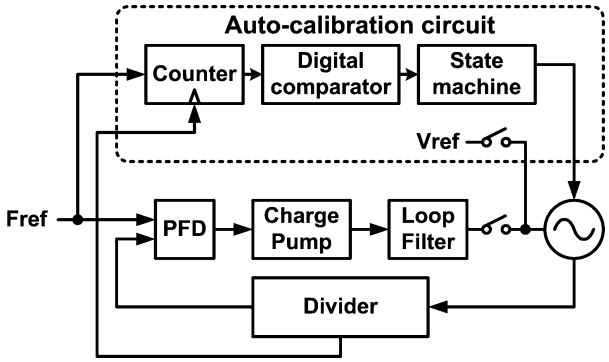

Fig. 15. Block diagram of the frequency synthesizer.

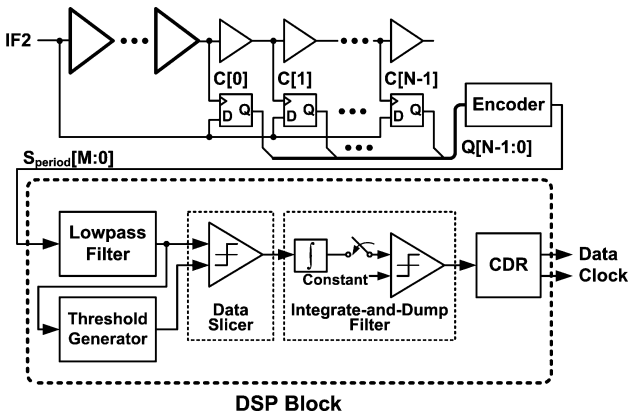

Fig. 16. Block diagram of the digital demodulator.

the complex bandpass filter. In addition to the frequency-tuning loop, a Q-tuning loop is also required. In the Q-tuning loop, the amplitude of the VCO is detected by a peak detector as a merit of the quality factor of the integrators. The detection result is compared with a reference, and, then, the comparison result is fed back to the VCO to tune the quality factor of the integrators in the VCO and the complex bandpass filter simultaneously. The overall voltage gain of the receiver front-end is 45 dB, and the noise figure is 7.5 dB.

B. Frequency Synthesizer

Fig. 15 shows the block diagram of the frequency synthesizer. The synthesizer is based on an integer-N PLL. Due to the dual-conversion architecture of the receiver, the VCO frequency tuning range must cover the entire 2.4-GHz ISM band and LO1 frequency range. Such large tuning range requires an excessively large VCO gain, which can raise phase noise, spurious tones, and frequency drift during open-loop modulation. To mitigate these problems, the required VCO frequency range is divided into several bands. The optimal band is determined by the VCO auto-calibration circuit.

The calibration circuit is a digital frequency-locked loop (FLL) containing a high-speed counter, a digital comparator, and a state machine for procedure control. When the frequency synthesizer enters the auto-calibration procedure, the PLL is opened, and the FLL starts to work. A fixed voltage is connected to the control voltage of the VCO. A reference signal (Fref) and a clock generated by dividing LO1 by 8 are fed to the high-speed counter, which acts as a frequency detector. According to the frequency detection result, the FLL adjusts the digital control bits from the state machine to tune the VCO frequency until the frequency is locked.

C. Digital Demodulator

Fig. 16 depicts the block diagram of the demodulator based on the proposed TDC. The TDC converts the limiter output signal into digital codes that represent the IF2 period. A DSP block follows to process the digital signal. It contains a lowpass filter, a threshold generator, a data slicer, an integrate-and-dump filter, and a clock/data recovery circuit (CDR). The lowpass filter implemented by a moving-average filter helps to further suppress noise. The threshold generator detects peaks and valleys of the lowpass filter output to generate a decision threshold for the following data slicer. Moreover, the threshold generator can track and cancel time-varying DC offset caused by the transmitter frequency drift. The data slicer compares the baseband signal with the decision threshold to generate raw data. There are 12 decisions in a bit duration, and glitches appear in the raw data when error decisions occur. The integrate-and-dump filter subsequently performs majority vote to remove these glitches. Finally, the CDR generates the corresponding 1-MHz clock and retimes recovered output data.

Frequency offset cancellation is an important design consideration for GFSK receivers since frequency offset can degrade demodulation performance significantly. To remove frequency offset, a peak-valley detection algorithm is built into the threshold generator. Fig. 17(a) shows the details of the peaks and valleys detection. Eight samples of the moving-average filter output (M0–M7) are observed simultaneously to detect peaks or valleys. If $M7 \geq M6 \geq M5 \geq M4 \geq M3 \geq M2 < M1 \leq M0$, M2 is a valley; if $M7 \leq M6 \leq M5 \leq M4 \leq M3 \leq M2 > M1 \geq M0$, M2 is a peak. Fig. 17(b) shows the generation and updating of the decision threshold. When a sequence of interlaced peaks and valleys are detected, the decision threshold is calculated. Moreover, to eliminate the effect of frequency drift, the decision threshold is updated whenever the same data pattern occurs.

The block diagram of the CDR is shown in Fig. 18. A digital PLL architecture is employed to implement the CDR. A divide-by-16 circuit is used to divide a 16-MHz reference clock to generate 16 1-MHz clocks, which are separated by one-sixteenth of the clock period from each other. A phase detector detects the input data phase. The phase estimator follows to decide the optimal phase and control a phase selector to select the phase for the recovery clock. Finally, a D flip-flop is used to retime the output data according the recovery clock. In order to increase the lock speed, the phase change step is not limited at the initial state. After the initial phase is determined, only the adjacent phases can be selected, so as to minimize the clock jitter.

Since the DSP block needs no calculation-intensive functions, the implementation complexity can be reduced in comparison with that of the DSP blocks required by conventional digital demodulators [5], [30].

V. Experimental Results

The proposed transceiver has been fabricated in a standard 0.18-μm CMOS technology. Fig. 19 shows its chip microphotograph. The chip has a total area of 4 mm^2, including its pad

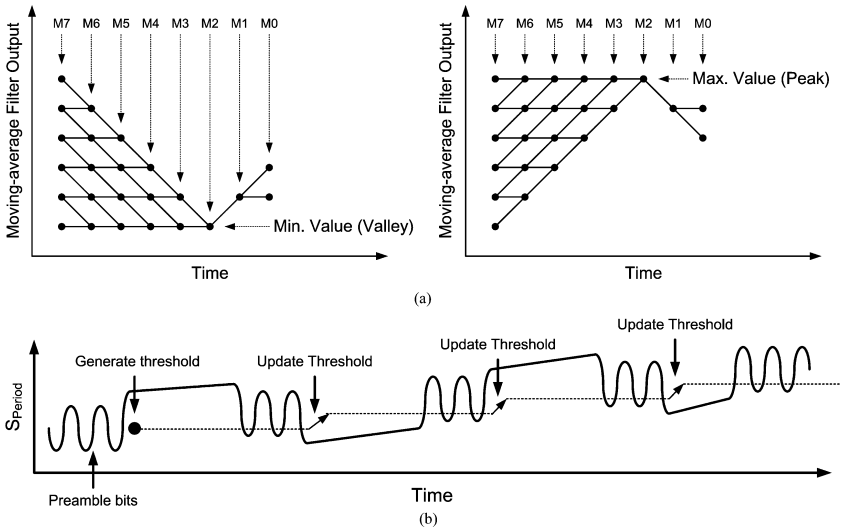

Fig. 17. (a) Detection of peaks and valleys of the moving-average filter output. (b) Generation and updating of the decision threshold.

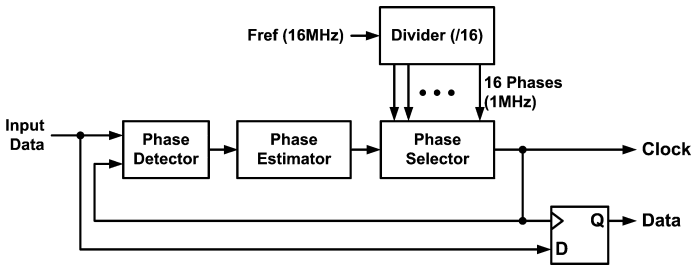

Fig. 18. Block diagram of the CDR.

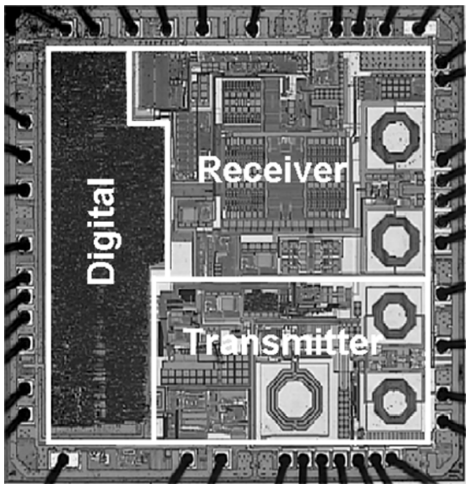

Fig. 19. Chip microphotograph.

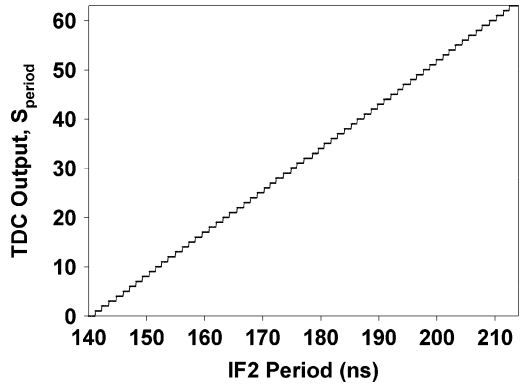

Fig. 20. Measured TDC transfer function.

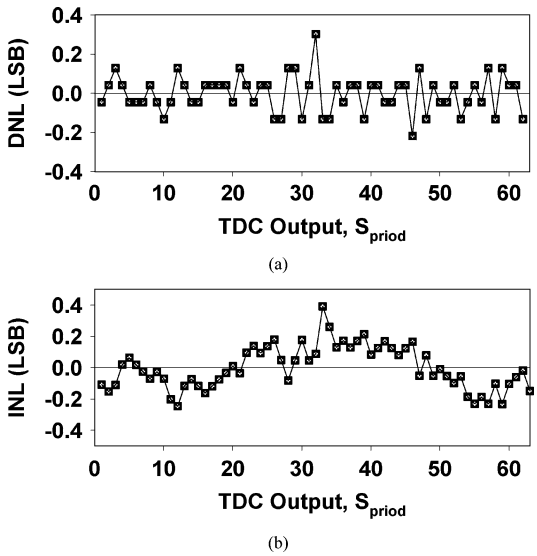

Fig. 21. (a) Measured TDC DNL. (b) Measured TDC INL.

area, and is packaged in a 20-pin QFN chip carrier. All pins can achieve 4-kV and 400-V ESD protection robustness under the human-body model and the machine model, respectively. Most data presented were measured at room temperature, but the transceiver has been verified to be able to function consistently over the temperature range of -40–85°C. The frequency deviation is set to be ± 160 kHz.

Fig. 20 shows the measured TDC transfer function. Fig. 21(a) and (b) show the curves of the measured TDC differential nonlinearity (DNL) and integral nonlinearity (INL), respectively, where the best-fit straight line is used. The maximum DNL and INL are 0.3 and 0.4 least significant bit (LSB), respectively, which are quite sufficient for our application.

Fig. 22 shows the measured demodulator BER versus input SNR. The demodulator only requires an input SNR of 13.9 dB

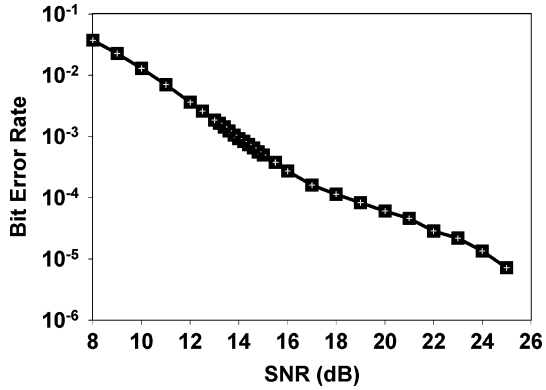

Fig. 22. Measured demodulator BER versus input SNR.

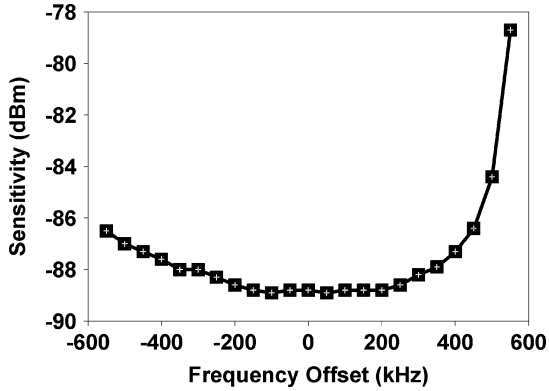

Fig. 24. Measured receiver sensitivity versus frequency offset.

TABLE I
COMPARISON TO PRIOR PUBLISHED GFSK DEMODULATORS FOR BLUETOOTH

Work	Required SNR	Co-channel C/I	Current consumption	Chip area
[31]	18.0 dB	12.0 dB	3.0 mA @ 2.7 V	N.A.
[2]*	17.5 dB	N.A.	27.7 mA @ 1.8 V	5.60 mm^2
[4]	16.2 dB	11.2 dB	3.0 mA @ 3 V	0.70 mm^2
[32]	15.7 dB	9.0 dB	N.A.	N.A.
[33]	16.5 dB	N.A.	3.0 mA @ 2 V	0.30 mm^2
This work	13.9 dB	9.1 dB	2.55 mA @ 1.8 V	0.26 mm^2

*The filter and limiter are included.

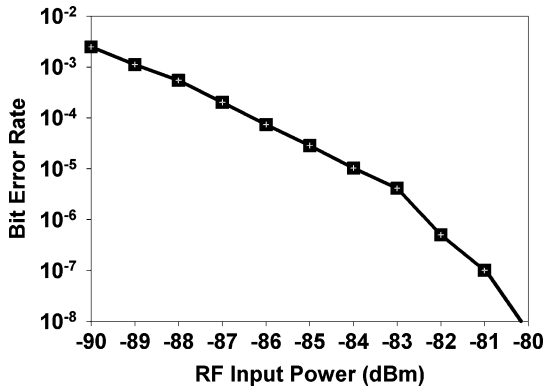

Fig. 23. Measured receiver BER versus RF input power.

TABLE II
PERFORMANCE SUMMARY

Technology	0.18-μm CMOS
Chip size	1960 μm × 2040 μm
Sensitivity	−89 dBm @ 0.1% BER
RX C/I co-channel	9.1 dB
RX C/I 1 MHz	3.3 dB
RX C/I 2 MHz	−25.3 dB
RX C/I 3 MHz	−40.5 dB
RX C/I image	−30.0 dB
TX output power	0 dBm
PLL lock time	94 μs
LO phase noise	−88 dBc/Hz @ 100-kHz offset
RX current consumption	13.3 mA
TX current consumption	10.7 mA @ 0-dBm output power

TABLE III
CURRENT CONSUMPTION OF EACH BLOCK

Receiver	
LNA+mixers	2.39 mA
IF section (channel-selection filter, Limiter, RSSI, RSSI ADC)	2.28 mA
Demodulator	2.55mA
Frequency synthesizer (also including buffers)	4.75 mA
Others (Regulator, Bandgap, bias, …)	1.30 mA
Transmitter	
PA	6.40 mA
Modulator (also including DAC, filter)	0.46 mA
Frequency synthesizer	2.58 mA
Others (Regulator, Bandgap, bias, …)	1.30 mA

to achieve 0.1% BER. Co-channel interference rejection is also measured by adding another GFSK-modulated interference into the input signal. The demodulator can achieve 9.1-dB co-channel interference rejection. It consumes only 2.55 mA and occupies 0.26-mm^2 chip area. Table I compares the performance of the proposed demodulator to prior published demodulators for Bluetooth.

Fig. 23 shows the measured receiver BER with different RF input power. The sensitivity can achieve -89 dBm at 0.1% BER with 1-Mb/s data rate. The maximum usable RF input power exceeds 0 dBm. Fig. 24 shows the measured receiver sensitivity at 0.1% BER versus frequency offset.

The measured overall frequency tuning ranges of the VCO are 2.256–3.047 GHz and 2.093–2.707 GHz in the receiver and the transmitter, respectively. For the sake that each required frequency range is divided into 32 sub-ranges, the VCO gain are adequate, which are approximately 178 MHz/V and 131 MHz/V in the receiver and the transmitter, respectively. The LO phase noise is -88 dBc/Hz at 100-kHz offset. The measured PLL lock time is 94 μs.

The transmitter frequency drift and frequency deviation are measured over the specified temperature range. The measured transmitter frequency drift is better than -58 kHz at the moment of 4 ms after the open-loop modulation starts. The frequency deviation is greater than ± 115 kHz with the 1010 data sequence and $\pm 145 - \pm 170$ kHz with 00001111 data sequence. The transmitter output power at the typical condition is 0 dBm. Table II presents a summary of the experimental results. Table III lists the current consumption of each block.

VI. Conclusion

A fully integrated GFSK low-power transceiver fabricated in a 0.18-μm CMOS technology is presented. A digital demodulator is designed with the technique of time-to-digital conversion. The demodulator requires only 13.9-dB input SNR to achieve 0.1% BER with 2.55-mA current consumption. With this demodulator, the architecture of the receiver is simplified, and the receiver achieves -89-dBm sensitivity. A dual-conversion structure is also utilized in the receiver design to further reduce the current consumption and provide better matching between the quadrature LOs. The transmitter employs the architecture of open-loop VCO modulation. With these techniques, the current consumption is 13.3 mA in the receiver and 10.7 mA in the transmitter.

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