TCAD/Physics-Based Analysis of High-Density Dual-BOX FD/SOI SRAM Cell With Improved Stability

Keunwoo Kim, *Senior Member, IEEE*, Jente B. Kuang, *Senior Member, IEEE*, Fadi H. Gebara, Hung C. Ngo, Ching-Te Chuang, *Fellow, IEEE*, and Kevin J. Nowka, *Senior Member, IEEE*

Abstract—This paper presents a new SRAM cell using a global back-gate bias scheme in dual buried-oxide (BOX) FD/SOI CMOS technologies. The scheme uses a single global back-gate bias for all cells in the entire columns or subarray, thereby reducing the area penalty. The scheme improves 6T SRAM standby leakage, read stability, write ability, and read/write performance. The basic concept of the proposed scheme is discussed based on physical analysis/equation to facilitate device parameter optimization for SRAM cell design in back-gated FD/SOI technologies. Numerical 2-D mixed-mode device/circuit simulation results validate the merits and advantages of the proposed scheme.

Index Terms—FD/SOI device, mix-mode simulator, read stability, substrate bias.

I. INTRODUCTION

SRAMS ARE key components in processor and SoC applications. Due to the increased portion of SRAM arrays in the total chip area, device dimensions in SRAM must be continuously scaled. SRAM cells use very short channel and narrow-width devices under the simultaneous constraints of stringent design rule, tight physical pitch, and cell aspect ratio determined by internal device beta-ratio and bit-line (BL) timing requirement. Consequently, the intrinsic device fluctuations and random mismatch among adjacent devices increase significantly due to random dopant fluctuations (RDFs), line-edge roughness, short-channel effects (SCEs), and narrow-width effects. Thus, the stability of SRAM degrades with technology scaling. The RDF is a major source of variation for SRAM. The use of lightly doped or undoped body in FD/SOI and FinFET devices significantly reduces the RDF effect. The RDF effect can be further mitigated with back-gate biasing to modulate V_T and reduce SCE in FD/SOI and FinFET devices [1]–[3]. However, individual back-gating schemes add process complexities and significantly degrade SRAM density

[4], [5]. In independent-gate controlled FinFET technologies, the limit and quantization of fin height significantly increase the area, particularly in multiple-fin devices [4]–[6]. In back-gated FD/SOI technologies, fabrication of self-aligned back gate is a formidable technology task [5]. Furthermore, a thin buried oxide (BOX) is needed for effective back-gate biasing, which increases the BL capacitance and degrades the read/write performance of SRAM. The advanced body-bias controlled SOI SRAM and a thin BOX SOI with a single metal gate were reported [7], [8].

This paper presents a novel back-gate bias scheme to achieve the desired selective back gating in dual-BOX FD/SOI CMOS technologies. The proposed scheme minimizes the area overhead compared with other back-gate biasing schemes to facilitate a very dense cell layout. The standby leakage, read static noise margin (RSNM), write ability, and read/write performance can be significantly improved without degrading leakage/dynamic power and area/density. Two-dimensional mixed-mode TCAD simulations [9] using physical models validate the merits of the proposed scheme and illustrate the advantages over conventional schemes.

II. PROPOSED SELECTIVE BACK-GATE BIAS SCHEME

In FD/SOI devices, wide-range V_T can be offered by the back-gate bias due to the electrical coupling of front and back gates through the depleted body in thin Si film and thin BOX structures [10]. The effect improves with device scaling due to stronger gate-to-gate coupling with thinner Si film and/or thinner gate oxides [10]. As reported in [10] and [11], the physical equation for the threshold voltage (V_T) of FD/SOI devices with depleted body can be written as

$$V_T = V_{T0} - rV_{BG} \qquad (1)$$

where V_{T0} is the V_T when the back-gate voltage (V_{BG}) is grounded and r is a gate–gate coupling factor which can be expressed as

$$r = ((\varepsilon_{Si}/\varepsilon_{ox})T_{ox}) / ((\varepsilon_{Si}/\varepsilon_{BOX})T_{BOX} + T_{Si}) \qquad (2)$$

where ε_{ox}, ε_{BOX}, ε_{Si}, T_{ox}, T_{BOX}, and T_{Si} are the permittivities and thicknesses of front-gate oxide, back-gate oxide, and Si film, respectively [10], [11]. Fig. 1(a) shows the conventional FD/SOI device structure. The V_T modulation effect is very
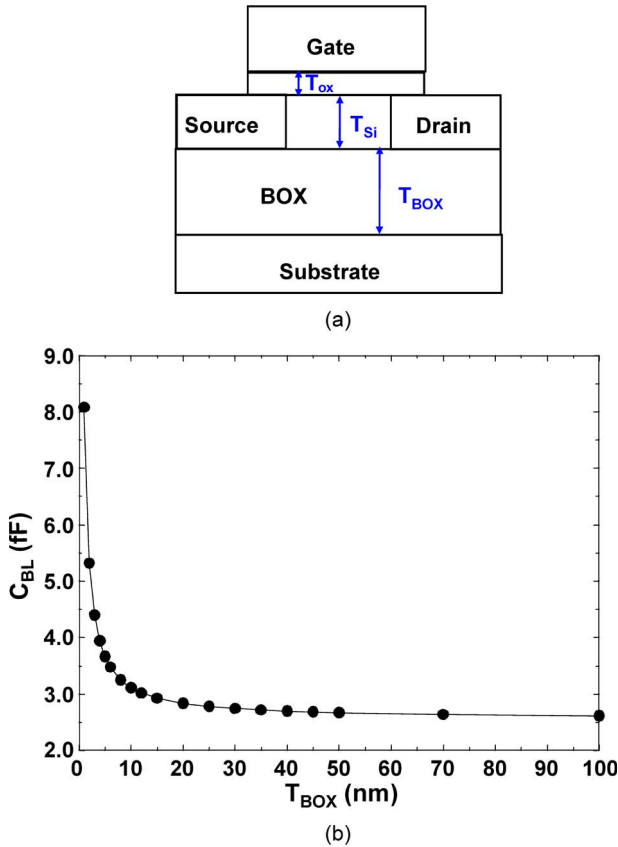
Fig. 1. (a) Conventional SOI structure. (b) MEDICI-predicted $C_{\rm BOX}$ versus $T_{\rm BOX}$ characteristics.

Fig. 2. (a) Proposed FD/SOI device. (b) 6T SRAM structures with dual BOX.

significant with thin $T_{\rm BOX}$. As $T_{\rm BOX}$ increases, the gate–gate coupling [r in (2)] is reduced, and larger $V_{\rm BG}$ is required to achieve a noticeable modulation of V_T. We used a 2-D device/circuit simulator (MEDICI) [9] for an SRAM column having 16 cells for brevity, considering wire and device parasitics. Fig. 1(b) shows the MEDICI-predicted $C_{\rm BOX}$ versus $T_{\rm BOX}$ characteristics [10], [11]. With thin $T_{\rm BOX}$, the BOX capacitance $C_{\rm BOX}$ $(= \varepsilon_{\rm ox}/T_{\rm BOX})$ increases. The BL capacitance $(C_{\rm BL})$ is an important factor of SRAM read/write delay (e.g., $\tau_{\rm Read} = C_{\rm BL}/I_{\rm Read}$, where $I_{\rm Read}$ is the read current though the cell access and pull-down devices). $C_{\rm BL}$ can be expressed as $C_{\rm BL} = C_{\rm wire} + C_{\rm BOX} + C_{\rm ov} + C_j$, where $C_{\rm wire}$ is the BL wire capacitance, $C_{\rm ov}$ is the gate-to-drain overlap capacitance of the access devices, and C_j is the drain-to-body junction capacitance of the access device. Therefore, thin BOX for the access nFETs increases the BL capacitance due to increased $C_{\rm BOX}$, while thin BOX for the pull-up pFETs does not add capacitance to the BLs.

We propose a new FD/SOI device structure and a 2-D array structure of SRAM cells with dual BOX as shown in Fig. 2. Thick BOX is used for nFETs, thus reducing the BL capacitance to enhance the read/write performance. Thin BOX is used for pFETs, thus allowing adaptive back-gate bias to optimize standby leakage, read/write margin, and write performance. The scheme employs a single global back-gate bias to reduce the area overhead. Selective back-gating capability is achieved through the use of dual BOX. The back-gate bias has essentially no effect on nFETs due to their thick BOX [as shown in
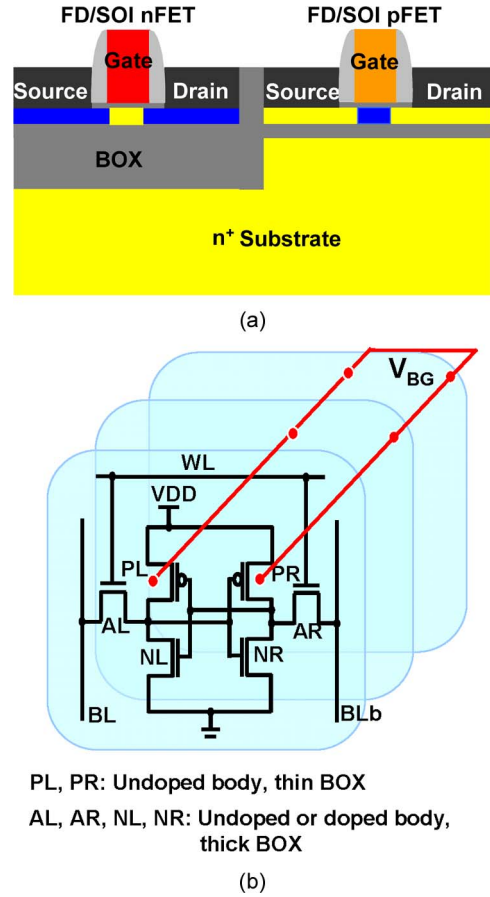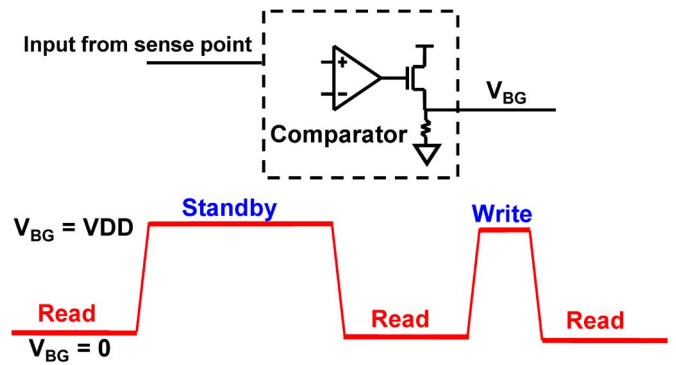

Fig. 3. Global back-gate bias control method.

Fig. 1(b)], while pFETs experience significantly V_T modulation due to their thin BOX. This "selective" back-gating effect can be exploited to improve the standby leakage, RSNM, write ability, and write performance of SRAM.

The use of undoped body for pFET reduces RDF effects and facilitates effective back-gate biasing. For nFET, a doped body is preferred as it reduces the sensitivity to the back-gate bias. The use of a common back-gate bias for nFETs and pFETs of cells in the entire columns or subarray results in a very dense layout. Fig. 3 shows the global back-gate bias control method. In standby mode, the back-gate voltage ($V_{\rm BG}$) is set to "High" to increase V_T of pFETs, thereby reducing the leakage current.
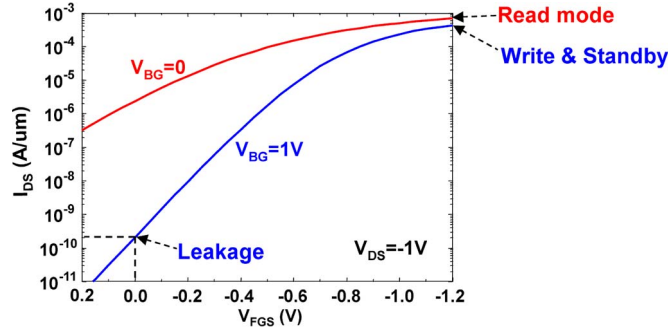
Fig. 4. MEDICI-predicted I_{DS}–V_{GS} characteristics at $V_{DS} = -1.0$ V with varying V_{BG} in the proposed FD/SOI pFET.

The trip voltage (V_{trip}) of the cell inverter (i.e., the switching voltage of the state) can be physically derived as

$$V_{trip} = \frac{V_{T(n)} + \frac{v_{sat(p)}W_p}{v_{sat(n)}W_n}\left(V_{DD} + V_{T(p)}\right)}{1 + \frac{v_{sat(p)}W_p}{v_{sat(n)}W_n}} \quad (3)$$

where $V_{T(n)}$ and $V_{T(p)}$ are the threshold voltages of nFET and pFET, $v_{sat(n)}$ and $v_{sat(p)}$ are the saturation velocities of nFET and pFET, and W_n and W_p are the device widths of nFET and pFET [12], [13]. Higher V_{trip} improves the SNM. During read operation, V_{BG} is set to "Low" (i.e., grounded on the substrate) to reduce V_T of pFETs and skew/raise V_{trip}, thereby improving the read stability. The read delay is determined by the pull-down nFET and access nFET and is not affected. In write operation, V_{BG} is set to "High" to increase V_T of pFETs, thereby improving the write ability and write performance. Note that the proposed scheme suffers no area/performance penalty in FD/SOI technology while improving the standby leakage, read stability, write ability, and write performance.

III. ANALYSIS OF PROPOSED SCHEME

The proposed scheme is analyzed using MEDICI [9] based on 45-nm FD/SOI devices with parameters and performance consistent with ITRS roadmap [14]. The "conventional" FD/SOI device has a gate length of 25 nm, front-gate oxide thickness of 1 nm, BOX thickness of 100 nm, and doped $(5 \times 10^{18} \text{ cm}^{-3})$ Si film thickness of 10 nm. For the proposed scheme, all cell nFETs, including pull-down and access devices, are the same as those in the conventional thick BOX FD/SOI devices. However, pull-up pFET devices have thin BOX $(T_{BOX} = 10 \text{ nm})$ and undoped body, and other device parameters are the same $(T_{ox} = 1 \text{ nm}$ and $T_{Si} = 10 \text{ nm})$ as the conventional case. Fig. 4 shows the MEDICI-predicted I_{DS}–V_{GS} characteristics of the proposed FD/SOI pFET at $V_{DS} = -1.0$ V for $V_{BG} = 0$ and 1.0 V. With $V_{BG} = 0$ V, I_{ON} can be increased by 2.14 times due to the significantly reduced V_T. In read mode, stronger pFET is preferred as it increases the cell inverter trip voltage, thus improving the read stability. In write operation, V_{BG} is switched to "V_{DD}" to increase V_T of pFETs, thereby improving the write ability and write performance. In standby mode, V_{BG} stays at V_{DD} to reduce the leakage current. Note that, due to the use of very thick BOX in
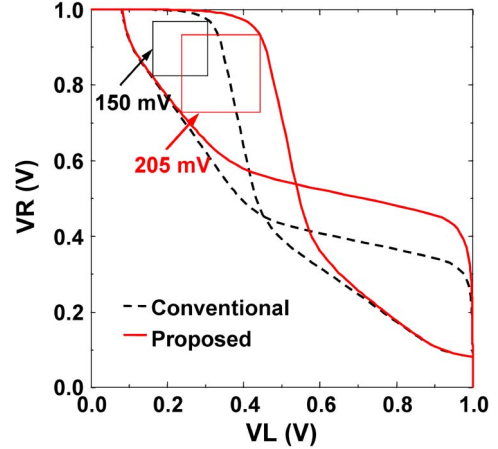

Fig. 5. MEDICI-predicted RSNM for the proposed and conventional schemes.

nFETs for the proposed scheme, the V_{BG} will not change all nFETs in the cell.

To demonstrate and validate the advantages of the scheme, mix-mode device/circuit simulations are performed. Fig. 5 shows MEDICI [9]-predicted RSNM for the conventional and proposed schemes. The terminology "conventional" (counter) that we used means the circuit technique without using the back-gate biasing method and dual-BOX technology. The RSNM for the proposed scheme is significantly improved (205 mV versus 150 mV for the conventional counterpart) due to the reduced V_T of pFETs, which increases the trip voltage of cell inverters. Notice that the mixed-mode feature of MEDICI simulator was used without any combination with external circuit simulator (such as SPICE) and/or model/equation/table-based approach [6]. With the circuit analysis advanced application module of MEDICI, we are able to embed multiple numerical device simulations within a single SPICE-like circuit simulation. In the module, the Kirchhoff equations describing the circuit and the semiconductor equations describing the devices are solved as a coupled set [6], [9]. Therefore, mix-mode device/circuit simulations can capture specific device physics of each transistor in the circuit.

The read stability of the proposed scheme is quite immune to variations of T_{Si} and T_{BOX}. Figs. 6 and 7 show TCAD-simulated results for RSNM with 20% variation of T_{Si} and T_{BOX} for the proposed scheme. As T_{Si} decreases, the pFET V_T increases due to the reduced SCEs. On the other hand, the back-gate bias has more significant V_T modulation/reduction effect for thinner T_{Si} as shown in the physical equations (1) and (2). Hence, the back-gate bias reduces the sensitivity of V_T to T_{Si} variation. Similarly, as T_{BOX} decreases, V_T increases due to the reduced drain fringing field from BOX to the region underneath the channel, while the back-gate bias becomes more effective as shown in (1) and (2) and in Fig. 1(b). Thus, the back-gate bias also reduces the sensitivity of V_T to T_{BOX} variation. Our study illustrates that the proposed SRAM cell can be very stable against the major sources of FD/SOI device variations such as RDF, T_{Si}, and T_{BOX}.

It is indicated that the undoped Si body is theoretically ideal in the nanoscale double-gate technology [15]. However, such a design is unwieldy in present and upcoming technologies due
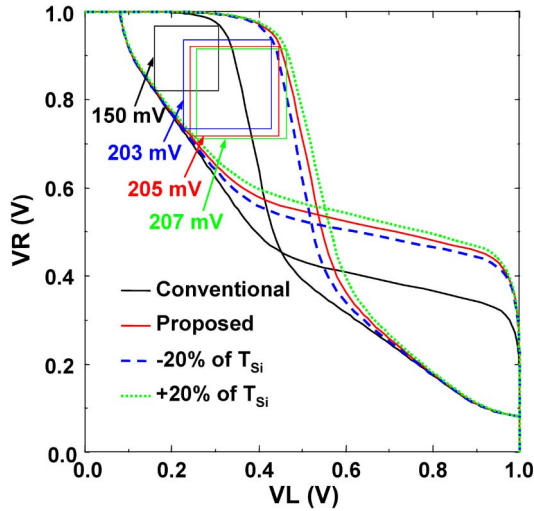
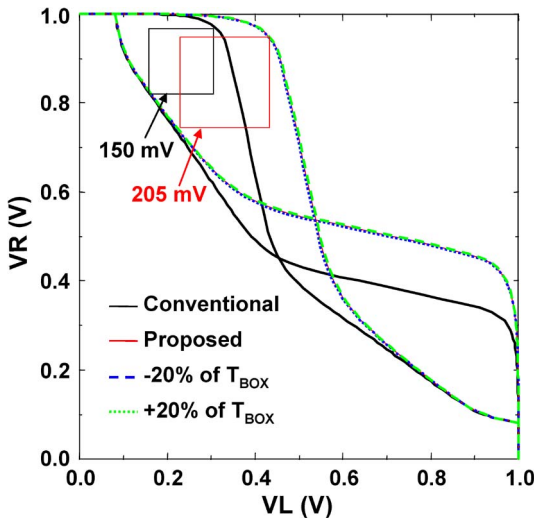Fig. 6. MEDICI-predicted RSNM for the proposed scheme with 20% variation of T_{Si}.
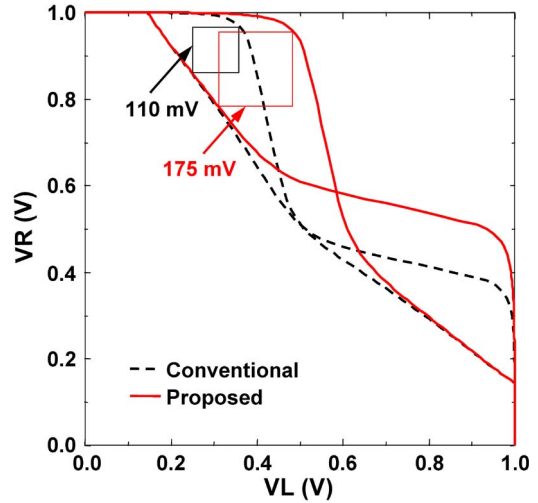

Fig. 8. MEDICI-predicted RSNM for the proposed and conventional schemes with 40% variation of N_{body} of the pass-gate and pull-down devices in the worst case stability corner (where N_{body} is 3×10^{18} cm^{-3} for a pass-gate device and 7×10^{18} cm^{-3} for a pull-down device).

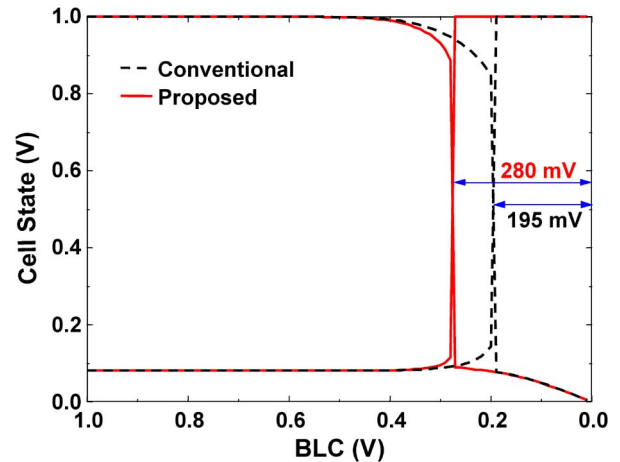Fig. 7. MEDICI-predicted RSNM for the proposed scheme with 20% variation of T_{BOX}.

Fig. 9. MEDICI-predicted write margin for the proposed and conventional schemes.

to the gate-material issue/integration for proper V_T. Note that, even in the undoped silicon channel, RDF effects are still significant particularly in narrow-width devices used in SRAM cells [16]. We analyze the conventional and proposed schemes with 40% variation of body-dopant density in pull-down and access devices in the worst case corner. Fig. 8 shows the MEDICI-predicted RSNM for the conventional and proposed schemes. The RSNM for the proposed scheme is significantly improved (175 mV versus 110 mV for the conventional counterpart). Note that the relative improvement becomes larger under the RDF effect compared with Fig. 5. Note also that RSNM of the proposed scheme under the RDF effect is even higher than that of the conventional scheme without RDF effect. This indicates that the proposed scheme can be more beneficial as variations of device and process are more significant.

We have studied other significant factors in SRAM circuits which are write ability, leakage power, and access time. Fig. 9 shows the MEDICI-predicted write margin comparisons for the conventional and proposed schemes. Write margin can be esti-

mated as maximum BL voltage that can flip the cell for $BL_b = V_{DD}$. It is observed that a very noticeable improvement (42.5%) can be achieved by the proposed scheme due to the reduced I_{DS} for pull-up pFET by the back-gate control during write operation as shown in Fig. 3. In the standby mode, the leakage current of pull-down pFETs is reduced for the proposed scheme, and it is estimated that 33% of leakage power saving can be achieved in the entire SRAM cells. The access time for SRAM circuits can be estimated as in (4), shown at the bottom of the next page, where V_{BL} and C_{BL} are the BL voltage and capacitance, N_{row} is the number of rows in a column, C_{wire}, C_{BOX}, C_{ov}, and C_j are wire, BOX, overlap, and junction capacitances, $C_{input(access)}$ is the input capacitance of the accessed device, and $I_{ON(access)}$ is the ON-state current of the accessed device [12]. From equation (4), the estimation of C_{BL} in Fig. 1(b), and typical values for other capacitances, we can evaluate 19% lower T_{cell} when 16 cells are in a column for the proposed scheme, compared with the conventional counterpart. Hence,
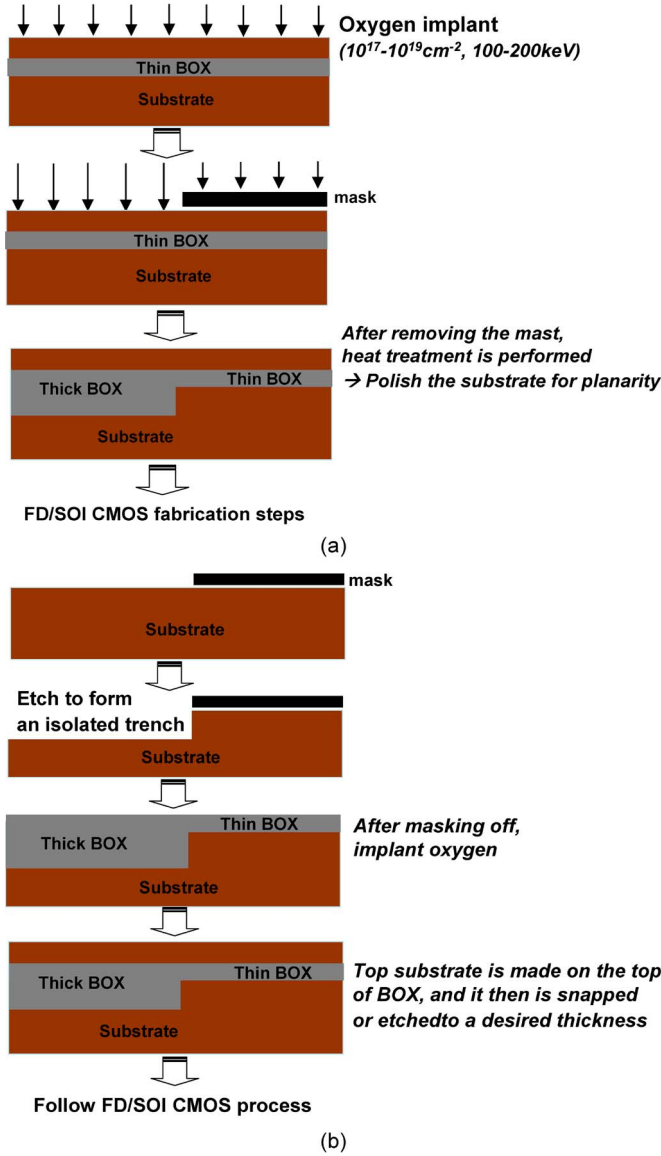
Fig. 10.   Two examples of simplified process flows for dual-BOX SOI structure [17].

the proposed selective back-gate bias technique can improve the standby leakage, read stability, write ability, and access delay.

IV. IMPLEMENTATION AND LAYOUT OF PROPOSED SCHEME

Process methods to fabricate dual-BOX SOI devices have been reported previously [17]. Fig. 10(a) and (b) shows examples of the basic process flow to form a dual-BOX SOI substrate. As shown in Fig. 10(a), first oxygen ions are implanted into the substrate to form a first continuous layer of oxide under the surface of the substrate. Then, a photoresist mast pattern is formed on the surface of the substrate where a thin BOX is

desired, and second higher energy oxygen ions are implanted into the region where a thick BOX is desired. After removing the mask, heat treatment is performed, followed by polishing to planarize the substrate. An alternative example is shown in Fig. 10(b). First, a mask is formed over the substrate, and etching process is performed to make isolated trenches (for the thick BOX regions). Then, after masking off, the trenches are filled with oxide. The surface is then planarized. The top substrate can then be made on the top of the BOX (e.g., through bonding process) and etched (thinned) down to the desired (silicon film) thickness. As described in the two process flows, the dual-BOX structure can be realized with a traditional BOX process with the additional steps. Notice that the thickness control of the thin BOX is crucial for adequate back-gate control, whereas the thickness control of the thick BOX is quite forgiving as long as it is thick enough to suppress the gate-to-gate coupling. Thus, the process needs to be optimized only for the thin BOX.

We adapt thin BOX pFETs and thick BOX nFETs for the proposed scheme. In the selective biasing method of the proposed scheme, the regulator for the back-gate bias can be implemented with divider, bandgap reference, or constant g_m-bias method. The appropriate output supply level (VGND or VVDD) can be selected for each mode using a voltage MUX such as design examples shown in [18] and [19]. Note that peripheral circuits [12] can also benefit from the back-gate bias-assisted V_t reduction. The final stages of word-line drivers are usually quite large in the traditional SRAMs because of the many SRAM cells on the word line and long wires. Word-line timing is usually one of the critical paths in typical array designs. The availability of modular V_T control allows us to use small device sizes and achieve a more compact layout, thereby improving the overall array area efficiency, in additional to the improved active and standby power efficiency. During standby, power-down, or low-performance modes, the higher V_T setting can be employed to minimize leakage power. Word and bit decode circuits, which select respective word lines or bit columns, are timing critical but usually do not occupy very large peripheral area. These circuits can be left at high current mode all the time without additional overhead of back-gate control circuitry. Since V_T matching is important for sense amplifiers, common centroid layout style and symmetry (i.e., analog style layout) [12] are required for best circuit performance for both front and back gates (to reduce the sensitivity of V_T and I_{DS} to process variations). It is suggested that the entire readout circuit block can be put in one common back-gate enclosed region.

Note also that the assist circuit that controls the subarray back gates is required to synchronize with the word-line high period. It is desirable to apply the assist technique in a fine-grained fashion [12], i.e., the assist mode is only enabled for the active subarrays where the local BL is selected. This reduces the power overhead when write assist is applied. Since the

$$T_{\text{cell}} \cong \frac{V_{\text{BL}}\left(C_{\text{BL}} + (N_{\text{row}} - 1)(C_{\text{wire}} + C_{\text{BOX}} + C_{\text{ov}} + C_j) + C_{\text{input(access)}}\right)}{I_{\text{ON(access)}}} \qquad (4)$$
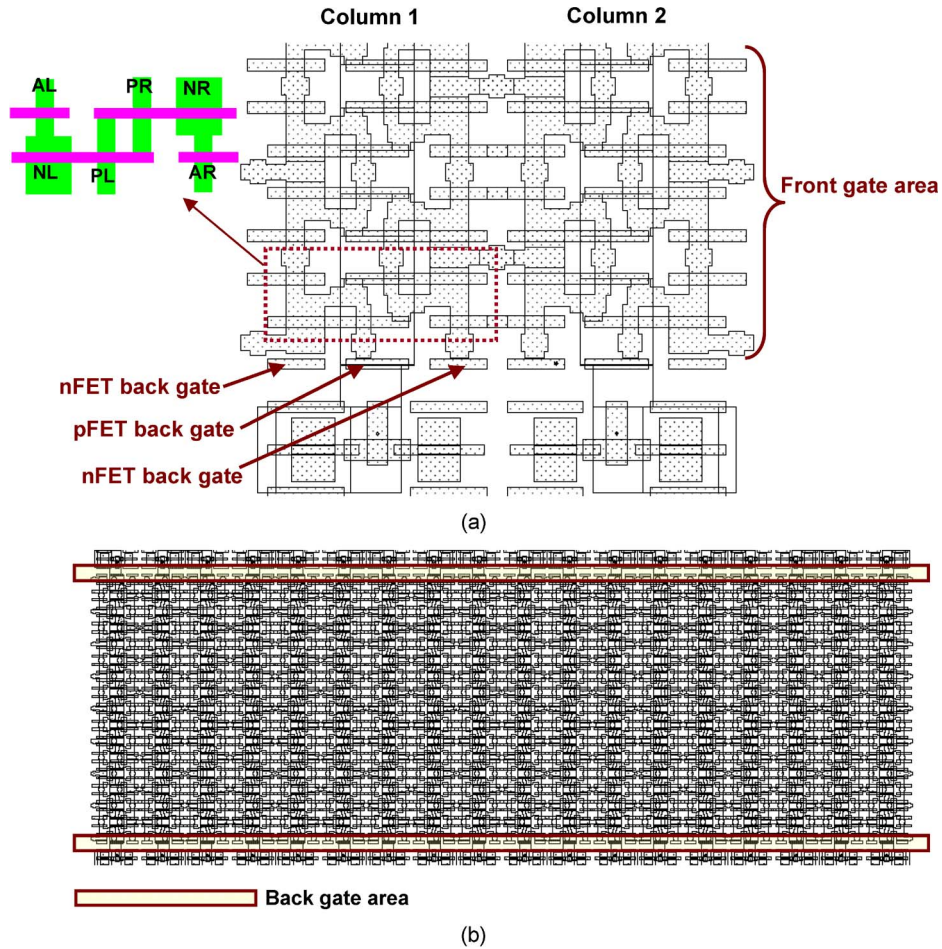
Fig. 11. Proposed SRAM layout at the edge of (a) two columns and (b) subarrays; the cell layout is inserted in (a).

subarray bank (seeing the common local BL for each column) is the natural granular building block for each assist region, only one assist control circuit is needed, which would reside alongside the sense amplifier (or the equivalent local evaluation circuit for the large-signal domino design style) and timing interlocked with the sense amplifier. We estimate the area overhead to be comparable to the front-gate style assist control circuit. The overall assist circuit area penalty should not exceed 10% of the peripheral circuit area to maintain array efficiency competitiveness. The area penalty is less for arrays with longer access time because the assist circuit on/off slew rate is more relaxed; therefore, driver size and timing requirement are more relaxed as well.

Fig. 11(a) and (b) shows the SRAM layouts at the edge of two columns and a subarray, respectively. It can be observed that there is no increase in cell area. A single global back-gate bias can be applied with only one contact for all cells in entire SRAM columns or subarray to reduce the area penalty. In such a case, V_T for nFETs can be controlled by channel dopants to reduce SCE, and V_T for pFETs can be controlled by back-gate biasing to minimize SCE (and RDF). The proposed scheme can be applied to other applications. When circuits are in power-down mode, the scheme can keep circuit blocks at low-leakage state using a single back-gate bias. The scheme can be extended and implemented with nFET, pFET, or mixed back-gate regions depending on area and circuit property considerations.

V. CONCLUSION

We have proposed a selective back-gate bias technique for FD/SOI SRAM using dual BOX to improve standby leakage, read stability, and write ability and to enhance subarray access speed while preserving the overall area efficiency. Physics-based analysis and numerical simulations showed that substrate/back-gate voltage effectively modulated V_t in pull-up pFETs without changing the device characteristics of pull-down and pass-gate nFETs in SRAM cells. Due to the enhanced current drive in read mode, the inverter trip voltage significantly increases, and nominal RSNM was noticeably improved. TCAD-simulated results showed that RSNM can be increased by 37% by the proposed scheme. It is demonstrated that RSNM of the scheme was quite immune to process variations such as RDF, T_{Si}, and T_{BOX}. Leakage power and write ability were significantly improved to reduced V_t of pFETs. Compact physical model-based analysis showed that subarray speed can be significantly improved due to the reduced BL capacitance for thick BOX of pass-gate devices in the proposed scheme. Area efficiency was also demonstrated by layout analysis. Compact process flow for the scheme was discussed. Due to

improved stability, lower sensitivity to parameter variations, lower area overhead, and feasible fabrication, the proposed design technique can be very suitable for high-performance on-chip cache and SOC embedded applications beyond 45-nm FD/SOI technologies.

REFERENCES

[1] H. Ngo, K. Kim, C. T. Chuang, J. B. Kuang, F. Gebara, and K. Nowka, "An asymmetrical double-gate VCO with wide frequency range," in *Proc. Tech. Papers Int. Symp. VLSI-TSA*, Hsinchu, Taiwan, Apr. 2006, pp. 147–148.

[2] M. Yamaoka, K. Osada, R. Tsuchiya, M. Horiuchi, S. Kimura, and T. Kawahara, "Low power SRAM menu for SOC application using Yin-Yang-feedback memory cell technology," in *VLSI Symp. Tech. Dig.*, Jun. 2004, pp. 288–291.

[3] M. Yamaoka, R. Tsuchiya, and T. Kawahara, "SRAM circuit with extended operating margin and reduced stand-by leakage current using thin-BOX FD-SOI transistors," in *Proc. IEEE A-SSCC*, Nov. 2005, pp. 109–112.

[4] K. Kim, C. T. Chuang, J. B. Kuang, H. Ngo, and K. Nowka, "Low-power high-performance asymmetrical double-gate circuits using back-gate-controlled wide-tunable-range diode voltage," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2263–2368, Sep. 2007.

[5] E. J. Nowak, I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C. T. Chuang, K. Bernstein, and R. Puri, "Turning silicon on its edge," *IEEE Circuits Devices Mag.*, vol. 20, no. 1, pp. 20–31, Jan./Feb. 2004.

[6] M. H. Chiang, K. Kim, C. T. Chuang, and C. Tretz, "High-density reduced-stack logic circuit techniques using independent-gate controlled double-gate devices," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2370–2377, Sep. 2006.

[7] Y. Hirano, M. Tsujiuchi, K. Ishikawa, H. Shinohara, T. Terada, Y. Maki, T. Iwamatsu, K. Eikyu, T. Uchida, S. Obayashi, K. Nii, Y. Tsukamoto, M. Yabuuchi, T. Ipposhi, H. Oda, and Y. Inoue, "A robust SRAM architecture using advanced ABC technology for 32 nm node and beyond LSTP devices," in *Proc. VLSI Symp. Technol.*, Kyoto, Japan, Jun. 2007, pp. 78–79.

[8] Y. Morita, R. Tsuchiya, T. Ishigaki, N. Sugii, T. Iwamatsu, T. Ipposhi, H. Oda, Y. Inoue, K. Torii, and S. Kimura, "Small Vth variability achieved by intrinsic silicon on thin BOX (SOTB) CMOS with single metal," in *Proc. VLSI Symp. Techol.*, Honolulu, HI, Jun. 2008, pp. 166–167.

[9] MEDICI: Two-Dimensional Device Simulation, *Synopsis Inc.*, Mountain View, CA, 2003.

[10] K. Kim and J. G. Fossum, "Double-gate CMOS: Symmetrical-versus asymmetrical-gate devices," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 294–299, Feb. 2001.

[11] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-30, no. 10, pp. 1244–1251, Oct. 1983.

[12] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*. Upper Saddle River, NJ: Prentice-Hall, 2003.

[13] Y. Tuar and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[14] International Technology Roadmap for Semiconductors, 2004. [Online]. Available: http://public.itrs.net/

[15] J. G. Fossum, "Physical insights on nanoscale multi-gate CMOS design," *Solid State Electron.*, vol. 51, no. 2, pp. 188–194, Feb. 2007.

[16] M.-H. Chiang, K. Kim, and C.-T. Chuang, "Random dopant fluctuation in limited-width FinFET technologies," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 2055–2060, Aug. 2007.

[17] M. Hargrove and S. Voldman, "Dual buried oxide film SOI structure and method of manufacturing the same," U.S. Patent 6 531 741, Mar. 11, 2003.

[18] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, and M. Bohr, "A 3-GHz 70 Mb SRAM in 65 nm CMOS technology with integrated column-based dynamic power supply," in *Proc. Dig. Tech. Papers ISSCC*, Feb. 2005, pp. 474–475.

[19] M. Khellah, N. S. Kim, J. Howard, G. Ruhl, M. Sunna, Y. Ye, J. Tschanz, D. Somasekhar, N. Borkar, F. Hamzaoglu, G. Pandya, A. Farhang, K. Zhang, and V. De, "A 4.2 GHz 0.3 mm² 256 kb dual-V_{cc} SRAM building block in 65 nm CMOS," in *Proc. Dig. Tech. Papers ISSCC*, Feb. 2006, pp. 624–625.
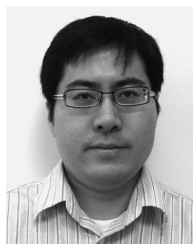
Keunwoo Kim (S'98–M'01–SM'06) was born in Daegu, Korea, in 1968. He received the B.S. degree in physics from Sungkyunkwan University, Seoul, Korea, in 1993 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Florida, Gainesville, in 1998 and 2001, respectively. His doctoral research was in the area of SOI and double-gate device design and modeling.

Since June 2001, he has been a Research Staff Member with the VLSI Design Department, IBM T. J. Watson Research Center, Yorktown Heights, NY. He has worked on the design of high-performance and low-power microprocessors, novel VLSI circuit techniques, scaled and exploratory CMOS technology performance/power evaluation, and physics/modeling for bulk-Si, SOI, strained-Si, SiGe, hybrid orientation/device, and double-gate technologies. He has published over 75 papers in technical journals and conference proceedings. He is the holder of 12 U.S. patents, with another six U.S. patents pending. His present work includes IBM's POWER7 processor design, next-generation microprocessor design, the analysis and prediction of SRAM variability/yields, and system-level performance/power projections.

Dr. Kim received five invention achievement awards from IBM. He has been a Reviewer of the journal publications for IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEM, and SOLID-STATE ELECTRONICS. He was listed in *Who's Who in America* in 2007 and 2008.
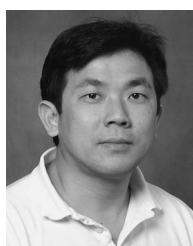
Jente B. Kuang (SM'02) received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1982, the M.S. degree in electrical engineering from Columbia University, NY, in 1986, and the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, in 1990.

From 1982 to 1984, he was an Electronics Instructor with the Electronics Training Center, Army Missile Command, Taiwan. From 1986 to 1990, he was a Research Assistant with the Compound Semiconductor Research Group and National Submicron Facility at Cornell University. In 1990, he joined IBM. Since then, he has been working on a variety of research and product development projects for bipolar, BiCMOS, and CMOS devices and circuits, including the design of flash memories, SRAMs, register files, and high-speed low-power digital circuits. He is currently a Research Staff Member with the IBM Austin Research Laboratory, Austin, TX.

Fadi H. Gebara was born in Detroit, MI, in 1978. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2000, 2002, and 2005, respectively.

In 2004, he joined the IBM Austin Research Laboratory, Austin, TX, where he has been a Research Staff Member since 2005. During his time at IBM, he developed numerous clocking strategies for high-performance microprocessors. Currently, he is working on adaptive and process-tolerant circuits for deep-submicrometer designs.

Hung C. Ngo received the B.S. degree in computer science from New York University, New York, and the B.S.E.E. degree from the Cooper Union for the Advancement of Science and Art, New York, in 1988.

From 1988 to 1993, he was a Logic Designer with IBM, Kingston, NY. From 1993 to 1996, he was a Circuit Designer with IBM, Poughkeepsie, NY. Since 1996, he has been with the IBM Austin Research Laboratory, Austin, TX.

Mr. Ngo was nominated twice as a Research Master Inventor.

Ching-Te Chuang (S'78–M'82–SM'91–F'94) received the B.S.E.E. degree from the National Taiwan University, Taipei, Taiwan, in 1975 and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1982.

From 1977 to 1982, he was a Research Assistant with the Electronics Research Laboratory, University of California, working on bulk and surface acoustic wave devices. In 1982, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY. From 1982 to 1986, he worked on scaled bipolar devices, technology, and circuits. He studied the scaling properties of epitaxial Schottky barrier diodes, did pioneering works on the perimeter effects of advanced double-poly self-aligned bipolar transistors, and designed the first sub-nanosecond 5-kb bipolar ECL SRAM. From 1986 to 1988, he was the Manager of the Bipolar VLSI Design Group, IBM T. J. Watson Research Center, working on low-power bipolar circuits, high-speed high-density bipolar SRAMs, multi-Gb/s fiber-optic data-link circuits, and scaling issues for bipolar/BiCMOS devices and circuits. In 1988, he managed the High Performance Circuit Group, IBM T. J. Watson Research Center, investigating high-performance logic and memory circuits. In 1993, his group was primarily responsible for the circuit design of IBM's high-performance CMOS microprocessors for enterprise servers, PowerPC workstations, and game/media processors. In 1996, he led the efforts in evaluating and exploring scaled/emerging technologies, such as PD/SOI, UT/SOI, strained-Si devices, hybrid orientation technology, and multigate/FinFET devices, for high-performance logic and SRAM applications. In 1998, he was responsible for the Research VLSI Technology Circuit Co-design strategy and execution. His group was very active and visible in leakage/variation/degradation tolerant circuit and SRAM design techniques. In February 2008, he took early retirement from IBM to join the National Chiao Tung University, Hsinchu, Taiwan, as a Chair Professor with the Department of Electronic Engineering. He is the holder of 27 U.S. patents, with another 14 pending. He has authored or coauthored over 270 papers. He has authored many invited papers in international journals such as *International Journal of High Speed Electronics*, PROCEEDINGS OF THE IEEE, *IEEE Circuits and Devices Magazine*, and *Microelectronics Journal*.

Dr. Chuang served on the Device Technology Program Committee for IEDM in 1986 and 1987 and the Program Committee for Symposium on VLSI Circuits from 1992 to 2006. He was the Publication/Publicity Chairman for Symposium on VLSI Technology and Symposium on VLSI Circuits in 1993 and 1994 and the Best Student Paper Award Sub-Committee Chairman for Symposium on VLSI Circuits from 2004 to 2006. He was elected an IEEE fellow in 1994 "for contributions to high-performance bipolar devices, circuits, and technology." He has presented numerous plenary, invited, or tutorial papers/talks at international conferences such as International SOI Conf., DAC, VLSI-TSA, ISSCC Microprocessor Design Workshop, VLSI Circuit Symposium Short Course, ISQED, ICCAD, APMC, VLSI-DAT, ISCAS, MTDT, WSEAS, VLSI Design/CAD Symposium, etc. He has received one Outstanding Technical Achievement Award, one Research Division Outstanding Contribution Award, five Research Division Awards, and 12 Invention Achievement Awards from IBM. He has also received the Outstanding Scholar Award from Taiwan's Foundation for the Advancement of Outstanding Scholarship for 2008–2013. He was the corecipient of the Best Paper Award at the 2000 IEEE International SOI Conference.

Kevin J. Nowka (SM'06) received the B.S. degree in computer engineering from Iowa State University, Ames, in 1986 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1988 and 1995, respectively.

In 1996, he joined the IBM Austin Research Laboratory, Austin, TX, where he conducted research on high-frequency microprocessors and low-power system-on-a-chip designs. He is currently a Senior Manager of the VLSI Systems Research organization in the IBM Austin Research Laboratory. His research activities include the development of high-performance power-efficient robust circuits for microprocessors, sensors and monitor structures, and power-efficient wired communications. He is the holder of over 50 patents and has authored over 50 refereed papers related to CMOS circuits and microprocessors.