A Novel Transmission-Line Deembedding Technique for RF Device Characterization

Hsiu-Ying Cho, Jiun-Kai Huang, Chin-Wei Kuo, Sally Liu, and Chung-Yu Wu, *Fellow, IEEE*

***Abstract*—A novel transmission-line deembedding technique is presented in this paper. With this technique, the left- and right-side ground–signal–ground probe pads can be extracted directly using two transmission-line test structures of length L and $2L$. An additional through structure is designed using via-stack deembedding, which is unique among current deembedding methods. The advantages of the proposed method include the following: 1) smaller silicon area; 2) discontinuity between the pad and interconnect; 3) substrate coupling and contact effects; and 4) employment of via-stack deembedding. The proposed novel methodology is a great breakthrough in the area of ultrahigh-frequency deembedding and should enable more accurate RF models to be developed. In the proposed methodology, intrinsic slow-wave CPW transmission-line structures are placed on the interlevel metallization layers, as they are the most appropriate RF device for cascade-based deembedding method involving the via-stack deembedding technique. Experimental results have demonstrated that attenuation loss and wavelength can be optimized by changing the metal density and the position of the metal layer on the floating shields. Both measurement and electromagnetic-wave simulations were performed up to 50 GHz. With a shortened wavelength, a reduction in silicon area of more than 66% can be achieved by using optimized slot-type floating shields.**

***Index Terms*—Characterization, deembedding, slow wave, transmission lines.**

I. Introduction

The extreme importance of accurate parasitic deembedding techniques to RF device characterization has already been established. In general, the parasitic contributions of device-under-test (DUT) structures mainly arise from probe pads, the interconnection lines connected to the intrinsic on-chip DUT structure, and the silicon substrate. Deembedding techniques can be classified as two groups. The first group is called the lumped-equivalent-circuit-model-based technique [1]–[9]. Between four to six deembedding structures are needed to obtain accurate results. However, this method involves a more complicated extraction and a larger chip in advanced CMOS processes. In this group, an extra grounded metal strip, which adds resistance and inductance to the short structure, is used as a connection between the two ports. The parasitic contribution of the extra grounded metal strip cannot be ignored if the frequencies are high or if the DUT structures are large. The second group involves a cascade-based deembedding technique [10]–[15] which enables the extraction of interconnection parameters using through structures. To obtain the most practical test-key design, the metal interconnection from the probe pad to the intrinsic DUT structure should be around 20–40 μm. It is important to design a good "through" structure where the left and right pads are effectively uncoupled and do not suffer from the effects of an extra grounded metal strip. Therefore, cascade-based techniques are suitable for larger DUT structures, such as transmission lines, inductors, or MOSFETs with larger widths. In situations where real silicon is involved, RF DUT structures are connected to the probe pad using low- to high-level metallization, and the cascade sequence is first metallization, then stacked metallization connected through via holes, and finally top metallization. The contribution of the interconnection and the proposed methodology becomes important as the frequencies increase. Unfortunately, currently existing techniques do not account for via-stack parasitic methodology. In this paper, a novel transmission-line deembedding method, which requires two transmission-line structures of length L_1 and L_2 and one additional through structure, is proposed to create a more accurate RF device characterization. Investigations on methodologies using via-stack deembedding, which have not been conducted previously, are performed in this paper. Two transmission-line structures are set up to achieve direct extraction of the left and right sides of ground–signal–ground (GSG) pads. One additional through structure is designed to solve the bottleneck resulting from via-stack deembedding and the uncertainty associated with direct measurement. Based on the experimental and simulation results from this paper, it can be concluded that direct extraction of the left- and right-side GSG pads and the via-stack deembedding method are the best options. When compared with conventional deembedding methods, the advantages of the proposed method include the following features: 1) smaller silicon area; 2) discontinuity between the pad and interconnect; 3) substrate coupling and contact effects; and 4) via-stack deembedding.

Coaxial transmission lines offer significant advantages for the design of integrated millimeter-wave circuits when compared to those offered by microstrip or coplanar-waveguide (CPW) transmission lines [16], [17]. Since coaxial transmission lines are shielded, lines and components can be closely spaced, and they can even pass over each other with minimal crosstalk, allowing for complex and compact signal routing. A slow-wave CPW transmission-line structure, where floating shields are both above and below the CPW structure, can be regarded as a rectangular coaxial transmission-line structure. Moreover,

Manuscript received April 24, 2009; revised August 19, 2009. Current version published November 20, 2009. This work was supported by the National Science Council (NSC), Taiwan, under Grant NSC 97-2221-E-009-179. The review of this paper was arranged by Editor C.-Y. Lu.

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Digital Object Identifier 10.1109/TED.2009.2032608

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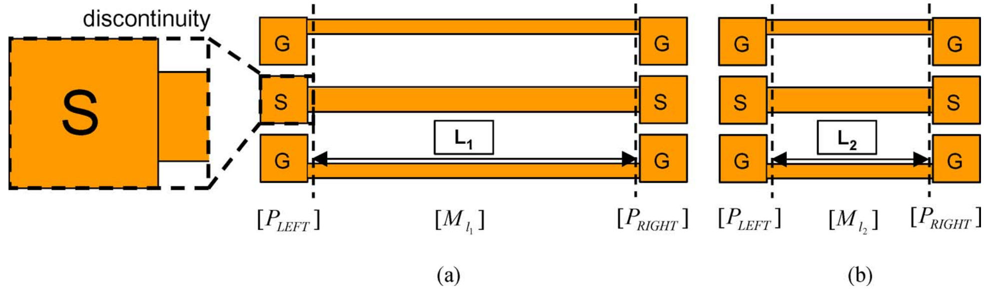

Fig. 1. Two transmission lines of lengths L_1 and L_2 are designed in a GSG configuration. (a) Transmission line of length $L_{1[TL_{l_1}]}$. (b) Transmission line of length $L_{2[TL_{l_2}]}$.

the design and performance of coaxial transmission lines are independent of any substrate. The slow-wave theory in the microwave range has been investigated with most grounded slow-wave structures [18]–[30]. As demonstrated in this paper, attenuation loss and wavelength can be adjusted by changing the metal density and the position of the floating shields on the metal layers.

II. New Deembedding Methodology

A. Left- and Right-Side GSG Pad Extraction

Fig. 1(a) and (b) shows the proposed deembedding test structures. Two transmission lines of length L_1 and L_2 are in a GSG configuration. The discontinuity between the pad and interconnect is combined with that of the left- and right-side GSG pads. The transmission-line structure is decoupled into a series cascade of three two-port networks, including the left- and right-side GSG pads, together with the intrinsic transmission line. If the length is properly designed as $L_1 = 2^* L_2$, the multiplication sum of ABCD matrix $[P_{\text{LEFT}}]$ and $[P_{\text{RIGHT}}]$ can be extracted using the following:

$$[TL_{l_1}] = [P_{\text{LEFT}}][M_{l_1}][P_{\text{RIGHT}}] = [P_{\text{LEFT}}][M_{l_2}][M_{l_2}][P_{\text{RIGHT}}] \quad (1)$$

$$[TL_{l_2}] = [P_{\text{LEFT}}][M_{l_2}][P_{\text{RIGHT}}] \quad (2)$$

$$[P_{\text{LEFT}}][P_{\text{RIGHT}}] = [TL_{l_2}][TL_{l_1}]^{-1}[TL_{l_2}] = \begin{bmatrix} A_{\text{LR}} & B_{\text{LR}} \\ C_{\text{LR}} & D_{\text{LR}} \end{bmatrix} \quad (3)$$

where

$[P_{\text{LEFT}}]$ and $[P_{\text{RIGHT}}]$ ABCD matrices for the left- and right-side GSG pads;

$[TL_{l_1}]$ and $[TL_{l_2}]$ ABCD matrices for the transmission-line structures of lengths L_1 and L_2;

$[M_{l_1}]$ and $[M_{l_2}]$ ABCD matrices for the intrinsic transmission-line structures of lengths L_1 and L_2.

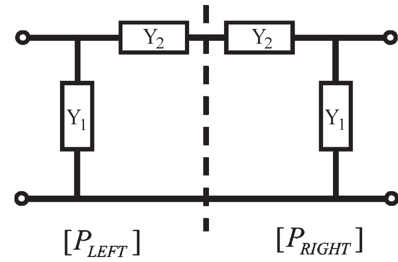

Fig. 2. Equivalent representation of a symmetrical structure.

The left- and right-side GSG pad structures are symmetrical, and the equivalent circuit is shown in Fig. 2. By definition [31], $[P_{\text{LEFT}}]$ and $[P_{\text{RIGHT}}]$ can be represented as

$$[P_{\text{LEFT}}][P_{\text{RIGHT}}] = \begin{bmatrix} 1 & 1/Y_2 \\ Y_1 & 1+Y_1/Y_2 \end{bmatrix} \begin{bmatrix} 1+Y_1/Y_2 & 1/Y_2 \\ Y_1 & 1 \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} 1 & 1/Y_2 \\ Y_1 & 1+Y_1/Y_2 \end{bmatrix} \begin{bmatrix} 1+Y_1/Y_2 & 1/Y_2 \\ Y_1 & 1 \end{bmatrix} = [TL_{l_2}][TL_{l_1}]^{-1}[TL_{l_2}] = \begin{bmatrix} A_{\text{LR}} & B_{\text{LR}} \\ C_{\text{LR}} & D_{\text{LR}} \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} 1+2Y_1/Y_2 & 2/Y_2 \\ 2Y_1(1+Y_1/Y_2) & 1+2Y_1/Y_2 \end{bmatrix} = \begin{bmatrix} A_{\text{LR}} & B_{\text{LR}} \\ C_{\text{LR}} & D_{\text{LR}} \end{bmatrix}. \quad (6)$$

Therefore, $[P_{\text{LEFT}}]$ and $[P_{\text{RIGHT}}]$ can be obtained using (7) and (8), shown at the bottom of the page. After extracting $[P_{\text{LEFT}}]$ and $[P_{\text{RIGHT}}]$, the performance of both the transmission lines

$$[P_{\text{LEFT}}] = \begin{bmatrix} 1 & B_{\text{LR}}/2 \\ C_{\text{LR}}/\left(1+(A_{\text{LR}}+D_{\text{LR}})/2\right) & 1+B_{\text{LR}}C_{\text{LR}}/2\left(1+(A_{\text{LR}}+D_{\text{LR}})/2\right) \end{bmatrix} \quad (7)$$

$$[P_{\text{RIGHT}}] = \begin{bmatrix} 1+B_{\text{LR}}C_{\text{LR}}/2\left(1+(A_{\text{LR}}+D_{\text{LR}})/2\right) & B_{\text{LR}}/2 \\ C_{\text{LR}}/\left(1+(A_{\text{LR}}+D_{\text{LR}})/2\right) & 1 \end{bmatrix} \quad (8)$$

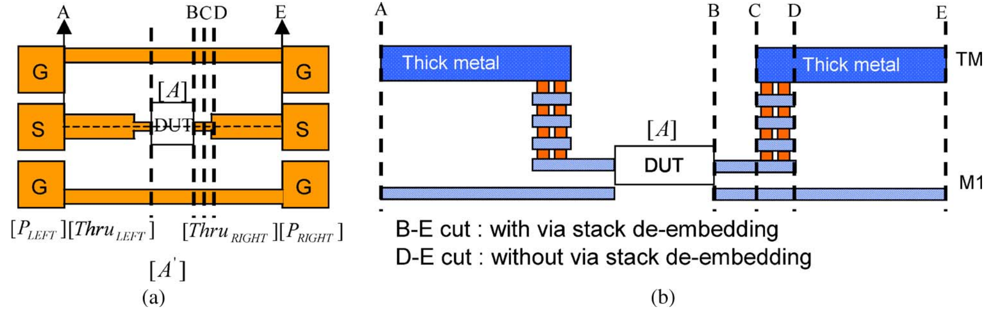

Fig. 3. Connection between the low- and high-level metallization layers. (a) Top view of the ABCD matrix $[A']$ of the DUT structure. (b) Cross section along the A–E cut.

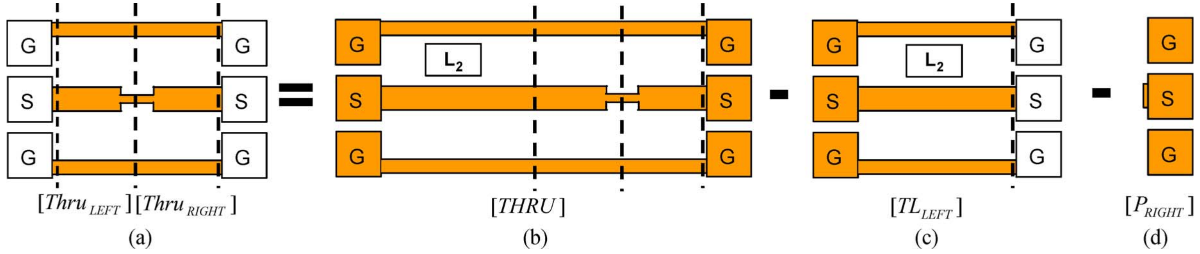

Fig. 4. Matrix manipulation for the series cascade of $[Thru_{\mathrm{LEFT}}][Thru_{\mathrm{RIGHT}}]$ with $[THRU]$, $[TL_{\mathrm{LEFT}}]$, and $[P_{\mathrm{RIGHT}}]$. (a) Cascade of $[Thru_{\mathrm{LEFT}}][Thru_{\mathrm{RIGHT}}]$. (b) One additional through structure $[THRU]$. (c) Left-side transmission line of length $L_2[TL_{\mathrm{LEFT}}]$. (d) Right-side GSG pad $[P_{\mathrm{RIGHT}}]$.

of lengths L_1 and L_2 can be extracted using the following, allowing for additional extraction data:

$$[M_{l_1}] = [P_{\mathrm{LEFT}}]^{-1}[TL_{l_1}][P_{\mathrm{RIGHT}}]^{-1} \qquad (9)$$

$$[M_{l_2}] = [P_{\mathrm{LEFT}}]^{-1}[TL_{l_2}][P_{\mathrm{RIGHT}}]^{-1}. \qquad (10)$$

Since $[P_{\mathrm{LEFT}}]$, $[P_{\mathrm{RIGHT}}]$, $[M_{l_1}]$, and $[M_{l_2}]$ can be extracted, more variable combinations can be further cascaded to create more flexible deembedding dummy structures, which can also lead to the creation of an additional through structure.

B. Via-Stack Deembedding

Fig. 3(a) shows a top view of the ABCD matrix $[A']$ of a DUT structure, where the ABCD matrices $[Thru_{\mathrm{LEFT}}]$ and $[Thru_{\mathrm{RIGHT}}]$ are the left- and right-side interconnections. In real tape-out, the intrinsic DUT structure can be placed on the interlevel metallization layer, while RF DUT structures are connected to the probe pad using low- to high-level metallization. First metallization, stacked metallization connected through via holes, and top metallization are included along the B–E cut, as shown in Fig. 3(b), using the proposed via-stack deembedding technique. An estimation of the impedance is obtained from an electromagnetic (EM) simulation (Ansoft HFSS), and the resistance ratio of the B–D cut over the B–E cut cannot be ignored. The ratio would be higher if either low-level metallization M1 or a shorter length D–E is involved. Since the minimum interconnect length between port1 and port2 is around 40 μm, probe-to-probe coupling with such short interconnect could be a potential limitation. For medium or large devices, or small-cascaded devices, the distance between port1 and port2 in Fig. 3(a) is above 100 μm. Therefore, it is necessary to design a good "through" test structure in order to obtain stable measurement results. One additional through structure is designed, as shown in Fig. 4(b), and its ABCD matrix $[THRU]$ is equal to $[TL_{\mathrm{LEFT}}][Thru_{\mathrm{LEFT}}][Thru_{\mathrm{RIGHT}}][P_{\mathrm{RIGHT}}]$, where the ABCD matrix $[TL_{\mathrm{LEFT}}]$ is the left-side transmission line of length L_2 and is equal to $[TL_{l_2}][P_{\mathrm{RIGHT}}]^{-1}$, as shown in Fig. 4(c). The optimized length of L_2 is designed based on two criteria: 1) The maximum length cannot be too long because the parasitics of interest will represent a smaller faction of the measured structure, and 2) the minimum length cannot be so short as to decrease probe-to-probe coupling.

$[Thru_{\mathrm{LEFT}}][Thru_{\mathrm{RIGHT}}]$ can be extracted from the following equation, and the corresponding explanation is shown in Fig. 4:

$$[Thru_{\mathrm{LEFT}}][Thru_{\mathrm{RIGHT}}] = [TL_{\mathrm{LEFT}}]^{-1}[THRU][P_{\mathrm{RIGHT}}]^{-1}. \qquad (11)$$

Using (7) and (8), the matrices $[Thru_{\mathrm{LEFT}}]$ and $[Thru_{\mathrm{RIGHT}}]$ can be calculated, respectively. The length of $[Thru_{\mathrm{LEFT}}]$ and $[Thru_{\mathrm{RIGHT}}]$ cannot be too long in order to maintain the validity of the deembedding technique when high frequencies are involved. After determining $[P_{\mathrm{LEFT}}]$, $[Thru_{\mathrm{LEFT}}]$, $[Thru_{\mathrm{RIGHT}}]$, and $[P_{\mathrm{RIGHT}}]$, the ABCD matrix $[A]$ of the intrinsic DUT structure can be extracted using (12) through the matrix manipulation of the ABCD matrix $[A']$ of the DUT structure with the left- and right-side interconnections and the left- and right-side GSG pad, as shown in Fig. 3(a). The proposed deembedding method can also be used with asymmetrical DUT structures by designing another through dummy structure

$$[A] = [P_{\mathrm{LEFT}}]^{-1}[Thru_{\mathrm{LEFT}}]^{-1}[A'] \times [Thru_{\mathrm{RIGHT}}]^{-1}[P_{\mathrm{RIGHT}}]^{-1}. \qquad (12)$$

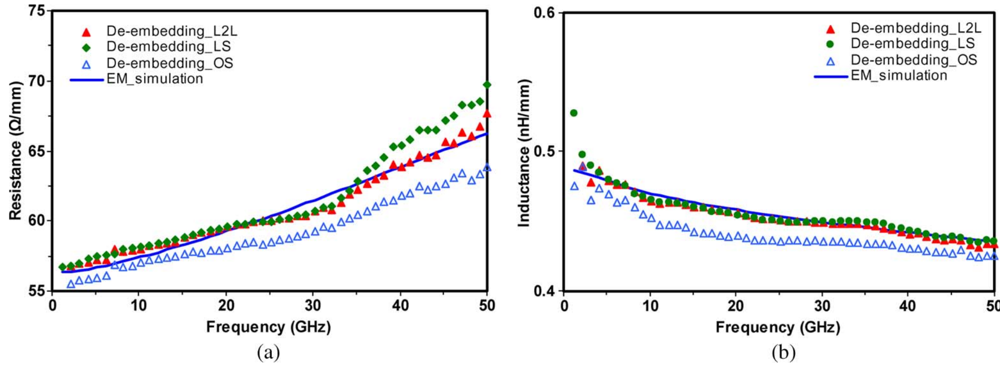

Fig. 5. Comparison of the measured transmission-line performances for Deembedding_L2L, Deembedding_LS [14], Deembedding_OS, and EM simulation with (a) resistance and (b) inductance.

C. Deembedding Procedure

The proposed deembedding procedure involves the following steps:

1) measurement of the scattering matrices of the transmission lines of lengths L_1 and L_2, the one additional through structure, and the DUT structure, as shown in Figs. 1(a) and (b), 3(a), and 4(b), respectively;
2) conversion of the scattered matrices of the transmission lines of lengths L_1 and L_2, the one additional through structure, and the DUT structure to their ABCD matrices $[TL_{l_1}]$, $[TL_{l_2}]$, $[THRU]$, and $[A']$, respectively;
3) calculation of the ABCD matrices of the left- and right-side GSG pads $[P_{\mathrm{LEFT}}]$ and $[P_{\mathrm{RIGHT}}]$, respectively, using (1)–(8);
4) calculation of the ABCD matrices of the left- and right-side through $[Thru_{\mathrm{LEFT}}]$ and $[Thru_{\mathrm{RIGHT}}]$, respectively, using (11), and (7) and (8);
5) calculation of the ABCD matrix $[A]$ of the intrinsic DUT structure using (12).

III. Expimental Results and Discussion

A. Comparative Results of Deembedding Techniques

One open, one short, and two microstrip transmission lines of lengths $L_1 = 1000$ μm and $L_2 = 500$ μm were designed. The S-parameters of the transmission-line DUT structures were measured up to 50 GHz using an Agilent 8510C. The proposed test structures were fabricated using 65-nm RF-CMOS technology. The results of a comparison of the proposed technique denoted as Deembedding_L2L, the Mangan's method [14] denoted as Deembedding_LS, an open-short deembedding technique denoted as Deembedding_OS, and an EM simulation are shown in Fig. 5. Lesser resistance and inductance values remain after the conventional open-short deembedding is performed. An extra grounded metal strip of the short structure results in over deembedding. Fig. 5 shows an adequate agreement between the proposed deembedding technique and EM simulation.

In general, the assumption for a two-step, a three-step, and a four-step deembedding method is valid only if the lengths of the DUT devices are much smaller than the distances between port1 and port2. However, this is not always true for larger DUT devices and may result in over deembedding when intrinsic device performance is involved. Therefore, the proposed deembedding technique can address the problem of over deembedding. Moreover, it is the best choice when larger DUT devices are involved, such as transmission lines, inductors, and MOSFETs with larger widths. As the left- and right-side GSG pads are extracted directly, in addition to substrate coupling and contact effects provided by a four-step deembedding method, the proposed method accounts for the discontinuity between the pad and interconnect.

B. Via-Stack Deembedding Applications and Slow-Wave CPW Transmission Lines

A capacitor device is chosen as the subject of a study to compare with and without via-stack deembedding methods. The B–E cut is deembedded using the via-stack technique, while the D–E cut is deembedded without the via-stack technique, as shown in Fig. 3(b). As the ideal deembedded data are known, the comparative results based on the 40% resistance ratio of the B–D cut over B–E cut are shown in Fig. 6. It is shown that there is an obvious improvement in accuracy and capacitance performance using the via-stack deembedding method. Intrinsic slow-wave CPW transmission-line structures are placed on the interlevel metallization layers as they are the most appropriate RF device for cascade-based deembedding methods involving the via-stack deembedding technique.

Two types of transmission lines were fabricated as listed in Table I, including as follows: 1) a CPW transmission line without shields (CPW) and 2) three slow-wave CPW transmission lines with slot-type floating shields (FSCPW1, FSCPW2, and FSCPW3), as shown in Fig. 7. A slow-wave CPW transmission line was designed where periodically aslot-type floating shields are located both above and below the CPW structure, and they are oriented transversely to the CPW structure. For all the transmission lines in Table I, the CPW structure is formed on the eighth (M8) metal layer, and the lower slot-type shields are created on either the seventh (M7) or second (M2) metal layer. The CPW part has a signal/ground linewidth of 10 μm/10 μm, with a 20-μm space between the signal and ground lines. The upper floating shields are formed on the ninth (M9) metal layer with a fixed strip length (SL) of 2 μm and a fixed strip space (SS) of 2 μm. The SL of lower floating shields is designed to be the minimum length required to achieve a high performance

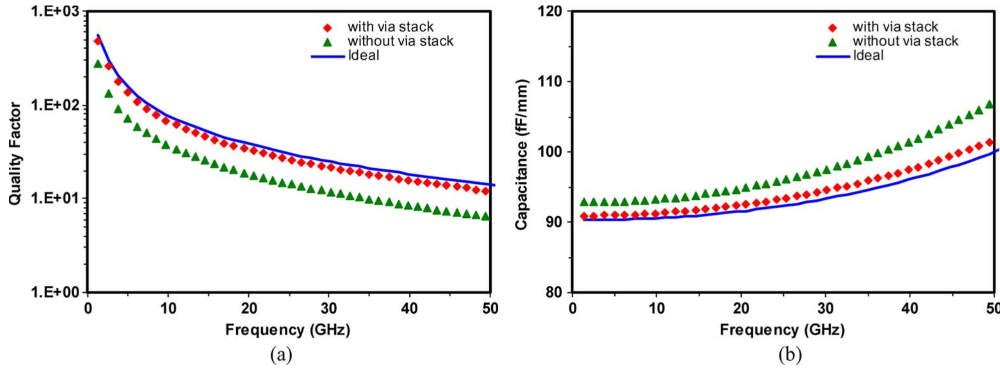

Fig. 6. Comparison of the simulated capacitor performances for via-stack deembedding and without via-stack deembedding with (a) quality factor and (b) capacitance.

TABLE I
TRANSMISSION LINE STRUCTURES

Name	Transmission Line Type	Metal Shield Layer	Strip Length (SL)	Strip Space (SS)	Shield Type
CPW	CPW	No strip shields			
FSCPW1	Floating slow-wave CPW	M9, M7	0.1um	0.1um	floating
FSCPW2	Floating slow-wave CPW	M9, M7	0.1um	0.9um	floating
FSCPW3	Floating slow-wave CPW	M9, M2	0.1um	0.1um	floating

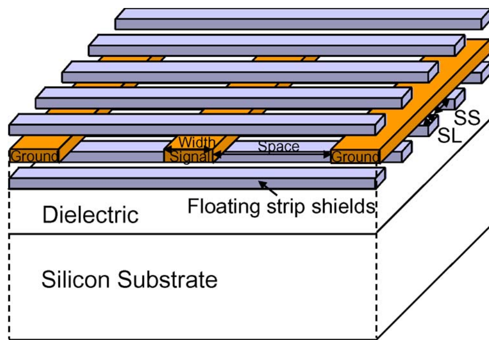

Fig. 7. Schematic view of a slow-wave CPW transmission line with slot-type floating shields.

with minimal eddy-current loss. The lower slot-type floating shields are designed with the following dimension splits: 1) the SL on M7 is 0.1 μm and the accompanying SS is either 0.1 or 0.9 μm, and 2) the SL on M2 is 0.1 μm and the accompanying SS is 0.1 μm.

The performance of a transmission line can be characterized by attenuation loss per unit length α in $Neper/m$, characteristic impedance Z_c in Ω, and effective relative permittivity ε_r, which can be expressed, respectively, as follows:

$$\alpha = real(\gamma)$$
$$Z_C = \left(\frac{R + j\omega L}{\gamma}\right)$$
$$\varepsilon_r = 9 \cdot 10^{16} \cdot \left(\frac{\beta}{\omega}\right)^2$$

where ω is the angular frequency, R is the resistance per unit length, L is the inductance per unit length, γ is the propagation constant, and $\beta = 2\pi/\lambda$ is the phase constant [32]. Generally, lower attenuation loss and shorter wavelength are required to achieve high-performance transmission line and compactness.

Fig. 8(a) shows that the attenuation loss of FSCPW3 is lower than that of FSCPW1, because the dielectric thickness between the signal line on M8 and the floating shields on M2 is greater than the dielectric thickness between the signal line on M8 and the floating shields on M7. These results indicate that the currently prevalent opinion which supports the view that highest density shields are the best choice [33] is not always true. As frequencies increase, lower density coverage FSCPW2 exhibits a lower attenuation loss than does FSCPW1. In summary, the smaller the SL and the greater the thickness between the signal line and the floating shields, the lower the induced attenuation loss.

Fig. 8(b) shows that lower characteristic impedance can be achieved by increasing floating shield density or by raising the position of the metal layer. Characteristic impedance tuning by changing the metal density and the position of the metal layer in the slot-type floating shields offers a new design approach.

The wavelength of a transmission line indicates whether the transmission-line design is compact. Therefore, the wavelengths of transmission lines with a variety of slot-type floating-shield designs are compared in Fig. 8(c). From this, it is shown that the best choice is FSCPW1, whose wavelength is reduced to 1.19 mm, i.e., by a factor of more than three when compared to that of a conventional CPW transmission line with a wavelength of 3.58 mm. As a result, a reduction in silicon area of more than 66% can be achieved, which demonstrates that this approach is potentially highly attractive for MMIC applications.

An optimized design requires a good quality factor, such as $Q = \beta/2\alpha$, where β is the phase constant and α is the attenuation loss, and it should be used to judge an overall tradeoff between attenuation loss and wavelength. Guidelines for designing a transmission line with a high quality factor are shown in Fig. 8(d). It is shown that FSCPW1 is the most appropriate choice for designs operating at frequencies below 50 GHz. As discussed earlier and demonstrated in the experiments,

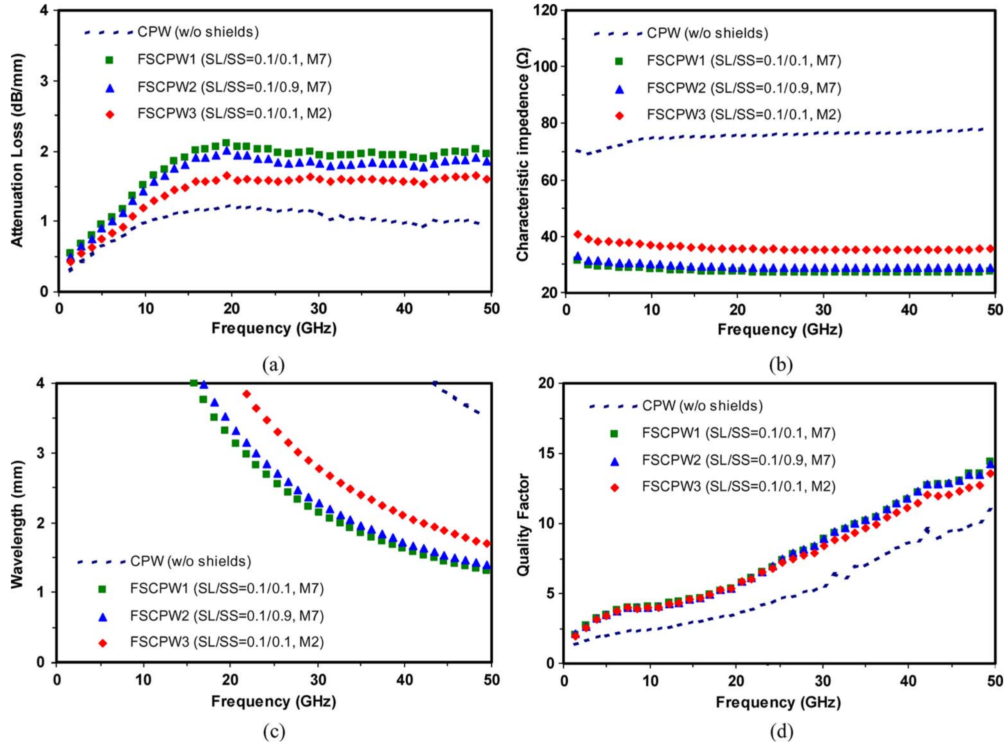

Fig. 8. Comparison of the measured transmission-line performances for different floating shields. (a) Attenuation loss. (b) Characteristic impedance. (c) Wavelength. (d) Quality factor.

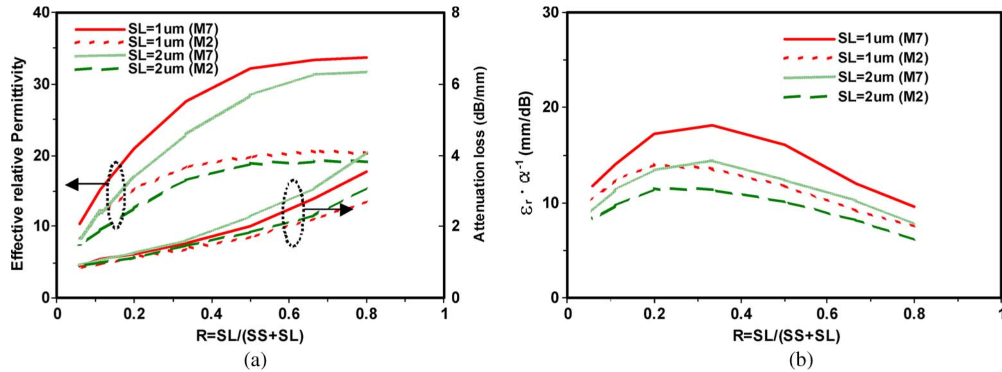

Fig. 9. Simulated slow-wave CPW transmission-line performance versus parameter R with different SL and metal layer position at signal frequency of 50 GHz. (a) Effective relative permittivity and attenuation loss. (b) Optimization index value of $\varepsilon_r \cdot \alpha^{-1}$.

the lower the attenuation loss, the longer the wavelength usually obtained. Therefore, a designer must weigh up the pros and cons between SL and SS dimensions together with metal layer positions in order to design a suitable slow-wave CPW to achieve a functional circuit at the desired operating frequency.

C. Optimized Simulation for Slot-Type Floating Shields in Transmission Lines

The optimization of slot-type floating shields to reduce simultaneously attenuation loss and wavelength is performed. Optimization analyses on SL, SS, and the position of floating shields are conducted by analyzing the EM simulation results. The density R of the slot-type floating shields is defined as follows:

$$R = \frac{SL}{SL + SS}. \tag{13}$$

Fig. 9(a) shows that a higher effective relative permittivity is achieved with a smaller SL, higher density R, and smaller dielectric thickness between the signal line and the floating shields. When the attenuation loss is taken into consideration, a minimized SL is the best choice for both effective relative permittivity and attenuation loss performance. The optimization index of the slot-type floating shields is defined as $\varepsilon_r \cdot \alpha^{-1}$ in millimeters per decibel, and Fig. 9(b) shows that an optimized performance is achieved when the $SL = 1\ \mu$m and $SS = 2\ \mu$m on M7. The optimized floating shields include a minimized SL, medium density R, and high metal layer position. Only after the specification requirements for the attenuation loss is determined, the density of the slot-type floating shields can be calculated. Consequently, the effective relative permittivity can be predicated from the minimized SL and the density of the slot-type floating shields. Since both SL and the SS can be adjusted in accordance with technology scaling, a scaled

slow-wave CPW can continue to offer lower attenuation loss and higher effective relative permittivity.

IV. Conclusion

Conventional deembedding methods suffer from an over-deembedding problem to which the proposed method offers a solution. In addition to the substrate coupling and contact effects provided by existing four-step deembedding methods, the proposed method also accounts for the discontinuity between the pad and interconnect. Current deembedding techniques do not deembed via-stack parasitic and the contribution of the proposed method becomes more important as frequency increases. As $[P_{\mathrm{LEFT}}]$, $[P_{\mathrm{RIGHT}}]$, $[M_{l_1}]$, and $[M_{l_2}]$ can be extracted, more flexible deembedding dummy structures can be created. Therefore, an additional through structure can be designed to perform via-stack deembedding. The proposed deembedding method can be extended to other RF devices, and this will allow for more accurate RF device characterization.

It has been shown that attenuation loss and wavelength can be optimized by changing the SL, SS, and metal layer position of the slot-type floating shields while keeping the same area. An optimization index of the slow-wave CPW transmission lines has been developed to enable circuit designers to determine expediently the most appropriate slot-type floating shields to meet design specifications. Designers, therefore, must weigh up the pros and cons concerning SL and SS dimensions, as well as with metal layer positions, in order to design a slow-wave CPW with suitable slot-type floating shields. The proposed floating slow-wave CPW transmission line has a better quality factor of 15 at 50 GHz and a shorter wavelength which results in a reduction of silicon area of more than 66% when compared to that of conventional CPW transmission lines. In short, a significant advantage for future technology scaling and RF circuit designing is made available through the use of more suitable SL and SS.

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