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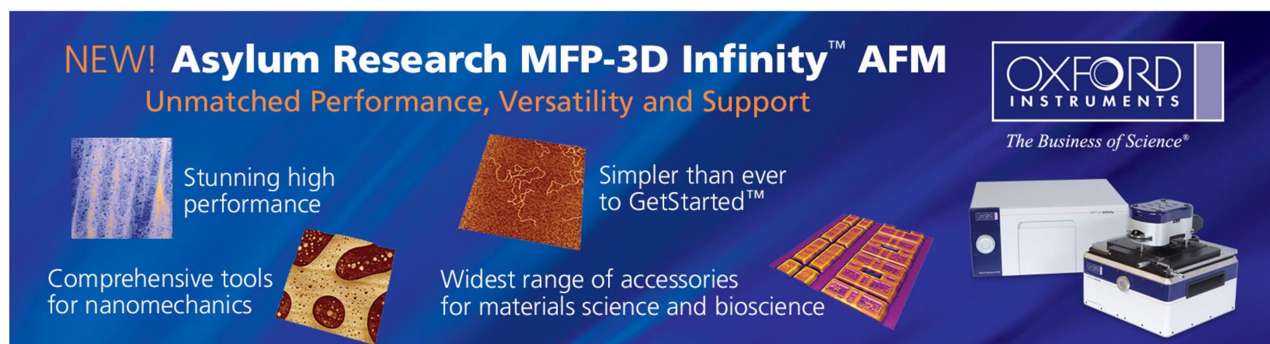

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Interfacial layer dependence on device property of high-κ TiLaO Ge/Si N-type metal-oxide-semiconductor capacitors at small equivalent-oxide thickness

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We have investigated the device property dependence of high dielectric-constant (high-κ) TiLaO epitaxial-Ge/Si n-type metal-oxide-semiconductor (n-MOS) capacitors on different GeO_2 and SiO_2 interfacial layers. Large capacitance density of 3.3 $\mu F/cm^2$, small equivalent-oxide thickness (EOT) of 0.81 nm and small C-V hysteresis of 19 mV are obtained simultaneously for MOS capacitor using ultrathin SiO_2 interfacial layer, while the device with ultrathin interfacial GeO_2 shows inferior performance of larger 1.1 nm EOT and poor C-V hysteresis of 93 mV. From cross-sectional transmission electron microscopy, secondary ion mass spectroscopy, and x-ray photoelectron spectroscopy analysis, the degraded device performance using GeO_2 interfacial layer is due to the severe Ge outdiffusion, thinned interfacial GeO_2 and thicker gate dielectric after 550 °C rapid-thermal anneal. © *2009 American Institute of Physics*. [doi:10.1063/1.3265947]

Germanium (Ge) has attracted much attention for metal-oxide-semiconductor field-effect transistor (MOSFET)[1–14] application due to both higher electron and hole mobility than Silicon (Si). However, the difficult challenges are the high leakage current of small energy band gap (E_G) Ge and the poor interface property with high dielectric-constant (κ) material. To lower the leakage current, we pioneered the defect free Ge-on-insulator (GOI or GeOI) (Ref. 1) structure, and the leakage current decreases with decreasing the Ge body thickness.[5] Nevertheless, the degraded interface property is still a tough challenge especially for the Ge n-type MOSFET (n-MOSFET)[6–12] at a small equivalent oxide thickness (EOT). The interface property is highly dependent on high-κ dielectrics, where Al_2O_3 (Ref. 1) and La_2O_3 (Refs. 8 and 11) show lower interface trap density than HfO_2. This is related to the different metal-oxygen-Ge and defect formations[11] after a rapid-thermal anneal (RTA). To improve the interface, several passivation methods have been proposed such as plasma nitridation,[4,8] NH_3 treatment, SiH_4 annealing, and interfacial GeO_2 layer[8–10,12–14] at larger EOT, but small EOT less than 1 nm is needed for 32 nm node and beyond.

In this letter, we have applied the ultrathin GeO_2 and SiO_2 interfacial layers[15] into high-κ TiLaO (Ref. 16) epitaxial-Ge/Si n-type MOS (n-MOS) capacitors, where the ultrathin body Ge of 5 nm is directly grown on Si to reach low leakage current. The TiLaO gate dielectric has the merits of unique negative flatband voltage (V_{fb}) from La_2O_3 (Ref. 17) and the much higher κ by adding TiO_2.[16] Such negative V_{fb} is needed for low threshold voltage (V_t) MOSFET. The control TaN/TiLaO/Ge/Si n-MOS capacitor without the ultrathin GeO_2 or SiO_2 interfacial layer showed poor EOT and large V_{fb} degradation after a 550 °C RTA, which is required to activate ion-implanted source-drain in the MOSFET. Such degradations are related to interface reaction and oxygen vacancy formation[18,19] that are much improved by inserting the ultrathin GeO_2 or SiO_2 (Ref. 15) interfacial layer. However, the high-κ TiLaO Ge/Si n-MOS capacitor with interfacial GeO_2 showed much poorer capacitance-voltage (C-V) hysteresis than that using SiO_2 at a smaller EOT less than 1 nm. This is due to the Ge outdiffusion and intermixing of high-κ $TiLaO/GeO_2$ as observed by cross-sectional transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS).

After standard cleaning, a 200 nm undoped Si buffer, 5 nm Ge, and 1.5 nm Si capping layer were epitaxial grown on 6 in. p-type Si substrate (10 Ω cm) by ultrahigh-vacuum chemical-vapor deposition. After removing the native oxide of Si-capping layer, various thick GeO_2 or SiO_2 and 5 nm high-κ TiLaO (Ref. 16) were deposited by physical vapor deposition and followed by postdeposition annealing at 400 °C in oxygen ambient to improve gate dielectric quality. Here the ultrathin Si capping is used to prevent Ge oxidation and process loss, where no interfacial Si was found by cross-sectional TEM after device process. Then a 50 nm TaN was deposited and patterned to form the metal gate. The formed gate stack was applied by a 550 °C RTA that is needed for Ge n-MOSFET fabrication. Finally, Aluminum was deposited on wafer backside to form the MOS capacitors. For comparison, control device without GeO_2 or SiO_2 interfacial layer was also made. The fabricated gate stack was examined by SIMS, TEM, x-ray photoelectron spectroscopy (XPS), and C-V measurements to investigate the physical, chemical bonding, and electrical properties, respectively.

Figure 1 shows the measured C-V characteristics of high-κ TiLaO Ge/Si n-MOS capacitors with or without the interfacial GeO_2 or SiO_2 layer. For device without the inserted GeO_2 or SiO_2 layer, both the capacitance density and V_{fb} were severely degraded. Such V_{fb} roll-off at high temperature was previously reported due to the interface reaction between high-κ and semiconductor.[19] In contrast, the capacitor with GeO_2 or SiO_2 layer shows much improved V_{fb} rolloff even after a 550 °C RTA. Besides, the needed negative V_{fb} of −0.48 V is obtained and important for low V_t Ge n-MOSFET. However, the device with GeO_2 interfacial layer

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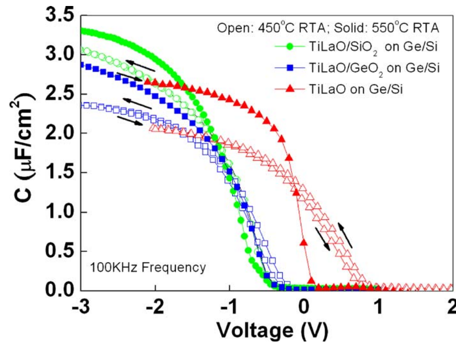

FIG. 1. (Color online) *C-V* characteristics of TaN/TiLaO Ge/Si *n*-MOS capacitors with or without the inserted GeO_2 and SiO_2 interfacial layer and after 450 or 550 °C RTA. The device size is 100×100 μm^2.

shows poorer *C-V* hysteresis of 93 mV at 1.1 nm EOT than the much improved 19 mV hysteresis at smaller 0.81 nm EOT for device using SiO_2 interfacial layer, by taking account of quantum-mechanical effect with parameters of Ge.[7] The *C-V* hysteresis and negative V_{fb} value are among the best reported data for Ge *n*-MOS capacitors at the smallest EOT and after a 550 °C RTA,[1–14] to our best knowledge.

We have used TEM to study the better electrical performance for device using interfacial SiO_2 layer. Figures 2(a) and 2(b) show the TEM images of $TaN/TiLaO/GeO_2/Ge/Si$ *n*-MOS structure before and after a 550 °C RTA. Sharp GeO_2 interfacial layer of 0.76 nm thickness was found for *as-deposited* sample but becomes blurred after the 550 °C RTA. The high-κ layer is also thicker after the 550 °C RTA, where intermixing of high-κ TiLaO and GeO_2 is observed. The thicker high-κ layer explains the lower capacitance density after a 550 °C RTA. In strong contrast, sharp SiO_2 interface shown in Fig. 2(c) is still preserved even after the 550 °C RTA.

We have further used SIMS to study the large difference for devices with different interfacial GeO_2 and SiO_2. Figures 3(a) and 3(b) show the measured SIMS profiles of TaN/TiLaO on Ge/Si structure with interfacial GeO_2 and SiO_2 layers, respectively. Severe Ge outdiffusion was found for device structure with interfacial GeO_2 layer after a 550 °C RTA, while much improved Ge outdiffusion was achieved

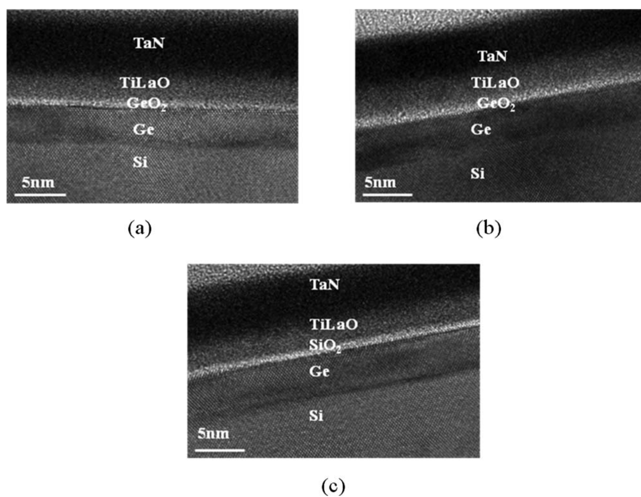

FIG. 2. Cross-sectional TEM images of $TaN/TiLaO/GeO_2/Ge/Si$ *n*-MOS capacitors (a) before and (b) after 550 °C RTA. (c) $TaN/TiLaO/SiO_2/Ge/Si$ *n*-MOS capacitors after 550 °C RTA.

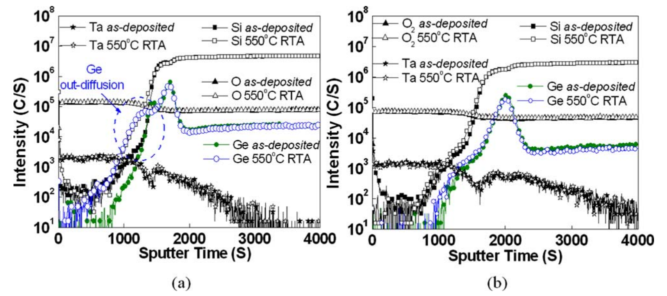

FIG. 3. (Color online) SIMS profile of TaN/TiLaO Ge/Si *n*-MOS structure with inserted (a) GeO_2 and (b) SiO_2 interfacial layer before and after 550 °C RTA.

using ultrathin SiO_2 interfacial layer even at a smaller 0.81 nm EOT.

The degraded interface property with ultrathin interfacial GeO_2 was also examined by XPS. Figure 4 shows the Ge $2p^3$ XPS spectra of $TiLaO/GeO_2/Ge/Si$ *n*-MOS structure before and after the 550 °C RTA. The as-deposited sample shows a strong Ge peak at 1217.4 eV, and a small higher energy side peak is attributed to Ge–O bonds of GeO_2.[20] However, this Ge–O peak becomes much weaker for the sample after the 550 °C RTA. This is consistent with the largely thinned GeO_2 and intermixed $TiLaO/GeO_2$ interface found from cross-sectional TEM and the large Ge outdiffusion measured by SIMS. The thinner interfacial GeO_2 after the high temperature 550 °C RTA may be related to the measured reaction at 758–589 K,[21]

$$GeO_{2(s)} + Ge_{(s)} \rightarrow 2GeO_{(g)}. \quad (1)$$

In contrast, the interface reaction between ultrathin SiO_2 layer and Ge is unfavorable due to the much higher bond enthalpy of SiO_2 (800 kJ/mol) than GeO_2 (659 kJ/mol).[22]

In conclusion, we have studied the high-κ TiLaO on Ge/Si MOS structure with GeO_2 and SiO_2 interfacial layers. Low EOT of 0.81 nm, small *C-V* hysteresis of 19 mV and needed negative V_{fb} are obtained using ultrathin SiO_2 interfacial layer. The device with ultrathin interfacial GeO_2 shows inferior device performance of larger EOT and poor *C-V* hysteresis, which is due to the severe Ge outdiffusion through GeO_2 from SIMS profile, thicker gate dielectric from TEM observation and thinned interfacial GeO_2 after a 550 °C RTA from TEM and XPS analysis.

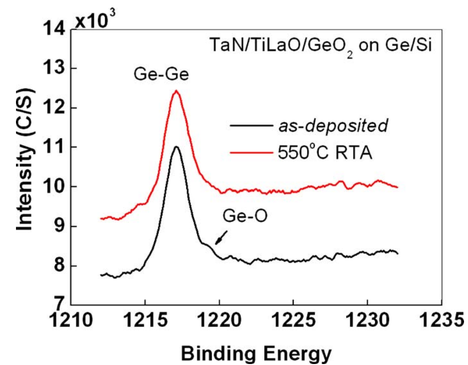

FIG. 4. (Color online) The Ge $2p^3$ XPS spectra of $TiLaO/GeO_2/Ge/Si$ structure before and after 550 °C RTA.

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[1]C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, *Symposium on VLSI Technology Digest* (IEEE, New York, 2003), p. 119.
[2]W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, *Symposium on VLSI Technology Digest* (IEEE, New York, 2003), p.121.
[3]K. Kita, K. Kyuno, and A. Toriumi, Appl. Phys. Lett. **85**, 52 (2004).
[4]T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, Y. Morita, and S. Takagi, Appl. Phys. Lett. **85**, 3181 (2004).
[5]A. Chin, H. L. Kao, Y. Y. Tseng, D. S. Yu, C. C. Chen, S. P. McAlister, and C. C. Chi, *Proceedings of the ESSDERC* (IEEE, France, 2005), p. 285.
[6]V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, Appl. Phys. Lett. **87**, 032107 (2005).
[7]Q. Zhang, J. Huang, N. Wu, G. Chen, M. H. Hong, L. K. Bera, and C. X. Zhu, IEEE Electron Device Lett. **27**, 728 (2006).
[8]T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita, and A. Toriumi Tech. Dig. - Int. Electron Devices Meet. **2007**, 697.
[9]D. Kuzum, A. J. Pethe, T. Krishnamohan, Y. Oshima, Y. Sun, P. Jim McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, Tech. Dig. - Int. Electron Devices Meet. **2007**, 723.
[10]A. Delabie, F. Bellenger, M. Houssa, T. Conard, P. C. McIntyre, S. Van Elshocht, M. Caymax, M. Heyns, and M. Meuris, Appl. Phys. Lett. **91**, 082904 (2007).
[11]G. Mavrou, P. Tsipas, A. Sotiropoulos, S. Galata, Y. Panayiotatos, A. Dimoulas, C. Marchior, and J. Fompeyrine, Appl. Phys. Lett. **93**, 212904 (2008).
[12]J. H. Park, M. Tada, D. Kuzum, P. Kapur, H. Y. Yu, H.-S. P. Wong, and K. C. Saraswat, Tech. Dig. - Int. Electron Devices Meet. **2008**, 389.
[13]Y. Nakakita, R. Nakane, T. Sasada, H. Matsubara, M. Takenaka, and S. Takagi Tech. Dig. - Int. Electron Devices Meet. **2008**, 877.
[14]S. Swaminathan, Y. Oshima, M. A. Kelly, and P. C. McIntyre, Appl. Phys. Lett. **95**, 032907 (2009).
[15]M. F. Chang, P. T. Lee, and A. Chin, IEEE Electron Device Lett. **30**, 861 (2009).
[16]C. H. Cheng, H. C. Pan, H. J. Yang, C. N. Hsiao, C. P. Chou, S. P. McAlister, and A. Chin, IEEE Electron Device Lett. **28**, 1095 (2007).
[17]Y. H. Wu, M. Y. Yang, A. Chin, and W. J. Chen, IEEE Electron Device Lett. **21**, 341 (2000).
[18]J. Robertson, O. Sharia, and A. A. Demkov, Appl. Phys. Lett. **91**, 132912 (2007).
[19]C. F. Cheng, C. H. Wu, N. C. Su, S. J. Wang, S. P. McAlister, and A. Chin, Tech. Dig. - Int. Electron Devices Meet. **2007**, 333.
[20]NIST x-ray photoelectron spectroscopy database, NIST standard reference database 20, version 3.5 (web version), http://srdata.nist.gov/xps.
[21]W. L. Jolly and W. M. Latimer, J. Am. Chem. Soc. **74**, 5757 (1952).
[22]D. S. Yu, A. Chin, C. H. Wu, M.-F. Li, C. Zhu, S. J. Wang, W. J. Yoo, B. F. Hung, and S. P. McAlister, Tech. Dig. - Int. Electron Devices Meet. **2005**, 649.

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