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Electrical characteristics dependence on the channel fin aspect ratio of multi-fin field effect transistors

Hui-Wen Cheng[1] **and Yiming Li**[1,2,3,4]

[1] Institute of Communication Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan
[2] Department of Electrical Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan
[3] National Nano Device Laboratories, Hsinchu 300, Taiwan

E-mail: ymli@faculty.nctu.edu.tw

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Abstract

In this work we investigate the impact of the fin number and structure on device dc and dynamic behaviors of multi-fin field effect transistor (FET) circuits. Based on the same channel volume, multi-fin FETs with different fin aspect ratio (AR ≡ fin height/fin width) are explored using an experimentally validated three-dimensional device simulation. The multi-fin FinFET (AR = 2) has a better channel controllability than the tri-gate (AR = 1) and the quasi-planar (AR = 0.5) FETs. Besides, the 6T SRAM with triple-fin FinFETs provides the largest static noise margin because of the largest transconductance. Notably, though the FinFETs are with a large effective fin width and driving current, the larger gate capacitance may limit the intrinsic device gate delay. The transient characteristics of multi-fin inverters are further examined with different load capacitance (C_{load}). As C_{load} is increased, the impact of the device intrinsic gate capacitance on transient characteristcs is decreased and the delay time compared with that of single-fin inverters is smaller due to being dominated by the driving current of the transistor. Consequently, the multi-fin FinFET circuits exhibit a smallest delay time. The results of the study provide an insight into the dc and transient characteristics of multi-fin transistors and associated digital circuits.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

As the gate length of a metal-oxide-semiconductor field effect transistor (MOSFET) shrinks below 32 nm, performance degradation due to serious short channel effects (SCEs) complicates the technological development in semiconductor industry [1]. Thus, diverse approaches have been proposed [2–10] to enhance the performance of the device, such as strain silicon [2], high-κ/metal gate material [3], and MOSFETs with vertical channels [4–8]. Among these promising techniques, the vertical-channel transistors draw people's attention owing to structural evolution. They feature high current drive, better control over leakage and manufacturing compatibility of MOSFETs. Devices with multiple channel fin (multi-fin) were fabricated recently [9, 10], but a theoretical study on device characteristic has not been clearly drawn yet. Computer simulation of electrical characteristics depending upon the channel fin aspect ratio of multi-fin devices will benefit the technology and design of multi-fin transistors.

In this work, experimentally validated three-dimensional (3D) quantum drift-diffusion device simulation [7, 8, 11, 12] coupled with device-circuit simulation [12, 13] is simultaneously conducted to explore the device and digital circuit characteristics of multi-fn transistors with different fin aspect ratios (AR = 2, 1, 0.5). The electrical characteristics of the devices are studied in terms of the threshold voltage (V_{th}) roll-off, driving current, transconductance, gate capacitance and intrinsic gate delay characteristics. In addition, the static noise margin (SNM) of the state-of-the-art static random-access memory (SRAM) using six multi-fin

[4] Author to whom any correspondence should be addressed.

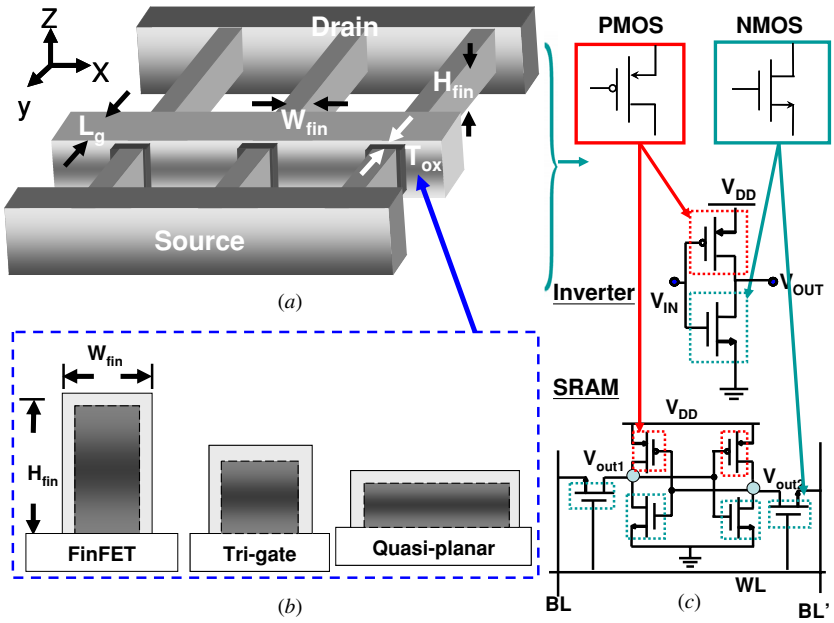

Figure 1. (*a*) A schematic and (*b*) cross-section view of the multi-fin MOSFET. Three different channel fin aspect ratio transistors are studied; they are FinFET (i.e., device with AR = 2), tri-gate (AR = 1) and quasi-planar (AR = 0.5) devices, respectively. (*c*) Inverter and SRAM are used as the tested digital circuits. BL and BL′ are bit lines; WL is the word line.

FETs is investigated to examine the transfer characteristics. The transient characteristics are also examined through the estimation of the delay time of the inverter circuit with multi-fin transistors.

This paper is organized as follows. Section 2 describes the explored devices and simulation procedure. In section 3, we report the characteristic sensitivity and transient behavior of the studied devices including SRAM and inverter circuit. Finally, we draw the conclusions and suggest future work.

2. The multi-fin structure and simulation methodology

Figure 1(*a*) illustrates the structure of studied 3D triple-fin transistors, where the transistors are with different AR. The ARs of FinFETs, tri-gate MOSFETs and quasi-planar MOSFETs are defined as 2, 1 and 0.5, respectively, as shown in figure 1(*b*). The dimensions of three fin shapes and adopted device parameters of N-typed transistors are summarized in tables 1 and 2; for P-typed devices, not shown here, we have similar parameters. To compare the device characteristics based upon a fair basis, the cross-section areas of the fin for the explored devices are fixed at about 128 μm^2. For devices' gate length starting from 32 nm, all threshold voltages of the explored transistors are first calibrated to 200 mV in order to examine V_{th} roll-off. The very similar cross-section area and V_{th} indicate having the same control volume of the device channel under the same operation condition. The device transport characteristics are then calculated by solving a set of 3D density-gradient equations coupled with Poisson equations as well as electron–hole current continuity equations [7, 8, 11, 12] under our parallel computing system [14, 15]. Figure 1(*c*) shows that the simulated 6T SRAM and inverter

Table 1. The dimension of channel fin height and channel fin width corresponding to three fin shapes: FinFET (AR = 2), tri-gate (AR = 1) and quasi-planar (AR = 0.5).

	AR = $\frac{H_{fin}}{W_{fin}} = 0.5$	AR = $\frac{H_{fin}}{W_{fin}} = 1$	AR = $\frac{H_{fin}}{W_{fin}} = 2$
H_{fin} (nm)	8	11.3	16
W_{fin} (nm)	16	11.3	8

Table 2. A list of device parameters for the explored N-typed transistors.

Parameter	Range
L_g (nm)	16–32
T_{ox} (nm)	1.2
Channel doping (cm^{-3})	1.48×10^{18}
S/D doping (cm^{-3})	$\sim 3 \times 10^{20}$
Gate workfunction	~4.4 eV

circuit using the 16 nm gate multi-fin devices are investigated for transfer and transient characteristics. There is no well-established compact model for 16 nm gate multi-fin devices, so the dynamic characteristic of the digital circuit is directly estimated using a coupled device-circuit simulation approach [12, 13]. It is worth noting that the physical models adopted in the 3D quantum-mechanically corrected device equations were calibrated with the fabricated and measured samples for the best accuracy [8].

3. Results and discussion

In this section, we first discuss the dc characteristics of the N-typed single- and multi-fin FETs. Based on the results of N- and P-typed FETs, we examine the transfer characteristics and

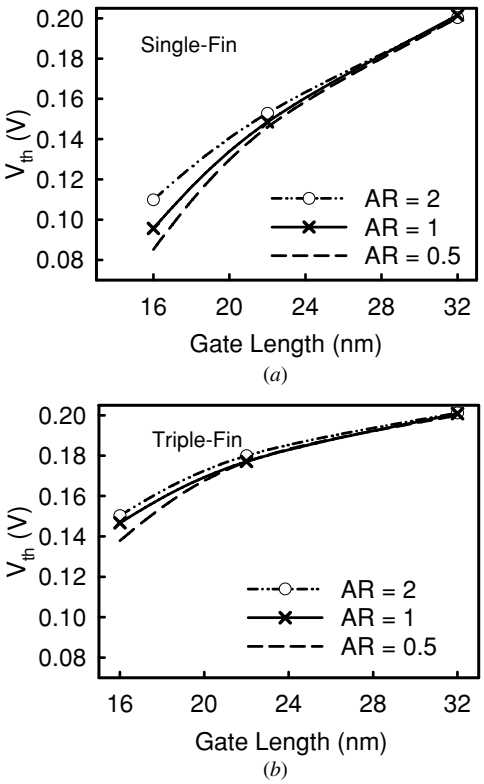

Figure 2. Plots of V_{th} roll-off characteristics for the 16 nm gate N-typed (*a*) single-fin and (*b*) triple-fin MOSFETs with different fin aspect ratios.

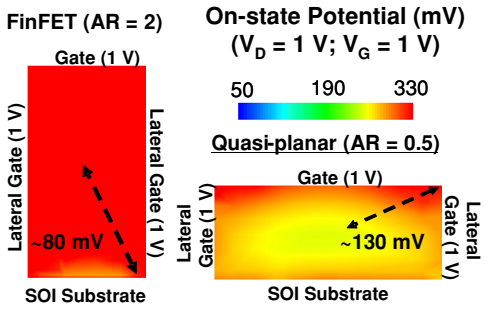

Figure 3. The on-state potential distribution of the FinFET (AR = 2) and quasi-planar (AR = 0.5), where the gate length of the device is 16 nm.

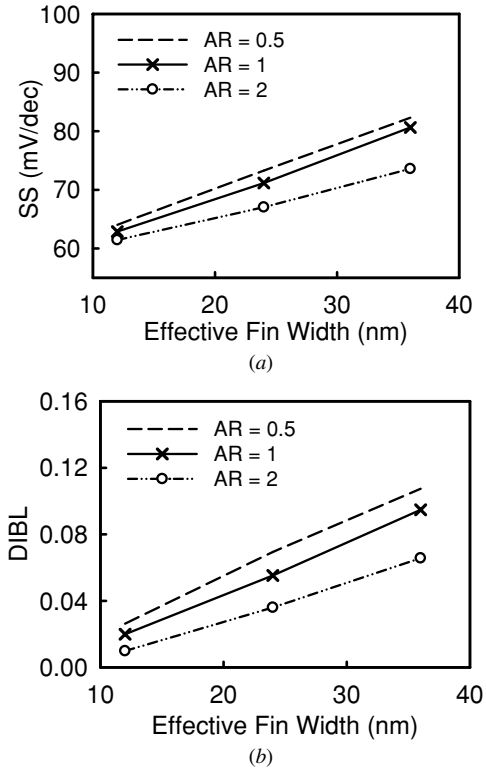

Figure 4. Plots of (*a*) SS and (*b*) DIBL as a function of the effective fin width for the studied 16 nm gate N-typed multi-fin transistors.

SNM of the 16 nm gate single- and multi-fin SRAM circuits. We further calculate the device capacitance for the analysis of the dynamic behavior of the CMOS inverter using 16 nm gate single- and multi-fin FETs.

Figures 2(*a*) and (*b*) show the V_{th} roll-off characteristics for the examined single- and triple-fin N-FETs with respect to different fin aspect ratios. The gate length of the devices varies from 32 nm to 16 nm. The results show that the multi-fin FinFET structure with AR = 2 is less sensitive to the gate length scaling. The alleviation of V_{th} roll-off implies that the FinFET possesses the better channel controllability and resistance to the intrinsic device parameter variations. Figure 3 shows the potential profile of the N-typed multi-fin FinFET and quasi-planar transistors. According to Coulomb's law, the FinFET structure has larger perimeter between two lateral gates, and therefore exhibits a more uniform potential profile than the quasi-planar structure. In addition, the longitudinal electric field within the fin will increase as the fin height is scaled down; consequently, it degrades the carrier mobility and limits the device saturation current. For the considered N-typed multi-fin transistors, figures 4(*a*) and (*b*) show that the transistor structure with AR = 2 has lower calculated subthreshold swing (SS) and drain-induced-barrier-lowering (DIBL) than that AR = 1 and 0.5. The effective fin width is $n \times (2 \times H_{fin} + W_{fin})$ (where n is the number of fins, H_{fin} is the fin height and W_{fin} is the fin width, as indicated in figure 1(*b*)). The layout area efficiency of FinFETs is higher than that of tri-gate and quasi-planar devices. For example, to have a device with SS < 70 mV dec^{-1}, the layout area of FinFETs is 1.67 and 1.33 times smaller than that of tri-gate and quasi-planar structures, as shown in figure 4(*a*).

Figure 5(*a*) shows the on-state current (I_{on}, at the bias condition: $V_D = V_G = 1$ V) of the explored 16 nm gate N-typed transistors, whose V_{th} are calibrated. Equation (1) estimates the dependence of I_{on} on the fin number and fin geometry:

$$I_{on} \approx \frac{n(2 \cdot AR + 1) \cdot W_{fin} \cdot \mu \cdot C_{ox}}{L}(V_G - V_{th})^2, \qquad (1)$$

where C_{ox} is the capacitance of per unit gate area, L is the gate length, μ is the mobility and V_G is the gate voltage. The device with a higher aspect ratio and more number of

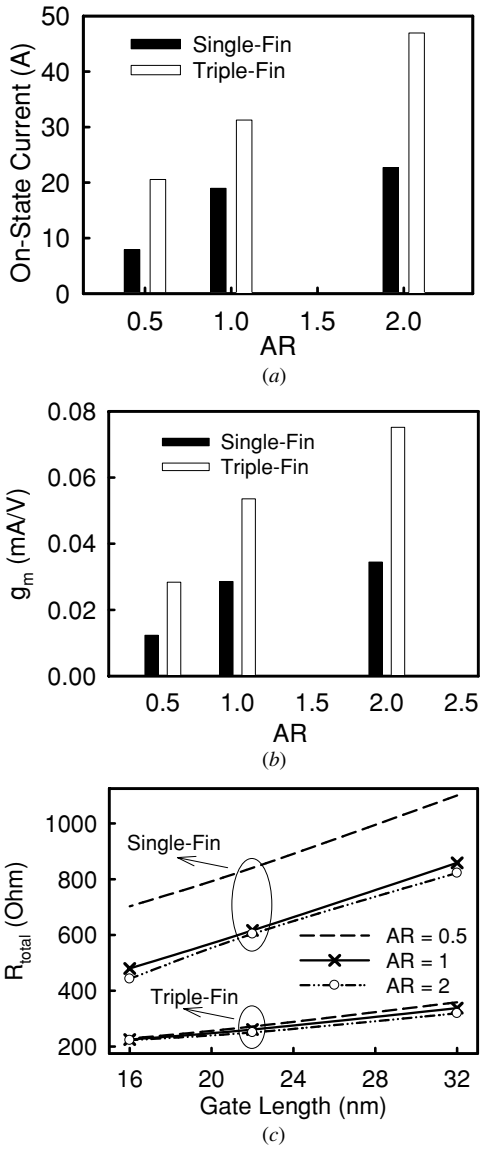

Figure 5. Plots of the (*a*) on-state current and (*b*) maximum transconductance for the studied 16 nm gate N-typed single- and multi-fin transistor with respect to different ARs. (*c*) Plot of the total output resistance (R_{total}) versus the gate length with respect to different ARs.

fins possesses a large on-state current. The FinFET structure provides 1.2 and 2.9 times larger I_{on} than the tri-gate and quasi-planar MOSFETs. Moreover, the triple-fin FinFETs offer a 2.1 times better driving capability than that with a single-fin structure. Figure 5(*b*) shows that the FinFET structure has the maximum transconductance ($g_{m,max}$) among these explored transistors, especially for the multi-fin structure. Generally speaking, the multi-fin device with a larger AR results in a larger on-state current as well as a smaller output resistance of the transistor which is smaller than that of a single-fin device, as shown in figure 5(*c*). Likewise, not shown here, we have also simulated the P-typed devices. We note that theoretically, the on-state current obtained from equation (1) is the approximation only in a gradual channel. It can be used only for qualitative discussion when the problem was solved using computer simulation.

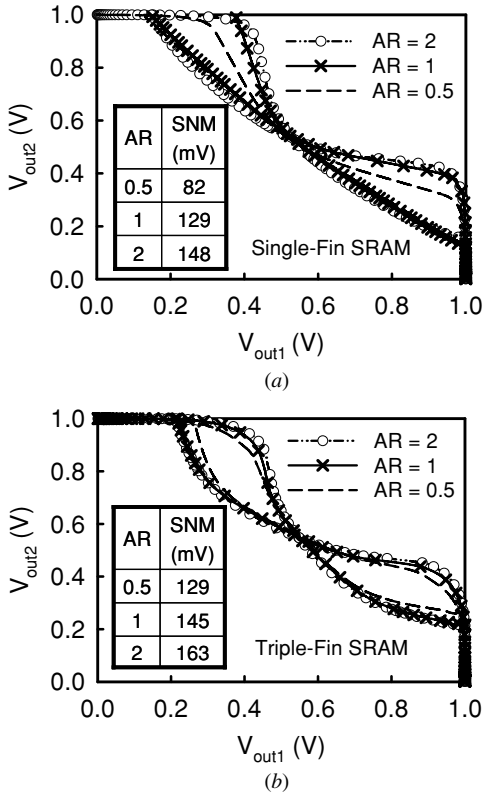

Figure 6. Plots of the SNM of the 6T SRAM, as shown in figure 1(*c*), with the 16 nm gate (*a*) single-fin and (*b*) triple-fin transistors, where V_{out1} and V_{out2} refer to the symbols, as shown in figure 1(*c*).

The calculated static noise margins of the 6T SRAM with 16 nm gate single- and triple-fin FinFETs are shown in figures 6(*a*) and (*b*). Here, the V_{th} of all 16 nm gate transistors has been calibrated to 200 mV. Based upon the 3D device simulation transfer curves, we can obtain SNMs which are numerically calculated by drawing and mirroring the inverter characteristics and find the maximum possible square between them [16]. The relation between the device transconductance and SNM of SRAM could be expressed as [17]

$$\mathrm{SNM} \propto \sqrt{1 - \frac{I_{nx}}{g_{m,pmos}}} - \frac{I_{ax}}{g_{m,nmos}}, \qquad (2)$$

where I_{nx} is the saturation drain current of the driver transistor of SRAM and I_{ax} is the saturation drain current of the access transistor. The simulation result shows that the large g_m of triple-fin FinFETs enlarges the SNM, as shown in figure 6(*b*). The 6T SRAM with 16 nm gate triple-fin FinFETs has a relatively larger SNM (about 163 mV from the inset of figure 6(*b*)) than that of single-fin FinFETs. Therefore, for the SRAM circuit, using a multi-fin FinFET structure is an effective way to improve performance. As described hereinbefore, the multi-fin FinFETs possess a better channel controllability, layout efficiency, driving current and SNM than the transistors with smaller aspect ratios, such as tri-gate and quasi-planar MOSFETs. It is known that the large I_{on} of multi-fin FinFETs provides fast charge and discharge capabilities; however, the increase of AR and fin number also increases the intrinsic gate capacitance (C_g) of transistors. Figure 7(*a*)

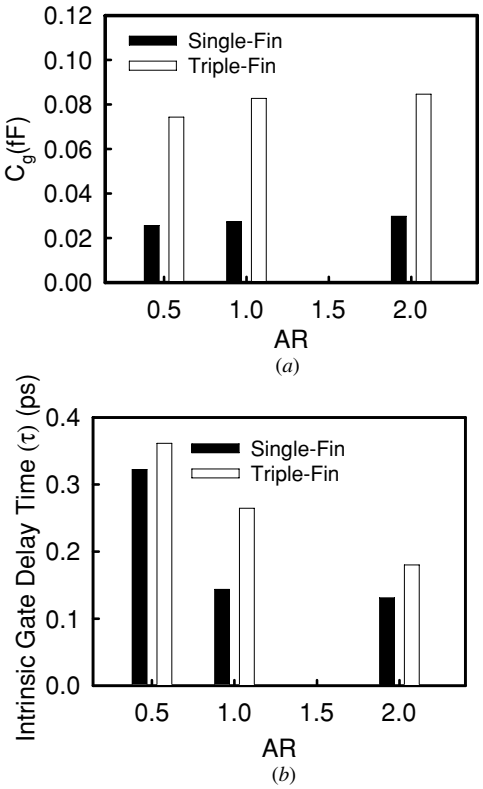

Figure 7. Plots of the (*a*) device gate capacitance and (*b*) intrinsic gate delay for the studied 16 nm gate N-typed single- and multi-fin transistor with different AR.

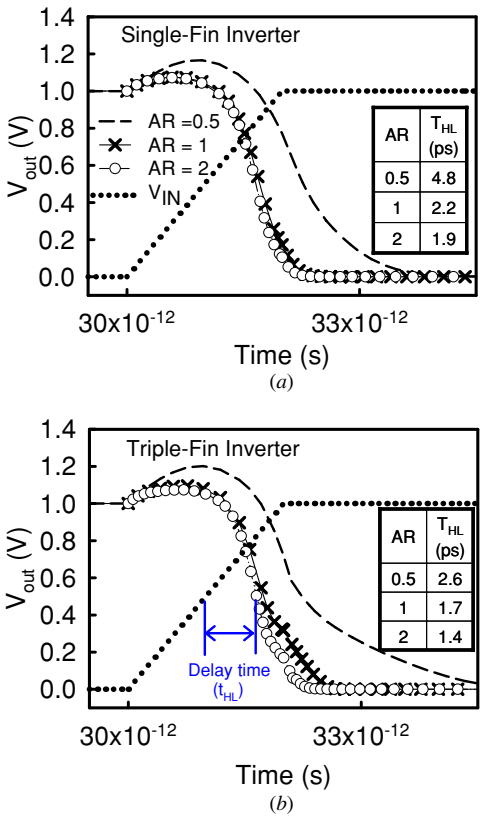

Figure 8. The transient characteristics of the (*a*) single- and (*b*) multi-fin inverters.

plots the C_g of the explored 16 nm gate single- and triple-fin transistors versus different ARs, where C_g is one of the important indexes for channel controllability. The C_g of 16 nm gate triple-fin transistors is about three times larger than that of single-fin transistors. Additionally, compared with the triple-fin quasi-planar MOSFETs, the C_g of the triple-fin FinFETs is increased by a factor of 1.13. Though the large C_g of the multi-fin transistor with a large aspect ratio can enhance the channel controllability, the increased C_g impacts the speed of the transistor. Therefore, the intrinsic gate delay of the transistor ($\tau = C_g V_{DD}/I_{on}$) is calculated, as shown in figure 7(*b*), to study the trade-off between I_{on} and C_g. We find that the intrinsic gate delay is dominated by C_g and the single-fin transistor exhibits a smaller delay than the multi-fin transistors. For example, the intrinsic gate delay of the triple-fin FinFET is 1.4 times slower than that of the single-fin FinFET transistor. The degraded intrinsic gate delay of the transistor may also impacts the cutoff frequency in high-frequency applications.

Figures 8(*a*) and (*b*) are the high-to-low transition characteristics for single- and triple-fin inverters with respect to different aspect ratios, in which the transistor's intrinsic C_g is used as the load capacitance (C_{load}). The solid lines are the output signal of devices with different fin shapes; the dotted line is the input signal. The rise time, fall time and hold time of the input signal are 2 ps, 2 ps and 30 ps, respectively. The high-to-low delay time (t_{HL}) is defined as the difference between the times of the 50% points of the input and output signals during the falling of the output signal. The delay times of the studied single- and multi-fin transistors are summarized in the inset of figures 8(*a*) and (*b*), respectively. As expected, both single- and multi-fin FinFET inverters present smallest t_{HL} among different ARs, and show the benefits of the FinFET structure in both dc and transient characteristics. In order to examine the associated delay time of the digital circuit, a load capacitance (C_{load}) is further added on the inverter circuits which is composed of the C_g of the N-FET and P-FET, as illustrated in figures 9(*a*) and (*b*). For the increased load capacitance, the required charge and discharge time are increased. Completely different from figure 7(*b*), the delay times of the triple-fin inverters are smaller than those of the single-fin inverters, since the delay time is dominated by the driving capability of transistors. As shown in figure 9, the solid lines are the inverter with merely the intrinsic device gate capacitance; the dashed and dashed-dotted lines are the inverter with the capacitive load of 1 fF and 10 fF, respectively. The delay time increases significantly as the load capacitance increases. For the multi-fin FinFET inverter with $C_{load} = 10$ fF, the delay time approaches 50 ps, which is 30 times larger than that of the inverter only with the intrinsic device gate capacitance. Because the load capacitance dominates the overall capacitive load, the difference of the device's intrinsic gate capacitance resulted from the fin structure becomes negligible. For the triple-fin FinFET inverter with $C_{load} = 10$ fF, the delay time is about two times smaller than that of the single-fin FinFETs. The multi-fin transistor provides a smaller transition delay than that of the single-fin transistor due to the increase of the driving current. In addition, the result shows that the multi-fin

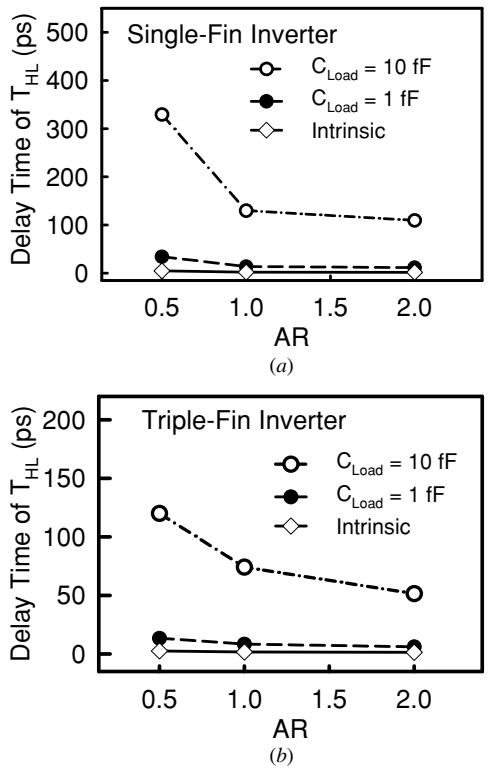

Figure 9. The delay time of the (*a*) single- and (*b*) multi-fin inverters with different load capacitances.

transistor with the FinFET structure exhibits a smallest delay time to benefit the timing of digital circuits. It is worth noting that the delay time for multi-fin FinFET inverters increases by a factor of 50, as the load capacitance increases from the device's intrinsic capacitance to 10 fF. Nevertheless, the delay time increases 70 times for multi-fin quasi-planar inverters. The increased difference of the delay time for the quasi-planar transistor indicates that the high driving current of the FinFET mitigates the impact of load capacitance variation from passive components.

4. Conclusions

In this study, the dc and transient behavior of 16 nm gate single- and multi-fin device with respect to different fin aspect ratios have been numerically investigated for the first time. The multi-fin device could offer a smooth V_{th} roll-off characteristic due to the larger effective device width. Especially for the multi-fin FinFET (AR = 2), it presents rather interesting dc and ac characteristics, compared with the devices with smaller ARs. Though the larger gate capacitance might degrade the device intrinsic gate delay, the multi-fin FinFET has provided small delay time in digital circuit applications due to the large driving current. The results of this study have shown that increasing the number of channel fins and higher AR might have promising timing characteristics in digital circuits, but the increase of gate should be treated carefully when the value of gate capacitance is similar to the load capacitance. The larger AR of the channel fin has improved the device performance; nonetheless it may aggravate the process variation effect [8]. Therefore, determination of an optimal fin number and the impact of pinch distance among channel fins are currently under consideration.

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