The Dependence of the Performance of Strained NMOSFETs on Channel Width

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***Abstract*—The dependence of the performance of strained NMOSFETs on channel width was investigated. When the channel width was varied, the stress in the channel varied accordingly. This changed the electron effective mass and, consequently, the ON-state current $I_{\rm on}$. By shrinking the channel width of a strained NMOSFET from 1 to 0.1 μm and by keeping the channel length at 55 nm, the ON-state drain current per unit channel width was enhanced by 22%. The gate leakage current was also affected by the stress in the channel, which can be explained by the increase in hole barrier height at the Si/SiO_2 interface. Furthermore, when the film stress was increased by 1 GPa, the gate leakage current density J_g of a strained NMOSFET with a channel width of 0.1 μm and a length of 55 nm under a negative bias −3 V was reduced by 63%.**

***Index Terms*—Contact etch stop layer (CESL), high-stress silicon nitride, MOSFET, strained silicon.**

I. Introduction

THE USE OF a contact etch stop layer (CESL) is one of the key methods to boost the performance of nanometer-scale MOSFETs [1]–[3]. The stress in the channel of a CESL-strained MOSFET can be enhanced by increasing the CESL film stress and the CESL thickness and by optimizing the device structure [1], [2]. The stress in the channel is also observed to depend on the layout of a MOS transistor [3]. However, few studies have been carried out to increase the stress in the channel by properly choosing the channel width. The optimal channel width to reach an $I_{\rm on}$ gain for a CESL-strained NMOSFET with a channel length of 55 nm has already been reported [4]. The stress in the channel is also found to affect the gate leakage current density J_g. However, the dependence of J_g on the channel width has not been fully investigated. This brief examined the dependence of $I_{\rm on}$ and J_g on the channel width, and its scope has been extended to the channel width for CESL-strained NMOSFETs with channel lengths ranging from 1 μm to 55 nm.

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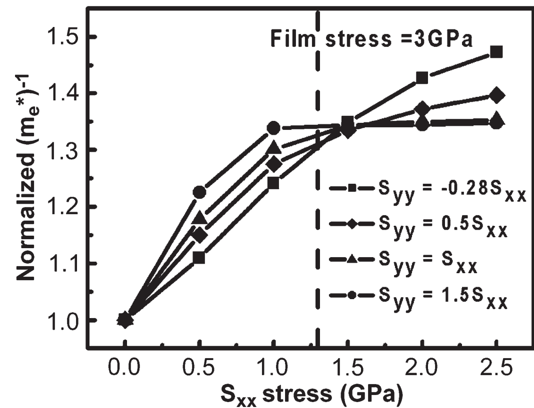

Fig. 1. Calculated inverse of the electron effective mass plotted as a function of S_{xx} in the channel. Various S_{yy}/S_{xx} ratios −0.28, 0.5, 1 (biaxial stress), and 1.5 are depicted.

II. Experiment

In this brief, NMOSFETs were processed using shallow trench isolation (STI), nitrided-SiO_2 gate dielectric, n+ polycrystalline silicon gate, and tensile silicon nitride CESL [5]. The filling material of the STI was silicon oxide that was deposited by a high-density-plasma chemical-vapor-deposition (CVD) process. The STI process followed the conventional STI process reported in [6]. The effective oxide thickness was about 1.9 nm, which was measured on a large gate square and operated at 1.1 V. The CESL was deposited by a CVD process. The 3-D stress distribution with different device geometric structures was simulated by a 3-D finite element mechanical stress simulation program, ANSYS. In the simulation, the elastic analysis was restricted to the effect of the nitride layer on the channel [7]. The change in the effective mass under the stress was calculated by the $k \cdot p$ model [8], [9].

III. Results and Discussion

Fig. 1 shows the calculated inverse electron effective mass m_e^* as a function of the simulated S_{xx}. Various S_{yy}/S_{xx} ratios of −0.28, 0.5, 1 (biaxial stress), and 1.5 are depicted. S_{xx} and S_{yy} represent the stresses in the channel, which are in parallel and transverse to the direction of the current flow. The inverse m_e^* is observed to increase with an increase in S_{xx} when the

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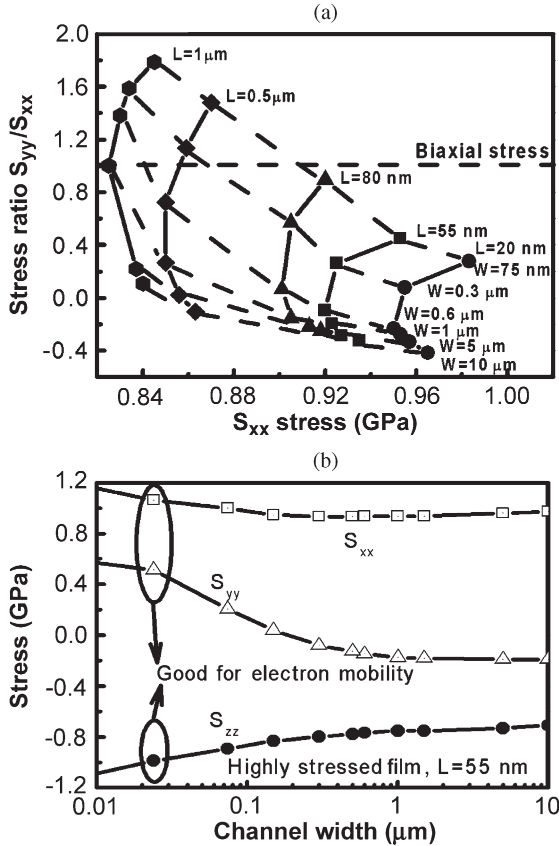

Fig. 2. (a) Calculated S_{yy}/S_{xx} plotted as a function of S_{xx} with various combinations of channel length and channel width. (b) Stress components plotted as a function of channel width for NMOSFETs with $L = 55$ nm.

value of S_{xx} is smaller than about 1.5 GPa. Furthermore, the film stress after annealing must be greater than 3 GPa to give an S_{xx} of 1.5 GPa in the simulation. It is unlikely that silicon nitride would ever reach such a high tensile film stress [10]. Thus, S_{xx} that is below approximately 1.5 GPa has been the focus of this study. Moreover, m_e^* is observed to further reduce with an increasing ratio of S_{yy}/S_{xx} from -0.28 to 1.5.

Fig. 2(a) shows the ways to reach a high S_{yy}/S_{xx} (small m_e^*) by optimizing the dimensions of the NMOSFETs. The calculated S_{yy}/S_{xx} was plotted as a function of S_{xx} with various combinations of channel length L and channel width W. For example, consider the curve with $L = 55$ nm in Fig. 2(a). It can be observed that, when W decreases from 10 to 0.6 μm, S_{yy}/S_{xx} increases; however, S_{xx} decreases with the reduction in W. When W decreases further from 0.6 μm to 75 nm, S_{yy}/S_{xx} keeps increasing with the reduction in W, but S_{xx} changes from a decreasing to an increasing value with the reduction in W. Fig. 2(b) (in our previous work, , Fig. 1(b)[4]) provides an explanation for this phenomenon. When W is greater than 0.6 μm, S_{yy} increases, whereas S_{xx} decreases, and, therefore, S_{yy}/S_{xx} increases with a reduction in W. Both S_{yy} and S_{xx} increase with a reduction in W when W is lesser than 0.6 μm. The rate of increase in S_{yy} with decreasing W is observed to be about eight times of that for S_{xx}. As a result, S_{yy} is found to dominate the width dependence of S_{yy}/S_{xx}, and the S_{yy}/S_{xx} ratio is observed to increase with a reduction in W. In

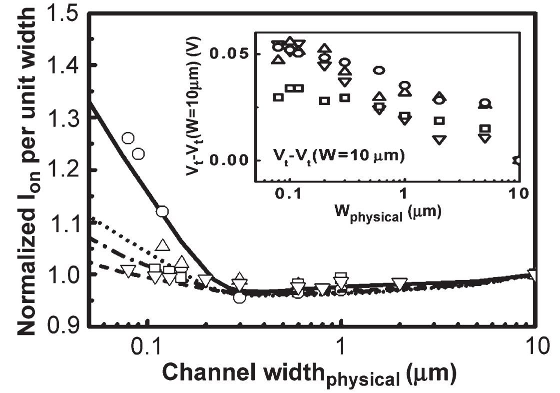

Fig. 3. Experimental $I_{\rm on}$ per unit width compared to the theoretical calculation is plotted as a function of channel width. (—) Theoretical $I_{\rm on}$, $L_{\rm physical} = 55$ nm (quasi-ballistic model). (···) Theoretical $I_{\rm on}$, $L_{\rm physical} = 80$ nm (quasi-ballistic model). (-.-) Theoretical $I_{\rm on}$, $L_{\rm physical} = 0.5$ μm (drift-diffusion model). (- - -) Theoretical $I_{\rm on}$, $L_{\rm physical} = 1$ μm (drift-diffusion model). (○) Measured $I_{\rm on}$, $L_{\rm physical} = 55$ nm. (△) Measured $I_{\rm on}$, $L_{\rm physical} = 80$ nm. (□) Measured $I_{\rm on}$, $L_{\rm physical} = 0.5$ μm. (▽) Measured $I_{\rm on}$, $L_{\rm physical} = 1$ μm. The value for the devices with $W = 10$ μm is normalized as one. The inset in Fig. 3 shows $V_t - V_t$ ($W = 10$ μm) as a function of channel width. (○) $L_{\rm physical} = 55$ nm. (△) $L_{\rm physical} = 80$ nm. (□) $L_{\rm physical} = 0.5$ μm. (▽) $L_{\rm physical} = 1$ μm.

addition, S_{xx} is found to take up a minimum value when W is about 0.6 μm, which gives rise to the turnaround in the curve with $L = 55$ nm [Fig. 2(a)]. A similar analysis can be applied to other L values.

As shown in Fig. 2(a), to reduce m_e^* by a large S_{yy}/S_{xx} ratio, the smallest W should be used. Furthermore, S_{xx} and S_{yy} became more tensile, and S_{zz} became more compressive with a decrease in W, and this trend was preferred to increase the electron mobility [2], [4]. Thus, the preferred S_{xx}, S_{yy}, and S_{zz} stresses and S_{yy}/S_{xx} ratio could be reached by adopting the smallest W value.

To prove the mechanism mentioned earlier, the measured $I_{\rm on}$ per unit width of the strained NMOSFETs with various W and L values is presented in Fig. 3. By reducing the value of W from 1 to 0.1 μm, the $I_{\rm on}$ per unit width was observed to increase to about 1%, 2%, 7%, and 22% for L of 1 μm, 0.5 μm, 80 nm, and 55 nm, respectively. Furthermore, the magnitude of the increase in the $I_{\rm on}$ per unit width increased with decreasing channel length mainly because of the smaller separation distance between the center of the channel and the sources of the applied stress with decreasing L. Thus, the film stress became more effective to affect the stress in the channel and reduce the electron effective mass. Furthermore, the film stress was also more effective in increasing $I_{\rm on}$. The stress-induced enhancement of the electron mobility was applied to the theoretical calculation of NMOSFETs with an L of 1 and 0.5 μm, based on the drift-diffusion model [11]. However, ballistic transport was observed in nano-MOSFETs [12]. To resolve this problem, a quasi-ballistic transport model was used for nano-NMOSFETs with an L of 80 and 55 nm (Fig. 3). The details of the calculation using quasi-ballistic transport were reported in [8] and [12]–[14].

To further validate the stress mechanism discussed earlier, J_g under the stress described in Fig. 2(a) was also studied. Fig. 4 shows the measured J_g as a function of W under

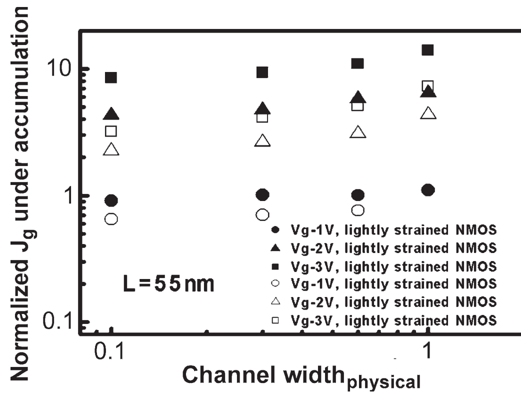

Fig. 4. I_g of the highly and lightly strained NMOS devices is plotted as a function of channel width. The CESL stress for the highly strained devices is 1 GPa higher than that for the lightly strained ones. $V_{\mathrm{substrate}} = 0$ V in this measurement.

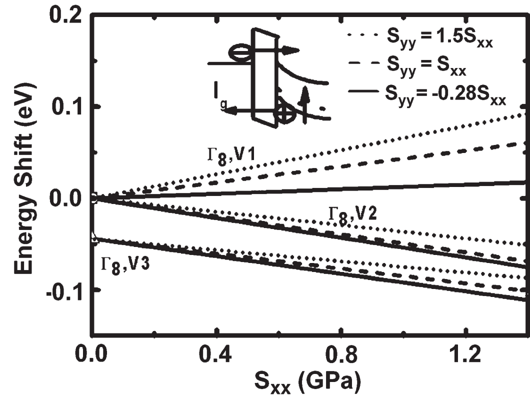

Fig. 5. Calculated valence band splitting of light holes (V1), heavy holes (V2), and split-off holes (V3) are plotted as a function of stress S_{xx}. Various S_{yy}/S_{xx} ratios from -0.28 to 1.5 are depicted.

accumulation. Both the highly and lightly strained NMOSFETs were measured, and the CESL stress for the highly strained devices was 1 GPa higher than the lightly strained ones. The J_g of the highly strained NMOSFET with a W/L of 0.1 μm/55 nm was reduced by 63% compared that of the lightly strained one under a negative bias of -3 V. Furthermore, the J_g of the lightly strained devices was reduced by about 17%, 33%, and 39% by decreasing W from 1 to 0.1 μm under V_g biases of -1, -2, and -3 V, respectively, and that of the highly strained devices by about 40%, 48%, and 56%, respectively. Thus, J_g could be reduced by decreasing W from 1 to 0.1 μm, and this effect was more obvious for the highly strained devices. Generally, the J_g of NMOSFETs with a smaller W was higher than those with a higher W because J_g near the STI edge was higher [15]–[17]. Hence, the J_g reduction in Fig. 4 may not have been caused by the STI process. Furthermore, the energy bands of the strained silicon and carrier distribution were altered by stress [2]. The influence of stress on the electron barrier height was relatively insignificant because the work functions of conductors and heavily doped polycrystalline silicon changed relatively little by stress [18]. Thus, the effect was mainly on holes. The calculation of the splitting of the sixfold degenerate valence band was reported in [19]. It involved linear splitting and spin-orbit splitting, expressed in terms of deformation potentials. The spin-orbit splitting for silicon was very small ($\sim$0.04 eV), and, hence, this term was neglected in the calculation. The required parameters to calculate the deformation potential can be obtained from [19]–[21]. The calculated result is shown in Fig. 5. A higher S_{yy}/S_{xx} value was observed to cause a greater shift of the valence band edge. Thus, the barrier height for light holes increased, and the probability of the hole injecting into the gate was reduced, which explains the reduction in J_g in Fig. 4. This J_g reduction was found to be more effective with decreasing channel length. This can be explained by the fact that the separation distance between the center of the channel and the sources of the applied stress became closer with decreasing channel length. As a result, for an NMOSFET with smaller channel length, the CESL film stress may become more effective to affect the stress in the channel and to increase the barrier height for light holes. Thus, the CESL film stress may be more effective in reducing J_g.

IV. Conclusion

Thus, in this study, the dependence of the performance of silicon-nitride-strained NMOSFETs on channel width was investigated. When the value of W was varied, the stress in the channel varied accordingly. This changed m_e^* and, consequently, I_{on}. By reducing the value of W, S_{xx} and S_{yy} became more tensile, S_{zz} became more compressive, and the S_{yy}/S_{xx} ratio became higher. All these changes aided in the reduction in m_e^* and increased the value of I_{on}. By decreasing the value of W from 1 to 0.1 μm, the I_{on} per unit width was observed to increase by about 1%, 2%, 7%, and 22% for an L of 1 μm, 0.5 μm, 80 nm, and 55 nm, respectively. The stress in the channel also reduced the value of J_g. This was explained by an increase in the barrier height for light holes. When the film stress was increased by 1 GPa, the J_g of an NMOSFET with a W/L of 0.1 μm/55 nm was reduced by 63% under a negative bias of -3 V.

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M. S. Liang, photograph and biography not available at the time of publication.