Improved Electrical Performance and Uniformity of MILC Poly-Si TFTs Manufactured Using Drive-In Nickel-Induced Lateral Crystallization

Chih-Pang Chang and YewChung Sermon Wu

Abstract—**A new manufacturing method for polycrystalline silicon (poly-Si) thin-film transistors (TFTs) using drive-in nickel-induced lateral crystallization (DILC) was proposed. In DILC, a F^+ implantation was used to drive Ni in the α-Si layer. To reduce Ni contamination, the remained Ni film was then removed and subsequently annealed at 590 °C. It was found that DILC TFTs exhibit high field-effect mobility, low threshold voltage, low subthreshold slope, high ON-state current, lower trap-state density, smaller standard deviations, and low OFF-state leakage current compared with conventional Ni-metal-induced lateral crystallization TFTs.**

Index Terms—**Drive-in nickel-induced lateral crystallization (DILC), fluorine ion (F^+) implantation, thin-film transistors (TFTs), uniformity.**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable interest for their application in active-matrix organic light-emitting diode (AMOLED) displays [1]. The luminance of the OLED material is proportional to the amount of current passing through it. Therefore, a pixel-to-pixel array needs to give uniform currents to the OLED material for the sake of creating uniform light [2].

Intensive studies on reducing the crystallization time and temperature of amorphous silicon (α-Si) have been carried out. Ni-metal-induced lateral crystallization (MILC) is one of these efforts [3], [4]. Unfortunately, poly-Si/oxide interfaces and grain boundaries trap Ni and $NiSi_2$ (Ni-related defects), which degrades its electric performance [5], [6]. There have been several attempts to reduce Ni contamination; however, all these require complex steps [7]–[9]. Recently, a fluorine ion (F^+) implantation and a CF_4-plasma treatment have been employed to improve the electrical performance of MILC TFTs [10], [11]. It was found that fluorine atoms effectively minimize the trap-state density.

Manuscript received July 31, 2009. First published October 6, 2009; current version published October 23, 2009 This work was supported in part by Sino-American Silicon Products Inc. and in part by the National Science Council of Taiwan under Grant 95-2221-E009-087-MY3. The review of this letter was arranged by Editor A. Nathan.

The authors are with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: chihpang.chang@gmail.com; SermonWu@stanfordalumni.org).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2009.2031130

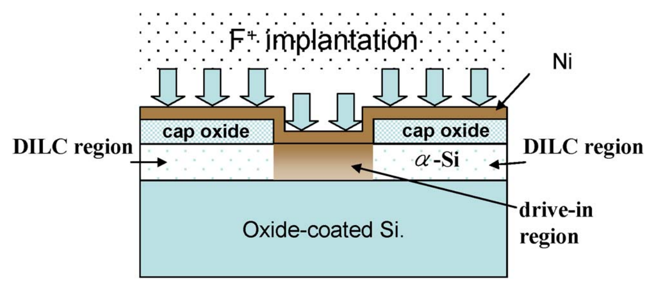

Fig. 1. Schematic illustration of the F^+ implantation process to drive Ni in the α-Si layer.

In this letter, a drive-in nickel-induced lateral crystallization (DILC) process was developed to reduce the Ni concentration and minimize the trap-state density of MILC TFTs.

II. Experiment

The preparation of DILC poly-Si began with a 4-in Si wafer. A 120-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by a low-pressure chemical vapor deposition system. A 65-nm-thick cap oxide was deposited and patterned to form 20-μm-wide lines, and a 20-Å-thick Ni film was then deposited. The samples were subjected to a F^+ implantation to drive Ni in the α-Si layer, as shown in Fig. 1. For the α-Si layer under the Ni line, the projection range was set at the middle of the α-Si layer. At the same time, for the α-Si layer under the oxide layer, it was located at the cap-oxide/α-Si interface. The dosage of F^+ ranged from 2×10^{12} to 2×10^{15} cm^{-2}. The ion-accelerating energy was 35 keV.

To reduce the Ni contamination/concentration, the remained Ni film and cap oxide were then removed by chemical etching and subsequently annealed at 590 °C for 3 h to form the DILC poly-Si. The islands of poly-Si regions were defined by reactive ion etching with the channels at the lateral growth region, which was 10 μm away from the Ni line and the front of the DILC poly-Si grains. TFT devices were fabricated by standard IC processes, as described elsewhere [11]. For the purpose of comparison, conventional MILC was prepared [11]. It is worthy to note that this DILC process does not need any additional annealing step and is compatible with MILC processes.

III. Results and Discussions

The MILC and DILC lengths that are perpendicular to the Ni lines are plotted as a function of annealing time in Fig. 2. The growth rate as a function of annealing time was estimated

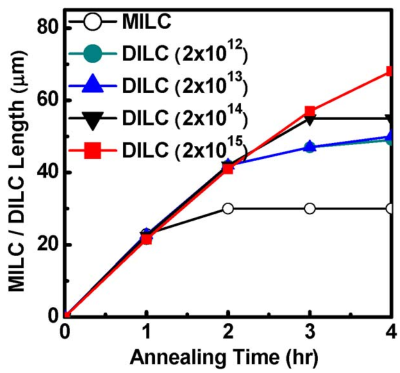

Fig. 2. MILC and DILC growth lengths as a function of annealing time at 590 °C.

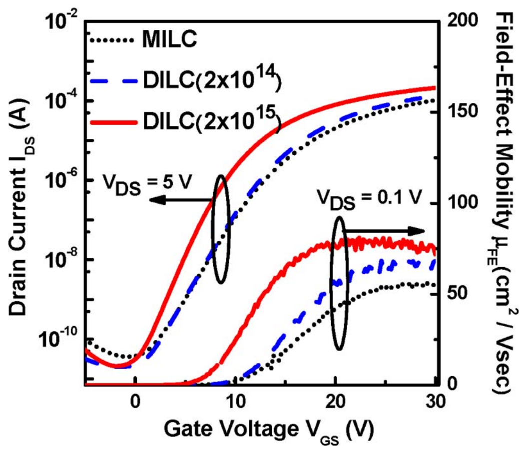

Fig. 3. Typical $I_{\rm DS}$–$V_{\rm GS}$ transfer characteristics and field-effect mobility of MILC and DILC TFTs with various F^+ dosages ($W/L = 10/10\ \mu$m).

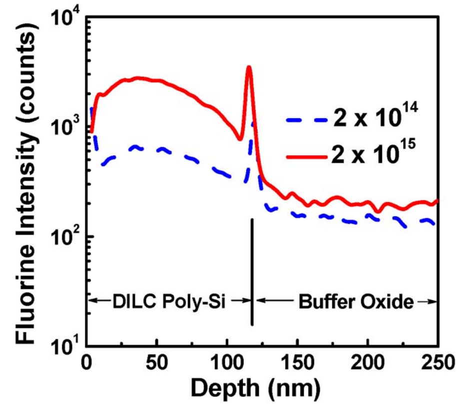

Fig. 4. SIMS depth profile of fluorine in the structure of the interface of DILC poly-Si/buffer-oxide film after annealing at 590 °C for 3 h.

TABLE I
AVERAGE VALUES OF THE FIELD-EFFECT MOBILITY, THRESHOLD VOLTAGE, SUBTHRESHOLD SLOPE, ON-STATE CURRENT, AND OFF-STATE LEAKAGE CURRENT OF TFTs WITH STANDARD DEVIATIONS IN PARENTHESES

Device Parameters	MILC	DILC		
		2×10^{13}	2×10^{14}	2×10^{15}
$\mu_{\rm FE}$ (cm^2 / V · s)	56.11(12.59)	57.52(4.62)	69.68(3.14)	79.92(7.11)
$V_{\rm TH}$ (V)	9.72(0.72)	10.63(0.31)	9.66(0.25)	6.76(0.21)
S.S. (V / dec)	2.32(0.22)	2.48(0.09)	2.26(0.08)	1.66(0.69)
$I_{\rm ON}$ (10^5 A)	10.40(3.17)	9.38(0.98)	13.52(0.99)	20.52(2.57)
$I_{\rm OFF}$ (pA / μm)	3.85(0.71)	2.37(0.06)	2.03(0.05)	2.20(0.06)

by the slope of the curve in Fig. 2. The growth rates of MILC and DILC were all the same before reaching the saturation. In other words, the growth mechanism of MILC was not changed by the F^+ implantation.

The MILC length was saturated around 30 μm when the time reached 2 h. The DILC saturation lengths were longer than that of MILC, and they increased with the drive-in dosage. This is because the saturation of MILC/DILC was stopped by the random poly-Si grains resulting from background solid-phase crystallization (SPC) [12]. The F^+ implantation caused higher degree of disorder at the cap-oxide/α-Si interface, which retarded the SPC nucleation rate [13]. As a result, the saturation length of DILC increased with the F^+ dosage.

Fig. 3 shows the $I_{\rm DS}$–$V_{\rm GS}$ transfer characteristics and field-effect mobility ($\mu_{\rm FE}$) of MILC and DILC TFTs with drive-in dosage that is greater than 2×10^{14} $\rm cm^{-2}$. It was found that DILC TFTs have superior electrical characteristics such as high field-effect mobility, low threshold voltage, low subthreshold slope, high ON-state current, and low OFF-state leakage current. This indicates that the trap-state density (N_t) in DILC poly-Si was effectively reduced. The performances of DILC TFTs with dosage that is less than 2×10^{13} $\rm cm^{-2}$ were not shown in Fig. 3 since their performances were similar to those of MILC TFTs. This might be because the F^+ dosage was not high enough.

In MILC poly-Si, there are two major kinds of defects that are related to N_t: 1) grain boundary and 2) Ni-related defects. These defects would degrade the electric performance [10], [11]. The trap-state density of TFTs was extracted using Levinson and Proano's method [14], [15]. As the F^+ dosage increased from 0 (MILC) to 2×10^{14} and 2×10^{15} $\rm cm^{-2}$, N_t decreased from 5.95×10^{12} to 5.78×10^{12} and 4.58×10^{12} $\rm cm^{-2}$, respectively. This reduction implies that those defects have been terminated. Moreover, a secondary-ion mass spectroscopy (SIMS) analysis revealed that high F contents at the DILC/buffer-oxide interface (Fig. 4), which means that F atoms have diffused to the interface to terminate the Ni-related defects [10].

These results are similar to our previous study on improving the electrical properties of MILC TFTs using a F^+ implantation [10], in which MILC poly-Si was subjected to the F^+ implantation. It was also found that F atoms can improve the performance and reliability of MILC TFTs. Unfortunately, the minimum off currents were nearly unchanged due to the high Ni contamination. In contrast to this study, the Ni concentration inside the poly-Si was controlled/limited by the F^+ implantation dosage. The Ni concentration inside the DILC poly-Si was less than that in MILC. As a result, the minimum off current of DILC was less than that of MILC TFTs, as shown in Fig. 3.

The other important issue of poly-Si TFTs is their uniformity for AMOLED application. As shown in Table I, the device parameters were extracted at $W/L = 10/10\ \mu$m, and ten TFTs were measured in each case to investigate the device-to-device variation [11]. As shown in Table I, the standard deviations of DILC TFTs were smaller than those of MILC TFTs, particularly in the case of DILC TFTs with dosage that is to equal 2×10^{13} cm^{-2}. Even though its performances were similar to those of MILC TFTs, its standard deviations were smaller than those of MILC TFTs. In other words, the uniformity of MILC TFTs was improved through the DILC process. This improvement was due to the suppression of SPC nucleation.

IV. Conclusion

An investigation of poly-Si TFTs using the DILC process had led to the development of a suitable process for AMOLED manufacturing. In DILC, a F^+ implantation was used to drive Ni in the α-Si layer. To reduce the Ni contamination, the remained Ni film was then removed by chemical etching and subsequently annealed at 590 °C for 3 h. It was found that the DILC saturation lengths were increased with the drive-in dosage. Moreover, DILC TFTs exhibit high field-effect mobility, low threshold voltage, low subthreshold slope, high ON-state current, lower trap-state density, smaller standard deviations, and low OFF-state leakage current compared with conventional MILC TFTs.

Acknowledgment

The authors would like to thank the National Nano Device Laboratory, Center for Nano Science and Technology, and the Nano Facility Center of National Chiao Tung University for the technical supports.

References

[1] M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 845–851, May 2001.

[2] X. Guo and S. R. P. Silva, "Investigation on the current nonuniformity in current-mode TFT active-matrix display pixel circuitry," *IEEE Trans. Electron Devices*, vol. 52, no. 11, pp. 2379–2385, Nov. 2005.

[3] S.-W. Lee and S.-K. Joo, "Low temperature poly-Si thin film transistor fabrication by metal induced lateral crystallization," *IEEE Electron Device Lett.*, vol. EDL-17, no. 4, pp. 160–162, Apr. 1996.

[4] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 404–409, Feb. 2000.

[5] P. J. van der Zaag, M. A. Verheijen, S. Y. Yoon, and N. D. Young, "Explanation for the leakage current in polycrystalline-silicon thin-film transistors made by Ni-silicide mediated crystallization," *Appl. Phys. Lett.*, vol. 81, no. 18, pp. 3404–3406, Oct. 2002.

[6] S. Y. Yoon, K. H. Kim, C. O. Kim, J. Y. Oh, and J. Jang, "Low temperature metal induced crystallization of amorphous silicon using a Ni solution," *J. Appl. Phys.*, vol. 82, no. 11, pp. 5865–5867, Dec. 1997.

[7] J. C. Kim, J. H. Choi, S. S. Kim, and J. Jang, "Stable polycrystalline silicon TFT with MICC," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 182–184, Apr. 2004.

[8] N. K. Song, Y. S. Kim, M. S. Kim, S. H. Han, and S. K. Joo, "A fabrication method for reduction of silicide contamination in polycrystalline-silicon thin-film transistors," *Electrochem. Solid-State Lett.*, vol. 10, no. 5, pp. H142–H144, Feb. 2007.

[9] C. M. Hu, Y. S. Wu, and C. C. Lin, "Improving the electrical properties of NILC poly-Si films using a gettering substrate," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 1000–1003, Nov. 2007.

[10] C. P. Chang and Y. S. Wu, "Improved electrical characteristics and reliability of MILC poly-Si TFTs using fluorine-ion implantation," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 990–992, Nov. 2007.

[11] C. P. Chang and Y. S. Wu, "Improved electrical performance of MILC poly-Si TFTs using CF_4 plasma by etching surface of channel," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 130–132, Feb. 2009.

[12] C. F. Cheng, T. C. Leung, M. C. Poon, C. W. Kok, and M. Chan, "Modeling of large-grain polysilicon formation under retardation effect of SPC," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2205–2210, Dec. 2004.

[13] J. W. Park, D. G. Moon, B. T. Ahn, H. B. Im, and K. Lee, "Recrystallization of LPCVD amorphous Si films using F^+ implantation," *Thin Solid Films*, vol. 245, no. 1/2, pp. 228–233, Jun. 1994.

[14] J. Levinson, G. Este, M. Rider, P. J. Scanlon, F. R. Shepherd, and W. D. Westwood, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, no. 2, pp. 1193–1202, Feb. 1982.

[15] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1915–1922, Sep. 1989.