Anomalous Capacitance Induced by GIDL in P-Channel LTPS TFTs

Chia-Sheng Lin, Ying-Chung Chen, Ting-Chang Chang, Shih-Ching Chen, Fu-Yen Jian, Hung-Wei Li, Te-Chih Chen, Chi-Feng Weng, Jin Lu, and Wei-Che Hsu

***Abstract*—In this letter, a mechanism of anomalous capacitance in p-channel low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) was investigated. In general, the effective capacitance was only the overlap region and independent with the frequency in LTPS TFTs under the OFF state. However, our experimental results reveal that the capacitance was related with the leakage current and that it was dependent with the measurement frequencies when operated at the OFF-state region. The increase of the capacitance value is verified to be due to the increase of the electron capacitance originating from a gate-induced drain-leakage (GIDL) one. Nevertheless, the GIDL-induced electron capacitance can be suppressed by employing band-to-band hot electron stress.**

***Index Terms*—Displays, low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs).**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon thin-film transistors (LTPS TFTs) have been widely investigated for flat-panel applications, such as for active matrix liquid crystal displays [1], because the electron mobility of LTPS TFTs is higher than that of conventional amorphous silicon TFTs (a-Si TFTs). Since the maximum process temperature is lower than 600 °C, LTPS TFTs can be fabricated on a cheap glass. Consequently, this technology will become more suitable to integrate both the pixel array and peripheral circuits on a system-on-panel display [2], [3]. In driving circuits, LTPS TFTs are designed using CMOS inverters. In previous reports, the results indicated that large leakage current is an important problem in p-channel LTPS TFTs [4]. The dominant mechanisms of the leakage current in LTPS TFTs have been widely studied [5], [6] and mainly focused on the analyses of current–voltage (I–V) transfer characteristics, and the relation of C–V and leakage current was hardly investigated. However, most studies of capacitance–voltage (C–V) transfer characteristics in LTPS TFTs were emphasized in the degradation caused by additional trap states [7], [8]. The leakage-current-dependent C–V transfer in LTPS TFTs was not investigated carefully. The purpose of our work is to investigate the leakage current on the C–V transfer characteristics in LTPS TFTs. The gate-induced drain-leakage (GIDL)-induced capacitance was observed and studied. In addition, we used an electrical stress to suppress the GIDL-induced capacitance.

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C.-S. Lin and Y.-C. Chen are with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan.

T.-C. Chang is with the Department of Physics, the Institute of Electro-Optical Engineering, and the Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan (e-mail: tcchang@mail.phys.nsysu.edu.tw).

S.-C. Chen, T.-C. Chen, C.-F. Weng, J. Lu, and W.-C. Hsu are with the Department of Physics, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan.

F.-Y. Jian is with the Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan.

H.-W. Li is with the Department of Photonics and the Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

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II. Experiment

The p-channel LTPS TFTs were fabricated on a glass substrate with top-gate structures. First, a 500-nm-thick buffer oxide was deposited on the glass. Next, a 50-nm a-Si film was deposited by plasma-enhanced chemical vapor deposition (PECVD) on the buffer oxide. Then, an a-Si–H film was crystallized by excimer laser annealing at room temperature. The average grain size is 2 μm. An 80-nm gate oxide was deposited by PECVD, and a 300-nm Mo was deposited as a gate metal by sputtering. After the source and drain region formations, an NH_3 plasma treatment was utilized at 300 °C to passivate the dangling bonds at the poly-Si/SiO_2 interface and at the grain boundaries. Finally, a 500-nm SiO_2 layer was deposited and identified as the interlayer dielectric layer.

The dimensions of the TFTs studied in this letter are 512 μm in width and 16 μm in length. The I–V and C–V curves were measured by an Agilent 4156C semiconductor parameter analyzer and an Agilent 4294A precision LCR meter, respectively. In the C–V measurement, the gate-to-channel capacitance ($C_{\rm ch}$), the gate-to-source capacitance ($C_{\rm gs}$), and the gate-to-drain capacitance ($C_{\rm gd}$) with different frequencies were measured, with all measurements performed at room temperature.

In the $C_{\rm ch}$–V_g measurement, a capacitance measurement high (CMH) was applied to the gate electrode, and both drain and source electrodes were connected to a capacitance measurement low (CML). In addition, $C_{\rm gs}$–V_g was measured with a floated drain, whereas $C_{\rm gd}$–V_g was measured with a floated source.

III. Results and Discussion

Fig. 1 shows the fresh $C_{\rm ch}$–V_g transfer characteristics for the p-channel LTPS TFT for different measured frequencies. Clearly, the $C_{\rm ch}$–V_g curves are aligned and independent of

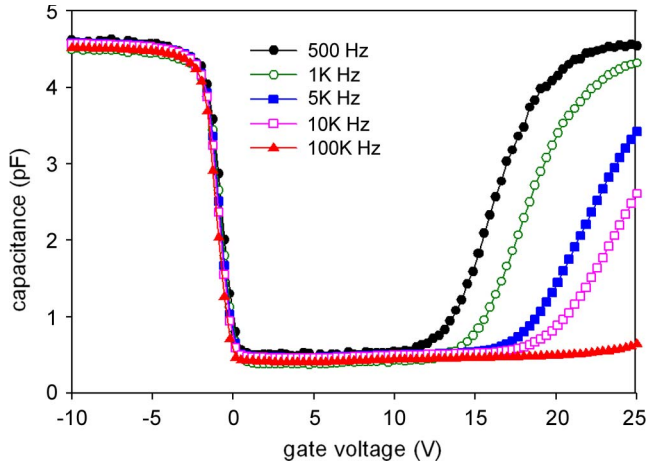

Fig. 1. $C_{\rm ch}$–V transfer characteristics of the p-channel LTPS TFT at different frequencies.

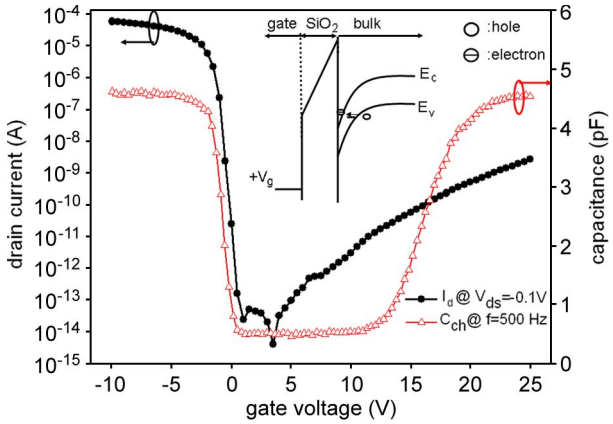

Fig. 2. $C_{\rm ch}$–V and I_d–V_g transfer characteristics of the p-channel LTPS TFT and the illustration shows the energy band diagram along the surface between the drain (P^+) and the gate.

different frequencies when the gate bias is operated in the region of -10 V $< V_g <$ 10 V. However, in the region of $V_g >$ 10 V, the $C_{\rm ch}$–V_g curves show a frequency-dependent nature. The capacitance value increases both as gate bias increases and as frequency decreases. As the device is measured at 500 Hz, this anomalous capacitance is gradually saturated and reached a value that is equivalent to the maximum value of $C_{\rm ch}$ when V_g was operated at -10 V. In general, when the TFT was operated in the OFF-state region $(V_g > 0)$ [9], the effective capacitance was only the overlapped region between the gate and the S/D, which is a frequency-independent constant in the region of 0 V $< V_g <$ 10 V in Fig. 1. Furthermore, previous studies have reported that, with increasing frequency, the transition regions of the TFT C–V curves displayed a stretching out of the curve when trap states were present in the interface or a shift of the curve due to grain boundary or oxide trapping [10], [11]. Nevertheless, neither was observed in our experimental data. Obviously, the anomalous capacitance did not result from either trap state or oxide trapping. As follows, we analyze the I_d–V_g curves to study the mechanism for the anomalous capacitance.

In order to realize the dominant mechanism in this unusual $C_{\rm ch}$–V_g curve, the I_d–V_g transfer characteristic was also measured for comparison. Fig. 2 shows the I_d–V_g curve of the

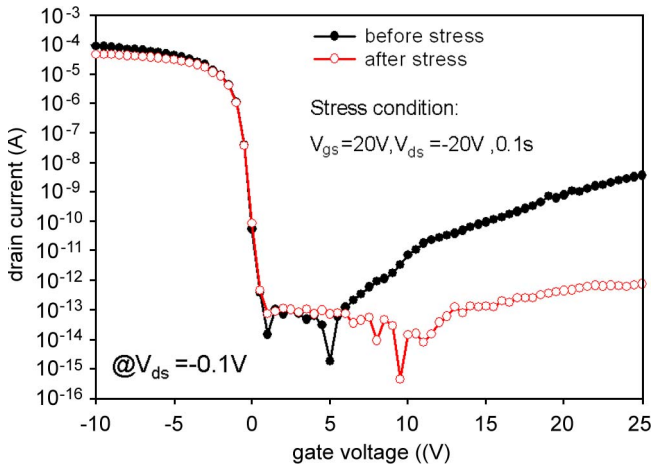

Fig. 3. I_d–V_g transfer characteristics of the p-channel LTPS TFT both before and after 0.1-s stress.

p-channel TFT with a drain voltage of -0.1 V and the $C_{\rm ch}$–V one at a frequency of 500 Hz, and the illustration shows the energy band diagram along the surface between the drain (P^+) and the gate when the device is operated at the OFF state. Clearly, the leakage current increased with increasing gate bias. The mechanism for the leakage current has been reported as due to the GIDL [12], [13]. As the gate bias increases, the increase of energy band bending will cause a large number of electrons to tunnel to the conduction band. The electrons drifted to the channel region due to the junction electric field between the S/D and the channel region. Additionally, the capacitance is directly affected by charge variation. Thus, when the C–V is measured at low frequency, numerous electrons induced by the GIDL have enough time to flow into the channel region and then cause the charge variation at the poly-Si/SiO_2 interface, which is a possible reason for the anomalous C–V curves in the OFF-state region.

Our previous study demonstrated that the GIDL in n-channel TFTs can be suppressed by band-to-band hot hole stress [14]. Similarly, band-to-band hot electron (BTBHE) stress has also been used to suppress GIDL for p-channel TFTs [15]. Fig. 3 shows the I_d–V_g curves of the p-channel TFTs before and after BTBHE stresses. The BTBHE stress was performed with a $V_{\rm gs}$ of 20 V and a $V_{\rm ds}$ of -20 V for 0.1 s. Clearly, the leakage current was significantly reduced after stress. During the stress, the band-to-band generated electrons were trapped in the gate oxide near the drain junction, resulting in a reduction of the vertical electric field near the trapping area. Therefore, GIDL can be suppressed as the TFTs operate in the OFF-state region.

Fig. 4 and illustration shows the $C_{\rm gd}$–V_g and $C_{\rm gs}$–V_g curves measured at 500 Hz before and after the stresses, respectively. In the $C_{\rm gd}$–V_g measurement, the gate was connected to CMH, and the drain was connected to CML. The $C_{\rm gs}$–V_g measurement is configured so that the source, rather than the drain, is connected to CML. Note that the GIDL-induced capacitance was suppressed completely after the BTBHE stress in the $C_{\rm gd}$–V_g curves. This is believed to be due to a series of effects. First, the electrons trapped near the drain induce two simultaneous effects: a lowering of the vertical electrical field and a reduction of energy band bending. This reduction of band bending

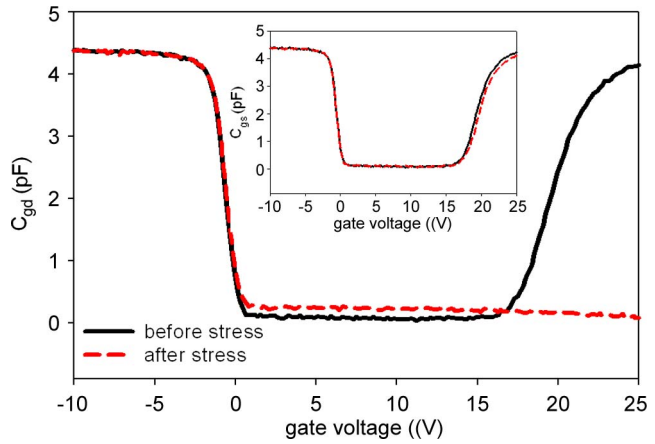

Fig. 4. Gate-to-drain capacitance characteristics of the p-channel LTPS TFT both before and after 0.1-s stress and the illustration shows the gate-to-source capacitance characteristics.

will prevent electrons tunneling from the valence band to the conduction band. As a result, the GIDL-induced capacitance will be suppressed. It can be seen in the $C_{\rm gd}$–V_g curves that the minimum capacitance value in the OFF-state region after stress is slightly larger than the value before stress. This result can be explained by the increment of the parasitic capacitance caused by the trap generation at the interface near the drain junction [7], [11]. It is clear that the $C_{\rm gs}$–V_g value was not altered after electrical stress. This is because the electron trapping affects the drain junction only. Consequently, the leakage current due to GIDL was not suppressed, and it continued to induce the anomalous capacitance effect. As expected, since the electron trapping at the gate oxide near the drain does not affect the overlapped capacitance near the source, the minimum capacitance value in the OFF-state region after stress is the same as the value before stress.

IV. Conclusion

In this letter, an anomalous capacitance due to GIDL in p-channel LTPS TFTs was investigated. The dominant mechanism of the observed anomalous capacitance was the large number of electrons injected into the channel region due to the significant band bending between the gate and the S/D. This phenomenon is successfully suppressed by BTBHE stress.

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