A 3–10 GHz CMOS UWB Low-Noise Amplifier With ESD Protection Circuits

Chung-Yu Wu, *Fellow, IEEE*, Yi-Kai Lo, and Min-Chiao Chen

***Abstract*—A low-power fully integrated low-noise amplifier (LNA) with an on-chip electrostatic-static discharge (ESD) protection circuit for ultra-wide band (UWB) applications is presented. With the use of a common-gate scheme with a g_m-boosted technique, a simple input matching network, low noise figure (NF), and low power consumption can be achieved. Through the combination of an input matching network, an ESD clamp circuit has been designed for the proposed LNA circuit to enhance system robustness. The measured results show that the fabricated LNA can be operated over the full UWB bandwidth of 3.0 to 10.35 GHz. The input return loss (S_{11}) and output return loss (S_{22}) are less than -8.3 dB and -9 dB, respectively. The measured power gain (S_{21}) is 11 ± 1.5 dB, and the measured minimum NF is 3.3 dB at 4 GHz. The dc power dissipation is 7.2 mW from a 1.2 V supply. The chip area, including testing pads, is 1.05 mm $\times$ 0.73 mm.**

***Index Terms*—CMOS, electrostatic discharge (ESD), low-noise amplifier (LNA), ultra-wide band (UWB).**

I. Introduction

IT is known that ultra-wide band (UWB) technology offers the advantages of low-power consumption and high data rate for short-range communications [1]. The recent implantation of 3.1–10.6 GHz UWB systems integrated with CMOS technology is an attractive option because of its low cost and high-level digital integration. To date, many UWB circuits designed using CMOS technology have been reported [2]–[6].

In a UWB receiver, a low-noise amplifier (LNA) is one of the most critical components due to the need for a high and flat gain response, good input matching, low noise figure of over 7.5 GHz bandwidth with a low power consumption and small chip area. Recently, different topologies for CMOS UWB LNAs have been proposed and investigated [3]–[6]. The use of a resistor feedback is one of the features adopted in the design of UWB LNA. However, it can hardly satisfy the needs for wideband gain and noise requirement simultaneously under low power dissipation levels [3], [4]. The inductorless broadband circuits have also been proposed to minimize chip area [5]; however, a high level of power consumption makes these unsuitable for an integrated low-power system. In [6], an inductively degenerated common source topology is employed, but it cannot be operated on full UWB bands.

Since the RF CMOS circuit has been designed using continuously scaled down CMOS technology, it is more vulnerable to damage from electrostatic discharge (ESD). However, the use of, ESD protection circuits may degrade RF circuit performance, in particular, in UWB LNAs, where the parasitic capacitance of ESD protection circuits may complicate the circuit design and seriously degrade its bandwidth. An inductive ESD protection technique [6] is proposed and simulated. Nonetheless, despite their good performance on ESD immunity, full UWB bands cannot be achieved and no measurement results are available.

In this work, a low-power and fully integrated 3.0–10.35 GHz UWB LNA with on-chip ESD protection circuits in 130 nm CMOS process is designed and measured. By using a common-gate (CG) scheme with a g_m-boosted technique, the proposed UWB LNA has a power dissipation of 7.2 mW on a 1.2 V voltage supply and achieves a power gain of 11 ± 1.5 dB, a minimum noise figure (NF) of 3.3 dB, and sufficient input matching within all UWB bands. Both the RF and power pins are protected by ESD diodes corresponding to the human-body model (HBM) ESD level of 1 kV.

In Section II, the circuit design is described. The experimental results are shown in Section III and a conclusion is provided in Section IV.

II. Circuit Design

A schematic diagram of the proposed UWB LNA is shown in Fig. 1, where C_{Pad} is the parasitic pad capacitance and C_1 is the dc blocking capacitor used to couple the input signal to the source of M_1. Inductor L_1 at the source of M_1 is utilized to cancel the imaginary part impedance for the input impedance matching. Load inductor L_3 and resistor R_1 at M_1 drain is employed to increase gain and bandwidth. The input CG stage is formed by M_1, C_1, C_{Pad}, L_1, L_3, and R_1. A g_m-boosted technique is realized by the inverting amplifier M_2 and L_2 which amplifies the input signal and feeds it to the gate of M_1 through the dc blocking capacitor C_2 to boost the equivalent transconductance of M_1. To improve bandwidth, a common-source (CS) amplifier consisting of L_4 and M_3 is cascaded to raise the overall gain and to extend the bandwidth. The sizes of L_1, L_2, L_3, and L_4 are 4.6 nH, 1.17 nH, 10.9 nH, and 2.1 nH, respectively. In addition, all transmission lines are simulated by a 3-D EM simulator HFSS and estimated to be around 0.1 nH per hundred micrometers with a line width of 3 μm. Finally, an output source-follower buffer M_4 and M_5 is designed to match the 50 Ω system used for measurement.

To enhance the system's robustness, an ESD protection circuit is co-designed with the CG input stage. The ESD diodes are placed on both the RF and dc pads as shown in Fig. 1 to shunt the discharge current to ground to protect the LNA core circuit as in [7]. The area of each ESD diode, D_P, D_N, and $D_1 - D_5$, is 5 μm $\times$ 5 μm with a capacitance of about 40 fF.

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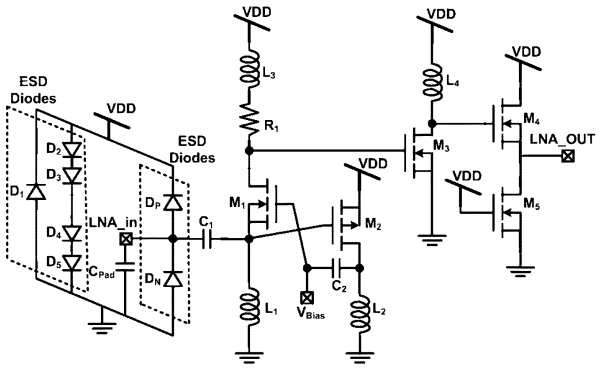

Fig. 1. Schematic of the proposed UWB LNA.

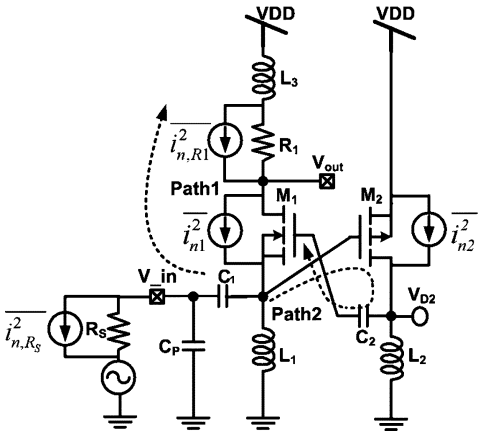

Fig. 2. Simplified small signal schematic of the proposed LNA.

Assuming that the drain-source resistance of $\mathrm{M_1}$ is much larger than the load impedance seen at the drain of $\mathrm{M_1}$ and by grouping the capacitance of input ESD diodes $\mathrm{D_P}$ and $\mathrm{D_N}$ and pad capacitance $\mathrm{C_{Pad}}$ to form $\mathrm{C_P}$ and neglecting the large dc blocking capacitors $\mathrm{C_1}$ and $\mathrm{C_2}$, $\mathrm{Z_{in}}$ can be derived as follows:

$$Z_{\mathrm{in}}(s) \simeq \frac{1}{g_{m1}(1+A) + sC_p + sC_{\mathrm{gs2}} + sC_{\mathrm{gs1}} + \frac{1}{sL_1}} \quad (1)$$

where $\mathrm{g_{m1}}$ is the transconductance of $\mathrm{M_1}$, A is gain of the inverting amplifier, and $\mathrm{C_{gs1}}$ and $\mathrm{C_{gs2}}$ are the gate-source capacitance of $\mathrm{M_1}$ and $\mathrm{M_2}$, respectively. The value of $\mathrm{C_P}$ is about 120 fF. $\mathrm{L_1}$ is chosen to cancel the imaginary part of Z_{in}. $\mathrm{Re}\{Z_{\mathrm{in}}(\mathrm{s})\}$ is set to 50 Ω for input matching

$$50 = \mathrm{Re}\{Z_{\mathrm{in}}(s)\} \simeq \frac{1}{g_{m1}(1+A)} \simeq R_S. \quad (2)$$

Fig. 2 represents the simplified small signal schematic of the proposed LNA where the gate-induced noise is neglected. In Fig. 2, $\mathrm{R_S}$ is the source impedance, $\overline{i_{n1}^2}$ and $\overline{i_{n2}^2}$ are the drain current noise of $\mathrm{M_1}$ and $\mathrm{M_2}$, respectively, and $\overline{i_{n,R1}^2}$ and $\overline{i_{n,Rs}^2}$ are the equivalent thermal noise currents of $\mathrm{R_1}$ and $\mathrm{R_S}$, respectively. The noise from the cascaded CS amplifier is negligible because it is suppressed by the gain of its preceding stage. The overall noise appearing at the output node mainly consists of two components: one is the direct contribution of the noise current generated by $\mathrm{R_S}$, $\mathrm{M_1}$, and $\mathrm{R_1}$ via Path1, and the other is the feedback noise power $\overline{v_{D2}^2}$ resulting from the noise generated by $\mathrm{R_S}$, $\mathrm{R_1}$, $\mathrm{M_1}$, and $\mathrm{M_2}$ through Path2.

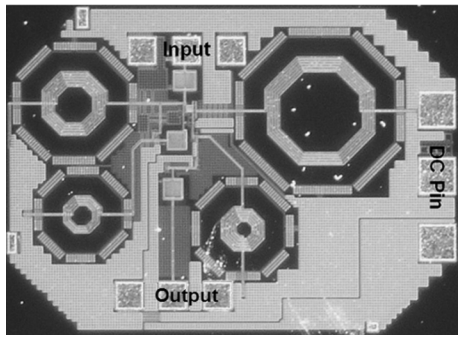

Fig. 3. Microphotograph of the proposed UWB LNA.

The noise contribution from Path1 is $\overline{i_{n1}^2}Z_{L1}^2 + \overline{i_{n,R1}^2}Z_{L1}^2 + 4kT\mathrm{R_S}(1+A)^2 g_{m1}^2 Z_{L1}^2$, where Z_{L1} is the impedance seen at the drain of $\mathrm{M_1}$. To calculate $\overline{v_{D2}^2}$, it is assumed that the input impedance Z_{in} is equal to 50 Ω and $Z_{\mathrm{in}} = 1/[(1+A)g_{m1}] = \mathrm{R_S}$ as in (2). Thus, the noise voltage generated by $\overline{i_{n1}^2}$ and $\overline{i_{R1}^2}$ can be calculated as $(i_{n,R1}+i_{n1})(\mathrm{R_S}/2)g_{m2}Z_{L2}$, whereas the noise from $\mathrm{R_S}$ can be determined as $(kT\mathrm{R_S})1/2g_{m2}Z_{L2}$, where Z_{L2} is the impedance seen at the drain of $\mathrm{M_2}$. The drain current noise of $\mathrm{M_2}$ is multiplied by the output impedance $Z_{D2,\mathrm{OUT}}$ seen at the drain node of $\mathrm{M_2}$, where $Z_{D2,\mathrm{OUT}} = Z_{L2}(1 + g_{m1}\mathrm{R_S})/2$. Therefore, the feedback noise power $\overline{v_{D2}^2}$ can be derived as follows:

$$\overline{v_{D2}^2} = \frac{\overline{i_{n1}^2} + \overline{i_{n,R1}^2}R_S^2 g_{m2}^2 Z_{L2}^2}{4} + kTR_S g_{m2}^2 Z_{L2}^2 + \overline{i_{n2}^2}\frac{Z_{L2}^2}{4}(1+g_{m1}R_S)^2 \quad (3)$$

where $\overline{i_{n1}^2} = 4kT\gamma_1 g_{m1}$, $\overline{i_{n2}^2} = 4kT\gamma_2 g_{m2}$, and γ_1 and γ_2 are the channel thermal noise coefficients.

The overall noise factor of the LNA is defined as

$$F = \frac{V_{n,\mathrm{out}}^2}{Av^2}\frac{1}{4kTR_S} \quad (4)$$

where $Av = (1+A)g_{m1}Z_{L1}$ is the gain of the LNA. Assuming the gain of the inverting amplifier $A = g_{m2}Z_{L2}$ is much greater than 1 and by using (3) and (4), the overall noise factor F of the LNA can be derived using the following equation:

$$F = 1 + \frac{\gamma_1}{(1+A)} + \frac{1}{(1+A)g_{m1}R_1} + \beta + \frac{\gamma_2 g_{m1} g_{m2} Z_{L2}^2}{4(1+A)}. \quad (5)$$

As can be seen from the second and third terms in (5), by using the $\mathrm{g_m}$-boosted technique, the noise resulting directly from $\mathrm{M_1}$ and $\mathrm{R_1}$ via Path1 can be reduced by a factor of $(1 + \mathrm{A})$. The noise from $\overline{v_{D2}^2}$ via Path2 appears in the fourth and last term of (5). The value of the fourth term β is $1/4(1+\gamma_1 g_{m1} + \mathrm{R_S}/\mathrm{R_1})$ and results from the noise of $\mathrm{R_S}$, $\mathrm{R_1}$, and $\mathrm{M_1}$ entering Path2 and then emerging at the drain of $\mathrm{M_1}$. The last term in (5) originates from the drain current noise of $\mathrm{M_2}$ and is suppressed by a factor of $(1 + A)$.

The inverting amplifier $\mathrm{M_2}$ and $\mathrm{L_2}$ lowers the noise factor of a conventional CG LNA. However, the utilization of the inverting

TABLE I
COMPARATIVE PERFORMANCE SUMMARY

	Technology	3 dB BW (GHz)	S_{21} (dB)	S_{11} (dB)	Min. NF (dB)	P_{1dB} (dB)	Supply (V)	Power (mW)	ESD level (kV)	FOM
This Work	**130 nm CMOS**	**3–10.35**	**11 ± 1.5**	**< −8.3**	**3.3–11.4**	**−14.0**	**1.2**	**7.2**	**1**	**15.9**
[3]	130 nm CMOS	3.1–10.6	7.92 ± 0.23	< −17.0	2.5–4.56	−14.0	1.2	10.68	None	5.9
[4]	0.18 μm CMOS	0.7–6.5	11 ± 1.5	< −11.0	3.5–4.2	−15.0*	1.8	11.1	None	13.3
[5]	130 nm CMOS	2.0–9.6	9.5 ± 1.5	< −8.3	3.6–4.8	−16.5	1.2	19.0	None	3.9

* The value is estimated by its input referred third-order intercept point (P_{IIP3})

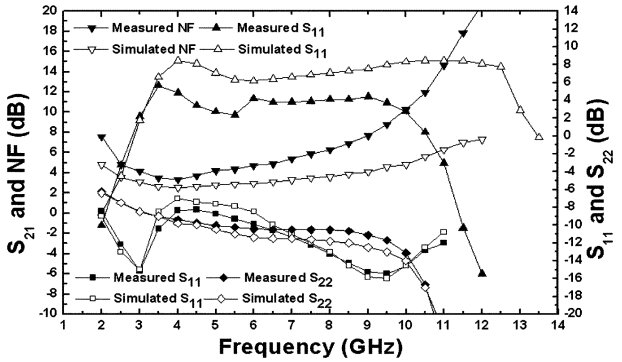

Fig. 4. On-wafer measurement and Advanced Design System post layout simulation results of the proposed LNA.

amplifier also contributes its own noise by introducing a feedback path at the output node. Therefore, A is 2–3 when noise contribution and suppression are taken into account.

III. EXPERIMENT RESULTS

The proposed ESD-protected UWB LNA is designed and fabricated using 130 nm CMOS technology. A source-follower output buffer M_4 and M_5 is integrated in the LNA for the purpose of measurement, as shown in Fig. 1. The simulated buffer loss is around 7.5 dB. With all the matching networks and ESD diodes located on the chip, the LNA occupies an area of 1.05 mm $\times$ 0.73 mm, as shown in Fig. 3. The fabricated LNA dissipates 7.2 mW from a 1.2 V power supply. The measured S_{21} of the proposed LNA is 11 ± 1.5 dB with a 3 dB bandwidth from 3.0 to 10.35 GHz, as demonstrated in Fig. 4, where the loss of the output buffer has been included. Due to process variations, the measured 3 dB bandwidth is about 3 GHz smaller than those in the simulation results. The measured minimum NF is 3.3 dB at 4 GHz and is below 5 dB from 3.0 to 7.5 GHz. However, the measured NF in the frequency range of 7.5–10.35 rises steeply because the measured peak gain and bandwidth at around 3 GHz is smaller than simulation results due to unexpected parasitics, and further degrades the noise suppression ability to the noise from the subsequent CS stage at high frequency. The measured S_{11} is lower than -8.3 dB, whereas S_{22} is lower than -9.3 dB over the full UWB bands as shown in Fig. 4. Finally, the input 1dB compression point (P_{-1dB}) of the proposed LNA is -14 dBm at 6 GHz.

Table I summarizes the measured performance of the proposed UWB LNA and presents the comparisons with other published UWB LNAs with measured data within the 3.1–10.6 GHz UWB bands. As seen from Table I, the proposed LNA uses a g_m-boosted technique has the best figure of merit (FOM). The FOM here appraises a maximum power gain (G), 3 dB bandwidth (BW), noise factor (F), and power consumption (P) of the LNA and is defined as [4]

$$\text{FOM} = \frac{G \times BW_{\text{GHz}}}{(F-1) \times P_{\text{mW}}}. \tag{6}$$

In (6), F and G are absolute values, BW is in units of GHz, and P is in units of mW. Moreover, only the proposed UWB LNA uses ESD protection circuits with a measured ESD level of 1 kV. As compared with those in [4]–[6], the proposed LNA can be operated in full UWB bandwidth. When compared with that in [3] where full UWB bandwidth is also achieved, the proposed LNA has a lower power consumption level and a better gain response. In addition, it is also evident that with integrated on-chip ESD protection diodes, the proposed LNA has sufficient S_{11} performance over the entire UWB bandwidth.

IV. CONCLUSION

In this work, a low-power ESD protected 3.0–10.35 GHz UWB LNA is designed, fabricated, and measured. The proposed LNA is fabricated using 130 nm CMOS technology and has the advantage of better FOM, lower power consumption, full UWB bandwidth, and on-chip ESD protection. The measurement results have verified that the proposed LNA can be applied to the CMOS UWB system.

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