Investigation of Channel Backscattering Characteristics in Nanoscale Uniaxial-Strained PMOSFETs

Wei Lee, Student Member, IEEE, and Pin Su, Member, IEEE

Abstract—This paper examines channel backscattering characteristics for nanoscale strained and unstrained p-channel MOSFETs (PMOSFETs) using the experimentally extracted backscattering coefficients by our modified self-consistent temperature-dependent extraction method. Through comparing the gate voltage and temperature dependence, we demonstrate that channel backscattering can be reduced by the uniaxial strain for PFETs. Besides, we show that the strain-reduced conductivity effective mass may raise the thermal velocity, mean-free path, and effective mobility. Contrary to previous studies, our results indicate that the ballistic efficiency can be enhanced for compressivestrained PFETs. In addition, the backscattering effect on the electrostatic potential is discussed.

Index Terms—Ballistic transport, channel backscattering, CMOS, mobility, SiGe, strained silicon.

I. INTRODUCTION

C HANNEL strain engineering has been actively pursued to enable the mobility scaling of CMOS devices. Especially, for nanoscale MOSFETs that suffer from mobility degradation due to halo implantation, strain technology is an important mobility booster. Several studies [1]–[3] have reported strain dependence of carrier mobility. However, as the gate length (L_g) scales into the nanoscale regime in which the carrier ballistic transport prevails [4]–[6], strain-induced enhancement becomes more complicated to predict [7], [8]. Characterizing nanoscalestrained MOSFETs from the perspective of channel backscattering becomes crucial to strain engineering [8]–[12].

Due to the uncertainty in the amount of the strain and the associated band structure modification [13], most studies regarding the impact of strain on backscattering characteristics relied on experiments [8]–[12]. Among the experimental methods [12], [14], [15], the temperature-dependent technique [14], [15] is suitable for providing guidelines in process monitoring [8]–[11]. For example, using the temperature-dependent method, Lin *et al.* [9], [10] found that uniaxially compressive strain increases the channel backscattering of p-channel

The authors are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: jarjar.ee92g@nctu.edu.tw; pinsu@faculty.nctu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2009.2020161

MOFETs (PMOSFETs). Nevertheless, this method assumes that the low-field mobility (μ_0) is phonon-limited and proportional to $T^{-1.5}$, which is questionable for state-of-the-art nanoscale PMOSFETs [13]. Moreover, the temperature dependence of the critical length l may change with device size [16] and has not been considered. In other words, the accuracy of the reported backscattering characteristics for strained PMOSFETs [9], [10] is under suspicion.

In this paper, we examine the impact of uniaxial strain on backscattering characteristics of nanoscale PMOSFETs using a modified temperature-dependent method that can selfconsistently determine the temperature sensitivity of μ_0 and *l*. Through comparing the extracted backscattering coefficients, we demonstrate that assuming constant temperature dependence of μ_0 and *l* in the extraction may result in unphysical gate bias and temperature dependence of backscattering characteristics. This paper is organized as follows. In Section II, we describe our devices with and without uniaxially compressive strainers. In Section III, we present the modified temperature-dependent method and the experimental extraction. Then, the impact of strain on the extracted backscattering coefficients and possible error sources are discussed in Section VI. Finally, the conclusion will be drawn in Section V.

II. DEVICES

PMOSFETs with channel direction $\langle 110 \rangle$ were manufactured based on state-of-the-art CMOS technology on 300-mm p-type (1 0 0) silicon substrate. Fig. 1 shows that processinduced uniaxial-strained silicon technologies featuring compressive SiGe source/drain and compressive contact etch stop layer (CESL) were employed in this study [2], [3], [17]. Coprocessed strained and unstrained PMOSFETs were implanted by the same pocket condition and showed similar draininduced barrier lowering (DIBL) characteristics. Devices with $L_q = 50 \text{ nm}$ were characterized at T = 223, 298, and 373 K. As shown in Fig. 2, the saturated drain current $(I_{d,sat})$ and the linear drain current $(I_{d,lin})$ of the strained device are improved by about $2.1 \times$ and $2.9 \times$ as compared with its unstrained counterpart, respectively. The threshold voltage of $I_{d,lin}$, $V_{T,lin}$, was determined by the maximum transconductance method. The threshold voltage of $I_{d,sat}, V_{T,sat}$, was calculated from $V_{T,lin}$ with DIBL consideration, i.e., $V_{T,sat} = V_{T,lin}$ -DIBL. DIBL was characterized from the subthreshold characteristics. In order to exclude the parasitic source/drain series resistance (R_{sd}) effect, the constant-mobility method is adopted [18]. The extracted R_{sd} values are about 125 and 214 $\Omega \cdot \mu m$ for strained and

Manuscript received November 8, 2008; revised January 17, 2009 and February 15, 2009. First published April 10, 2009; current version published November 11, 2009. The review of this paper was arranged by Associate Editor L.-E. Wernersson. This work was supported in part by the National Science Council of Taiwan under Contract NSC 97-2221-E-009-162 and in part by the Ministry of Education in Taiwan under ATU Program.



Fig. 1. Schematic diagram of channel backscattering phenomena in a nanoscale device. The impact of compressive strain on backscattering coefficients is investigated.



Fig. 2. Measured drain-current versus gate voltage characteristics for 50-nm- L_g PMOSFETs with and without uniaxially compressive strain at T = 233, 298, 373 K for (a) $|V_{ds}| = 1.3$ V and (b) $|V_{ds}| = 0.05$ V.

unstrained devices, respectively. Based on the measured $I_{d,sat}$ -T and $V_{T,sat}$ -T characteristics, the following backscattering extraction can be carried out.

III. CHARACTERIZATIONS AND EXTRACTION

According to the channel backscattering theory [4], [5], the transistor ballistic current in saturation region can be expressed as $I_{d,sat} = WC_{ox}(V_{gs}-V_{T,sat})\nu_{inj}$, where $C_{ox}(V_{gs}-V_{T,sat})$ is the inversion-layer charge density and ν_{inj} is the average velocity of carriers at the beginning of the channel (Fig. 1) [19]–[21]. The maximum value of ν_{inj} is approximately the equilibrium

unidirectional thermal velocity ν_{therm} . Backscattering from the channel determines how close to this upper limit the device operates. Therefore, ν_{inj} can be related to the channel backscattering coefficient r_{sat} according to $\nu_{\text{inj}} = \nu_{\text{therm}}(1 - r_{\text{sat}})/(1 + r_{\text{sat}})$ [19]–[21]. The r_{sat} depends on the mean-free path λ and the critical length l as $r_{\text{sat}} = 1/(1 + \lambda/l)$ [19]. In other words, the ratio λ/l controls the channel backscattering of the transistor ballistic current.

Based on the temperature-dependent version of backscattering model [9], [14], [15], λ/l has been expressed as

$$\frac{\lambda}{\ell}$$

$$=\frac{-2(1+(\beta_{\mu}-\beta_{l})-\gamma)}{\gamma-((\partial I_{d,\text{sat}}/I_{d,\text{sat}}\partial T)+\{\partial V_{T,\text{sat}}/(V_{gs}-V_{T,\text{sat}})\partial T\})T}-2$$
(1)

where β_{μ} , β_{l} , and γ are defined as the temperature sensitivity of μ_{0} , l and ν_{therm} , respectively [19]:

$$\iota_0 \propto T^{\beta_\mu} \tag{2a}$$

$$\ell \propto \left(\frac{k_B T}{q}\right)^{\beta_l}$$
 (2b)

$$\nu_{\rm therm} = \sqrt{\frac{2k_BT}{\pi m^*}} \left\{ \frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)} \right\} \propto T^{\gamma}$$
(2c)

where \Im_n is the Fermi–Dirac integral of order n, and $\eta_F = (E_F - E_i)/k_BT$. The second factor of (2c) describes the effect of degeneracy on $\sqrt{2k_BT/\pi m^*}$ [19]. The variable β_μ in (2a) represents the temperature dependence of carrier mobility. It has been shown that β_μ may change from $\beta_\mu = 1$ for Coulomb scattering to $\beta_\mu = -1.7$ for phonon scattering [22], [23]. Since l is roughly the distance over which the channel potential drops by k_BT/q [19], [20], the β_l in (2b) is determined by the potential gradient within the k_BT layer. It has been calculated in [19] that $\beta_l = 0.66$ and 0.75 for diffusive and ballistic transport, respectively. Besides, β_l was observed to be 0.7–1.24 for different L_g by Monte Carlo simulation [16]. From (2a) to (2c) and $\lambda \propto 2k_BT\mu_0/q\nu_{\text{therm}}$ [19], the temperature dependence of λ/l can be derived as [24], [25]

$$\frac{\lambda}{\ell} \propto \frac{2k_B T \mu_0}{q \nu_{\text{therm}}} \left(\frac{q}{k_B T}\right)^{\beta_l} \propto T^{1 + (\beta_\mu - \beta_l) - \gamma}.$$
 (3)

Equation (1) reveals an opportunity to experimentally extract λ/l as well as r_{sat} from the measured $I_{d,\text{sat}}-T$ and $V_{T,\text{sat}}-T$ characteristics. However, the accuracy of the extracted λ/l relies on the values of $(\beta_{\mu} - \beta_l)$ and γ . From (2c), we know that γ ranges from 0.5 (nondegenerate limit) to 0 (degenerate limit). To a first approximation, $\gamma = 0.5$ is assumed as in [9], [14], and [15]. (The error due to the γ assumption will be discussed in the next section.) For the value of $(\beta_{\mu} - \beta_l)$, the previous method [9], [14], [15] assumes constant β_{μ} and β_l (e.g., $\beta_{\mu} = -1.5$ and $\beta_l = 1$) in (1) to determine λ/l and r_{sat} .

Fig. 3 shows the extracted λ/l of the unstrained PFET using constant $(\beta_{\mu} - \beta_l)(\blacktriangle)$. It can be seen that when using constant β_{μ} and β_l , the constraint on the temperature dependence of λ/l in (3) cannot be satisfied. Therefore, we propose to use (1)



Fig. 3. Extracted λ/l versus T characteristics showing the need of selfconsistent ($\beta_{\mu} - \beta_{l}$). Note that values of $I_{d,sat}$ and $V_{T,sat}$ were considered at the corresponding T.



Fig. 4. (a) Extracted $(\beta_{\mu} - \beta_l)$ and (b) $r_{\rm sat}$ versus $\left|V_{gs} - V_{T,\rm sat}\right|$ characteristics for 50-nm- L_g PMOSFETs with and without uniaxially compressive strain. $V_{T,\rm sat}$ is determined by maximum transconductance method with DIBL considered. The R_{sd} effect has been corrected. ($R_{sd} \sim 125 \ \Omega \cdot \mu m$ for the strained device and 214 $\Omega \cdot \mu m$ for the unstrained device).

and (3) to determine $(\beta_{\mu} - \beta_l)$ and λ/l self-consistently. As shown in Fig. 3, notable discrepancy in the extracted $(\beta_{\mu} - \beta_l)$ and λ/l between the self-consistent $(\beta_{\mu} - \beta_l)$ and the constant $(\beta_{\mu} - \beta_l)$ can be found. Besides, the decreasing λ/l (i.e., the increasing r_{sat}) with increasing T can be explained by reduced λ and increased l as T increases. Most importantly, using the self-consistent $(\beta_{\mu} - \beta_l)$, the temperature dependence of λ/l can satisfy (3).

IV. RESULTS AND DISCUSSION

Fig. 4 shows the extracted $(\beta_{\mu} - \beta_l)$ and r_{sat} versus $|V_{gs} - V_{T,\text{sat}}|$ characteristics for the unstrained and strained PMOSFETs with $L_q = 50 \text{ nm}$, respectively. It can be seen that

the self-consistently determined $(\beta_{\mu} - \beta_l)$ is far from -2.5 and shows significant V_{gs} dependence for both devices. The increased $(\beta_{\mu} - \beta_l)$ with decreasing V_{gs} manifests the importance of Coulomb scattering in the weak inversion region [2]. We have also noted that the r_{sat} value extracted from the self-consistent $(\beta_{\mu} - \beta_l)$ increases with decreasing V_{gs} . Besides the Coulomb scattering effect [2], such V_{gs} dependence of r_{sat} can be explained by the decreased potential gradient of the source-channel junction barrier (i.e., increased l) with decreasing V_{gs} [15]. It is worth noting that the assumption of $(\beta_{\mu} - \beta_l) = -2.5$ [9], [14], [15] results in insensitive $r_{sat} - V_{gs}$ dependence.

Fig. 4(a) also shows that the value of $(\beta_{\mu} - \beta_l)$ for the strained PFET is smaller than that of the unstrained one. This result is consistent with the measured $I_{d,sat}-V_{gs}$ [Fig. 2(a)], in which the $I_{d,sat}$ of the strained device shows more phonon-limited behavior (i.e., $I_{d,sat}$ decreases as temperature increases), and thus, $(\beta_{\mu} - \beta_l)$ decreases. Moreover, as shown in Fig. 4(b), r_{sat} is actually reduced in the compressive-strained PFET, which is contrary to previous studies [9], [10] using $(\beta_{\mu} - \beta_l) = -2.5$.

To further consider the impact of the $\gamma = 0.5$ assumption on the extracted r_{sat} behavior in Fig. 4(b), $dr_{\text{sat}}/d\gamma$ can be expressed [from (1)]

$$\frac{\partial r_{\text{sat}}}{\partial \gamma} = \frac{r_{\text{sat}}(1 - r_{\text{sat}})}{\gamma - \left(\left(\frac{\partial I_{d,\text{sat}}}{I_{d,\text{sat}}}\partial T\right) + \left\{\frac{\partial V_{T,\text{sat}}}{\partial V_{T,\text{sat}}}/\left(V_{gs} - V_{T,\text{sat}}\right)\partial T\right\}\right)T}.$$
(4)

Note that the right-hand side of (4) is positive, so an overestimated $\gamma(d\gamma)$ results in an overrated $r_{\rm sat}$. Since the degenerate effect increases with V_{gs} and is enhanced by strain effects, γ decreases faster for the strained device than that for the unstrained one. In other words, γ as well as $r_{\rm sat}$ is more overestimated in Fig. 4(b) for the strained device. Note that the extracted $r_{\rm sat}$ [with self-consistent ($\beta_{\mu} - \beta_l$) in Fig. 4(b)] for the strained device is already smaller than that of the unstrained one. Therefore, the $\gamma = 0.5$ assumption will result in underestimation of the impact of compressive strain on the reduction of $r_{\rm sat}$.

To further understand the strain effect, we have investigated $\nu_{\text{therm}}, \lambda$, and effective mobility μ for both strained and unstrained PFETs. Based on the self-consistent extracted r_{sat} [Fig. 4(b)] and the measured $I_{d,\text{sat}}$ [Fig. 2(a)], ν_{therm} was calculated from $I_{d,\text{sat}} = WC_{\text{ox}}(V_{gs}-V_{T,\text{sat}})\nu_{\text{therm}}(1-r_{\text{sat}})/((1+r_{\text{sat}}))$. In addition, λ can be extracted [from (6)]

$$\frac{I_{d,\text{lin}}}{V_{ds}I_{d,\text{sat}}} = \frac{(V_{gs} - V_{T,\text{lin}})(q/2k_BT)(\lambda/(\lambda + L_g))}{(V_{gs} - V_{T,\text{sat}})((1 - r_{\text{sat}})/(1 + r_{\text{sat}}))}$$
(5)

where the ratio of $I_{d,\text{lin}}/V_{ds}$ is determined from the slope of $I_{d,\text{lin}}-V_{ds}$ characteristics at $V_{ds} = 0$ V. The effective mobility μ was measured using the split C-V method with R_{sd} correction, as presented in our previous study [2]. Fig. 5 shows the extracted $\nu_{\text{therm}}, \lambda$, and μ versus V_{gs} characteristics, respectively. It can be seen that the strain-reduced conductivity effective mass m^* leads to an increase of $\nu_{\text{therm}}, \lambda$, and μ . Although the effective mobility μ extracted from the split



Fig. 5. Extracted (a) thermal velocity ν_{therm} , (b) mean-free path λ , and (c) effective mobility μ versus $|V_{gs} - V_T|$ characteristics for 50-nm- L_g PMOSFETs with and without uniaxially compressive strain at T = 298 K. λ is extracted from the slope of $I_{d,\text{lin}}-V_{ds}$ characteristics at $V_{ds} = -20$ to 20 mV. Effective mobility is extracted from the split C-V method at $V_{ds} = 50$ mV with R_{sd} correction [2].

C-V method may not be exactly equivalent to the low-field mobility μ_0 as the definition of λ [4]–[6], it is worth noting that the enhancement of backscattering coefficients follows the relation of $\lambda \propto (2k_BT\mu_0/q\nu_{\rm therm})$, i.e., $1.9 \times (\lambda$ enhancement) $\sim 3.3 \times (\mu$ enhancement)/ $1.5 \times (\nu_{\rm therm}$ enhancement). The strain effect on the enhancement of $1/m^*$ and the relaxation time τ can also be obtained $\sim 2.3 \times$ from ($\nu_{\rm therm}$ enhancement)² and $\sim 1.3 \times$ from (λ enhancement)/($\nu_{\rm therm}$ enhancement), respectively. Besides, the λ enhancement is the main reason for the reduction of $r_{\rm sat}$ and pushes the transport of carriers closer to the ballistic regime. Contrary to previous reports [9], [10], our study indicates that the ballistic efficiency can be enhanced by compressive strain for nanoscale PFETs.

From the extracted r_{sat} and λ , the critical length l can be calculated through $r_{sat} = 1/(1 + \lambda/l)$ [6]. Since r_{sat} and λ are strongly dependent on V_{qs} , l is extracted under the same gate overdrive for strained and unstrained PFET at different temperatures. Fig. 6(a) shows the potential $-k_B T/q$ versus $(l_T - l_{233K})$ characteristics, which can be viewed as the potential gradient of the source-channel junction barrier (Fig. 1). It can be seen that the potential gradient is smaller for the unstrained device. Similar variation in electrostatic potential has been simulated by Svizhenko et al. [26] for different scattering conditions. It can be understood that more backscattering events for the unstrained device with smaller λ raise the electrostatic potential to higher energy to maintain the same carrier density. Our experimentally observed backscattering effect on the electrostatic potential supports the prediction in [26]. It is, to the best of our knowledge, the first experimental demonstration. In addition, the V_{gs} dependence of the potential gradient is shown in Fig. 6(b). It is clear that the potential gradient decreases with decreasing V_{qs} . The decreased potential gradient of the source-channel junction barrier (i.e., increased l) can explain the V_{gs} dependence of r_{sat} for the self-consistent $(\beta_{\mu} - \beta_{l})$ in Fig. 4(b).



Fig. 6. Extracted potential $-k_B T/q$ versus $(l_T - l_{233\text{K}})$ characteristics for (a) strained and unstrained PMOSFETs with $L_g = 50 \text{ nm}$ at $|V_{gs} - V_{T,\text{sat}}| = 0.8 \text{ V}$ and $|V_{ds}| = 1.3 \text{ V}$, and (b) the strained PMOSFET with $L_g = 50 \text{ nm}$ at $|V_{gs} - V_{T,\text{sat}}| = 0.4-0.8 \text{ V}$ and $|V_{ds}| = 1.3 \text{ V}$.

V. CONCLUSION

We have examined characteristics for strained and unstrained PMOSFETs using the experimentally extracted r_{sat} , λ , μ , and ν_{therm} by our modified temperature-dependent extraction method with self-determined ($\beta_{\mu} - \beta_{l}$). Through comparing the extracted backscattering coefficients, we demonstrate that assuming constant temperature dependence of μ_{0} and l in the extraction may result in unphysical V_{gs} and temperature dependence of backscattering characteristics. Contrary to previous studies, our results indicate that the ballistic efficiency can be enhanced for compressive-strained PFETs because λ is enhanced. Besides, the $\gamma = 0.5$ assumption will result in underestimation of the impact of compressive strain on the reduction of r_{sat} . In addition, the backscattering effect on the electrostatic potential has been discussed.

ACKNOWLEDGMENT

The authors would like to thank W. P.-N. Chen for the help during the work.

REFERENCES

- O. Weber and S. Takagi, "New findings on Coulomb scattering mobility in strained-Si nFETs and its physical understanding," in *Proc. Symp. VLSI Tech.*, 2007, pp. 130–131.
- [2] W. P.-N. Chen, P. Su, and K.-I. Goto, "Investigation of Coulomb mobility in nanoscale strained PMOSFETs," *IEEE Trans. Nanotechnol.*, vol. 7, no. 5, pp. 538–543, Sep. 2008.
- [3] W. P.-N. Chen, P. Su, and K.-I. Goto, "Impact of process-induced strain on Coulomb scattering mobility in short-channel *n*-MOSFETs," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 768–771, Jul. 2008.
- [4] K. Natori, "Ballistic metal–oxide–semiconductor field effect transistor," J. Appl. Phys., vol. 76, no. 8, pp. 4879–4890, Oct. 1994.
- [5] M. S. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 361–363, Jul. 1997.
- [6] M. S. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electron Device Lett.*, vol. 22, no. 6, pp. 293– 295, Jun. 2001.

- [7] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo, and T. Skotnicki, "Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.
- [8] M.-H. Liao, C.-W. Liu, L. Yeh, T.-L. Lee, and M.-S. Liang, "Gate width dependence on backscattering characteristics in the nanoscale strained complementary metal-oxide-semiconductor field-effect transistor," *Appl. Phys. Lett.*, vol. 92, no. 6, pp. 063506-1–063506-3, Feb. 2008.
- [9] H.-N. Lin, H.-W. Chen, C.-H. Ko, C.-H. Ge, H.-C. Lin, T.-Y. Huang, and W.-C. Lee, "Channel backscattering characteristics of uniaxially strained nanoscale CMOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 676–678, Sep. 2005.
- [10] H.-N. Lin, H.-W. Chen, C.-H. Ko, C.-H. Ge, H.-C. Lin, T.-Y. Huang, and W.-C. Lee, "Channel backscattering characteristics of strained PMOS-FETs with embedded SiGe source/drain," in *IEDM Tech. Dig.*, Dec. 2005, pp. 141–144.
- [11] K.-W. Ang, H.-C. Chin, K.-J. Chui, M.-F. Li, G. Samudra, and Y.-C. Yeo, "Carrier backscattering characteristics of strained n-MOSFET featuring silicon-carbon source/drain regions," in *Proc. Eur. Solid-State Device Res. Conf.*, 2006, pp. 89–92.
- [12] V. Barral, T. Poiroux, F. Rochette, M. Vinet, S. Barraud, O. Faynot, L. Tosti, F. Andrieu, M. Casse, B. Previtali, R. Ritzenthaler, P. Grosgeorges, E. Bernard, G. LeCarval, D. Munteanu, J. L. Autran, and S. Deleonibus, "Will strain be useful for 10 nm quasi-ballistic FDSOI devices? An experimental study," in *Proc. Symp. VLSI Tech.*, 2007, pp. 128–129.
- [13] A. Khakifirooz and D. A. Antoniadis, "MOSFET performance scaling— Part I: Historical trends," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1391–1400, Jun. 2008.
- [14] M.-J. Chen, H.-T. Huang, K.-C. Huang, P.-N. Chen, C.-S. Chang, and C. H. Diaz, "Temperature dependent channel backscattering coefficients in nanoscale MOSFETs," in *IEDM Tech. Dig.*, Dec. 2002, pp. 39–42.
- [15] M.-J. Chen, H.-T. Huang, Y.-C. Chou, R.-T. Chen, Y.-T. Tseng, P.-N. Chen, and C.-H. Diaz, "Separation of channel backscattering coefficients in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1409–1415, Sep. 2004.
- [16] M. Zilli, P. Palestri, D. Esseni, and L. Selmi, "On the experimental determination of channel back-scattering in nanoMOSFETs," in *IEDM Tech. Dig.*, Dec. 2007, pp. 105–108.
- [17] P. Su and J.-Y. Kuo, "On the enhanced impact ionization in uniaxial strained p-MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 649–651, Jul. 2007.
- [18] D.-W. Lin, M.-L. Cheng, S.-W. Wang, C.-C. Wu, and M.-J. Chen, "A constant-mobility method to enable MOSFET series-resistance extraction," *IEEE Electron Device Lett.*, vol. 28, no. 12, pp. 1132–1134, Dec. 2007.
- [19] A. Rahman and M. S. Lundstrom, "A compact scattering model for the nanoscale double-gate MOSFET," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 481–489, Mar. 2002.
- [20] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 133–141, Jan. 2002.
- [21] E. Fuchs, P. Dollfus, G. Le Carval, S. Barraud, D. Villanueva, F. Salvetti, H. Jaouen, and T. Skotnicki, "A new backscattering model giving a description of the quasi-ballistic transport in nano-MOSFET," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2280–2289, Oct. 2002.

- [22] D. S. Jeon and D. E. Burk, "MOSFET electron inversion layer mobilities— A physically based semi-empirical model for a wide temperature range," *IEEE Trans. Electron Devices*, vol. 36, no. 8, pp. 1456–1463, Aug. 1989.
- [23] G. Reicherta, T. Ouisse, J. L. Pelloie, and S. Cristoloveanu, "Mobility modeling of SOI MOSFETs in the high temperature range," *Solid-State Electron.*, vol. 39, no. 9, pp. 1347–1352, Sep. 1996.
- [24] E. Pop, C. O. Chui, S. Sinha, R. Dutton, and K. Goodson, "Electronthermal comparison and performance optimization of thin-body SOI and GOI MOSFETs," in *IEDM Tech. Dig.*, Dec. 2004, pp. 411–414.
- [25] W. Lee, J. Kuo, W. Chen, P. Su, and M. Jeng, "Impact of uniaxial strain on channel backscattering characteristics and drain current variation for nanoscale PMOSFETs," in *Proc. 2009 Symp. VLSI Technol.*, pp. 112–113, Jun. 2009.
- [26] A. Svizhenko and M. P. Anantram, "Role of scattering in nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1459–1466, Jun. 2003.



Wei Lee (S'03) was born in Taipei, Taiwan, in 1979. He received the B.S. degree from the Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan, in 2001, and the M.S. degree in 2003 from the Department of Electrical Engineering, National Chiao Tung University (NCTU), Hsinchu, where he is currently working toward the Ph.D. degree at the Institute of Electronics.

From 2003 to 2009, he conducted his doctoral research in physics and characterization of advanced CMOS devices at the NCTU. He has also been an In-

tern Student of the Taiwan Semiconductor Manufacturing Company, Hsinchu. His current research interests include mesophysics, carrier transport, singleelectron transistors, channel backscattering characteristics, and silicon-based nanoelectronics.



Pin Su (S'98–M'02) received the B.S. and M.S. degrees in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, and the Ph.D. degree from the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley (UC Berkeley), Berkeley, in 2002.

From 1997 to 2003, he conducted his doctoral and postdoctoral research in physics and modeling of silicon-on-insulator (SOI) devices in the Device Group, UC Berkeley. Since August 2003, he has been

with the Department of Electronics Engineering, National Chiao Tung University, where he is currently an Associate Professor. He has authored or coauthored 85 research papers published in international journals and presented at conference proceedings. His current research interests include silicon-based nanoelectronics, advanced CMOS devices, and device modeling.