0.13-μM CMOS Q-BAND LEVELED-LO SUBHARMONIC MIXER WITH INJECTION-LOCKED FREQUENCY-DIVIDER QUADRATURE GENERATOR

Jen-Yi Su,[1] Chinchun Meng,[1] Po-Yi Wu,[1] and Guo-Wei Huang[2,3]

[1] Department of Communication Engineering, National Chiao Tung University, Hsinchu, Taiwan, Republic of China; Corresponding author: qxchu@scut.edu.cn

[2] National Nano Device Laboratories, Hsinchu, Taiwan, Republic of China

[3] Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, Republic of China

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ABSTRACT: *In this article, a 40-GHz subharmonic Gilbert down-conversion mixer with an accurate quadrature local oscillator (LO) input is demonstrated using a standard 0.13-μm CMOS technology. The quadrature-output frequency divider is realized by injection-locked oscillators and is used at the LO port to replace conventional RC-CR polyphase filters at higher frequencies. Furthermore, the proper Marchand balun at an RF stage is suitable for the standard Si-based process to generate precisely balanced signals despite the substrate loss. The measured conversion gain is 4 dB at 40 GHz. The IP_{1dB} and IIP_3 of -7 dBm and 2 dBm, respectively, are achieved. The measured 3-dB RF bandwidth is very broad and about 12-GHz bandwidth when the 10-MHz IF frequency is fixed. The die size is about 1 mm $\times$ 1 mm.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 2663–2665, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24714

Key words: *0.13-μm CMOS; Q-band; subharmonic; Gilbert mixer; injection-locked; divider; quadrature; polyphase*

1. INTRODUCTION

Recently, advanced CMOS technology which is favorable for circuit design at high frequencies has been demonstrated in the microwave and millimeter-wave regimes [1–4]. Mixers are one of the key parts in a transceiver. A double-balanced Gilbert cell mixer has advantages in terms of a conversion gain, isolation, and compact size [2–4]. A subharmonic mixer is still a popular choice and overcomes conventional difficulties in generating high-frequency local oscillator (LO) signals for a fundamental mixer [5] because an LO frequency is only half of the RF frequency. Furthermore, a quadrature LO input is needed for the subharmonic Gilbert mixer. The quadrature generator can be implemented by RC-CR polyphase filters or divide-by-2 frequency dividers. Although a polyphase filter is a passive component without dc power consumption, power loss and phase noise are introduced. Furthermore, in a CMOS process, RC-CR polyphase filters have larger parasitic effects and larger process variations at high frequencies. The polyphase filters based on CMOS technology are not suitable for a quadrature generator at high frequencies. Thus, the most precise quadrature signal generation is offered by using divide-by-2 frequency dividers [6]. The little LO pumping power and the broadband quadrature-output signals are benefits in the differential-input divide-by-2 frequency dividers.

In this article, using the standard 0.13-μm CMOS technology, we propose the 40-GHz leveled-LO subharmonic Gilbert down-converter with the quadrature LO input generated by two injection-locked frequency dividers (ILFDs).

2. CIRCUIT DESIGN

A schematic diagram of the subharmonic Gilbert down-converter with the quadrature LO input generated by two divide-by-2 ILFDs is depicted in Figure 1. The subharmonic mixer uses the leveled-LO structure, and the ILFD adopts a conventional cross-coupled differential pair in an LC tank. For quadrature LO generation with high phase accuracy and balanced magnitude at wideband frequencies, two ILFDs with a differential input is used in a CMOS technology. The quadrature-output ILFDs replace RC-CR polyphase filters because the RC-CR polyphase filters have larger parasitic effects and larger process variations in a CMOS process. A mixer using the polyphase filter must require higher LO input power to compensate the power loss of the polyphase filter.

A CMOS transistor is a nonlinear device with a square law between the drain current and the gate-source voltage. The subharmonic Gilbert mixer is composed of source-coupled transistor pairs (M1-M2, …, M7-M8) at an LO stage and transconductance pairs (M9-M10) at an RF stage. The source-coupled pairs including drain-connected pairs form the leveled-LO cell [5]. The fundamental signals are eliminated and the even harmonic signals appear at the drain-connected nodes when differential quadrature signals inject into the gate terminals of the leveled-LO cell. The RF stage uses a Marchand balun connected with common-gate-configured transistors (M9-M10) [7]. The single-ended RF input is transformed to the differential signals by the wideband Marchand balun [8]. Moreover, the RF stage uses the Marchand balun because the Marchand balun has ac-

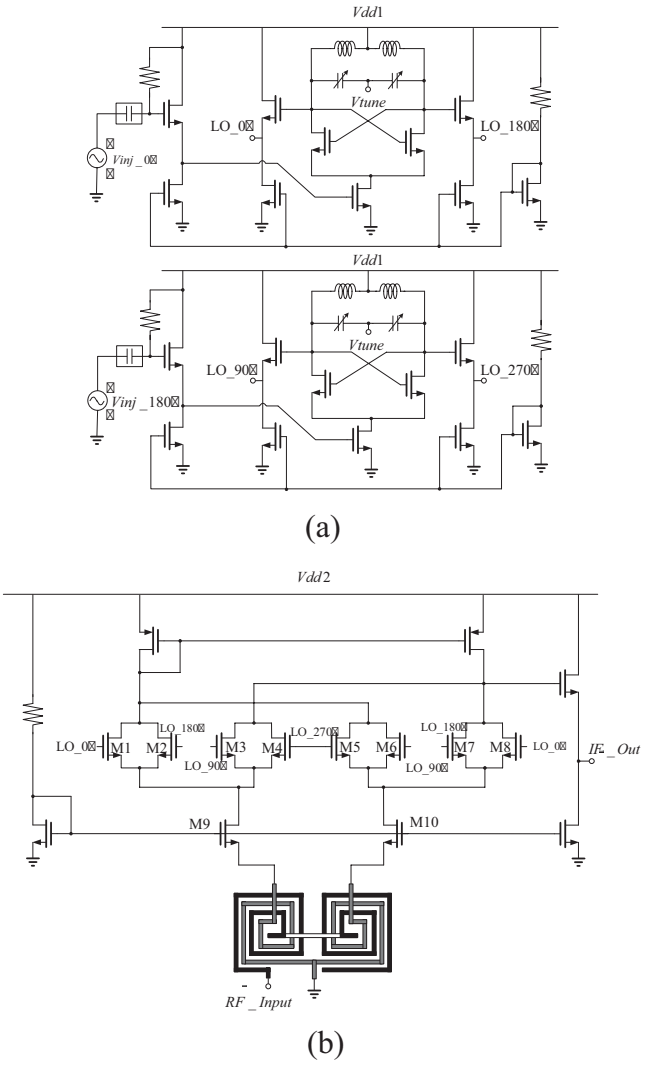

Figure 1 (a) Quadrature generator by the injection-locked frequency dividers. (b) 40-GHz leveled-LO subharmonic Gilbert down-converter with quadrature LO inputs

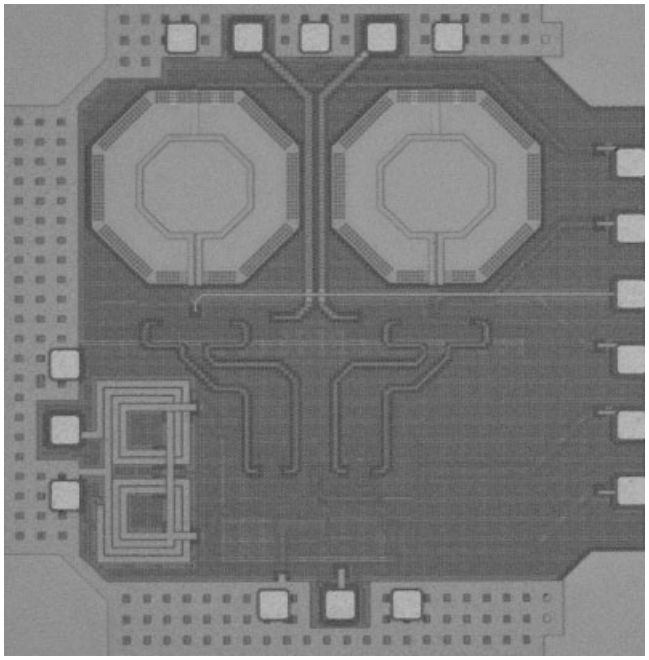

Figure 2 Die photo of the 40-GHz subharmonic Gilbert down-converter with two injection-locked frequency dividers using the 0.13-μm CMOS technology

grounded terminals which can be treated as the dc grounds of the common-gate-configured transistors (M9-M10).

3. MEASUREMENT RESULTS

The fully integrated subharmonic Gilbert mixer with the quadrature-output ILFDs is fabricated using a 0.13-μm CMOS technology. Figure 2 illustrates the microphoto of the Figure 1, and the chip size of this circuit with an integrated Marchand balun is only about 1 mm $\times$ 1 mm. The measured conversion gain with sweeping LO input power is shown in Figure 3. The maximum conversion gain is about 4.0 dB when input LO power is above 4 dBm with the fixed RF frequency of 40 GHz. The wide bandwidth of the subharmonic mixer is shown in Figure 4. When an IF frequency is fixed at 10 MHz, the 3-dB RF bandwidth is about 12 GHz from 35 to 47 GHz. This subharmonic mixer with the RF input of the Marchand balun has

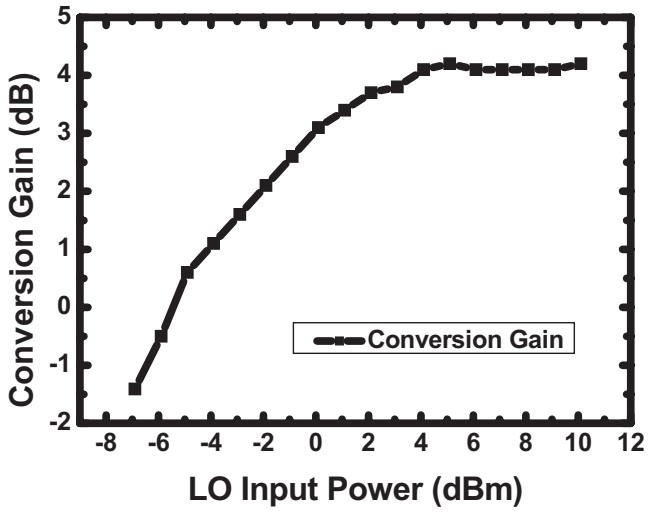

Figure 3 Conversion gain with sweeping LO input power

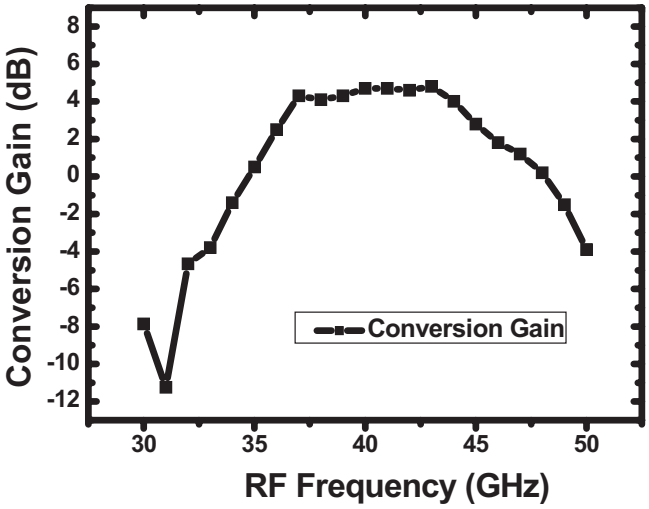

Figure 4 Measured 3-dB RF bandwidth of the 40-GHz subharmonic down-converter

about 35-dB LO-to-RF isolation and 40-dB LO-to-IF isolation at the 40-GHz band, as shown in Figure 5. In Figure 6, the input 1-dB compression point ($IP_{1\ dB}$) and the input third-order intercept point (IIP_3) are -7 dBm and 2 dBm, respectively.

4. CONCLUSIONS

In this article, a subharmonic Gilbert down-conversion mixer with quadrature-output divide-by-2 frequency dividers is fabricated and implemented using the standard 0.13-μm CMOS technology. At higher frequencies, a polyphase filter has larger parasitic effects and cannot be accurately implemented on a Si substrate. The quadrature generator formed by two ILFDs at the LO port is used at the LO port to substitute RC-CR polyphase filters. These divide-by-2 frequency dividers can be successfully demonstrated for wideband quadrature accuracy at high frequencies. In addition, the proper Marchand balun has wide bandwidth and generates precise balanced signals for a standard Si-based technology despite the substrate loss. The 12-GHz bandwidth is achieved from 35 to 47 GHz for 3-dB RF bandwidth with the fixed IF frequency of 10 MHz. For future, an

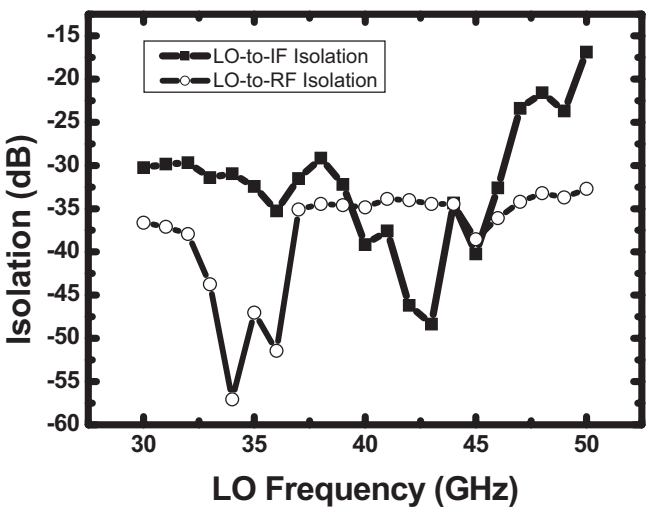

Figure 5 Isolations of LO-to-RF and LO-to-IF ports

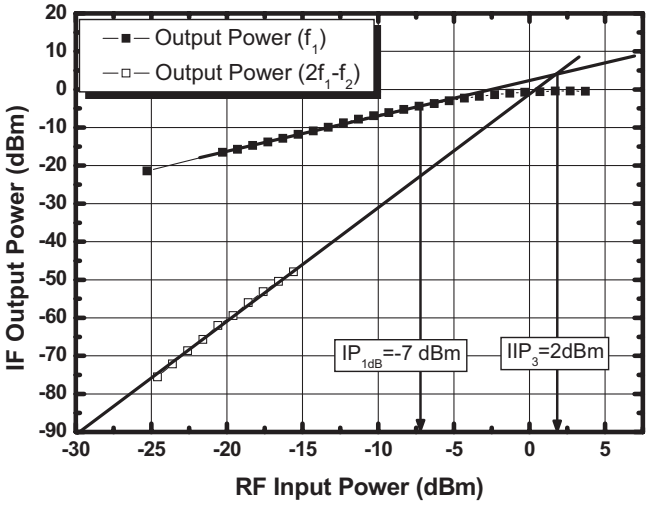

Figure 6 Linearity performance of two-tone measurement

advanced Si technology will widely provide a new choice for millimeter-wave applications.

ACKNOWLEDGMENTS

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THE RF CHARACTERISTICS OF MICROMACHINED COPLANAR WAVEGUIDE IN 0.13 μm CMOS TECHNOLOGY BY CMOS COMPATIBLE ICP DRY ETCHING

Tao Wang,[1] Shey-Shi Lu,[1] Yo-Sheng Lin,[2] Yin-Zong Juang,[3] and Guo-Wei Huang[3]

[1] Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, Republic of China; Corresponding author: sslu@ntu.edu.tw

[2] Department of Electrical Engineering, National Chi Nan University, Puli, Taiwan, Republic of China

[3] National Nano Device Labortories, Hsinchu, Taiwan, Republic of China

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ABSTRACT: *A coplanar waveguide (CPW) was implemented in 0.13 μm CMOS technology and then postprocessed by CMOS compatible inductively-coupled plasma etching, which removed the silicon underneath the coplanar strips. Transmission line parameters such as characteristic impedance Z_O, attenuation constant α, substrate capacitance/conductance C/G, series inductance/resistance L/R, as a function of frequency were extracted. It is found that α, C, and G can be greatly improved after silicon removal. Specifically, a 0.45 dB/mm reduction (from 0.5 to 0.05 dB/mm) in α, a 1.6 mS/mm reduction (from 1.6 to ~0 mS/mm) in G, and a 43.9% reduction (from 92.8 to 52.1 fF/mm) in C were achieved at 20 GHz. In addition, this work also investigates the dielectric loss α_d and conductive loss α_c of the CPW.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 2665–2668, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24693

Key words: *CMOS; coplanar waveguide (CPW); inductively-coupled plasma (ICP) etching; radio frequency (RF)*

1. INTRODUCTION

Thanks to the advance of silicon technology, silicon microwave or millimeter-wave monolithic integrated circuits (MMIC) have become a reality [1]. The on-chip transmission line such as the coplanar waveguide (CPW) is one of the indispensable devices toward the goal of microwave or millimeter-wave single-chip radio. However, it is well known that the attenuation constant of the on-chip transmission line increases as the operating frequency increases due to losses in the conductive silicon substrate as well as the series resistance of the metallization. Various methods, such as high-resistivity silicon [2], front/back side micromachining [3], porous silicon [4], and proton implantation [5], have been reported to reduce the substrate loss. Nevertheless, most of the proposed methods are very difficult, if not impossible, to be integrated into the standard CMOS technology because of their inherent nonstandard processing steps. Therefore, while the abovementioned methods have been applied to many passive devices, seldom have they been adopted in an integrated circuits with passive and active devices, simultaneously. In addition, the front-side etching has inherent limitations as to how far circuits can be placed from the inductors [6]. Recently, we have demonstrated that the CMOS compatible inductively-coupled-plasma (ICP) deep trench technology, which selectively removes the notorious conductive silicon substrate underneath the passive components, can significantly improve the gain and noise figure performances of a 1–12.6 GHz CMOS distributed amplifier [7]. In this work, we further report the RF characteristics of CPW postprocessed by the CMOS-compatible ICP deep trench technology.