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WSiN Cap Layer for Improvement of Ohmic Contact Morphology in AlGaN/GaN High Electron Mobility Transistors

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A new technique using WSiN film as a protective cap layer of the internal ohmic metallization scheme and the GaN surface was developed to improve the surface morphology of the contact of AlGaN/GaN high electron mobility transistors (HEMTs). After annealing, this layer was selectively removed by patterning and dry etching. Metal contact surfaces covered with WSiN preserved a good surface morphology and edge definition. Moreover, the devices have a saturation current of 1 A/mm and a maximum transconductance of 235 mS/mm. When biased at 30 V, the output power density is 5.8 W/mm at 2 GHz. These results indicate a damage-free process for the smooth ohmic contacts formation.

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1. Introduction

Smooth contact morphology and low contact resistance are the requirements of good ohmic contact schemes for the semiconductors devices. While latter is related to the electrical performance and the efficiency, former is more associated with the edge definition and possibility for more precise lithography alignment. For AlGaN/GaN heterostructure high electron mobility transistors (HEMTs), both issues proved to be a challenge. Ti/Al-based multilayer metals stacks and high temperature annealing were widely adopted in order to achieve a low contact resistance below 1 Ω mm.[1)] The proposed mechanism was the extraction of the nitrogen from the AlGaN or GaN through the formation of AlN/TiN leading to highly n-type surface.[2–4)] However, the results of these metallurgical reactions were also accompanied by formation of complex phases,[3,4)] and this is often associated with a rough surface.[5)] To achieve both a flat surface with better line definition and a low contact resistance, several metallization schemes, including Ti/Al/Mo/Au[6–9)] and Ti/Al/Ti/Au/WSiN[9–12)] have been proposed.

In previous works, Ti/Al/Ti/Au contacts with WSiN layers were deposited using the same layer of photoresist and the approach has demonstrated flat surfaces after annealing in the presence of this WSiN cap layer.[10)] But the sputter deposition technique inevitable leads to overhangs on the sidewall of the photoresist, and these residues would degrade the edge line profile.[9)] This would be a critical issue for devices which require more precise dimension control.

In this work, we used sputtered WSiN as a cap layer to cover the whole wafer during annealing. The morphology of the ohmic metal was flat after annealing. High contrast and good edge line definition can be obtained for precise alignments of the following optical lithography and electron-beam lithography as a result of the smooth surface morphology. The excess WSiN on the active region was removed by low damage dry etching after ohmic contact annealing. Electrical characteristics of the devices were evaluated to assess the plasma damage during the sputter deposition and dry etching.

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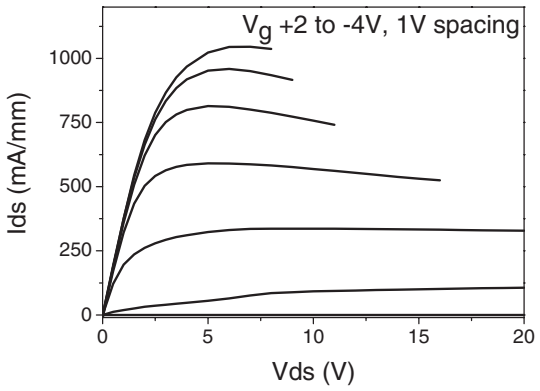
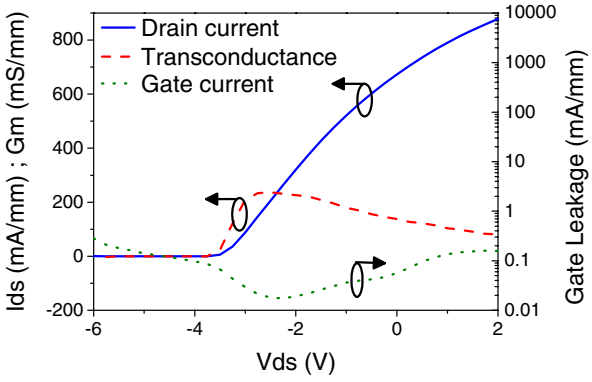
2. Experiments

The epitaxial structure was grown by metal–organic chemical vapor deposition (MOCVD) on sapphire. The layers consisted of 1.5 μm-thick undoped GaN buffer layer, followed by 0.5 nm of AlN spacer, 25 nm $Al_{0.25}Ga_{0.75}N$ and finish with 5 nm GaN n-doped cap layer (Si-doped to 7×10^{18}). Sheet resistivity was 330 Ω/sq. The formation of the ohmic contacts started with the deposition of the Ti/Al/Ti/Au multilayer metal stacks by electron beam evaporation. Following the lift-off of the ohmic metals, the wafer surface was covered with a 160 nm WSiN film deposited by direct-current (DC) reactive sputtering, and annealed using rapid thermal annealing (RTA) at 830 °C for 30 s. The excess WSiN outside the ohmic region was patterned by lithography and etched using inductively-coupled plasma (ICP) etching with SF_6/He plasma. The etching conditions were as follows: SF_6 20 sccm, He 10 sccm, chamber pressure of 0.5 Pa, ICP power of 400 W, and reactive ion etching (RIE) power of 20 W. The parameters were chosen for good anisotropic etch and low plasma damage. The resulted DC-bias was as low as 60 V. Device isolation was realized by mesa technology, using RIE in $Cl_2/BCl_3/Ar$ ambient. Device passivation was done with PECVD SiNx and the gate foot was defined by using electron beam lithography and followed by dry etching for realizing an opening through SiN_x. The dimension of the gate foot is 0.5 μm and gate head is 0.9 μm with a Pt/Ti/Au metal stack. Pads connections and air bridge of these devices were done by electrochemical-plated 6 μm-thick gold. The total gate width is 100 μm and the source to drain distance is 5 μm.

The devices were characterized for typical DC parameters. The pulse current–voltage (I–V) measurement was used to evaluate the possible traps introduced during the process in the proximity of the gate. This was done by measuring and comparing the device response using an Accent DiVA D265 with the static bias points set to gate zero-bias condition $(V_d, V_g) = (0, 0)$ and gate-biased condition $(V_d, V_g) = (0, -5)$ while sweep to each point on the I–V curves with transient time fixed at 200 ns. Sheet resistance of the wafer was extracted from the test structure and compared with the data before process. Contact resistance was measured using transmission line model (TLM) method. S-parameter measurement up to 50 GHz and load–pull



(a)



(b)

Fig. 1. (Color online) (a) I_d–V_d characteristics, (b) transconductance and gate leakage current of the WSiN capped AlGaN/GaN HEMTs.

measurements under class AB bias condition at 2 GHz were performed to characterize the device at high frequencies.

3. Results and Discussion

Figure 1 shows output and transfer characteristics from the DC measurements. The device has a good pinch-off characteristics. The saturation current was 1 A/mm, and the maximum transconductance was 235 mS/mm. Low leakage current suggests that there was no residue of the WSiN and no damage induced conduction path on the region beneath the gate and between drain and source. The pulse measurement with pulse time of 200 ns was shown in Fig. 2. This transient response is similar to conventional Ti/Al/Ti/Au ohmic contact devices and no serious gate-lag was observed, which suggested a low surface trap density. The sheet resistance of the sample before and after process remained the same value of 330 Ω/sq, implying that the plasma etching did not introduce significant damage. The contact surface remained smooth as shown in scanning electron microscope (SEM) image in Fig. 3(a) while the surface of the conventional Ti/Al/Ti/Au ohmic contact roughens as in Fig. 3(b). The contact resistance of both ohmic contact scheme were 0.6 Ω mm.

As for the high frequency characteristics, the device had an F_t of 22 GHz and F_{max} of 76 GHz when biased at V_{ds} of 15 V and V_{gs} of −2.5 V as shown in Fig. 4(a). Load–pull measurement at 2 GHz when using class AB bias point of V_{ds} at 30 V and V_{gs} of −1.8 V demonstrated a maximum output power density of 5.8 W/mm and a power added

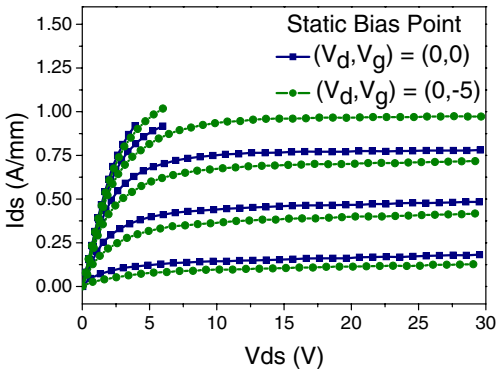
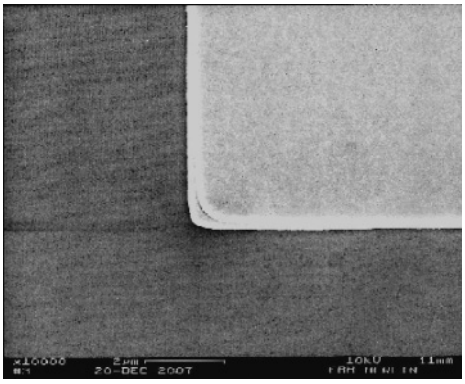
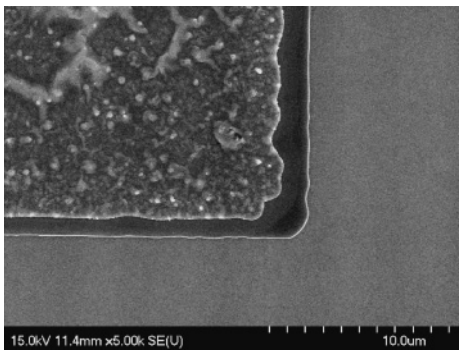


Fig. 2. (Color online) Pulse *I*–*V* measurements of the WSiN capped AlGaN/GaN HEMTs. The gate voltage sweeps from −2 to 2 V with step of 1 V and pulse time of 200 ns.



(a)



(b)

Fig. 3. (a) SEM image of the smooth and sharp edged WSiN capped ohmic contacts and (b) conventional Ti/Al/Ti/Au ohmic contacts.

efficiency (PAE) of 60%, as shown in Fig. 4(b). These results are comparable to typical GaN HEMT devices on sapphire substrate with traditional ohmic contact. It demonstrates that the new GaN ohmic process consisting of WSiN cap layer deposition, annealing and sequential low damage etching removal techniques can be integrated into the GaN HEMT process.

Furthermore, the WSiN deposited on GaN can withstand at least 830 °C annealing with only minimal reactions with the underlying layer, and can be effectively removed by ICP etching without inducing significant damages. Thus, this approach can also be used for other processes on GaN which require a sacrificial or cap layer to protect the sensitive surface.

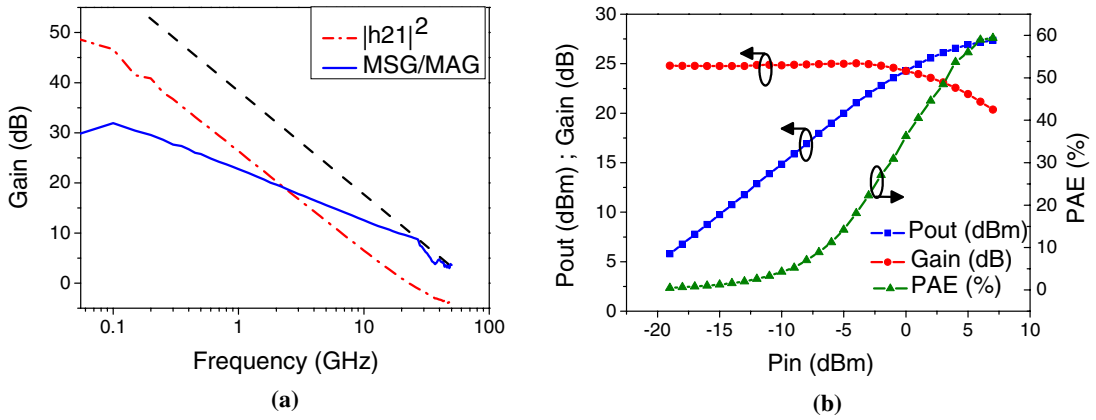


Fig. 4. (Color online) RF performance of the 2 × 50 μm^2 WSiN capped AlGaN/GaN HEMTs (a) F_t and F_{max}, calculated from *S*-parameter measurements. (b) Power sweep at 2 GHz, biased at the drain voltage of 30 V. Maximum output power density is 5.8 W/mm and PAE is 60%.

4. Conclusions

AlGaN/GaN HEMTs with WSiN cap layer on Ti/Al/Ti/Au ohmic contact that achieve smooth contact surface morphology with well defined contact edges have been demonstrated. The WSiN were annealed at 830 °C for 30 s and the excess WSiN was removed by low damage ICP dry etch. The devices exhibited high saturation current of 1 A/mm and maximum tranconductance of 235 mS/mm. No significant gate lag was observed and the maximum output power density at 2 GHz was 5.8 W/mm. It can be concluded that the WSiN process did not cause additional damage or wafer-surface degradation, and that the WSiN cap layer can be used to effectively suppress the uneven rough surface formation for the ohmic metals after annealing.

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