Physical Mechanism of High-Programming-Efficiency Dynamic-Threshold Source-Side Injection in Wrapped-Select-Gate SONOS for NOR-Type Flash Memory

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***Abstract*—For the first time, a programming mechanism for conventional source-side injection (SSI) (normal mode), substrate-bias enhanced SSI (body mode), and dynamic-threshold SSI (DTSSI) (DT mode) of a wrapped-select-gate SONOS memory is developed with 2-D Poisson equation and hot-electron simulation and programming characteristic measurement for NOR Flash memory. Compared with traditional SSI, DTSSI mechanisms are determined in terms of lateral acceleration electric field and programming current (I_{PGM}) in the neutral gap region, resulting in high programming efficiency. Furthermore, the lateral electric field intersects the vertical electric field, indicating that the main charge injection point is from the end edge of the gap region close to the word gate.**

***Index Terms*—Memory, programming mechanism, wrapped-select-gate SONOS (WSG SONOS).**

I. Introduction

THE SOURCE-SIDE injection (SSI) technique has been used to program nitride-based trapping nonvolatile Flash memory devices [1], [2]. Unlike channel-hot-electron injection (CHEI), the major advantages of SSI are high-speed programming and high programming efficiency due to its clever separation of the incompatibilities of optimal programming conditions of CHEI [3]. Therefore, SSI can generate and inject a sufficiently large number of hot electrons for multilevel operations. However, most published papers have focused only on drain field variations with increasing drain bias [4], [5]. As a result, important pointers to improved efficiency for SSI may have been missed. Furthermore, substrate dopant concentration control for reducing drain bias becomes both more important and more difficult as devices are scaled down [6].

Recently, a high-speed multilevel wrapped-select-gate SONOS (WSG-SONOS) memory using a dynamic-threshold SSI (DTSSI) programming method has been proposed [7]. This letter explores the DTSSI mechanism in a very high speed NOR-type array of WSG-SONOS memory under normal, DT, and body modes. The results clearly delineate the electric field influences on the WSG-SONOS memory under each of the different modes.

II. Device Structure and Proposed SSI Scheme

The major processes and cross-sectional images of the WSG-SONOS memory structure are detailed in [7] and [8]. Unlike single-gate channel-hot-electron programming SONOS devices, I_{PGM} induced by a wrapped MOSFET can maintain a high value due to the structural separation between the left bit and the right bit. Therefore, the electrical effects of the nitride-trapping charges can be as low as possible. Based on these concepts, there are three kinds of programming methods for WSG-SONOS devices: normal, DT, and body mode, as illustrated in Fig. 1. To investigate the physical mechanism of SSI under theses different modes, an ISE TCAD with hot-electron and Poisson equation calculation models was used. For the DT mode, the selected gate is tied to a well, whereas V_{Well} in the body mode is fixed at 0.45 V. Owing to the dynamic variation of the threshold voltage in the DT mode, the power consumption can be lower than that in the body mode during the charging process of programming. In addition, the higher hot-electron generation efficiency is another important factor for DTSSI applications discussed in detail in this letter.

III. Results and Discussion

Fig. 2 shows the effect of V_{SG} with 100 ns of programming for each mode of WSG-SONOS memory under the same

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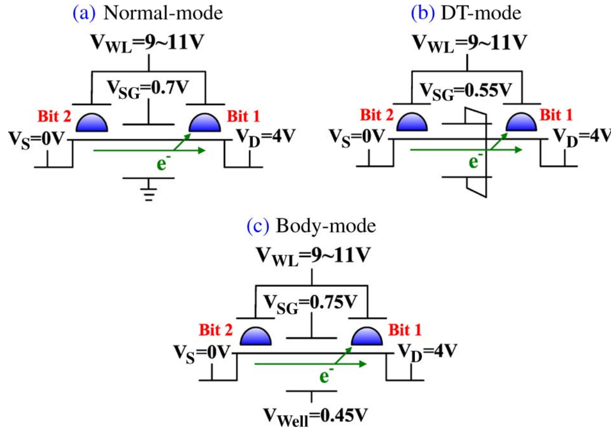

Fig. 1. Comparison of (a) traditional SSI, (b) DTSSI, and (c) body-bias enhanced SSI programming schemes.

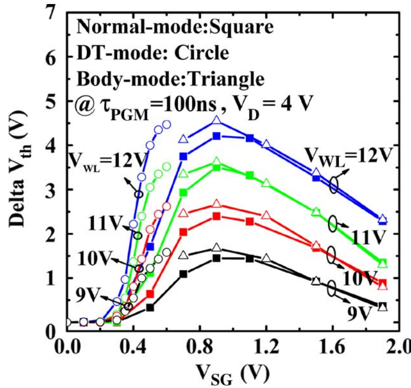

Fig. 2. Programming characteristics of WSG-SONOS memory as a function of V_{SG} and V_{WL} at fixed $V_{\mathrm{BL}} = 4$ V with $\tau_{\mathrm{PGM}} = 100$ ns for each mode. A typical bell-shaped distribution of the threshold voltage shift is observed in normal and body modes ($V_{\mathrm{Well}} = 0.45$ V).

programming conditions ($V_{\mathrm{WL}} = 9-12$ V, $V_{\mathrm{BL}} = 4$ V). A typical bell-shaped distribution is observed in both normal and body modes but not in the DT mode. Here, the DTSSI must be operated below $V_{\mathrm{SG}} = 0.65$ V; otherwise, the junction diode of the well and source will activate. In our device, the V_{th} of the embedded select-gate MOSFET is only 0.4 V, which is defined by the constant current method $I_{\mathrm{PGM}} = 0.1$ μA, in the WSG-SONOS memory under DT mode by appropriately adjusting the device process. Across all three modes, the higher V_{WL} exhibits a larger programming window. This is because high V_{WL} not only enhances the collection ability with increasing normal electric field but also raises the hot-electron generation rate by increasing the voltage drop across the gap region. To understand the SSI mechanism, we simulate the dependence of V_{WL} and V_{SG} on the electrical field. Both lateral and vertical electrical fields increase exponentially from the pinchoff point to the end of the neutral gap region, as shown in Fig. 3. The higher V_{WL} increases the maximum field peak due to the higher potential transmission from the drain terminal by increasing the inversion charge density beneath the word gate. By the same token, the higher V_{SG}, although it sufficiently enhances I_{PGM}, degrades the electric field peaks at the same time. This is because, as the wrapped-MOSFET overdrive becomes higher, the voltage drop across the neutral gap region decreases,

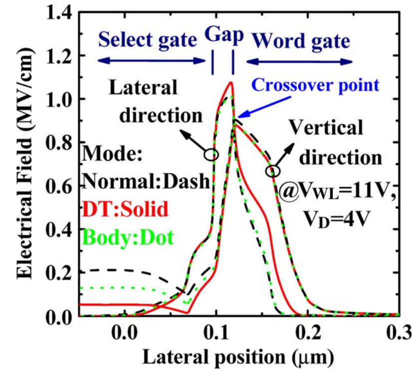

Fig. 3. Comparison of the electrical field variations for each mode (normal mode: $V_{\mathrm{SG}} = 0.7$ V; DT mode: $V_{\mathrm{SG}} = V_{\mathrm{Well}} = 0.55$ V; body mode: $V_{\mathrm{SG}} = 0.75$ V, $V_{\mathrm{Well}} = 0.45$ V). The DTSSI shows the better hot-electron generation rate in terms of enhancement of the lateral electrical field than the other modes. The crossover point indicates that the hot-electron injection point has shifted from the end edge of the neutral region to the drain in the nitride storage layer beneath the word gate, resulting in better erase speed.

decreasing the efficiency of programming. This explains the typical bell-shaped distribution found in Fig. 2.

Furthermore, the DT mode exhibits different behaviors from those of the normal and body modes, as shown in Fig. 2. The typical programming characteristics of the DTSSI have a higher memory window while V_{SG} is still at a low voltage. To detail this phenomenon, we simulate the electrical field dependence of each mode, as shown in Fig. 3. Compared to the normal and body modes, the DT mode possesses a larger acceleration electrical field between the WSG and the word gate. Therefore, the hot-electron generation rate can be enhanced. By contrast, the body mode improves only I_{PGM} and degrades the lateral electrical field because of the higher V_{SG}. As a result, the body mode produces a traditional bell-shaped distribution (Fig. 2).

In sum, there are two major enhancing mechanisms for high programming speed of WSG SONOS under DTSSI operation. First, I_{PGM} increases in the DT mode [7]; second, the maximum lateral electrical field enhancement occurs at the same time in the gap region. Owing to the body effect in the DT mode, the equivalent oxide capacitance is increased by decreasing the depletion region under wrapped MOSFET. The increase of the inversion charge density per area leads to the strong I_{PGM} injection into the gap region. Furthermore, the charge reduction of the depletion width can effectively increase the lateral electric field by decreasing the vertical electric field effects, further resulting in better gate disturbance in the WSG SONOS. The hot-electron generation efficiency can be enhanced due to the tradeoff between the lateral and vertical electric fields in the gap region.

Fig. 3 also shows that the crossover point of both electrical fields indeed occurs near the end of the gap region close to the word gate in all three modes. Since DTSSI is used for programming, the slight reduction of potential differences between the word gate and the well, due to the positive body bias, can induce the hot-electron injection point to move toward to the drain terminal. This phenomenon is similar to a slight decrease in the word gate voltage. This improves the band-to-band hot-hole erasing process [7] without degrading the programming speed. In other words, the crossover point pointed out the

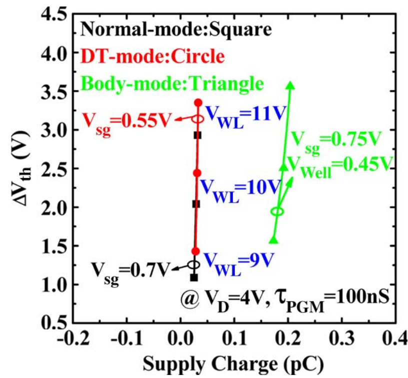

Fig. 4. Programming efficiency with the same supply charge $(\mathrm{Q}_{\mathrm{Supply\,charge}} = I_{\mathrm{PGM}} \times \tau_{\mathrm{PGM}})$ under $V_{\mathrm{WL}} = 9$ V, $V_{\mathrm{WL}} = 10$ V, and $V_{\mathrm{WL}} = 11$ V for each mode, respectively. This confirms the results and simulated conclusions from this figure.

most possible electron injection place due to its maximum vertical electrical field. It also implies that the charge storage spatial distribution in the nitride storage layer will vary with the applied program bias [2] across different SSI mechanisms when the hot-electron injection point is beneath the word gate, not beside it.

Fig. 4 displays the comparisons of programming efficiency for WSG-SONOS memory using different SSI modes under the same programming conditions $(V_{\mathrm{WL}} = 9\text{–}11\ \mathrm{V}, V_{\mathrm{BL}} = 4\ \mathrm{V})$, where the supply charge is defined as $Q_{\mathrm{Supply\,charge}} = I_{\mathrm{PGM}} \times \tau_{\mathrm{PGM}}$. We found that, at the same supply charge, the DT mode exhibits a lower word gate bias with lower V_{SG}, resulting in higher programming efficiency. Similar to the simulation results in Fig. 3, the very high programming speed with improvement of the programming efficiency can be attributed to the simultaneous enhancement of I_{PGM} and the lateral electrical field in the gap region. In addition, in the body mode, there is still a larger threshold voltage shift even with the lower lateral field. The drawback of body mode is its greater power consumption for higher supply charge due to its lower programming efficiency.

IV. Conclusion

The SSI mechanism under normal, body, and DT modes of WSG-SONOS memories was thoroughly investigated. Under DT mode, the devices exhibited increased lateral electric field and I_{PGM}. These changes enhanced the programming efficiency of WSG SONOS for NOR-type Flash memory.

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