國立交通大學

光電工程研究所

博士論文

多晶矽薄膜電晶體於主動矩陣式有機發光二極體顯示器之應用

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摘　要

近年來平面顯示技術不論在電腦資訊或家用電視領域上的發展，均大幅吸引人們的注意，由於平面顯示器具有輕、薄、低功耗、廣視角及全彩化之能力，因此在各個層面的應用上都具有相當大的潛力。有機發光二極體 OLED (Organic Light Emitting Diode) 因具有低操作電壓與高發光效率的特性的，利用此元件與技術所製成的顯示器具有輕薄、可撓曲式、易攜性、全彩高亮度、省電、可視角廣及無影像殘影……等優點，為未來平面顯示器的新趨勢。

由於被動矩陣(passive matrix)驅動方式在畫質相較主動矩陣式(active matrix)，在解析度、灰階數受到限制且無法實現精細化，因而採用薄膜電晶體(Thin Film Transistor; TFT)來控製 OLED 元件形成主動矩陣式顯示器，將是高畫質平面顯示器的趨勢，因為 OLED 是屬於電流驅動的元件，目前使用多晶矽(Poly-Silicon; poly-Si)技術來製作的薄膜電晶體，其物理特性較非晶矽的薄膜電晶體要來更好，由於電子移動率較快，不僅在 OLED 的畫素驅動電路上具有較好的特性，也能將週邊驅動電路一併整合至顯示面板上，以實現高度整合性之有機發光顯示器。

主動矩陣驅動顯示技術雖然具備實現高解析度顯示器的潛力，但由於 OLED 必須由電流來驅動以產生亮度，因此當 OLED 的電流通過每個畫素電極時，因導線的寄生電阻造成驅動電壓下降，使得主動矩陣式 OLED 面板仍存在亮度均勻性不佳的缺點，在本論文研究中則成功開發出「交流電壓驅動方法」來驅動 OLED 畫素電晶體。此驅動法利用儲存電容的耦合效應，配合交流電壓驅動信號，對導線

寄生電阻所造成的壓降進行補償的動作，經實驗證實顯示器亮度均勻性能有效提升，此外採用交流驅動方法所製作之面板，在電功率消耗上仍舊能維持與傳統直流電壓驅動法相同的水準。

在半導體製程中常因環境或人為因素造為元件特性穩定性不足，如 TFT 元件的閘電壓或是載子遷移率在玻璃基板各處之分布並非一定值，當畫素電路中的 TFT 特性產生漂移時，整體面板的亮度均勻性就受到相當大的影響，在此論文研究中，我們提出一具備電流驅動能力之 AM-OLED 顯示器，此顯示器中包含了由電流驅動之畫素電路，以及整合在面板上的電流型式驅動電路，利用高效能之電流記憶體電路配合參考電流產生器，此整合驅動電路能產生能符合顯示灰階所需的完整驅動電流，提供給 AM-OLED 畫素電路做為驅動信號，藉此電流驅動方式補償半導體元件特性漂移之現象，此外整合在基板內之驅動電路具有操作簡單及運作速度快等優點，利於高解析度 AM-OLED 顯示器之應用。

隨著 OLED 材料不斷進步，所需之驅動電流也逐漸降低，因為傳統的電流驅動方式在低灰階狀態下會遭遇資料寫入時間不足之現象，在此研究中我們發展一具有驅動電流放大功能之 AM-OLED 畫素電路，此電路中利用電容耦合之方式，來放大寫入畫素之資料驅動電流，在不須要增加 TFT 尺寸之下，此畫素電路具有廣泛的操作範圍，在高灰階狀態下有較低的放大率以避免過高的功率消耗，而當操作於低灰階狀態時也具有較高的放大率，藉此將輸入電流信號放大以提升信號寫入速度，同時此電流驅動之畫素電路仍能補償因製程或長時間操作所造成 TFT 之特性漂移，以實現高均勻性的亮度與畫質。

在畫素電路設計上不僅須考慮顯示畫質均勻性，且必須同時兼顧一畫素陣列的可測試性，在此論文研究中，我們發展出一新式畫素電路架構，在此架構中僅額外設計一測試電容於畫素電路當中用來確保畫素電路的完整性，藉此測試電容，在畫素電路中所有的 TFT 元件及儲存電容均可用偵測儲存電荷的方法來確認元件的特性與電路的功能。

論文中展現了薄膜電晶體技術在於有機發光顯示器上的重大應用潛力，提供系統設計者更多的技術來源與設計創意空間來開發更佳的顯像技術，此結合顯示電路設計與半導體製程的顯示面板開發技術，也將在未來高科技產業中具有益形重要的地位。

Applications of Poly-Silicon Thin Film Transistor for Active-Matrix Organic Light-Emitting Display

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Abstract

In recent years attractions have been made on producing flat panel display to replace the bulky CRT displays for computer monitors and televisions. Displays with the features of light weight, low power, high brightness, wide viewing-angles, and full color are essential for various applications. Combining Organic Light Emitting Devices with poly-Si TFTs to form an AM-OLED is an unique technology to meet those requirements. However, the AM-OLED still has several issues needed to be addressed. This dissertation presents a detailed study of the design of pixel and integrated driver circuitries to improve the image quality, functionality and testability for AM-OLED based on the poly-Si TFT technology.

In this dissertation we successfully developed an AC voltage driving scheme which can improve the brightness uniformity of AM-OLED displays. Through the use of a charge feed-through mechanism and an AC driving voltage, the voltage drop caused by the parasitic resistance can be compensated. A 2.2 inch AM-OLED panel has been improved by the low temperature polycrystalline silicon technology to evaluate the performance of the AC driving scheme. Experimental results show that a brightness uniformity of higher than 91.6% can be achieved by the AC driving scheme, in sharp contrast with 74% achieved by a DC driving scheme.

An integrated driving system including switch-current memory, digital-to-current converter, and reference current generator circuits has been developed for improving the accuracy of data programming and the operating frequency for AM-OLED's. The proposed switch-current memory, constructed from the current memory structure, can not only reduce the influence of charge-injection without using larger storage capacitor, but also realize the significant improvement in speed by use of small

storage capacitors. Furthermore, the capability of copying the current signal is achieved without relying on the matching of device characteristics. The switch-current memory circuit coordinating with reference current generator to form a digital to current converter is capable of generating accurate data currents for adequate gray scales. The experimental results not only demonstrate an achievement of uniform display luminance but also show great potential for high-resolution AM-OLED based on the current driving scheme.

A poly-Si TFT based pixel electrode circuit with a function of current scaling is proposed for AM-OLED's in this dissertation. In contrast to the conventional current mirror pixel electrode circuit, a high current scaling ratio can be achieved by using a cascade structure of storage capacitors, without increasing the size of the driving TFT in the pixel. Moreover, the proposed pixel circuit can also compensate for the variations of the TFT threshold voltage. Simulation results, based on poly-Si TFT and OLED experimental data, showed that a current scaling ratio of larger than 10 and a fast pixel programming time can be accomplished with the proposed circuit.

In this dissertation we present a functional testing scheme using a two TFT pixel electrode circuit of AM-OLED displays. This pixel circuit and the co-operative charge sensing scheme can not only evaluate the characteristics of each TFT, but also determine the location of line and point defects in the TFT array. Information on defects can be used in the repair system for cutting and repairing these defects. Furthermore, the functional testing scheme can be applied as a part of yield management of the AMOLED array process.

This dissertation has successfully demonstrated the great potentials of integrated driving circuits implemented by poly-Si TFT technology for portable AM-OLED applications. By using semiconductor process to fabricate AM-OLED panels with integrated current driving systems, the AM-OLED's are appealing for variety of novel applications in the near future.

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雖然這段旅程已經結束，但是學習的路途是如此的無窮無盡，此階段的開始象徵著另一個階段的到來，期許自己在下一段人生旅程能夠更加精進。

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Chapter 1

Introduction

As the necessity for mobile computing grows, the demands for good quality and reliable displays have also increased. The main objective for constructing a display is to achieve lightweight and flexibility together with high brightness, contrast and resolution suitable for the various applications. A wide viewing angle, low power consumption and low manufacturing cost are also desirable. The most common form of television and computer displays in use is the cathode ray tube (CRT). The CRT accelerates electrons (cathode rays) through an electrical potential to strike a certain area on a screen. The phosphors that can emit photon when the electron strikes it are attached to this screen. The color contrast and resolution from CRT displays are very good, but the device is bulky and thus impractical for portable and lightweight applications.

In recent years attractions have been made on producing flat panel display to replace the bulk CRT display in computer monitor and television applications. In general, there are two main categories among the display technologies used today: emissive and non-emissive. The main difference is that the non-emissive displays in which light is modulated to show information need external light sources. In comparison with emissive displays, which have no need of external light sources. Examples of non-emissive displays are liquid crystal display (LCD) and among the emissive displays are CRTs and light-emitting diode (LED). Organic light-emitting device (OLED), another common and also the new technology used for display applications, is also of emissive type. General aspects of LCD and OLED are briefly

introduced in the following.

1.1 Liquid crystal display limitation

The current display technology used in portable televisions and lap top computers is LCD. These displays utilize liquid crystal materials that align in certain direction when an electric potential is placed across them, to create an image on a screen [1]. Thus, the LCD operates on the basis of either passing or blocking light that is produced by an external light source usually from a backlight system. Aligning the crystals with electricity is very energy efficient, but due to the non-emissive property, LCD requires a great deal of energy for the backlight system, as shown in Fig. 1-1.

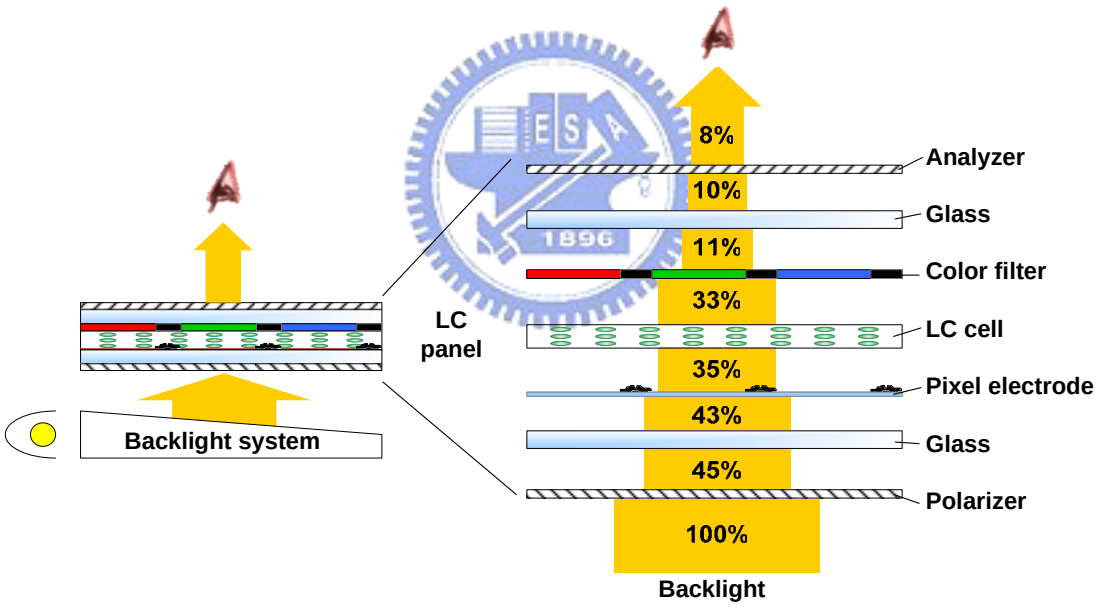


Fig. 1-1. A transmissive type LCD with backlight system and the light transmittance after light passes through each component of the LCD.

Besides, the devices in the LCD embodiment including polarizer, pixel electrode, LC cell, color filter, and analyzer absorbs or blocks the backlight, so that the transmittance is only about 8%. Therefore, such low light throughput requires a powerful backlight system to achieve sufficient brightness, thus inefficient in energy

usage. Consequently the applications that utilize this technology, like notebooks, have great concern on battery. Moreover, the optical properties of the LC material and the polarizer also causes the “viewing angle effect”.

1.2 Organic Light Emitting Device as a Promising Alternative

With these remain issues of LCD’s, there has been a lot of effort to find alternatives for display applications. Since the report of high efficiency electro-luminescence from organic light-emitting device in 1987 by Tang et. al [2], OLED has raised a great interest among the display community. Later, Burroughes et. al. demonstrated that a conductive organic polymer film consisting of poly paraphenylenevinylene, or PPV, can be used as the active element in a large-area light emitting device [3]. As a relatively new technology, OLED uses thin layers of organic small molecules or polymers whose behaviors are much like single-crystal semiconductors. A light-emitting layer sandwiched between an electron-transport and a hole-transport layer can act much like a conventional LED with electrons and holes combining in the emitting layer to produce light. Unlike LCD’s, the OLED is self-emissive thin-film device that requires neither the backlight, top glass, nor the color filter. Color can be achieved either through selective doping of the organic small molecules or through alternating the organic polymer structures. OLED-based displays have the potential of being lighter, thinner, brighter and much more power-efficient than LCD. Moreover, OLED-based displays do not suffer from the viewing angle issues. There are several important features for OLED as display applications.

1. In organic devices the materials are usually fabricated as thin amorphous films, which can be processed easily over large areas;

2. Amounts of organic materials are relatively small (100 nm thick) in the display fabrication process so that large-scale production (chemistry) is easier than for inorganic materials (growth processes of single crystals etc.);
3. OLED can be tuned chemically in order to adjust the band gap separately, charge transport as well as solubility and several other structural properties;
4. The amorphous nature of polymers provides additional advantages in terms of film fabrication;

Recent improvements in the quantum efficiency of OLED have given a much needed boost to the several key applications [4]. A complete overview of several techniques to improve the resolution and brightness of these displays can be found in these works [5][6][7]. In the future, OLED displays are likely to compete with LCD's in applications ranging from cellular phone displays to high information content notebook computers due to its unique features.

1.3 Polysilicon TFTs for active-matrix addressing

During the past few decades, the passive-matrix addressing technology for either LCD or OLED was optimized to achieve the maximum performance. However, the contrast ratio of passive-matrix addressing is limited because the duration of pulsed signal decreases as the display resolution and gray level increase. Passive-matrix addressing has been replaced by active-matrix addressing in high-information content applications. Active-matrix arrays contain many individual elements commonly known as pixels, which are generally addressed or read out by a grid structure of interconnecting lines termed gate and data lines. In active-matrix array, each pixel is usually composed by either two-terminal or three-terminal devices which work as a switch to store and retain the video information on a storage capacitor during a

complete frame time. The two-terminal device, typically a Schottky or PIN diode that passes current one way, is usually made of amorphous silicon, a bidirectional current-passing metal-insulator-metal (MIM) structure with an insulator film composed of PECVD-deposited silicon nitride (SiN_x), diamond-like carbon, or tantalum pentoxide (Ta_2O_5) [8][9][10]. The three-terminal array switches are field-effect transistors (FETs), such as crystalline Si (c-Si) metal oxide-semiconductor field-effect transistors (MOSFETs) or thin-film transistors (TFTs). Since the lithography-stitching limits, large area c-Si manufacturing is still very costly, and the temperature required for bulk crystalline formation make it difficult to integrate c-Si with plastic or glass substrates. Therefore the c-Si active-matrix arrays are only restricted to small size (< 1 $in.^2$), high-resolution displays, such as head-mounted displays and light valves commonly used in projection displays. By contrast, the thin-film transistors can be easily fabricated for large size substrate by either amorphous or polycrystalline silicon technologies.

Hydrogenated amorphous-silicon (a-Si:H) is used extensively to fabricate TFTs for flat-panel displays. a-Si:H TFTs have a low leakage current and sufficient on-current for most applications, and can be fabricated at low temperatures (< 350ºC) on inexpensive glass substrate. However, a-Si:H TFTs suffer from poor carrier mobility and large threshold voltage shift. The mobility of amorphous-silicon is too low (0.1~1 cm^2/V-s) to be used in the peripheral driving circuitry, so that single-crystal integrated circuitry must be bonded to a substrate containing the amorphous-silicon active matrix, consequently, increasing the cost and decreasing the reliability. Besides, the low mobility also causes a limitation on the aperture ratio and the pixel size for display applications, and the poor hole mobility prohibits a usable p-channel TFT. The drifting threshold voltage also imposes reliably in integrated

display drivers, such like column multiplexer and the shift register circuits of scan line.

Polycrystalline silicon (poly-Si) TFT technology presents advantages over a-Si technology on the achievable size-versus-resolution limits for the display, as well as the opportunity to integrate additional functionalities on the panel. The advantages of poly-Si technology primarily originate from the significant performance of poly-Si TFT and the fabrication compatibility with CMOS technology which is capable to monolithically integrate peripheral drivers on the panel. Essentially, the effective carrier mobility in poly-Si of 10~500 cm^2/V-s is significantly higher than that of a-Si. The higher mobility can:

Reduce the size of the TFT and increase aperture ratio resulting in higher brightness and lower power. The higher mobility enables smaller channel widths to be used for a given channel length while retaining sufficient driving current. Higher aperture ratio is also achieved through full self alignment of the source/drain regions which can reduce the parasitic and overlap capacitance and the size of the storage capacitor.

Enable the integration of driver and the possibility of a complete system on glass and increase the panel reliability. The ability of poly-Si TFT to integrate driver circuitry on active-matrix display panels can lead to more reliable displays. Driver integration not only eliminates the weight and thickness of the display module, but also reduces a number of driver ICs and the interconnections between the display panel and the external print circuit boards (PCBs) so that the display module can significantly withstand the greater shock and vibration. Driver integration can be matched to an analog display interface or to a fully digital display interface. In the former case, key circuitries such as buffers, shift

registers, and scan driver are required. In the last case, the digital-to-analog converter (DAC), operational amplifier (OPAMP) and high speed register are needed, in addition to the components for the analog interface, as shown in Fig. 1-2.

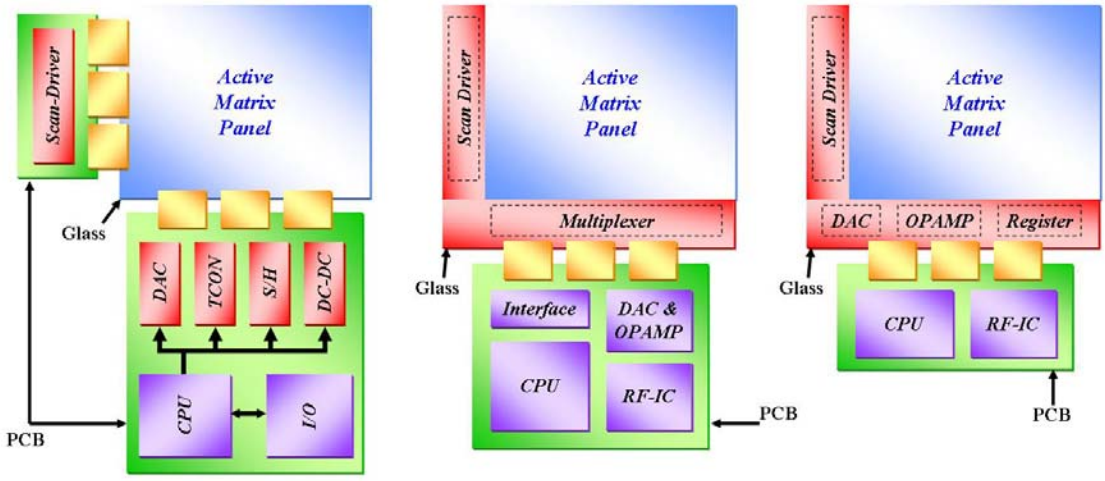
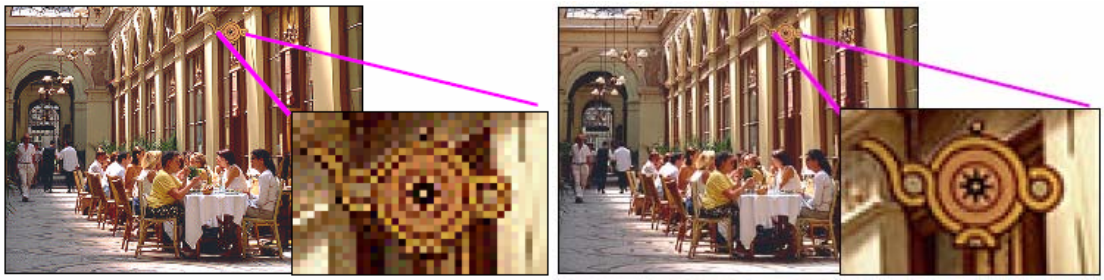


Fig. 1-2. Block diagrams for (a) conventional a-Si TFT display, (b) poly-Si TFT display with integrated driver, and (c) poly-Si TFT display with fully digital-interface integrated driver.

Enable the panel with higher pixel density and result in increased information content and legibility. The smaller transistors and reduced TFT "ON" resistance result in a reduced resistance capacitance (RC) delay which allows more pixels to be squeezed on a given display and while still satisfying the programming time, power consumption, and luminance requirements. The time required to settle a pixel to the required voltage accuracy to achieve the desired gray level is called the programming time which is a function of RC delay. Poly-Si TFT has a lower RC delay so that the multiplexed addressing scheme for high resolution display is easily achieved. In a-Si TFT technology, as the resolution increases with the fixed mobility and channel length, a larger TFT and high operation voltage are needed to charge the pixel in an available time,

therefore, result in the reduced aperture ratio, lower luminance and high power consumption. Consequently, poly-Si TFT is a better candidate to achieve smaller pixel pitch and higher pixel density to meeting the requirements of high resolution display, as shown in Fig. 1-3.



(a) (b)

Fig. 1-3. Picture quality resolution for active-matrix displays achieved by (a) a-Si TFT and (b) poly-Si TFT technologies.

1.3.1 Mobility

The effective velocity of carriers through a given material is the product of the mobility which is termed μ_n (electron mobility) and μ_p (hole mobility) and the electric field strength. In semiconductor theory, the drain current of TFT is proportional to mobility. To achieve a given current, the higher mobility the TFT possesses, the smaller the transistor width to length ratio (W/L) can be employed. As shown in Table 1-1, mobility for c-Si semiconductor devices is in the range of 500 to 600 cm^2/V-s, while poly-Si TFT mobility ranges from 100-500 cm^2/V-s for top gate NMOS devices and 10-50 cm^2/V-s for bottom gate NMOS devices. In the case of a-Si TFT, mobility is typically 0.1-1 cm^2/V-s. Because top gate device with fully aligned source and drain regions results in significantly higher mobility performance, it has been adopted for most poly-Si TFT fabrications.

Higher mobility is essential in order to integrate more driver circuitries. Mobility

performance is closely related to the grain size. C-Si, with a single grain has the highest mobility among the mentioned fabrication technologies. In poly-Si the nature of the crystallization process typically results in the formation of numerous small grains under 1μm which reduces the mobility. Because there are typically numerous grains in the channel, the uniformity of the grain size is also critical. A great deal of researches have studied the variations in laser energy density as the cause of grain size non-uniformity problems. Thus, despite the mobility of poly-Si today is at the lower end of the range, it is expected to be improved in the near future if larger grain size with controlled grain boundaries are implemented which will shorten the performance gap with c-Si devices.

Table 1-1. Electrical characteristics of poly-Si TFT

	c-Si NMOS	Poly-Si top gate NMOS	Poly-Si bottom gate NMOS	a-Si NMOS
Mobility (cm^2/V-s)	500-600	100-500	10-50	0.1-1.0
Leakage current (pA/μm)	0.002-0.004	0.05	0.1	0.01
Threshold voltage (V)	0.7-1.0	1-4	2-5	2-5

1.3.2 Leakage current

A low “OFF” current , I_{OFF}, or called leakage current is essential for good pixel voltage retention. Leakage current has been a serious issue for poly-Si TFT active-matrix array and manifests itself in the form of image degradation. Poly-Si leakage current is typically 5-10 times larger than that of a-Si and 25-50 times larger than c-Si silicon, as shown in Table 1-1. High leakage current in poly-Si TFT is

caused by grain boundaries in the high electric field region between the drain and the gate edge. Based on the nature of the device structure, leakage current is typically larger for bottom gate devices than that of top gate devices. To reduce the leakage current, it is necessary to suppress the electric field density in the channel at the edge of the drain. The reduced electric field density not only suppresses leakage current when the gate and drain are biased, but prevents degradation of device characteristics over time due to the injection of “hot” electrons into gate oxide. Numerous methods have been proposed for reducing the leakage current, for example, adopting a single or double lightly doped drain (LDD) or implementing multiple gates. An LDD can reduce the high gate-to-grain field and the multiple gates can decrease the probability of grain boundaries occurring at the drain edge.

1.3.3 Threshold voltage

Threshold voltage (V_{th}) is the value of gate-to-souce voltage (V_{GS}) at which a sufficient number of mobile electrons accumulate in the channel region to form a conduction region. V_{th} is of positive value for an n-channel device and negative for a p-channel device. The value of V_{th} is controlled during device fabrication and is of less than 1V for c-Si devices as shown in Table 1-1. The drain-to-source voltage (V_{DS}) causes a current to flow through the induced channel. The current is carried by free electrons traveling from the source to drain. The magnitude of the drain current depends on the density of electrons in the channel, which depends on V_{GS}. When $V_{GS}=V_{th}$, the channel is nearly induced and the current is negligibly small. As V_{GS} exceeds V_{th}, more electrons are attracted into the channel and the conductance of the channel is proportional to the overdrive gate voltage ($V_{GS}-V_{th}$). Since threshold voltage is a function of the drain current, it follows that devices with lower mobility

will operate at a higher V_{th} and require higher source voltage, implying greater power consumption.

1.3.4 Poly-Si TFT fabrication flow

As already discussed, a key advantage of poly-Si TFT technology is the ability to integrate the driver circuitries with the pixel array on the same substrate. The following illustration shows a representative process flow for the simultaneous fabrication of n- and p-channel TFTs which are compatible with conventional CMOS process. This particular process flow yields self-aligned, top-gate poly-Si TFT with the LDD configuration. The process is outlined next and shown schematically from Fig. 1-4(a) to Fig. 1-4(l).

Typical process flow for self-aligned top-gate poly-Si TFT

1. Sequential deposition of base coat (SiO_2, SiN_x) and a-Si film on the glass substrate.
2. a-Si de-hydrogenation
3. Low-temperature crystallization of a-Si film with excimer laser to obtain poly-Si film.
4. **Mask #1**: active island definition, Fig. 1-4(a).
5. **Mask #2**: Channel doping for n-channel TFT, Fig. 1-4(b).
6. **Mask #3**: Source/Drain (S/D) region doping, Fig. 1-4(c).
7. Deposition of gate dielectric layer, Fig. 1-4(d).
8. Gate metal deposition
9. **Mask #4**: Gate definition, Fig. 1-4(e).
10. LDD region doping with self-aligned structure, Fig. 1-4(e).
11. **Mask #5**: S/D doping for p-channel TFT, Fig. 1-4(f).

12. Deposition of interlayer dielectric film, Fig. 1-4(g).

13. **Mask #6**: S/D contact hole definition, Fig. 1-4(h).

14. S/D metal deposition.

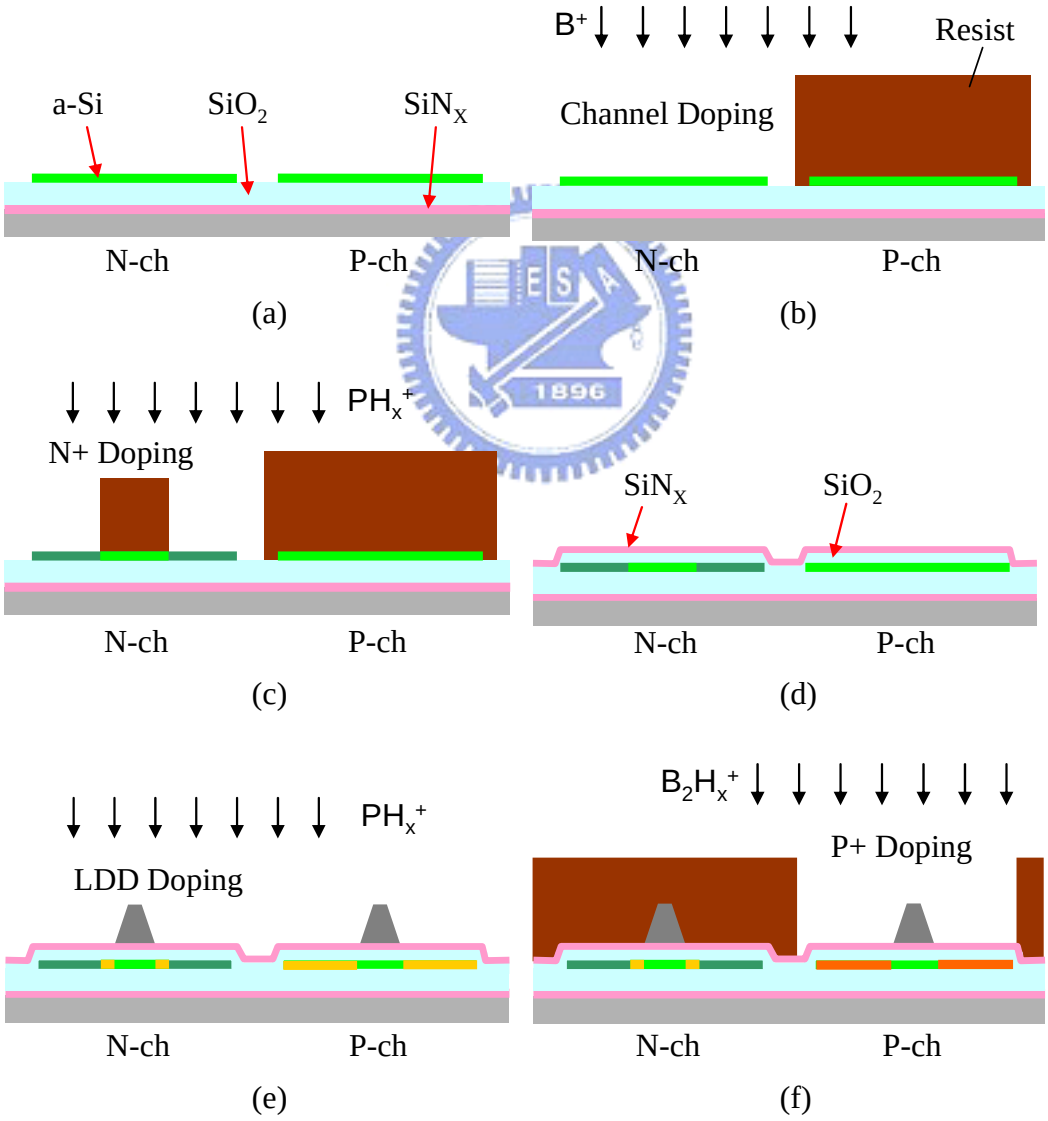
15. **Mask #7**: S/D electrode definition, Fig. 1-4(i).

16. Deposition of organic planarization layer, Fig. 1-4(j).

17. **Mask #8**: ITO electrode contact hole definition, Fig. 1-4(k).

18. Pixel ITO deposition.

19. **Mask #9**: ITO electrode definition, Fig. 1-4(l).



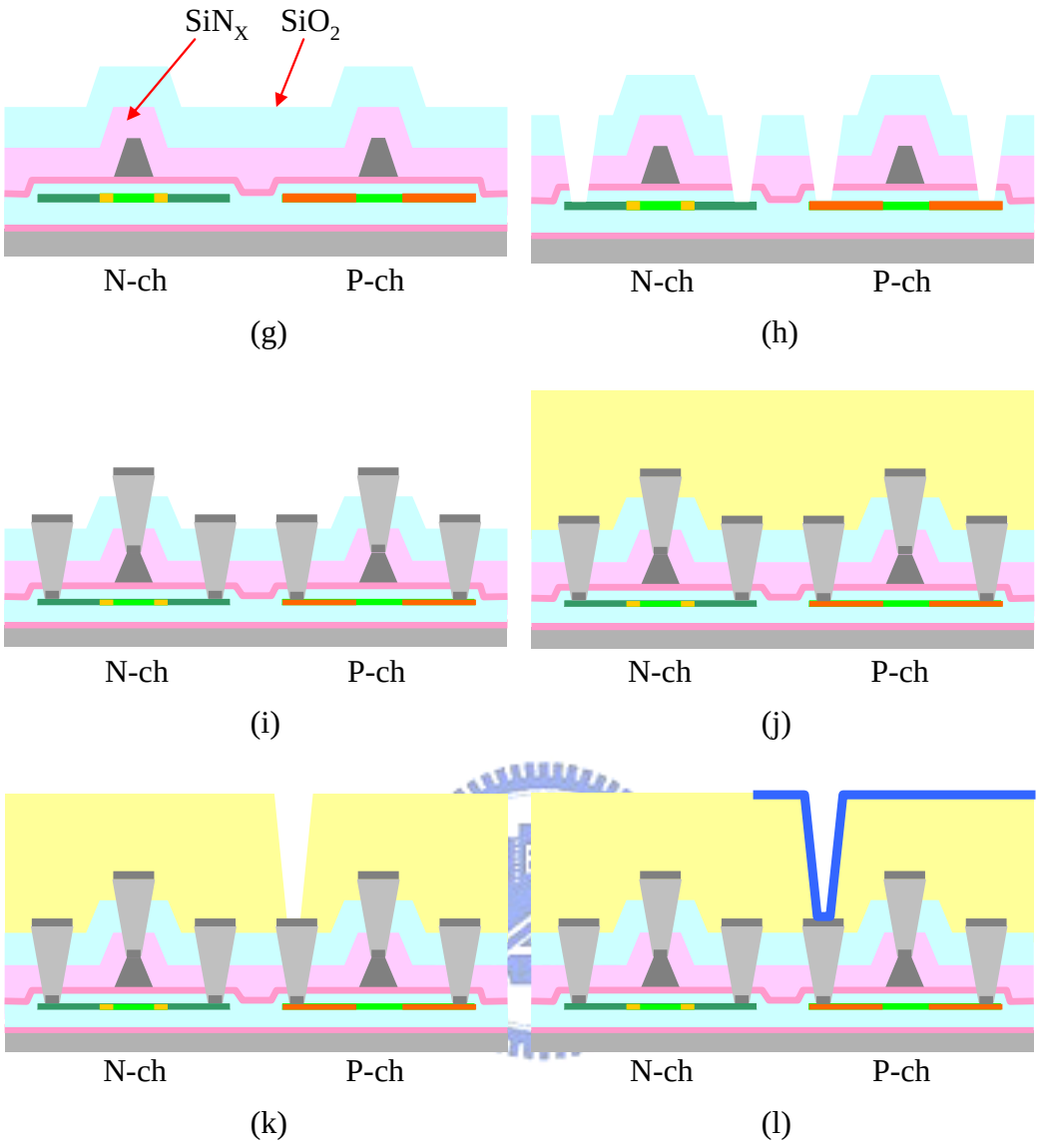


Fig. 1-4. Process flow of self-aligned top-gate poly-Si TFT with lightly doped drain configuration. (a) Deposition of a-Si and buffer layere (SiOx and SiNx). (b) Channel doping for N-channel TFT. (c) Source/drain doping for N-channel TFT. (d) Gate oxide deposition. (e) LDD doping with self-alignment structure. (f) Source/drain doping for P-channel TFT. (g) Deposition of insulation layers. (h) Contact hole etching. (i) Metal electrode deposition. (j) Organic preservation layer deposition. (k) Contact hole etching and (l) ITO electrode depositon.

1.4 OLED combined with poly-Si TFT

Since OLED is a current driven device, higher current supplied to OLED results

in higher brightness. In the case of a-Si TFT, a device with larger W/L and higher operation voltage are essential to provide enough current supply to the OLED. Nonetheless, larger W/L TFT design results in less OLED emission, which means smaller aperture ratio in the bottom emission structure AM-OLED. Because a pixel consists of TFT area and OLED emitting area, the larger the occupation area of TFT, the smaller the OLED emitting area. As the resolution gets higher, pixel size becomes smaller but the area of TFT remains the same. Hence, the OLED emitting area becomes smaller, prohibiting the a-Si TFT to be used in small sizes with very high-resolution AM-OLED applications. Therefore, the motivation for the integration of OLED and poly-Si TFT technology is desired to give a power-efficient operation and increase the reliability of the panel. This is due to the high drive currents and the long term stability of the poly-Si TFT compared to the a-Si TFT, while a sufficient current supply from TFT is essential for panel operation [11][12][13].

Nonetheless, even poly-Si technology offers the potential of great driving capability and driver circuitry integration, the AM-OLED design still has several technical challenges:

Poly-Si TFT V_{th} uniformity - Poly-Si TFT threshold voltage uniformity is primarily a function of the laser annealing process stability. The uniformity variance should be of less than 5% across the panel to allow for adequate margins in designing the proper gate and data voltages. When the uniformity exceeds the design margins, the potential for not fully charging the pixel exists. That will result in uneven brightness for a give gray level. Compensating for non-uniformity by increasing voltage inversely increases the power consumption.

Lifetime - It was already known that a high drain voltage and a relatively high gate voltage (hot-carrier conditions) in poly-Si TFT can decrease the maximum

transconductance and causes the variation of threshold voltage [14][15][16][17]. The degradation of transconductance and the threshold voltage variation associating with bias and temperature stress are of great concern to integrate TFTs on the substrate. Besides, the degradation alters the characteristics of poly-Si TFTs in pixel electrode circuitry so that the output current for driving OLED deviates with given voltage signals as well. In other words, the variation of display luminance accompanied with device degradation results in image quality degradation.

1.5 Motivation and objective of this dissertation

New generation mobile communication and personal information systems, such as mobile phone, hand-held personal computer (HPC), digital camera, and game-boy player have progressed rapidly. Displays with the features of light weight, low power, bright, wide viewing-angle, and full color are essential for above applications. OLED combined with poly-Si TFT technology to form an AM-OLED is an unique feature those requirements. However, the AM-OLED still has several issues needed to be improved.

This dissertation presents a detailed study of the design of pixel electrode and integrated driver circuitries to improve the image quality and functionality testability for AM-OLED based on poly-Si TFT technology. The theoretical analysis of the performance of pixel electrode circuit and integrated driver circuitries will base on the principle of poly-Si TFT. Additionally, the 9-masks fabrication process for poly-Si TFT was utilized to realize the design.

Since the luminance of OLED is directly proportional to the driving current, each pixel in active-matrix TFT array consumes a certain amount of current supplied by the power electrode. The power electrode in active-matrix array is usually fabricated by

metal materials such as molybdenum (Mo), aluminum (Al) and copper (Cu). The current signal passing through these metal wires can generate the voltage drop due to the intrinsic resistance and affect the luminance uniformity. Increasing the wire width of the electrode can reduce the parasitic resistance, however, the aperture ratio will be decreased. It is expected that the voltage drop caused by the parasitic resistance will become the critical drawback in display applications of large size and high resolution. In this dissertation, we propose a simple AC voltage driving scheme with an adequate design of conventional two transistors (2-T) pixel circuit for AM-OLED displays. By means of the charge feed-through mechanism of storage capacitor, the proposed AC driving scheme can counteract the voltage drop caused by the parasitic resistance. Without employing the complicated driving system, the AC driving scheme can effectively improve the brightness uniformity.

Ensuring the brightness uniformity of each pixel is essential for rendering of high quality images of poly-Si TFT AM-OLED. The variations of device characteristics caused by device aging or manufacturing process are still an issue in poly-Si TFT technology. More specifically, the variations of threshold voltage can affect the drain current and lead to change of the pixel luminance. Due to the variation of device characteristics, the current driving technology with self-compensation function is the leading scheme for achieving the uniform image quality for AM-OLED. In this research, we proposed a fully-integrated current-type driving system including the pixel electrode circuitry, current generator, current-type DAC, and current-type memory. With this integrated driver, only small digital voltage signals are needed for the display interface so that the conventional driver ICs for active-matrix display still can be used. Besides, the precise current signal for various gray levels can be correctly manipulated in this driver system to compensate the characteristic variations

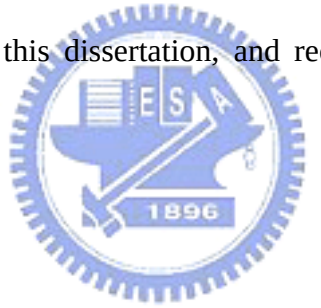
of poly-Si TFT.

In active-matrix TFT array processes for both AM-LCD and AM-OLED applications, TFT array inspection and yield management are important to ensure the reliability of display applications. In-line testing of TFT array in a manufacturing process is beneficial for yield improvement because the faulty TFT array can be repaired or scrapped before encapsulation, and external driver assembly. Likewise, utilizing TFT array testing for failure analysis can detect the location of the faults and identify the categories of faults in TFT array. The conventional AM-OLED pixel circuit does not provide for fully functional testing with electrical charge sensing scheme as the AM-LCD pixel does, unless an additional component can be added-in. Here, we propose the modified pixel circuit for not only the voltage-driven but also the current-driven pixel circuitries to measure the characteristics of TFT and detect defects. The convenient charge sensing scheme can be used to effectively determine and analyze the circuit breaks, shorts, and leaky transistors or capacitances. The proposed TFT array testing scheme is demonstrated to be a good tool for managing the yield of the array process of AMOLED.

1.6 Organization of this dissertation

The dissertation is organized as following: The review of OLED technology is presented in **Chapter 2.** The physical mechanism, fabrication process, full-color technologies and lifetime issues are described in this chapter. In **Chapter 3,** the basic analysis of passive-matrix addressing scheme is described to derive the limitation of PM-OLED. Following is the fundamental design principle of conventional voltage-driven AM-OLED. To suppress the issues of conventional voltage-driven AM-OLED due to the parasitic resistance effect, AC driving scheme, which can yield

high luminance uniformity and long device lifetime, is shown in **Chapter 4.** Due to inherent characteristics variations of poly-Si TFT that result in inferior luminance uniformity, using current-driven scheme with full-integrated driver circuitries for enhancing the image uniformity are demonstrated in **Chapter 5.** In this chapter, different designs of pixel circuit are detailed to improve the long programming time issue induced by current-driven scheme. Moreover, the design for peripheral driver system including current-type DAC, and high-speed current memory are also described. An modified current-driven pixel electrode circuit with current scaling function which can enhance the data programming speed is discussed in **Chapter 6**. In **Chapter 7**, the charge-sensing approach with the modified pixel schematic is presented to easily enhance the functionality testability of AM-OLED. Finally, discussions and summary of this dissertation, and recommendations for the future works are given in **Chapter 8**.



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Chapter 2

OLED - Organic Light Emitting Device

2.1 Introduction

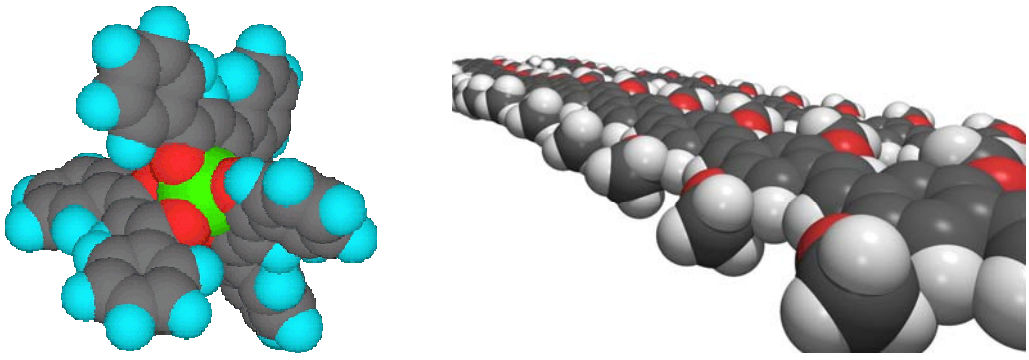
During the last fifty years, the semiconductor physics have played an important role in industrial and technical developments and are used in numerous applications, e.g. diodes, transistors and sensors. Compound materials with combinations of the III– and V-groups of periodic system possess semiconductor properties. The principle of light generated by applying an electrical field to this semiconductor material is known as electroluminescence. A conventional LED constructed of semiconductor materials is based on this luminescence phenomenon and has been mass-produced in the last thirty years. The applications for the LED are found in several areas including optical communication and dot matrix displays because of their ability to emit intensive light.

In spite of the fact that the organic material carbon (C) is positioned in the IV-group as the semiconductors materials, it is considered as an isolator. Nevertheless, Hideki Shirakawa discovered a conducting ability of the organic material in 1977 [1][2][3][4] for his the Nobel Prize in chemistry in 2000 and started a new era of the semiconductor technology for new applications.

In 1987, the group of Tang and Van Slyke at Eastman-Kodak presented luminescence by an organic material [5]. The group constructed an efficient OLED, which was driven by a rather small voltage. The technique they used to emit light was vacuum deposition of small molecules to form a multi-layer thin-film structure. The layered structure is sandwiched between two electrodes: anode and cathode. The thin layer (<1 μm) of organic material permits a high electrical field at low voltage. Thus,

light from thin film organic materials is usually produced at low voltage. High quality thin molecular layers were an important condition for the development of OLED.

In 1990, a group at the Cavendish Laboratories at Cambridge University presented the first LED using polymers as active material. The active polymer was a conjugated polymer [6]. In comparison to the traditional solid state LED, the new organic approaches were believed to be much more efficient. The conjugated polymers and small molecules are considered as the two classes for OLED. The two classifications of light-emitting organic layers in the OLED devices both possess luminescent and conductive properties. Small molecules have molecular structures of relatively short chain length and consequently low molecular weights. The most commonly used material with the most explored properties among the small molecules is tris-(8-hydroxyquiniline) aluminum (Alq_3), as shown in Fig. 2-1(a). The conjugated polymers are composed of a long repeating chain of similar smaller molecules, called monomers. They possess consequently, compared to small molecules, a molecular weight twenty to fifty times higher. A frequently used conjugated polymer is the poly-paraphenylene vinylene (PPV), as shown in Fig. 2-1(b).



(a) (b)

Fig. 2-1. Chemical structures of (a) tris-(8-hydroxyquiniline) aluminum (Alq_3) and (b) poly-paraphenylene vinylene (PPV).

2.2 Luminescence of organic materials

Organic materials refer to a base of the IV-group carbon and with additional elements such as hydrogen (H), nitrogen (N), oxygen (O), phosphorus (P) and sulfur (S). Since polymers and organic materials are not referred to conducting materials because of the large band gap between conduction and valence bands, a very high electrical field has to be applied. When applying an electrical field, charge carriers including hole and electron are injected from the electrodes into the organic layer respectively and result in geometrical defects on the symmetric organic structure and exhibit a lower band gap according to

Fig. 2-2. The charged carriers move along the structure and the attraction between the carriers results in a recombination of electron and hole to form an exciton which has a possibility to emit light as photons. The exciton is either in singlet or in triplet-state according to the Pauli's principle [7]. The exciton will form two new energy bands inside the band gap. The energy level of the exciton is below the conduction band and the released energy is emitted as photons. Upon the relaxation of exciton, heat and photons will be emitted with an energy set according to the gap between the energy bands. The states of the exciton have certain influence of the emission of light and quantum efficiency since the singlet states release its energy as an emission of photons. However the triplet-state is regarded as the heat forming state and can not transfer to light. In some special cases, the triplet-state generates light as well.

The backbone of the organic materials is strongly localized bonds between the carbon atoms. The conductivity is enabled through bonds that are orthogonal to the backbone. The length of the conjugation, i.e. the conjugation length, set certain characteristics of the molecule. The conjugation length defines the length where the

electron is free to move within. In general, small molecules tend to have short conjugation length, while longer conjugated molecules, polymers, may have a longer. Longer conjugation length results in a smaller band gap. It is therefore easier to produce red light with conjugated polymers compared to small molecules, and consequently small molecules can more easily generate blue light.

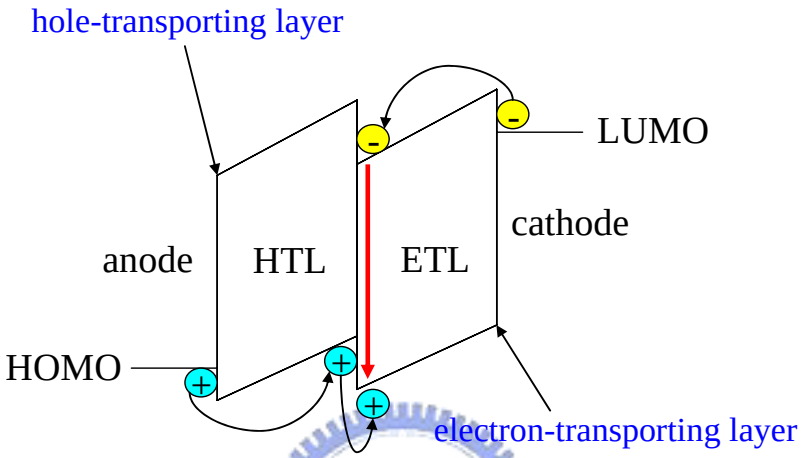


Fig. 2-2. Schematic energy band diagram of OLED and electron-hole recombination in forward bias condition.

2.3 The composition of OLED

2.3.1 The mono-layer device

The simplest OLED, a mono-layer device, is constructed of a thin layer of organic material sandwiched between two electrodes. As shown in Fig. 2-3(a), the function of the anode is to supply positively charged holes and a frequently used material, due to the requirement of transparency, is the Indium Tin Oxide (ITO). The cathode electrode supplies electrons to the organic layers. The charged carriers of electrons and holes are injected into the thin emitting layer material where they form an exciton and generate photons afterwards. The fact of the singlet and triplet states of the excitons has a certain influence and limitation on the device quantum efficiency.

Because of the disordered structure in organic materials, the behaviors of the charged carriers in organic materials are not similar to that in metal. This fact impedes a recombination and decreases its probability [8]. Therefore, there is always one dominant charge carrier that moves through the material without recombining with the opposite charge carrier. Another problem related to mono-layer devices is that the charge carriers tend to remain at one of the electrodes and creating space charges that prevent further hole and electron injections. Furthermore, if charges form an exciton near a metal, quenching mechanism can destroy the exciton and reduce the light generation efficiency.

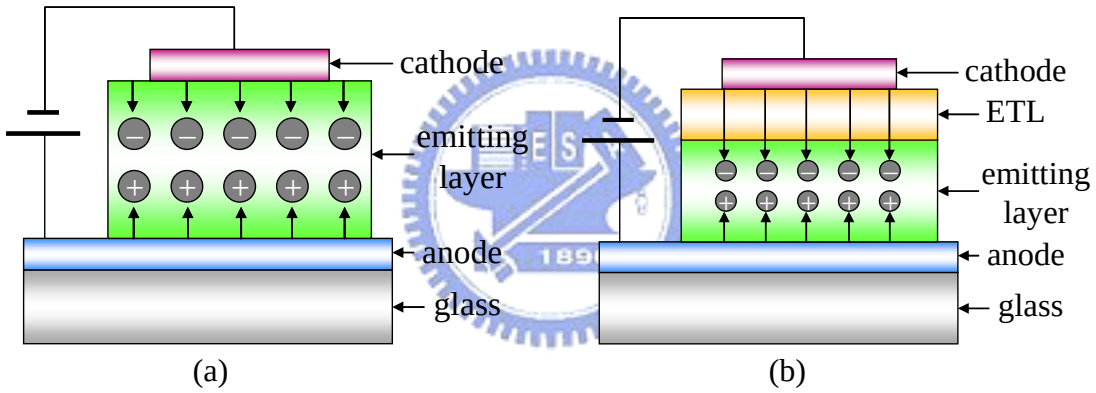


Fig. 2-3. Configurations of OLED for (a) fundamental single-layer structure and (b) double-layer heterostructure structure.

2.3.2 The double-layer device

A minimization of the energy barrier between the electrodes and the organic material is another approach to enhance the injection of the carriers. The mono-layer device is then upgraded to a double-layer device. Instead of one organic layer, two layers, an emission and an electron-injection layer, are placed between the electrodes, as shown in Fig. 2-3(b). By choosing the materials according to their properties of mobility, band gap, the charged carriers can be injected and transported in an easier

manner into the emission zone where an emission of light takes place [9].

The band diagram of the materials can be matched better to the specific electrodes through the double-layer construction and result in improved equilibrium of the currents of holes and electrons. The electrical field can consequently be decreased, which increases the efficiency and lifetime of the device. The difference in energy levels between the two organic layers creates a potential barrier at the interface. The barrier confines the holes and electrons and contributes to an increased recombination probability [10].

2.3.3 The multi-layer device

The functionality of the double-layer device and its components can be further improved with regard to several layers and minimal potential barriers. The greatest advantage of a multi-layer structure, compared to a double-layer, is the possibility to separate transport regions from the emitting region. This multi-layer structure accomplishes a better performance and an increased range of colors of the emitted light. By tuning the voltage over the electrodes, a proper placement of the emitting zone can be achieved, which may improve the efficiency of the device. The structure in Fig. 2-4 is an example of a multi-layer bottom-emission OLED, which has its light emitted through the transparent anode.

The substrate on which the OLED is fabricated consists of a material with a rigid or a flexible structure, e.g. glass or plastics. Compared to flexible substrates, rigid materials are of advantage for their ability to prevent the device from moisture and air. An outer exposure of moisture and air without any protection significantly degrades the lifetime and performance of the device.

To enhance the injections from the anode, according to Fig. 2-4, a hole injection

layer (HIL) is introduced for control and an enhancement of the injection of the holes into the hole transport layer (HTL). An effective HTL of p-type material can effectively enhance the transportation of holes to the emitting zone. The excitons are expected to be formed in the emitting layer (EL) and eventually emit light. Since equilibrium of mobilities between the carriers is difficult to achieve, a blocking layer can be used to confine the charge carriers to perform a maximum recombination.

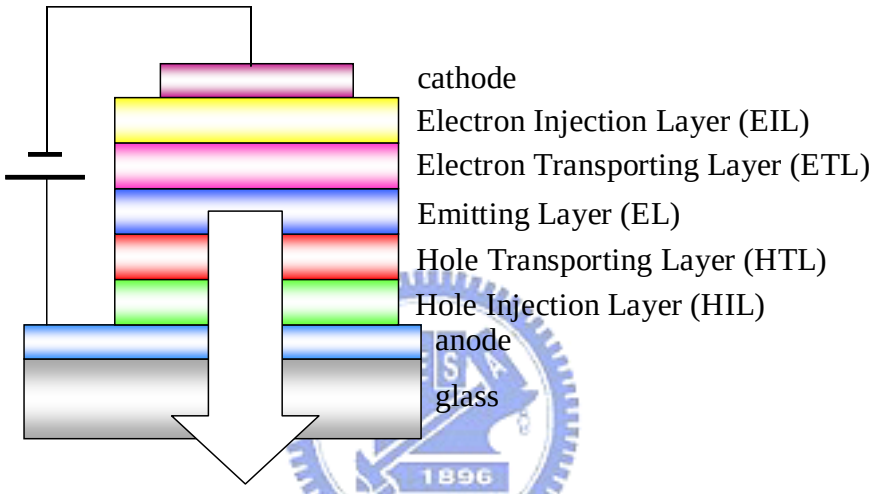


Fig. 2-4. Multi-layer OLED structure with additional functioning HIL, HTL, EIL and ETL.

The electron transport layer (ETL) is of n-type doped material which can enhance the mobility of the charge carriers and the transportation of electrons to the emitting layer. The layer also functions as hole blocking and is suitable to control specific charged carries. The ETL can, similar to the HTL, be used as an emitting layer. Similar to the holes, an organic electron injection layer (EIL) is used to assist the electrons to cross the barrier between the cathode and the ETL. Due to the enhanced transportation of electrons, a low electrical field is adequate for the multi-layer device and leads to a more power efficient OLED. It is furthermore possible to use the same material for the two electrodes, yet at a reduced efficiency.

2.3.4 Modifications

A bottom-emission OLED has a transparent substrate such like the glass. A silicon backplane can be used as the substrate as well and with a different combination of the electrodes and the organic layers to form a top-emission device can be accomplished. In comparison with conventional bottom-emission OLED, the top-emission OLED presents more advantageous for some micro-displays appllications[11][12]. When using a transparent cathode in the bottom-emission OLED, the device has become a transparent OLED (TOLED). The transparency of the device then is nearly as transparent as the chosen substrate. For advanced multi-stacked OLED devices, e.g. stacked OLED (SOLED), the transparent device is required.

It is also possible to apply the OLED on a flexible material to make a bendable or foldable display, enabling a completely new era of display types, e.g. displays directly deposited on the windshield or the helmet visor. Although more research has to be done in order to make the efficient non-glass encapsulation against humidity and oxidation, flexible OLED also brings a more rugged structure due to no need for the glass substrate and their bendable nature. Since standard OLED uses a cathode of a metallic material, approximately 75% of the incident light is reflected back and causes a poor contrast when ambient light passes through the display [13]. The use of a TOLED in combination with an absorber or an optical interference structure improves the contrast, e.g. Luxell's black layer results in a 180° phase shift to cancel out the ambient radiation [14].

2.4 Fabrication of OLED devices

The difference between the small molecules and conjugated polymers is mainly

the fabrication and patterning process. All processes need a pure deposition of the organic material on a cleaned substrate. As moisture and UV-light have certain effects on the degradation mechanism of the device during manufacturing [15][16], the processes for either small molecules or conjugated polymers should be elaborated for long device lifetime.

2.4.1 Patterning small molecules

Small molecule layers are deposited through a vacuum evaporation process, as shown in Fig. 2-5. The surfaces roughness of the organic layers deposited by evaporation process sequentially are important for the lifetime of the device. A disadvantage of vacuum evaporation process is the different for large-size substrate.

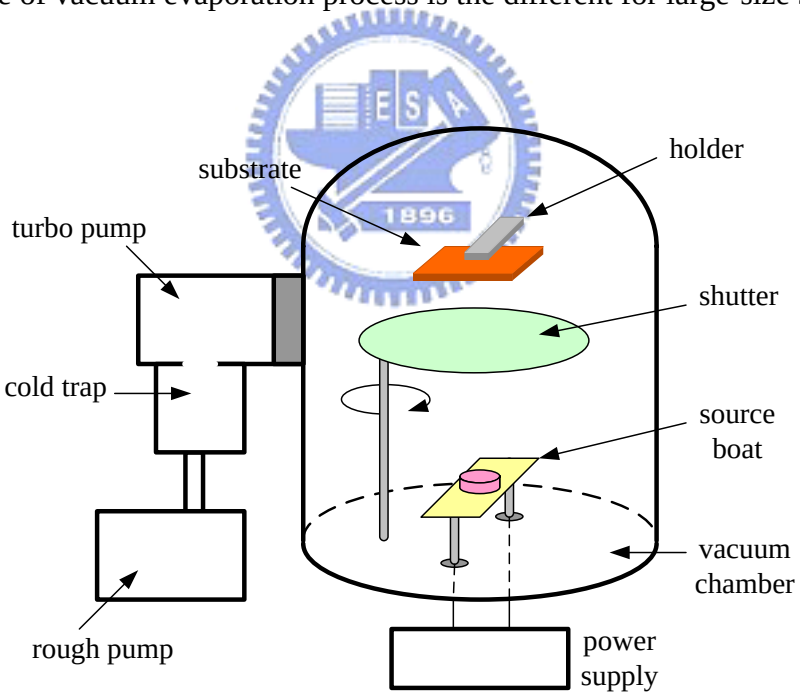
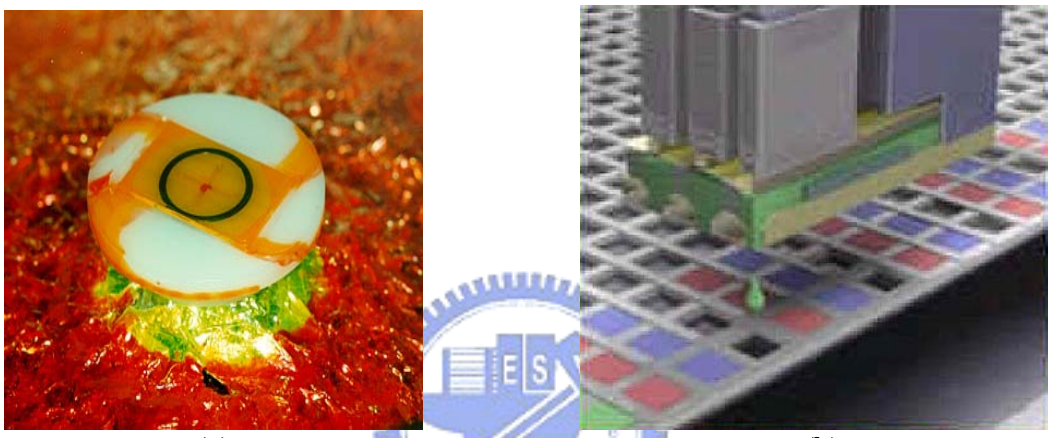


Fig. 2-5. Schematic diagram of vacuum evaporation system for OLED fabrication.

2.4.2 Patterning polymers

Conjugated polymers can be applied to a surface through either dip-coating or spin-coating. Dip-coating is a method where the substrate is slowly dipped into the polymer solution, which results in a cover of polymers at both sides. The spin-coating

method is performed by dripping the polymer solution onto a rotated plate where the polymer solution is spread out to form a uniform thin film, as revealed in Fig. 2-6(a). The thickness of the layers is dependent on the composition of the polymer and the concentration of the polymer solution. However, spin-coating results in non-smooth and non-parallel surfaces, which would cause degradation of devices because of the different distances between the electrodes.



(a) (b)

Fig. 2-6. Fabrication approaches for solvent based PLED. (a) spin-coating process and (b) ink-jet printing process.

An advantage of the spin-coating method compared to the vacuum deposition is the simplicity. However, it is also a less material efficient utilized process, and it should be taken into account in fabricating large size display, the spin-coating method can result in much higher costs. A drawback of spin-coating is the requirement of the removal of water and oxygen before the metal deposition [17]. However, the conventional spin-coating process is difficult to integrate the multiple color materials on the pixels individually with high resolution to realize a full-color display.

Ink jet printing is another promising candidate for the patterning of pixels to achieve the full-color display with polymers. This allows direct pattering of polymer

layers with high resolution and large-size substrate to yield full-color displays without the use of expensive vacuum deposition systems [18][19][20], as shown in Fig. 2-6(b). The ink-jet printing technology requires optimization of the solvents used to dissolve the polymers to formulate the inks. Selection of a suitable solvent is important since it affects the film morphology, which can influence the device performance in terms of device efficiency and stability. In addition, the surface energy of ITO electrode and the material of bank which defines the pixel region are as well the key parameters that control the spreading of polymer solvent and the resulted film uniformity.

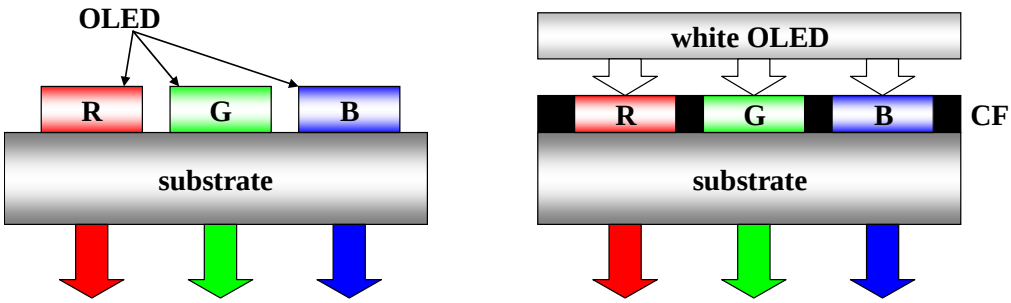
2.5 Full-color approaches in manufacturing

In a similar manner for small molecules and polymers, fabrication technologies to achieve higher color purity have been proceed. The synthesizing and doping of organic materials have modified their chain structure and color characteristics. For emission of several colors, a host material can be doped with dye and new luminescent properties are then accomplished [21]. In order to achieve the full-color displays, several approaches will be introduced in following sections.

2.5.1 Patterning RGB

The patterning RGB is a straightforward approach in much the same way as CRT to achieve colors without an additional color-filter. As shown in Fig. 2-7(a), each pixel is divided into three parts called subpixels. By the combination of various gray levels of three primary colored subpixels, an arbitrary color can be generated. Since each OLED must have a different organic thin film as its light emitting layer, a drawback of this approach is in high-resolution because the arrangement of the subpixels becomes three times tighter to achieve a similar resolution compared to other approaches. In

other words, for an achievement of high-resolution, the patterning process is considered to be a difficulty for a small pixel pitch. A patterning technique called shadow masking was proposed. Besides, to enhance the color gamut, it is proposed to combine the emitting subpixel with an additional color filter.



(a) (b)

Fig. 2-7. Schematic diagrams for achieving full-color displays based on OLEDs. (a) patterning RGB approach with separate subpixels. (b) Filtering white light with color-filter.

2.5.2 White light OLED combined with color-filter (CF)

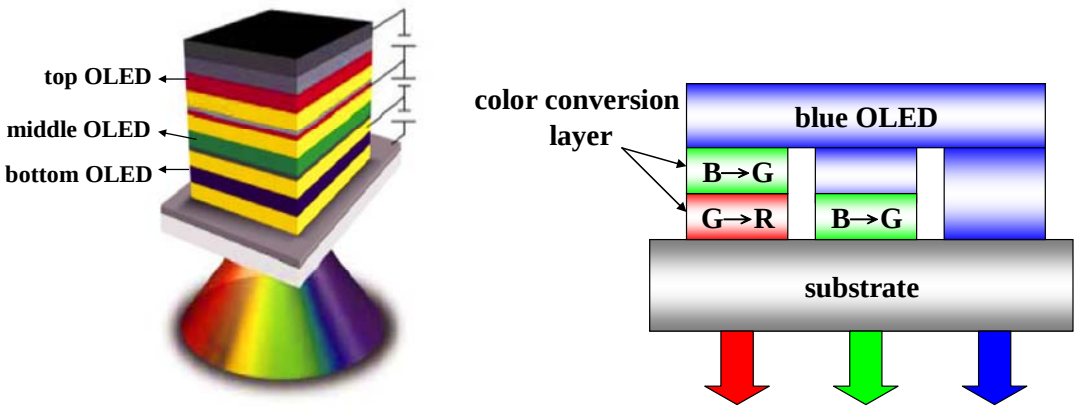
Filtering white light with color-filter is commonly used in AM-LCD to achieve full color. The main advantage with this method is no need to pattern the bottom substrate with different types of OLEDs and therefore only one white light OLED is used over the whole surface. The different colors are then obtained through a band-pass filtering, as depicted in Fig. 2-7(b). The principal drawback of this approach is that much of the white OLED output must be absorbed by the filter to obtain the required primary colors. For example, up to 66% of the optical power from the white OLED is filtered in order to obtain three originals in ideal case, with the result that the OLED must be driven up to three times brighter than the required RGB pixels brightness. Since the rate of OLED degradation is a function of drive current,

this technique substantially results in a high power consumption, which can shorten the lifetime of OLED [22]. Besides, degradation is further enhanced as the filtered light generates heat in the substrate. In practical, the eMagin OLED micro-display light throughput reduction is 88 %, because of the color-filters [23].

2.5.3 Stacked OLED

Another approach to achieve full-color is through the stacked OLED (SOLED) device. Due to the fact that a complicated multi-layer structure is used in SOLED, as shown in Fig. 2-8(a), the approach is suitable for small molecules but not appropriate for OLED based on conjugated polymers [24]. Instead of patterning RGB, three separately addressed devices are placed on top of each other. The bottom and the middle device are OLEDs with both transparent cathode and anode, allowing down emitting light from the top layer. A patterning RGB approach with a large pixel pitch requires a certain viewing distance for an accurate color representation, which is not the fact for SOLED. SOLED is therefore suitable for helmet-mounted and head-up displays for a short eye relief and high-resolution [25].

The ability to tune specific colors is an additional advantage of the SOLED compared to the patterning RGB approach. Another advantage can be observed in the fabrication process, since the pixel pitch is minimized with maximum fill factor, consequently, resulting in a factor of 3 higher in resolution. The entire SOLED can be as thin as 500 nm, but a lack of proper efficiency makes the method unattractive at present [25].



(a) (b)

Fig. 2-8. Schematic diagrams for achieving full-color displays based on OLEDs. (a) OLED of stacked RGB materials and (b) Down conversion of blue OLED.

2.5.4 Down conversion of blue light

Emission of blue light from a layer can be filtered and produce red, green and blue. The method, shown in Fig. 2-8(b), converts blue to green and further green to red or directly converts blue to respective colors in terms of pre-patterned films of fluorescent material which efficiently absorbs blue light and re-emits the energy as either green or red light, depending on the compound used. Luminescent organic systems can have a conversion quantum efficiency approaching 100%, although the power efficiency is reduced since the energy of the emitted photon is of less than that of the absorbed photons. If necessary, color-filter may be adopted to sufficiently narrow the spectrum to achieve saturated color [26] [27].

2.6 Power efficiency in an OLED

The power efficiency is defined as the ratio between the power the display consumes and the amount of light emitted. For OLEDs, the power efficiency is of great concern because improved efficiency can lead to a longer device lifetime. The power efficiency for an OLED device is the same as the external quantum efficiency.

The external efficiency not only includes the internal efficiency but also takes outer factors as light emission from the side of the device and internal refraction into consideration. Internal quantum efficiency is defined as the amount of emitted photons in comparison to the amount of charges injected into the emitting layer. The internal quantum efficiency for OLEDs depends on the electron-hole recombination in the emitting layer, where an increased amount of recommendations leads to a better efficiency. It is therefore important to choose a material with good recombination property.

Even if all electrons and holes form an excited state, the quantum efficiency can not be theoretically higher than approximately 50%, depending on a fact that only the singlet excited states can contribute to the light emission. In conjugated polymers there are approximately 50% singlet and 50% triplet excited states [28]. Instead of emitting light, the triplet state emits heat that contributes to the degradation of the device. For small molecules there is about 25% singlet state so that the small molecule materials therefore inherently possess lower power efficiency compared to conjugated polymers [29][30][31].

According to the limitation of the quantum efficiency, due to the triplet excited state, an approach of improvement can be through doping with phosphorescent materials [28][32]. The contribution of a phosphorescent dye, such like platinum, accomplishes a mixture of the singlet- and triplet excited states, which generates a higher speed of the emission of light, known as phosphorescence [33]. Phosphorescent dopants enable small molecule OLEDs to have internal quantum efficiencies approaching 100%, as compared to an approximated 25% maximum for conventional fluorescent devices [34]. The increase in OLED efficiency directly translates into a reduction of display power consumption.

The conjugated polymers are considered to yield higher quantum efficiency due to the 1:1 singlet-triplet state ratio compared to small molecules with a singlet-triplet ratio of 1:3 [28][29]. It is considered that the conjugated polymers do not have any particular need for doping [35]. However, the internal quantum efficiency of a real device is much lower than the theoretical value but doping of the materials does enhance their performance. The reduction of the internal efficiency is mainly due to the absorption of the emitted light due to "Stokes shift" [36]. Table 2-1 shows a comparison of luminous efficiencies for red, green and blue materials with their respective CIE coordinates, for the three main types of organic light emitting devices: phosphorescent device system [37], fluorescent small molecule materials [38] and spin coated polymer light emitting materials [39].

Table 2-1. Comparison of luminance efficiencies and CIE coordinates of phosphorescent OLEDs, fluorescent OLEDs, and polymer OLEDs (PLED) [37][38][39].

	Red cd/A, CIE	Green cd/A, CIE	Blue cd/A, CIE
phosphorescent OLED	**11**, (0.65, 0.35)	**24**, (0.30, 0.63)	**11**, (0.16, 0.32)
fluorescent OLED	**3**, (0.63, 0.37)	**7**, (0.31, 0.63)	**3**, (0.15, 0.17)
PLED	**2**, (0.60, 0.31)	**13**, (0.39, 0.59)	**3**, (0.15, 0.17)

2.7 The degradation process for OLEDs

The mechanisms affecting the degradation process are strongly linked to the physical properties of the materials used and result in different degradation properties between inorganic and organic LEDs [21]. The degradation mechanisms for OLEDs are not fully clarified in comparison to inorganic LEDs where the processes are more widely understood and the lifetime is much longer. Although the development of the OLED technology has resulted in a better lifetime, it is still much lower than that of

the inorganic LEDs. The difference is that the nature of the organic materials makes them more sensitive to environmental changes and degradation.

For OLEDs with lower power efficiency, a higher current density is needed in order to generate light. Only a few percentage of the power applied to the display results in an emission of photons, the rest is converted to heat. Heat generated in the device causes degradation of the display. The increase of heat has been found to be proportional to the driving current of the display, consequently the development of more power efficient displays should result in a reduction of the heat developed, thus, a longer lifetime.

The degradation process depends on which color the material emits. To emit a blue color, a material with a larger band gap is needed, which makes it harder to inject charged carriers into display and consequently more energy is required. The high amount of current density makes the display more fragile and therefore results in a faster degradation for blue than for red and green emitting materials. The problem of high luminance value and lifetime is more evident when constructing color displays than monochrome displays. The large reduction of the light for color displays is a result of the color-filter used and reduces up to 90% of the display light intensity [23].

At the interfaces of the different materials, diffusion of the materials can lead to a decline in effectiveness and lifetime. To prevent the diffusion, an intermediate protective layer can be used to separate two layers without affecting the charge transport between them. Another way is to choose a material with more stable properties in order to suppress the material diffusion. Some materials used for intermediate layers can even enhance the carrier transport by smoothing the barrier. The most widely used layer materials for intermediate layer purpose is polymers, carbon or a thin layer of oxide [21].

An important factor that affects the lifetime is the encapsulation of the display. An OLED exposed to air degrades in hours due to the oxidation. Encapsulation with an inert gas has to be used in order to protect the display from oxygen and humidity diffusing into the layers. The drawback of efficient encapsulation is the increased weight and the reduced flexibility of the display.

There are several indications for the degradation of a display [21]. As mentioned above, the emitted light from the display reduces over time and instead the applied current density on the device must increase to maintain the original emission intensity. The decrease of brightness can occur in two different ways, either directly as the voltage is applied resulting in a short-term decrease or as slow decrease in brightness during the whole operating period of the display.

The degradation can also be noticed as the dark spots on the surface of the display. The phenomena of black spot can appear in both displays based on small molecules or conjugated polymers [40][41][42]. The black spots are areas on the displays, which not emit any light and contributes to an overall decrease in light emission from the display. The spots are commonly situated at the interfaces between the different materials often between the metallic electrode and the organic layer. The position of the spots also reduces the interface effectiveness leading to the need of a larger input current. The occurrence of the spots is still not fully understood but some suggestions of their origin have been made. It is generally believed that some types of spots occur as a result of an electrical short, often with its origin at one of the two electrodes. The shorts appear as a result of defects and impurities in the different materials. These spots have a circular shape and can reach a size of 300 μm in diameter. Observations have been made in polymer based diodes where small black dots first appear on the periphery of a white dot in the centre. The black dots continue to grow until the whole

region within the periphery is covered with black spots, only leaving the initial white dot in the center.

In other cases, the spots appear a bubble-like structure as well. These spots appear suddenly and do not grow as in the case with the spots mentioned above. It was reported that these spots are a result of gases, mostly water, trapped in the spot [43]. The crystallization of some materials like the Alq3 is also assumed to be the source of black spots. Crystallization is overall believed to be a parameter that decreases lifetime due to changes in morphology and in some cases causing unwanted diffusion of the interfaces in the layered structure. The crystallization is believed to be a result of moderate heating during long operation periods or as a result of humidity in the device.

2.8 Factors that reduce and prevent the degradation in OLEDs

It is possible to reduce the degradation process as the organic materials with higher power efficiency have been developed. Various types of doping of the organic materials can result in higher power efficiency and longer lifetime [44]. As mentioned before, the triplet excited states are able to emit light instead of heat through phosphorescent doping, [37] which can not only yield a higher power efficiency but also reduce the time spent in the excited state. In the excited state, the molecules can be considered more reactive and can cause a degradation of the emitting layer due to unwanted chemical reactions. The reduction of triplet excited states would also lead to less heat generated and consequently to a better lifetime of the device.

Multi-layer structure can also bring a longer lifetime [24]. Depending on layers order designed, the lifetime can be possibly extended. The emitting layer plays a great role by affecting the lifetime as a result of its position. The addition of a hole

transporting layer enhances the lifetime by function as a stabilizer for the flow of holes and also in an overall better power efficiency due to more recombinations. Both transporting layers not only function as transport medium but also in some case function as buffer layers preventing humidity and oxygen to diffuse into the active emitting layer.

Due to the fact that OLEDs degrade under high temperatures, cooling is another effective method in order to achieve a longer lifetime. How the displays are fabricated is a factor in the desire of enhancing the lifetime, the process can be undertaken in vacuum or under great pressure or in some cases at low pressure, depending on materials used. During manufacturing the conjugated polymers and the small molecules are very sensitive to UV-light in combination with humidity. The fabrication has to be precise because the structure asymmetry and varying thickness of the layers are sources for local heating which can lead to damages on the display.

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Chapter 3

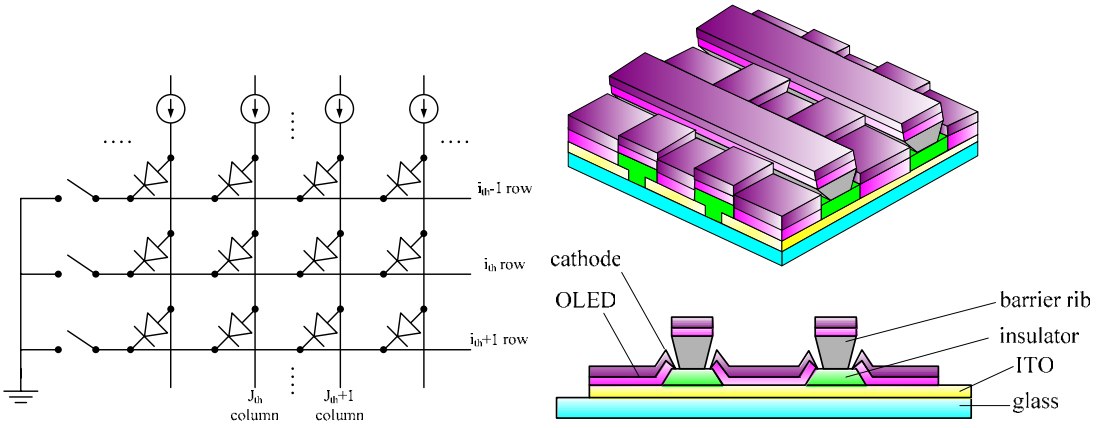
Addressing scheme for OLED displays

A display is an array of controllable pixels and the number of which depends on the dimension and resolution required by a particular application. For example, specifications of desktop monitor may emphasize higher visual performance, such as higher spatial resolutions and higher pixel content. The addressing of a large number of pixels in an array is an important issue in the display technology. Among the five addressing schemes used in electronic display [1], matrix addressing is the most suitable for OLED-based display system. In a matrix addressed display, pixels are arranged in rows and columns, and each pixel is electrically connected between one row electrode and one column electrode. The matrix addressing where active switch devices are added to the pixels are called active-matrix (AM) addressing. While the array without any active component in the pixels is termed as passive-matrix (PM) addressing.

3.1 Passive-matrix addressing

A passive-matrix array consists of two sets of electrically isolated conducting electrodes arranged orthogonally with an OLED to form the pixel at each intersection, and connected to the external drivers that supply the necessary voltage and timing sequence. Fig. 3-1(a) and (b) show the electrical schematic and functional cross-sectional diagram of a PM-OLED, respectively. Normally, the display is scanned or multiplexed row by row from the top to the bottom at a rate that is sufficient to produce flicker-free images (> 60Hz). To turn on a pixel, a certain

voltage needs to be decreased across the OLED material. The row electrode delivers a fraction of this voltage, and the column electrode provides the remainding.



(a) (b)

Fig. 3-1. (a) Schematic diagram of passive-matrix OLED panel. (b) Cross-section view of passive-matrix OLED structure.

A pixel receiving only part of the full voltage will be off. This row-at-a-time mode is chosen to maximize the pixel duty factor (defined as the percent of the total time each pixel is driven into the ON state by the column signal). The pixel duty factor of such a row-scanned array is $1/N_s$, where N_s is the number of scan electrodes. Since the selected pixel must be driven with a pulsed voltage signal at a duty cycle, instantaneous luminance L_0 should be high enough to achieve an average display luminance L_d:

$$L_0 = N_s \cdot L_d \qquad \text{Eq. 3-1}$$

Even the EL response time of small-molecule OLED has been found to be < 1 μs [2], sufficient for most pulse-driven passive matrix, the number of rows in an array may limit the average display luminance [3][4]. However, this PM addressing approach limits the contrast and restricts the format of the display to smaller pixel counts [5]. For example, an instantaneous luminance should be about 10000 cd/m^2 to achieve an

average luminance of 100 cd/m^2 for a passive-matrix display with 100 rows, In addition, this approach requires patterning of both the row and column electrodes, which is difficult if the most common electron injecting materials (Al-Li, MgAg) is used as the column electrode. Besides, the high driving voltage and the instantaneous driving current corresponding to the high instantaneous-luminance requirement can also lower the OLED power conversion efficiency and OLED lifetime.

3.2 Voltage-type active-matrix addressing

Active-matrix addressing overcomes the crosstalk limitation of passive-matrix by integrating switching devices at the cross point of the row (scan or gate) and column (data) lines, and thereby isolating the off pixels from these select voltage lines. The TFT active-matrix array designs are commonly optimized using computer simulations to analyze electrical performance based on statistically extracted TFT and fabrication process parameters. While this approach is the most accurate way to predict the statistical mean and variance in display performance, it is more instructive to carry out a simple, physically based parameter analysis to identify functional dependencies, performance limits, and minimum requirements. The analysis presented here is applicable to any kind of TFT processing technology.

Using an active-matrix addressing can solve the image contrast and column electrode pattering concern of passive-matrix addressing. In the AM addressing, a transistor is placed at each pixel to separate the effect of the data line (column electrode) voltage and the scan line (row electrode) voltage on the voltage across the OLED material. A common cathode material (MgAg, Al-Li) is used to eliminate the need of patterning the electron injecting electrode. Within AM-OLED designs, a variety of pixel architectures have been proposed [6]. Different pixel architectures may

contain different numbers of transistors per pixel. The simplest design uses one transistor per pixel which is similar to the pixel circuit for AM-LCD, as shown in Fig. 3-2. A single transistor design approach has the advantage of increased contrast by isolating the data line and scan line from OLED compared to a passive matrix design, and will have a higher yield than other designs containing more than 1 TFT per pixel. However, in this approach the voltage signal in storage capacitor C_{ST} is leaking out through OLED even the TFT T_{SW} is OFF, so that the luminance cannot be kept constant during entire frame time. Therefore, each pixel is needed to pulse ON for a duty factor $1/N_s$ of the frame time. This requires the instantaneous OLED current to be much higher than the average current, which still leads to faster degradation of the OLED material.

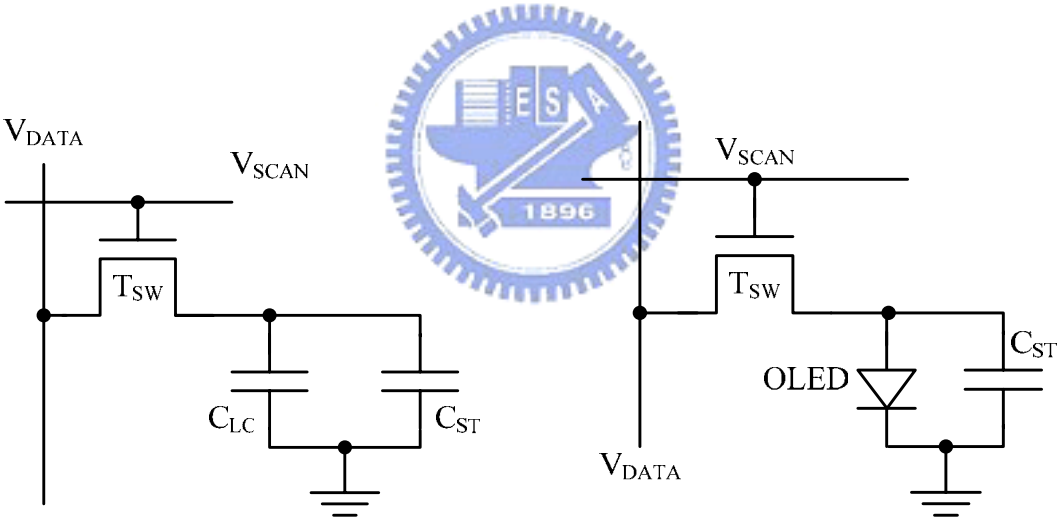


Fig. 3-2. (a) Conventional single-transistor-single-capacitor (1T-1C) pixel circuit for AM-LCD. (b) 1T-1C pixel circuit for AM-OLED using OLED instead of LC.

The pixel circuit for AM-OLED must have a function to generate the stable driving current for the OLED throughout one frame period to avoid the high current pulse native to the single TFT design. A pixel design involving two transistors using n-channel TFTs is shown in Fig. 3-3(a). When a scan line is selected, the voltage

signal V_{DATA} from data line is written via the switching transistor T_{SW} to the gate of the driving transistor T_{DV}. The written voltage V_{DATA} is thereby retained in C_{ST} for a complete frame period. Driving transistor T_{DV} operates in the saturation regime where the OLED driving current has little dependence on the source-to-drain voltage. This pixel circuit allows the pixel to deliver a small current during the entire frame period.

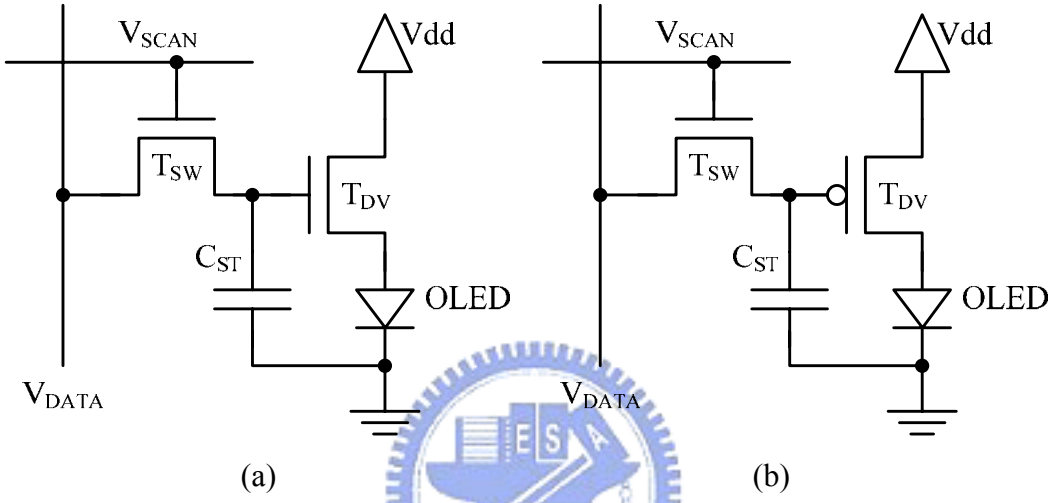


Fig. 3-3. Double-transistor-single-capacitor configuration of AM-OLED pixel circuit with (a) n-channel driving TFT (T_{DV}) and (b) p-channel T_{DV}.

Though the average current through the OLED material is the same, the peak current is greatly reduced which leads to increased brightness and OLED material lifetime. The OLED driving current I_{OLED} generated by n-channel T_{DV} is

$$I_{OLED} = \frac{1}{2}\mu_{FE} \cdot C_{OX} \cdot \frac{W_{DV}}{L_{DV}} \cdot \left(V_{DATA} - V_{OLED} - |V_{th}|\right)^2 \qquad \text{Eq. 3-2}$$

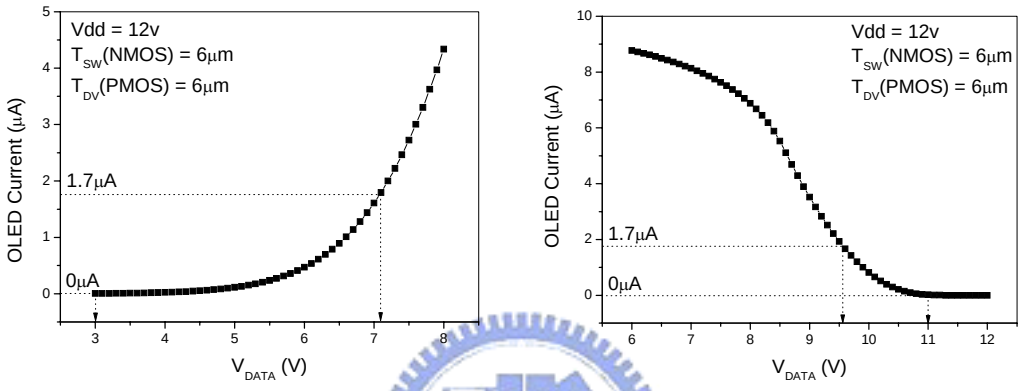
where μ_{FE}, C_{OX}, W_{DV}, L_{DV}, V_{OLED} and V_{th} are the field-effect mobility, gate oxide capacitance per unit area, channel width, channel length, OLED cross voltage and TFT threshold voltage, respectively. With n-channel T_{DV} configuration, designing data voltage V_{DATA} should take consideration of the OLED voltage. In other word, the V_{DATA} includes not only the over-drive voltage of T_{DV} but also the OLED cross

voltage so that the voltage swing is large. The pixel circuit can also be implemented with p-channel TFT as shown in Fig. 3-3(b). Since the most commonly used technologies for conventional AM-LCD are a-Si and poly-Si TFTs, both of them are compatible with large area glass substrate processes, which is necessary to fabricate displays at reasonable cost. Poly-Si TFT technology was chosen for AM-OLED display because of its higher mobility and greater stability compared with a-Si TFT. In addition, poly-Si TFT technology has ability to provide p-channel devices for not only pixel circuits but also integrated drivers. The performance of p-channel TFT is typically lower than that of n-channel TFT made from the same material. However, as p-channel TFT is used as driving transistor T_{DV} in pixel design, the gate-to-source voltage of T_{DV} is related to the gate node and Vdd electrode and the driving current can be expressed as:

$$I_{OLED} = \frac{1}{2}\mu_{FE} \cdot C_{OX} \cdot \frac{W_{DV}}{L_{DV}} \cdot \left(V_{dd} - V_{DATA} - |V_{th}|\right)^2 \qquad \text{Eq. 3-3}$$

According to this configuration, the OLED turn-on voltage is of little significance to the driving current, therefore the voltage swing can be reduced. The OLED driving current as a function of data voltage in n-channel and p-channel T_{DV} configurations are shown in Fig. 3-4. As discussed above, the swing of V_{DATA} for n-channel T_{DV} is 4V in order to achieve the maximum driving current or 1.7 μA, almost a factor of three larger than that of p-channel T_{DV}. Although the n-channel TFT has higher mobility than p-channel TFT, the large data voltage swing increases the high transient power consumption as well as the long charge-up time for the pixel circuit. Besides, the degradation of OLED material may affect the OLED threshold voltage and then change the gate-to-source voltage of T_{DV}, consequently, resulting in the luminance variation. Due to the native property of p-channel TFT, the stable luminance can be achieved by the voltage-to-current conversion of T_{DV} regardless of

OLED degradation. The small data voltage swing can speed up the programming time and reduce the power consumption. Nevertheless, it should be noted that the resistance against to the noise must be high enough when design the gray levels of AM-OLED because the small voltage swing leads to the small voltage step between each gray level.



(a) (b)

Fig. 3-4. OLED driving current as a function of input data voltage at different types of T_{DV}: (a) n-channel T_{DV}, (b) p-channel T_{DV}.

3.3 Definition of operation point

Since the pixel circuit with p-channel TFT in Fig. 3-4(b) can be similarly analyzed as the n-channel TFT in Fig. 3-4(a), the following discussion only focuses on the pixel electrode circuit with n-channel TFT. The I_D–V_{DS} characteristics of an n-channel TFT are shown schematically in Fig. 3-5, along with the load line resulting from the OLED I–V characteristics. The knees in the I_D–V_{DS} curves between the linear and saturation regimes are at $V_{DS}=V_{GS}-V_{th}$, and the saturation current is $I_D = \frac{1}{2}\mu_{FE} \cdot C_{OX} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2$, where W and L are the channel width and length of the TFT respectively [7]. The criterion for the operation in the saturation regime is

$V_{GS} - V_{th} \le Vdd - V_{OLED}$, i.e.

$$Vdd \ge V_{OLED} + \sqrt{\frac{2I_{OLED}}{\mu_{FE} \cdot C_{OX} \left(W_{DV} / L_{DV}\right)}} \qquad \text{Eq. 3-4}$$

where I_{OLED} is the OLED drive current required to achieve full brightness, and V_{OLED} is the corresponding OLED voltage. A low Vdd is desirable to achieve low-panel power consumption and to make the technology suitable for portable, battery-powered applications. The power penalty due to the introduction of T_{DV} is $\Delta P = V_{OLED} / Vdd$. For a pixel driven to full brightness, $\Delta P = 1 + \sqrt{\left(2I_{OLED} / \mu_{FE} \cdot C_{OX} \cdot \left(W_{DV} / L_{DV}\right)\right)} / Vdd$. The channel width of T_{DV}, i.e. W_{DV}, is limited by the pixel dimension, channel length L_{DV} is limited by short channel effects; C_{OX} is determined by the oxide layer thickness and material properties, and depends on the channel material.

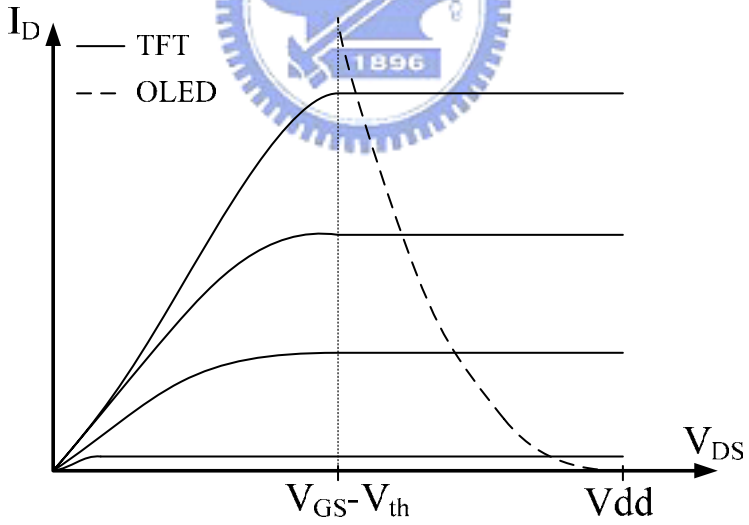


Fig. 3-5. Operation point calculation according to the loading line of TFT and OLED.

The average current necessary to produce a bright display (100cd/m^2) is approximately 10mA/cm^2 [8]. If we assume a pixel size of 150μm x 150μm, an OLED driving current of 2.25μA is necessary. Assuming a TFT operating in saturation region,

the required field-effect mobility can be calculated according to

$$\mu_{FE} = \frac{2I_{OLED}}{(W_{DV}/L_{DV})C_{OX}(V_{GS}-V_{th})^2} \qquad \text{Eq. 3-5}$$

To achieve the proper current levels using small device geometry i.e. $W_{DV}/L_{DV}=2$, and a thin gate oxide layer, a high mobility is required. Since amorphous silicon cannot be used because of mobility less than 1 cm^2/V-s and therefore cannot deliver enough current, polysilicon based transistors becomes the better choice for AM-OLED's. It is important to note that the quantum efficiency of OLED material is substantially improved in recent days. As a result, the mobility requirement is much less and, strictly from a drive current perspective, a-Si TFTs may be adequate.

3.4 Pixel voltage error due to parasitic capacitance of TFT

The switching TFT T_{SW} in the pixel operates as an analog switch, whereby, when the gate of the TFT in turn-on, it is desired that the TFT can accurately transfer a precise data voltage to the C_{ST} and the gate of T_{DV}. The available precision of charging up the total pixel capacitance to the data voltage depends on many factors, most of which are physical dimensions related to the fabrication and layout design process. The TFT parasitic capacitances C_{GD} and C_{GS} are determined by the overlay area between the drain and gate electrodes, and the source and gate electrodes, respectively. The smaller the channel length, the larger the parasitic capacitance can be formed from overlap area. Therefore, the TFT parasitic capacitance is minimized by making the area of the drain, source, and gate electrodes as small as possible or by increasing the thickness of oxide insulation layer.

The design of T_{SW} is similar to that of the switching transistor in AM-LCD [9][10]. Assume that the gate voltage of T_{SW} is $V_{G\text{-}SW}=V_H$ when a scan line is addressed, and

the voltage on the data line is V_{DATA}. At the end of the charging period, the pixel capacitance, C_{PIX} (the sum of the storage capacitance C_{ST}, the C_{GD}, and the C_{GS} of T_{DV}), stores charge $C_{PIX} \cdot V_{DATA}$, while the C_{GS} of T_{SW} stores charge $C_{GS\text{-}SW}(V_{DATA}-V_{th})$. When V_G is brought to zero, the C_{PIX} and $C_{GS\text{-}SW}$ form a voltage divider of transfer ratio $C_{GS-SW}/(C_{GS-SW}+C_{PIX})$. During the holding period, the voltage at the gate of T_{DV} (also the storage node) can be expressed as

$$V_{G-DV} = V_{DATA}\left[1-\frac{C_{GS-SW}\cdot(V_H/V_{DATA})}{(C_{GS-SW}+C_{PIX})}\right] \qquad \text{Eq. 3-6}$$

and

$$\Delta V_{G-DV} = -\frac{C_{GS-SW}\cdot V_H}{(C_{GS-SW}+C_{PIX})} \qquad \text{Eq. 3-7}$$

To have $V_{G\text{-}DV} \approx V_{DATA}$ during this period, it is important that $C_{PIX} >> C_{GS\text{-}SW}$, therefore necessitating a separate storage capacitance. Even with a large C_{ST}, $V_{G\text{-}DV}$ is still small than V_{DATA} due to the C_{GS} during the holding period. To eliminate this difference, the C_{ST} can be connected to the previous scan line instead of ground to form the "C_{ST} on gate" configuration. A compensation voltage $V_{COMP} = -(C_{GS-SW}/C_{ST})\cdot V_H$ introduced from previous scan line coupling through the C_{ST} can substantially offset the voltage error as shown in Eq. 3-7. It should be noted that the C_{ST} is included in the design of the pixel for two reasons, one of which is to reduce the magnitude of the error $\Delta V_{G\text{-}DV}$, and to reduce the percentage of pixel charge loss when leakage current presents during the TFT OFF state.

3.5 ON/OFF ratio and leakage current

The required on–off ratio of T_{SW} is estimated as follows: to charge the C_{ST} to a voltage $V_{G\text{-}DV}$ within the scanning time, the on current I_{ON}, must satisfy

$$I_{ON} \geq \frac{C_{PIX} \cdot V_{G-DV}}{T_f / N_s} \qquad \text{Eq. 3-8}$$

where T_f is the frame time. To maintain the $V_{G\text{-}DV}$ for entire frame time, the leakage current in OFF state, I_{OFF}, must satisfy:

$$I_{OFF} \leq \frac{C_{PIX} \cdot \Delta V_{G-DV}}{T_f (N_s - 1)/N_s} \qquad \text{Eq. 3-9}$$

where $\Delta V_{G\text{-}DV}$ is the change in $V_{G\text{-}DV}$ when the pixel brightness is changed by one gray-level increment. After the pixel is turn-off, the data voltage may unintentionally decrease due to leakage current. Several sources for leakage current may exist, such as TFT drain-to-source leakage, TFT channel photon current, and low-resistance storage capacitance insulator film. Since the leakage current of storage capacitance insulator, typically made of SiO_x and SiN_x, are less than 1nA/cm^2, the black matrix can be used to shield the incident light to reduce the photon current. Hence the source-to-drain leakage of TFT can be considered as the only source of leakage current. As seen in Eq. 3-9 $I_{OFF} \leq \frac{C_{PIX} \cdot \Delta V_{G-DV}}{T_f (N_s - 1)/N_s}$ Eq. 3-9, the maximum allowed leakage current is proportional to the pixel capacitance C_{PIX}. In addition, differences in TFT fabrication technologies, device structure, and physical layout dimensions, such as channel width and length, can also influence the TFT leakage current. From Eq. 3-8 to Eq. 3-9, the number of gray levels is derived:

$$\frac{I_{ON}}{I_{OFF}} \geq \frac{(N_S - 1)V_{G-DV}}{\Delta V_{G-DV}} = (N_S - 1) \cdot G_L \qquad \text{Eq. 3-10}$$

where G_L is the number of gray levels. If N_S=480 and G_L=256, then $I_{ON}/I_{OFF} \cong 10^5$. At room temperature, $I_{ON}/I_{OFF} \approx 10^7$ for a-Si TFT, and $I_{ON}/I_{OFF} \approx 10^6$ for poly-Si TFT, as listed in Table 3- 1. Therefore, both types of TFT can satisfy the ON–OFF ratio requirement.

Table 3- 1. Field effect mobility and ON-OFF ratio of TFTs for different technologies.

Channel material	Field effect mobility (cm^2/V-sec)	ON-OFF ratio
a-Si	0.1-1.0	10^7
n-channel poly-Si	100-500	10^6
p-channel poly-Si	10-50	10^6
pentacene	1.5	10^8

3.6 Mobility for T_{SW}

The field-effect mobility μ_{FE} of the T_{SW} required by AM-OLED displays is estimated as follows. Since T_{SW} operates in the linear regime, the drain current variation related to the drain-to-source voltage is expressed as

$$\frac{\partial I_{D-SW}}{\partial V_{DS-SW}} = \mu_{FE} \cdot \frac{W_{SW}}{L_{SW}} \cdot C_{OX} \cdot (V_{GS-SW} - V_{th}) \quad \text{Eq. 3-11}$$

In order to charge C_{ST} within the scanning time, we require that

$$C_{PIX} \cdot \left(\frac{\partial V_{D-SW}}{\partial I_{DS-SW}} \right) \leq \frac{T_f}{N_S} \quad \text{Eq. 3-12}$$

From Eq. 3-11 and Eq. 3-12, we obtain

$$\mu_{FE} \geq \frac{C_{PIX} \cdot N_S}{T_f \cdot (W_{SW}/L_{SW}) \cdot C_{OX} \cdot (V_{GS-SW} - V_{th})} \quad \text{Eq. 3-13}$$

if C_{PIX}=700 fF, T_f=16 ms, C_{OX}=3.4x10^{-8} F/cm^2, W_{SW}/L_{SW}=2, N_S=480, and V_{GS-SW}-V_{th}= 5 V, then μ_{FE}=0.06 cm^2/V-s is required. This requirement is readily achieved by conventional a-Si TFT, and all poly-Si TFT. Consequently, the mobility is not a critical issue for T_{SW} in AM-OLED pixel design.

3.7 Summary

Basic design considerations of PM-OLED and AM-OLED were introduced.

Especially for AM-OLED, we systematically and quantitatively analyzed the design of AM-OLED based on the characteristics of TFTs. The device parameters including leakage current, threshold voltage, mobility and parasitic capacitance were taken into account to estimate the basic requirements for AM-OLED's.

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Chapter 4

AC Driving Scheme for Voltage Driven AMOLED

4.1 Introduction

Since device aging and fabrication processes cause variations in the characteristics of OLEDs and TFTs, the current driving scheme is capable of compensating the variations and produce the desired brightness uniformity [1][2]. In recent years, owing to the progress of processing technology and development of OLED material, the characteristic variations can be eliminated. In this case, the voltage driving scheme becomes more attractive because of its simple structure, high aperture ratio, and compatibility with AM-LCD drivers. However, the intrinsic display loading effects induced by voltage drops across the parasitic resistance of the AM addressing wires still result in brightness non-uniformity in voltage driven AM-OLED displays. Increasing the width of the addressing wires can reduce the parasitic resistance, however, the aperture ratio will also be decreased. It is expected that the voltage drop caused by the parasitic resistance will become the critical drawback in display applications of large size and high resolution.

In this chapter, we propose a simple AC voltage driving scheme with a conventional 2 transistor (2-T) pixel circuit for AM-OLED displays. By means of the charge feed-through mechanism, the proposed AC driving scheme can counteract the voltage drop caused by the parasitic resistance. The experimental results show that the AC driving scheme can effectively improve the brightness uniformity.

4.2 AC driving scheme & panel architecture

The conventional DC voltage driving scheme drives the pixel electrode circuit with invariable voltages at both the power source and the ground electrode. The OLED driven by 2-T pixel circuit is always in forward bias condition, as schematically shown in Fig. 4-1. In this pixel circuit, the OLED is connected to ground and the data voltage stored in a storage capacitor (C_{ST}) keeps the OLED illuminating continuously. The gate-to-source voltage (V_{GS}), equivalent to $|V_{DATA} - V_{DD}|$, can generate the current signal to the OLED based on the transconductance of the driving TFT (T_{DV}). However, the driving current passing through the V_{DD} electrode produces a voltage drop on account of the parasitic resistance (R) of the addressing wire. Even if an identical data voltage is programmed into storage node and stored by C_{ST}, V_{GS} at each T_{DV} is different from pixel to pixel along the V_{DD} electrode, consequently, generating different driving currents. This intrinsic resistance of the addressing wire results in a brightness gradient from both sides to the central part of the panel.

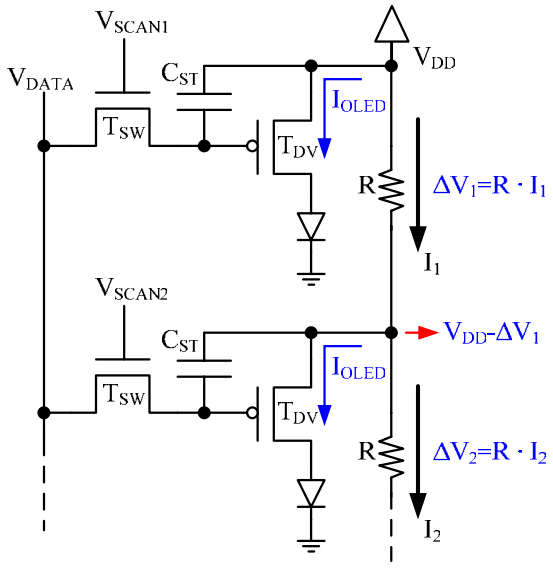


Fig. 4-1. A schematic diagram demonstrates the voltage drop caused by the intrinsic parasitic resistance (R) at V_{DD} electrode.

In the proposed AC voltage driving scheme, the OLED cathode is connected to an AC power supply instead of the ground, as shown in Fig. 4-2. The alternating voltage signal of the AC power supply divides the pixel operation into programming and flashing periods.

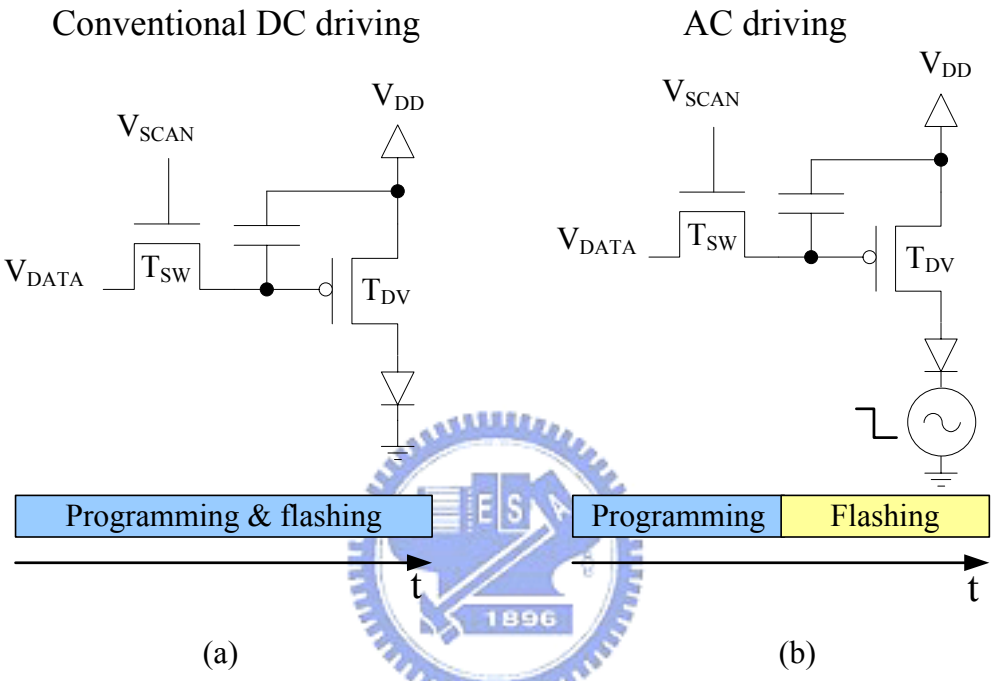


Fig. 4-2. The pixel circuits for (a) conventional DC and (b) AC voltage driving schemes.

First, in the programming period the voltage at the OLED cathode is switched to V_{DD} to turn the OLED off. At this moment, neither a driving current nor a voltage drop is generated in the AM-OLED display panel. Therefore, the initial V_{GS} which is identical to the difference between V_{DD} and V_{DATA} will be stored in C_{ST} in each pixel. In the following flashing period, the cathode voltage is switched to ground after programming all of the pixel circuits and the OLED begins to flash. Owing to the parasitic capacitance formed by OLED anode and cathode and that is connected serially with gate overlap capacitance of T_{DV} ($C_{GS\text{-}DV}$), the change of OLED cathode

voltage will alter the data voltage stored in the C_{ST} and reduce the accuracy. Therefore the changed V_{DATA} can be expressed as:

$$V'_{DATA} = V_{DATA} - \frac{V_{DD} \cdot C_{OLED} \cdot C_{GS-DV}}{C_{OLED} \cdot C_{GS-DV} + C_{ST} \cdot C_{GS-DV} + C_{OLED} \cdot C_{ST}} \qquad \text{Eq. 4-1}$$

Fortunately, the deviation of V_{DATA} (second term in Eq. 4-1) is constant and can be taken into consideration in advance when designing the display panel. By adding an additional voltage to the original V_{DATA} before writing into C_{ST}, the reverse bias induced data voltage deviation can be effectively compensated.

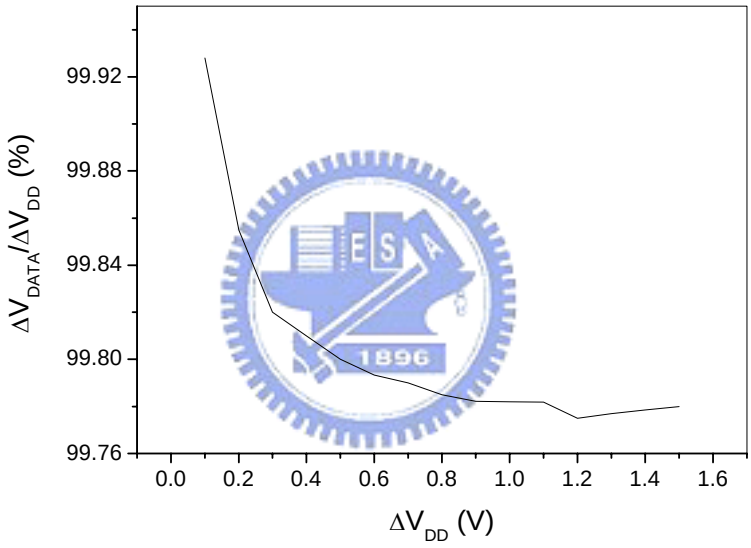


Fig. 4-3. ΔV_{DATA} to ΔV_{DD} ratio as a function of ΔV_{DD}.

Even though the driving current still produces the voltage drop ΔV_{DD} along the V_{DD} electrode, V_{DATA} at the storage node is also decreased by the feed-through effect of C_{ST} and the C_{GD} of T_{SW} and T_{DV}. The data voltage drop ΔV_{DATA} at the storage node can be expressed as:

$$\Delta V_{DATA} = \frac{\Delta V_{DD} \cdot (C_{ST} + C_{GD-DV})}{(C_{ST} + C_{GD-DV} + C_{GD-SW})} \qquad \text{Eq. 4-2}$$

If C_{ST} is much larger than the parasitic capacitance of T_{SW} and T_{DV}, e.g. 600 fF (C_{ST})

>> 3 fF (C_{GS} or C_{GD}), ΔV_{DATA} is almost equal to $\Delta V_{DD,}$ implying that the V_{GS} of T_{DV} is always kept at the initial value. Hence, the voltage drop does not affect the brightness of the panel. According to our design (W_{SW}/L_{SW}=6/5, W_{DV}/L_{DV}=6/15, C_{ST}=500 fF), the ratio of ΔV_{DATA} to ΔV_{DD} is from 99.92% to 99.78% as ΔV_{DD} varies from 0.1 to 1.5V, as shown in Fig. 4-3. ΔV_{DATA} to ΔV_{DD} ratio as a function of $\Delta V_{DD.}$.

4.3 Experiment & Discussion

In order to demonstrate an AM-OLED display with the proposed AC driving scheme, we have fabricated a 2.2 inch panel with a resolution of 176 x RGB x 220, by a top-gate poly-Si process. A buffer and an a-Si layer were deposited by PECVD. Next a XeCl excimer laser was used to crystallize the a-Si layer. After definition of the active island and deposition of the gate insulator, the gate metal was sputtered and patterned. The n-channel TFT S/D and LDD and the p-channel TFT S/D were then doped. Finally, the TFTs were formed after dopant activation, interlayer dielectric deposition, hydrogenation, contact via formation and metallization. Once the TFT process is completed, a hole injection material PEDOT:PSS and a green light-emitting copolymer were spin-coated sequentially onto the ITO anode. Finally, a Ca/Al bi-layer cathode was thermally evaporated through a shadow mask to form the common cathode.

The pixel size is 66 x 198 μm^2 with an aperture ratio of 25.3%. A 2 mm wide power rail surrounds the active area, and each column of the VDD electrode is connected to this power rail, as shown in Fig. 4-4. The active area was divided into 5 x 5 regions and the brightness of each region was measured using a GmbH Conoscope. The diameter of the measuring spot size, which covers about 80 pixels, was 2 mm. The brightness of the top left region (A5) was set to 730 cd/m^2 as a reference in the

measurement.

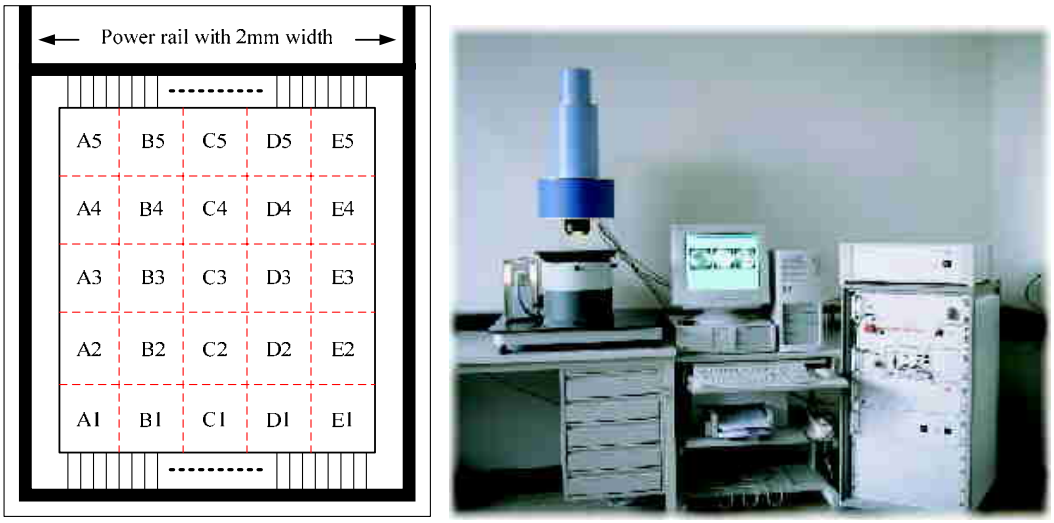


Fig. 4-4. The active area of AM-OLED display panel is divided into 5 x 5 regions for brightness measurement and the photograph of Conoscope.

The conventional DC driving scheme, where the parasitic resistance of addressing electrode can induce a voltage drop, shows inferior brightness uniformity to the AC driving scheme. The driving current I_{OLED} of each pixel was calculated by dividing the current measured at the cathode by the number of pixels. Although I_{OLED} is only 1.6 μA for the DC driving scheme, the voltage drop still causes a significant brightness decrease from the surrounding to the central regions. The lowest brightness was at region (C2), which was found to be only 74.54% of that at the reference region A5, as depicted in Fig. 4-5(a). Since the voltage drop ΔV_{DD} at V_{DD} electrode cannot be measured directly in display operation, ΔV_{DD} can be evaluated approximately by the measured data and the I-V equation of TFT as shown below.

$$74.5\% \cdot \beta \cdot \left(\left|V_{DATA} - V_{DD}\right| - \left|V_{TH}\right|\right)^2 = \beta \cdot \left(\left|V_{DATA} - V_{DD}'\right| - \left|V_{TH}\right|\right)^2 \qquad \text{Eq. 4-3}$$

where $\beta = \frac{W_{DV}}{2L_{DV}} \cdot \mu_{FE} \cdot C_{OX}$

The parameters for DC driving scheme are V_{DATA}=8.9V, V_{DD}=12V and V_{TH}=-1V so that the maximum ΔV_{DD} of 0.287V can be calculated.

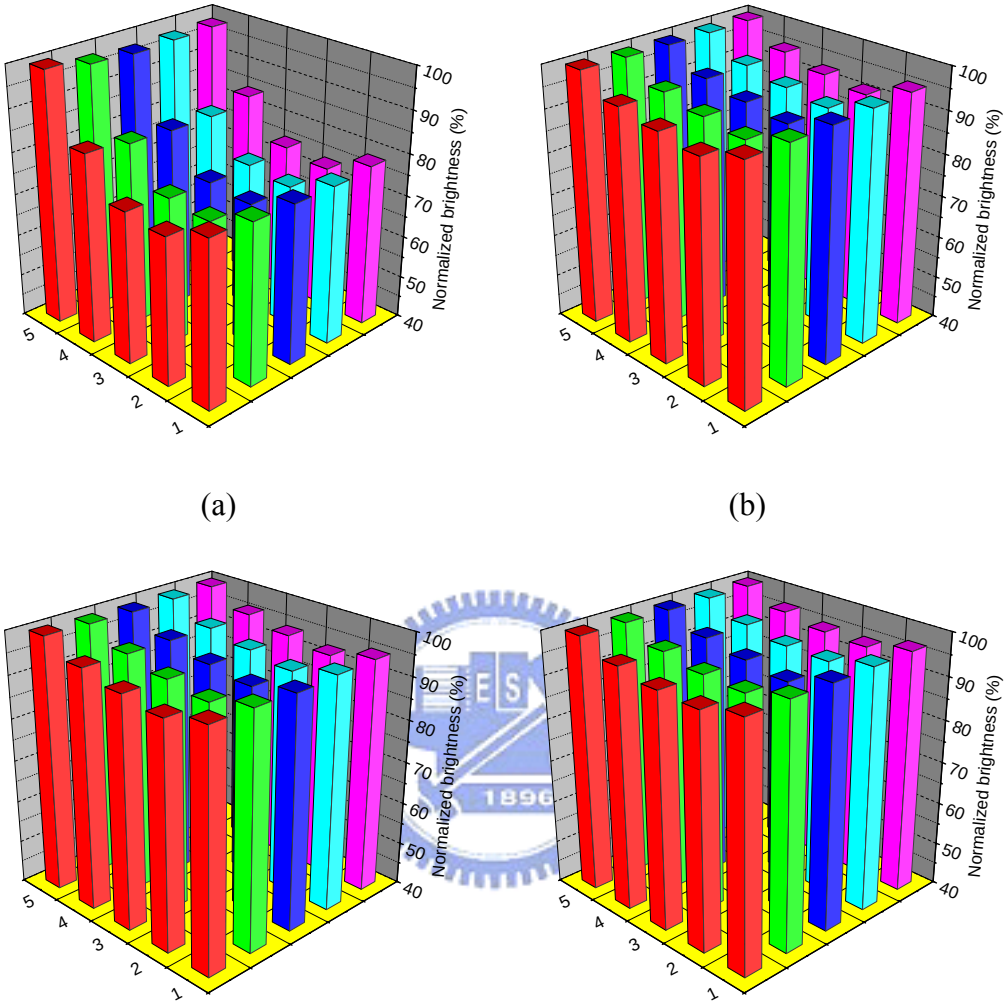


Fig. 4-5. Normalized brightness of AM-OLED display panel for the DC and AC driving schemes. (a) DC driving scheme with 100% duty cycle, I_{OLED}=1.6 uA. (b) AC driving scheme with 80% duty cycle, I_{OLED}=1.99 uA. (c) AC driving scheme with 40% duty cycle, I_{OLED}=3.9 uA. (d) AC driving scheme with 20% duty cycle, I_{OLED}=7.6 uA.

In contrast, the AC driving scheme shows effective compensation for brightness uniformity variation. In Fig. 4-5(b), the normalized brightness of all measured regions were well above 91.6%, for a duty cycle of the flashing period of 80% and an I_{OLED} of

1.99 μA. The RC time constant of each data line, which is a critical issue for reducing the programming period, is 100 ns. Even though the programming period is reduced to 20% of the entire frame time, the data voltages still can be programmed accurately into the pixels. When the duty cycle of the flashing period decreases to 40%, so as to possess more programming time, the driving current is increased to 3.9 μA to keep the reference brightness at 730 cd/m^2. Meanwhile, the AC driving scheme is still capable of maintaining the brightness uniformity higher than 92.4%, Fig. 4-5(c), even though the higher driving current can lead to a significant voltage drop. Although a higher driving current is needed in the AC driving scheme, the treatment of reversed bias voltage can accelerate the recovery from degradation and lead to an improvement in the J-V characteristics and device lifetime of the OLEDs [3][4]. In other words, the higher driving current may degrade OLED performance rapidly, however, the AC driving scheme, with proper reversed bias voltage, can alleviate the degradation. Fig. 4-6 shows the normalized brightness at region C2 versus the duty cycle in which the duty cycle of 100% represents the DC driving scheme. The experimental results show that the normalized brightness is higher than 91.6% when the AM-OLED panel operates in the AC driving scheme with various flashing duty cycles. In contrast, once the panel is driven by the DC driving scheme, the brightness drastically decreases to 74.5%. Nonetheless, the parasitic capacitance of T_{SW} between the storage node and the gate of T_{SW} causes the voltage drop at the storage node to be reduced so that ΔV_{DATA} is smaller than ΔV_{DD}. Besides, the thickness of spin-coated polymer film has a slight variation from the central to the outer areas. Consequently, the brightness uniformity cannot be compensated completely and a remaining nonuniformity of about 8% can be observed.

The AC driving scheme changes the voltage at cathode dynamically and will induce additional power consumption. The power consumption for the DC driving scheme are 2.3W and the power consumption for the AC driving scheme with varied flashing periods is 2.33W, as shown in Fig. 4-6.

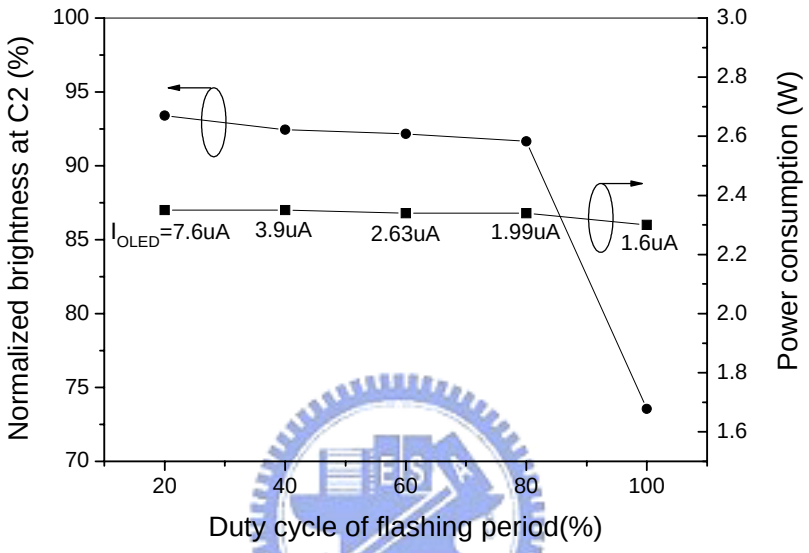
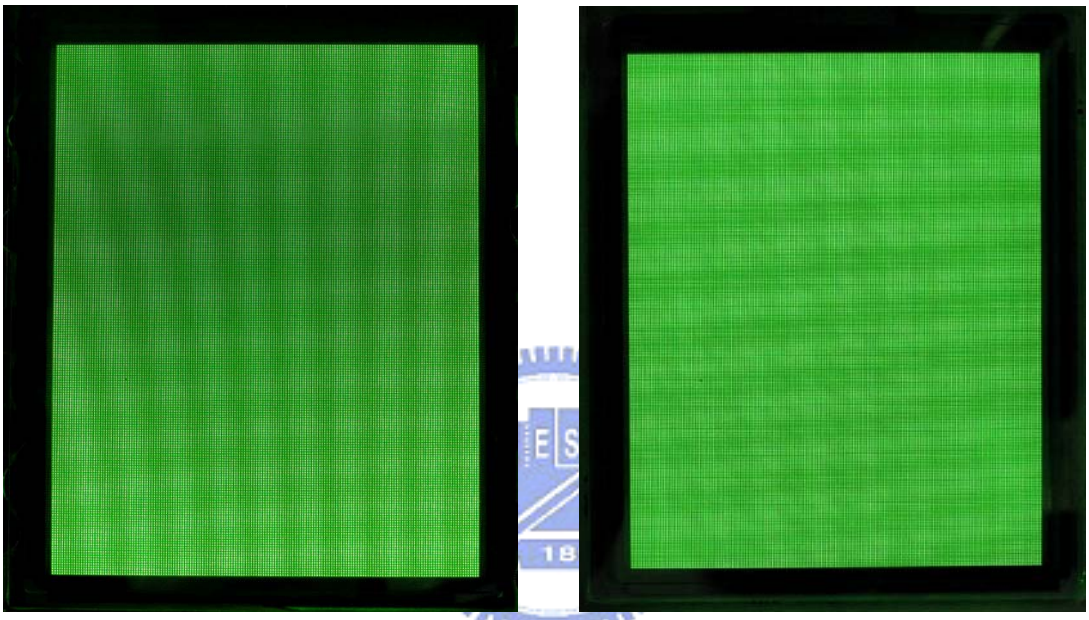


Fig. 4-6. Normalized brightness at region C2 as a function of flashing duty cycle.

Although an additional transient power is generated by the AC driving scheme, the total power consumption just increases 40mW. Since the OLED consumes static power of 2.3W during operation, the transient power induced by charging and discharging the capacitance of cathode only accounts for 1.74% increase of the entire power consumption. Therefore, the AC driving scheme will not significantly increase the power consumption even though the higher driving current is required. Two demo photographs of AM-OLED with conventional DC and proposed AC voltage driving schemes are shown in Fig. 4-7. The obvious luminance gradient can be observed in AM-OLED with DC driving scheme. The bottom area is close to the input pads so that the influence of resistance of addressing wire is uncritical. However, when the

driving currents propagate to a far away pixels in upper area, the large parasitic resistance can generate significant voltage drop and results in an luminance decay. In contrary, the AC driving scheme substituting for DC driving can effectively compensate the resistance induced voltage drop and is superior to improve the luminance uniformity, as shown in Fig. 4-7(b).



(a) (b)

Fig. 4-7. The color photographs of voltage-driven AM-OLED deposited with green copolymer. (a) Conventional DC and (b) proposed AC driving schemes.

The AC driving scheme divides the whole frame time into a programming and a flashing periods hence comparatively decreases the scan time T_{SCAN} of each scan line. Display size and resolution that the AC driving scheme is applicable are evaluated and shown in Fig. 4-8. The RC delay of a scan line can be calculated by using the product the total scan line resistance and the total scan line capacitance to ground. The product of scan line RC is a conservative estimate of the RC delay compared to the actual distributed RC delay.

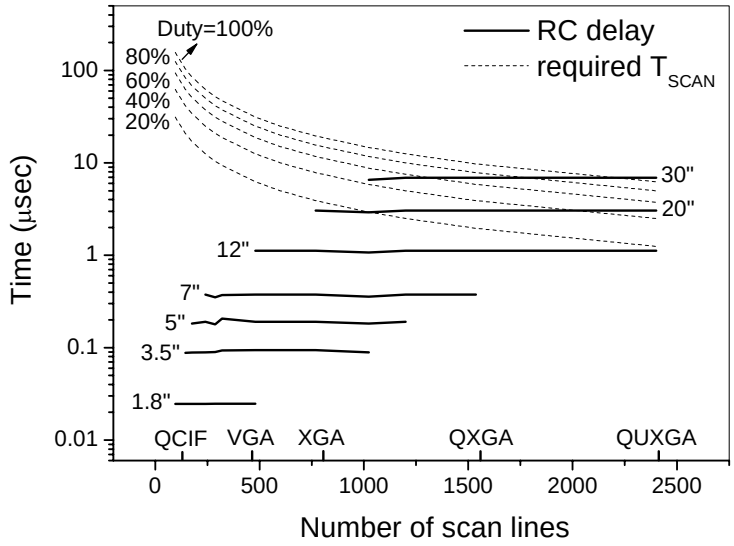


Fig. 4-8. The RC delay and the required T_{SCAN} as a function of the number of scan lines.

The solid lines shown in Fig. 4-8 denote the RC delay as a function of the number of scan lines for a range of display diagonals from 1.8” to 30”. The dash lines are the required T_{SCAN} calculated with corresponding number of scan lines and varies flashing duty cycle. It is explicit that increasing the number of scan lines and reducing the duty cycle will result in the lower T_{SCAN}. In other words, the AC driving scheme may affect the data programming accuracy when the display resolution and size increase. From small (1.8”) to moderate (12.1”) display size, the RC delay is of less than about 1 μsec, and that a high resolution display with AC driving scheme shows good capability to improve the brightness uniformity. However, as the display size becomes larger than 20”, the influence of RC delay is inevitable. For example, the duty cycle cannot lower than 60% for a 20” display with QUXGA resolution (3200 x 2400), otherwise, the RC delay can cause the data programming error. Consequently, the most suitable display resolution, size, and duty cycle that the AC driving scheme is used for can be evaluated according to Fig. 4-8.

4.4 Summary

An effective AC driving scheme and the corresponding pixel circuit were designed to improve the brightness uniformity of AM-OLED. By means of an alternating polarity of the cathode voltage and the corresponding pixel circuit, the voltage drop at the V_{DD} electrode caused by the intrinsic parasitic resistance of the addressing wire can be compensated. The experimental results demonstrate that the proposed AC driving scheme can achieve the uniform brightness of higher than 91.6% with various flashing duty cycle. Furthermore, this AC driving scheme shows exceptional competence for the high resolution displays from small to moderate diagonal sizes.

Reference

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Chapter 5

Current Driven AMOLED with Fully Integrated Driver

5.1 Introduction

Driving OLED uniformly with TFT is more challenging than driving liquid crystal due to OLED current-dependent luminance. Since the threshold voltage variation and mobility degradation become serious problems for the 2-T pixel with analog voltage driving scheme and result in luminance non-uniformity, digital driving schemes have been proposed to improve the luminance uniformity [1][2]. In the digital driving scheme, the switching TFT samples a digital voltage signal and the driving TFT controls the OLED in digital mode, i.e. OLED is either on or off. Grayscales are generated by either Area Ratio Gray scale (ARG) or Time Ratio Gray scale (TRG) schemes or by the combination of both. In ARG scheme, the pixel circuit consists of plural sub-pixels and the number of sub-pixel is corresponding to the required bits of gray scale, as shown in Fig. 5-1. The gray scale is acquired by selecting the number of the on-state sub-pixels that is the ratio of the light emitting portion. In TRG scheme, pulse width modulated is used instead of sub-pixels. Similar to ARG, the frame time in TRG is divided into plural sub-frames which is weighted by binary.

The digital voltage signal with large swing can effectively eliminate the influence of threshold voltage variation and maintain the luminance uniformity of the pixels. However, both the ARG and TRG divide either the pixel area or the frame time into several sub-pixels and sub-frames associated with the gray scales. Thus, not only the number of electrodes becomes larger but also the operation frequency is much

higher than the conventional analog driving AM-OLED panel. In other words, the peripheral driver and driving scheme are too complicated to be implemented. Therefore the digital driving schemes are only suitable for low resolution and low gray scale applications.

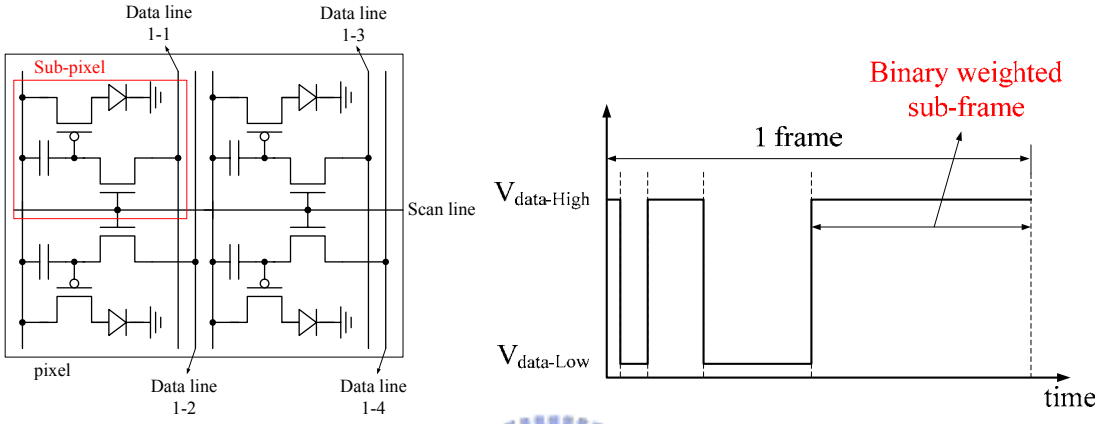


Fig. 5-1. Digital driving schemes: (a) area ratio gray scale and (b) time ratio gray scale.

Several V_{TH}-compensation AM-OLED pixel electrode circuits using voltage signals have been proposed to be compatible with conventional AM-LCD driving system [3][4][5]. In addressing period, more than two operations are performed sequentially to address each pixel to couple the data voltage onto the capacitor in which the V_{TH} of driving TFT has been memorized. In addition to the original data and scan lines, more electrodes and higher operation speed are needed to ensure the correct pixel functions, consequently increasing the complexity of the driving system. As the panel size and resolution increase, the programming time will not be sufficient to accurately set the threshold voltage and write the data voltage. Furthermore, the voltage-type V_{TH}-compensation pixel electrode circuits are incapable of compensating mobility degradation that may occur sooner or later according to the different value of

OLED current.

In order to ensure the luminance uniformity, a current driving schemes has been proposed [6][7]. In the current driving scheme, the design of pixel electrode circuit is based on the switch current (SI) memory cell which must be driven by external current signal instead of the conventional voltage signal. Since the OLED is a current driven device, the pixel electrode circuit should not only ensure the matching of OLED current between addressing and non-addressing phase, but also compensate the variations in OLED and TFT characteristics e.g. threshold voltage variations and aging effects.

In previous works, the pixel electrode circuits are fabricated by a-Si:H TFT technology because of the low-cost fabrication steps and compatibility with AM-LCD industry [6][7]. Since the driving TFT should provide a continuous current over a large portion of the frame time to efficiently drive the OLED for desired luminance levels. The pixel area limits the number of TFTs and their geometric widths, which are directly proportional to TFT transconductance. As a result, the a-Si:H TFT technology is limited due to the low transconductance as discussed in Chap. 1. The mobility μ of poly-Si TFT can be of one to two orders of magnitude higher than that of a-Si:H TFT. As a consequence, poly-Si TFT widths can be smaller, with possibilities of allowing for more TFTs in the pixel area for additional error correction. In addition, while a-Si:H TFT is able to produce steady-state currents suitable for reasonable brightness levels, the terminal voltages at each electrode are fairly large. Due to the high terminal voltages resulting from low mobility the two transistors in series between the power supply and the OLED in the pixel circuit significantly increase the power dissipation [6]. As a result, the a-Si:H TFT may not be suitable for large-sized displays having high luminance. Besides, due to high gate-to-source and gate-to-drain overlap

capacitances, the ON/OFF switching of a-Si:H TFT can create large voltage offsets and affect the accuracy of stored signal in C_{ST}. Thus, poly-Si TFT possessing low gate overlap capacitances is more attractive than a-Si:H TFT. The lack of p-channel TFT in a-Si:H TFT technology decreases the design flexibility so that more control signals are needed for the current-driven pixel electrode circuit. Furthermore, unlike poly-Si technology where the current data drivers can be designed and integrated into the display panel, a-Si backplanes must incorporate c-Si data drivers but now the commercial current-type drivers are not available. A current-type driver for various display sizes, formats, pixel designs, and brightness levels are more complex and costly than conventional voltage-type drivers.

5.2 Design of current-driven pixel with poly-Si TFT

With high mobility, high transconductance and implementation capability of p-channel device, poly-Si TFT technology is beneficial for current-driven AM-OLED to compensate the threshold voltage and mobility variations due to non-uniform grain size and time-related electrical stress. The schematic of pixel electrode circuit based on SI memory as well as the timing diagram are shown in Fig. 5-2. The operation of the pixel electrode circuit operates can be defined into programming and reproduction periods. In the **programming period**, the scan line signal is HIGH to turn on T1 and T2, then the input data current I_{DATA} flows through the transistors T1, T4, and OLED to the ground. Since the drain and gate electrodes of T4 are connected together by T2, the gate voltage of T4, V_{G4}, is automatically charged to a suitable value for the flow of this current and then stored in storage capacitor $C_{ST,}$ as shown from Eq. 5-1 to Eq. 5-3 where μ_{FE}, C_{OX}, W and L are field-effect mobility, capacitance of gate oxide per meter square, width and length of TFT.

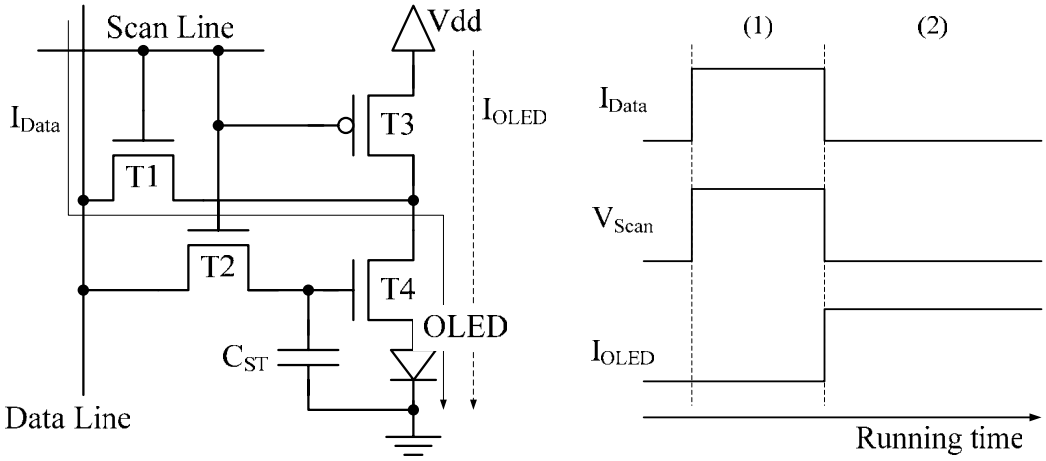


Fig. 5-2. (a) Schematic diagram of 4-T current-driven pixel electrode circuit. (b) Timing chart of pixel operation. ((1) programming and (2) reproduction period)

$$I_{DATA} = \beta_4 (V_{GS4} - V_{TH})^2, \qquad \beta_4 = \frac{1}{2}\mu_{FE} C_{OX} \frac{W_4}{L} \qquad \text{Eq. 5-1}$$

Therefore the overdrive voltage is

$$V_{GS4} - V_{TH} = \sqrt{I_{DATA}/\beta_4} \qquad \text{Eq. 5-2}$$

Since the source voltage of T4 is equivalent to the OLED voltage V_{OLED}, the T4 gate voltage is

$$V_{G4} = \sqrt{I_{DATA}/\beta_4} + V_{TH} + V_{OLED} \qquad \text{Eq. 5-3}$$

The voltage V_{G4} is variable and can be different from pixel to pixel and from time to time, according to the desired current flow and the magnitude of the V_{TH} shifts of both OLED and T4 of the addressed pixel. If an OLED and/or T4 threshold voltage variation appears, V_{G4} will always be set to ensure the desired OLED current corresponding the precise data current supplied by external driver. In this manner, the OLED current can be maintained to the set-value, no matter how large the V_{TH} shift is for the driving TFT and the OLED.

When the pixel electrode circuit is deselected and the scan line signal is LOW,

both the T1 and T2 are OFF and the pixel operates in **reproduction period**. At the same time, the T3 is ON due to the opposite polarity of the charge carriers, allowing the current flowing from T3 to T4. Because the gate voltage tracks the threshold voltage of T4, the effect of V_{TH} variation is practically cancelled in this circuit and the constant current ensures a minimum variation of the gray scales. Consequently the threshold voltage shifts of TFTs in this circuit will not have a major impact on the output current and display luminance.

An important issue of this current-driven pixel is a mismatch between the input diving current and output OLED current. Ideally the relationship between these two currents should be linear, however, there are a number of factors resulted in non-linearity in this transfer characteristic and limit the useful current range and thereby also the gray scales. It should be noted that transistor T4 must operate in the saturation mode either during the programming or reproduction periods. In other words, nonlinearity between the I_{DATA} and I_{OLED} will appear as the T4 operates in the undesirable non-linear mode. This is understandable because only in the saturation mode, the transistor can act as a current source in which the current is only dependent on the gate-to-source voltage. In practical, the T1 and T3 are not ideal switches, hence the I_{DATA} and I_{OLED} passing them can generate voltage drops that drive T4 to operate in linear mode. In programming period, a voltage drop between drain and source electrodes of T1 results from the I_{DATA}. The T1 source voltage T_{S1} equivalent to T4 drain voltage T_{D4} is smaller than T1 drain voltage T_{D1}. Because no current will pass through T2, the turn-on resistance is like an ideal switch, the T4 gate voltage V_{G4} is equal to T1 drain voltage V_{D1}. Based on above reasons, the V_{D4} can be a bit lower than V_{G4} and T4 may probably work in linear region, consequently, resulting in output current deviation. In order the ensure T4 working in saturation region in programming

period, the overdrive voltage should be defined as following.

$$V_{GS4} - V_{TH} \le V_{DS4} \qquad \text{Eq. 5-4}$$

Because $V_{G4}=V_{D1}$ and $V_{D4}=V_{S1}$, Eq. 5-4 is rewritten as

$$V_{GD4} = V_{DS1} \le V_{TH} \qquad \text{Eq. 5-5}$$

The turn-on voltage of scan line is usually set to Vdd which is high enough to make sure the T1 and T3 work in deep linear region. The data current passing through T1 is

$$I_{DATA} = \beta_1 (V_{GS1} - V_{TH}) V_{DS1} - {V_{DS1}}^2/2, \qquad \beta_1 = \frac{1}{2}\mu_{FE} C_{OX} \frac{W_1}{L} \qquad \text{Eq. 5-6}$$
$$\cong \beta_1 (V_{GS1} - V_{TH}) V_{DS1}$$

Therefore,

$$V_{DS1} = \frac{I_{DATA}}{\beta_1 (V_{GS1} - V_{TH})} = \frac{I_{DATA}}{\beta_1 (V_{dd} - V_{S1} - V_{TH})} \qquad \text{Eq. 5-7}$$

According to $V_{S1}=V_{G4}-V_{DS1}$ and Eq. 5-3, the V_{DS1} can be expressed as

$$V_{DS1} = \frac{I_{DATA}}{\beta_1 (V_{dd} - V_{G4} + V_{DS1} - V_{TH})} \qquad \text{Eq. 5-8}$$
$$= \frac{I_{DATA}}{\beta_1 (V_{dd} - \sqrt{I_{DATA}/\beta_4} - V_{OLED} - 2V_{TH} + V_{DS1})}$$

Taking account of Eq. 5-5, the non-ideal effect of T1 can be derived as following equation.

$$\beta_1 \ge \frac{I_{DATA}}{V_{TH} (V_{dd} - \sqrt{I_{DATA}/\beta_4} - V_{OLED} - V_{TH})} \qquad \text{Eq. 5-9}$$

It is evident that during the programming period, the size of T1 should be deliberated designed based on Eq. 5-9 to prevent the T4 operation in linear region.

In reproduction period, the non-ideal switch T3 possessing a certain quantity of turn-on resistance can result in a voltage drop as an I_{OLED} passing through it. The drain voltage of T4, V_{D4}, cannot be maintained to Vdd and the decrease of V_{D4} can force T4 to work in linear region. The design criterion for the reproduction period is

similar to that of programming period and derived as following.

$$V_{D4} = V_{dd} - V_{DS3}$$
$$\cong V_{dd} - \frac{I_{OLED}}{\beta_3 (V_{dd} - V_{D4} - V_{TH})} \quad \text{Eq. 5-10}$$

For ensuring T4 operating in saturation region,

$$V_{GD4} \le V_{TH}$$
$$\Rightarrow V_{D4} \ge V_{G4} - V_{TH} \quad \text{Eq. 5-11}$$

Assuming I_{DATA}=I_{OLED} and substituting Eq. 5-3 and Eq. 5-10 into Eq. 5-11, respectively, we obtain

$$V_{dd} - \frac{I_{DATA}}{\beta_3 (V_{dd} - V_{D4} - V_{TH})} \ge \sqrt{I_{DATA}/\beta_4} + V_{OLED}$$
$$\Rightarrow \beta_3 \ge \frac{I_{DATA}}{\frac{I_{DATA}}{\beta_4} + (V_{dd} - \sqrt{\frac{I_{DATA}}{\beta_4}})(V_{dd} - 2V_{OLED} - V_{TH}) + V_{OLED}(V_{OLED} + V_{TH})} \quad \text{Eq. 5-12}$$

The Eq. 5-12 reveals the design condition of T3 which can keep the T4 operating in saturation region when pixel is in reproduction period.

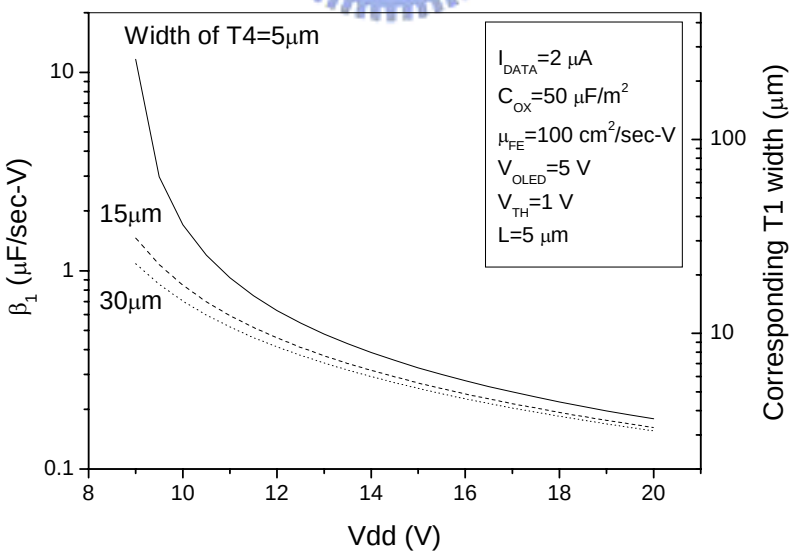


Fig. 5-3. Minimum required β and geometric size of T1 as a function of turn-on voltage of scan line at various width of T4.

The higher turn-on voltage of scan line which is usually identical to Vdd is used,

the smaller necessary size of T1 can be introduced. As shown in Fig. 5-3, a higher voltage applied to the gate electrode of TFT can induce larger channel and result in lower turn-on resistance than a smaller voltage. In other words, the high Vdd can reduce the voltage drop across the drain and source electrodes of T1, moreover, ensuring the operation of T4 in saturation region. Besides, increasing the T4 size from 5 to 30 μm is useful to reduce the T1 size as well. The large T4 can conduct the I_{DATA} with low gate voltage due to the high transconductance. Consequently, it is difficult to drive T4 into saturation region on account of the voltage drop of T1. In addition, as an OLED material with high quantum efficiency is used, the low I_{DATA} is necessary to achieve adequate display luminance. Therefore, the low I_{DATA} is helpful to reduce the required transconductance and size of T1, because the gate voltage of T4 and the voltage drop of T1 are simultaneously decreased, as shown in Fig. 5-4. In contrast, higher T4 gate voltage is required when decreasing the T4 size at high data current condition so that T4 hardly operates in saturation region, consequently, the T1 size should be increased to maintain the T4 operation in saturation region.

For the aspect of β3, the influence of Vdd and T4 size should be taken into account in pixel design. For a given condition, the transconductance and size of T3 is gradually decreased as the Vdd increases, as shown in Fig. 5-5. In the reproduction period, the higher Vdd can make the drain voltage of T4 distant from the gate voltage so that T4 can be driven into deep saturation region regardless of T3 turn-on resistance, therefore, the size of T3 can be reduced. In terms of the influence of T4 size, the size of T3 should be increased as the T4 size becomes larger. Since the T3 is serially connected to T4 in the reproduction period, its equivalent circuit is similar to two series resistors. In this condition, the decreased T4 resistance associated with the increased T4 size may be much lower than T3 resistance, hence, forcing T4 to operate

in linear region. In order to prevent an operation in linear region, the T3 size should be increased so as to make the resistance of T3 and T4 compete with each other.

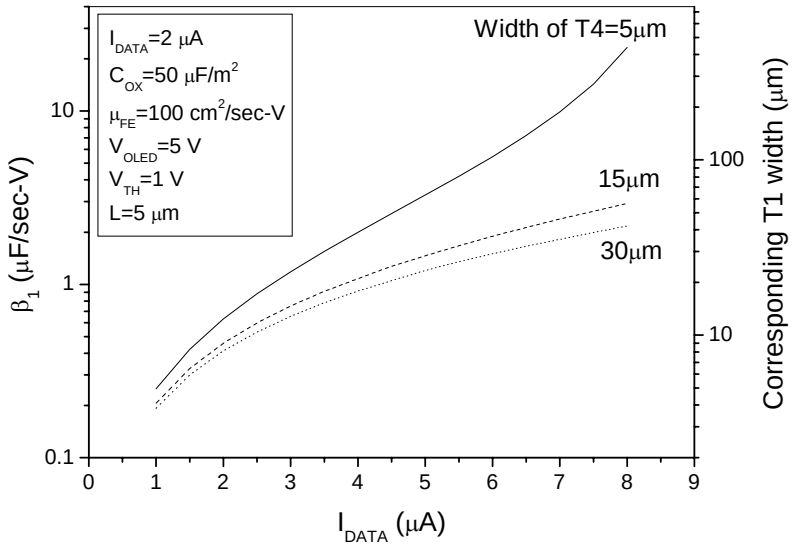


Fig. 5-4. Minimum required β and geometric size of T1 as a function of input data current I_{DATA} at various width of T4.

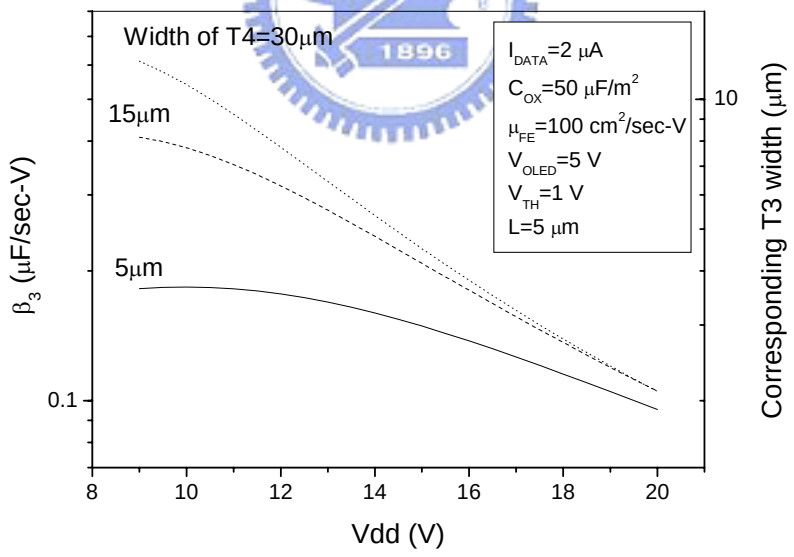


Fig. 5-5. Minimum required β and geometric size of T3 as a function of turn-on voltage of scan line at various width of T4.

The high I_{DATA} which induces a large drain-to-source voltage of T3 can decrease the T4 drain voltage. In the meanwhile, the T4 gate voltage becomes higher in large

I_{DATA} condition so that T4 is situated in linear region and causes output current nonlinearity. The design trend is toward the large T3 size when a high I_{DATA} is required, as shown in Fig. 5-6. The large T3 possessing a small resistance which can avoid large voltage drop across the drain and source electrode is helpful to raise the drain voltage of T4 and mitigate the possible operation in linear region. The above equations and analyses are derived by using the basic MOS physical model and can be used as guidelines when designing the current-driven AM-OLED pixels. From these results, the trade-off between the TFT size and supplied voltage or driving current is easily quantified so as to achieve a maximum pixel performance.

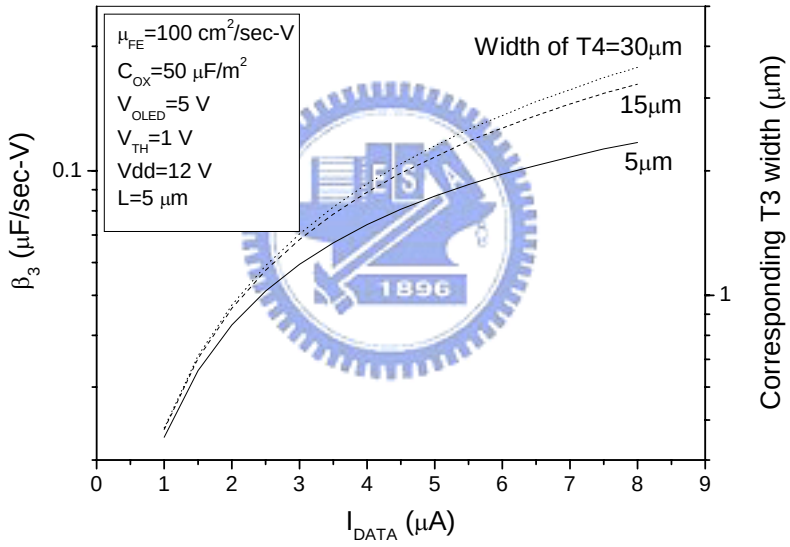


Fig. 5-6. Minimum required β and geometric size of T3 as a function of input data current I_{DATA} at various width of T4.

5.3 Electrical reliability and uniformity

The significant function of the current-driven AM-OLED pixel electrode circuit is to consistently provide a constant current for the OLED regardless of V_{TH} of mobility variation due to device aging or fabrication processes. A bias-temperature-stress (BTS) experiment was performed for the current-driven pixel

to accelerate the aging process using a Keithley 4200 semiconductor characterization system with a probe station, as shown in Fig. 5-7.

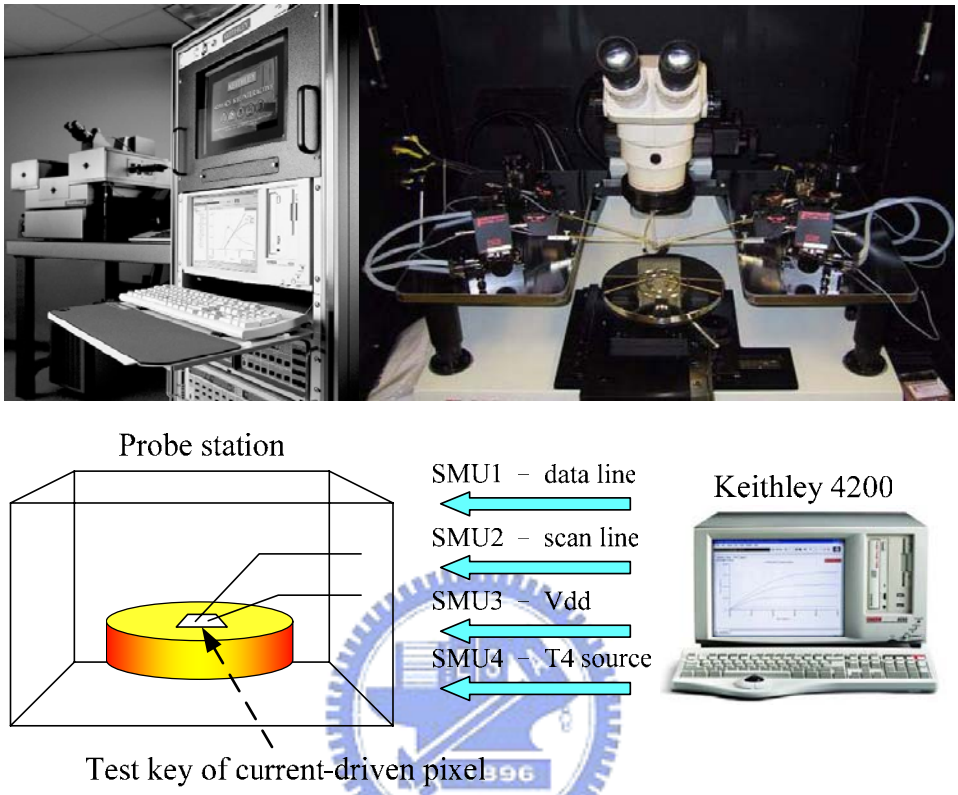


Fig. 5-7. A bias-stress experiment setup with Keithley 4200 semiconductor characterization system and probe station.

The ground probe station is equiped with an electrically isolated, water-cooled thermal plate within shielding box. The plate can be controlled by Temptronic TPO315A thermal controller, which can operate temperature from 25 to 300°C. The Keithley 4200 precision semiconductor characterization system can provide I-V measurement, bias for BTS, and quasi C-V measurement. To avoid any OLED-related degradation issues, the experiment was performed without connecting the OLED (i.e., we directly connected the T4 source to ground). Four source measurement units (SMUs) were used as controlled voltage sources that can measure the current flowing through them and vice versa. In all measurements, the system ground was connected

to the source of the TFT T4 in the pixel. SMU1 was connected to the data line to supply an input data current and monitored the voltage at data line simultaneously as the experiment was performed. The SMU2 was connected to scan line and supplied a voltage of 12 V to always turn on the T1 and T2. The SMU3 of 0 V and SMU4 of 12 V were connected to the Vdd and T4 source, respectively as reference voltages. The parameters used for the pixel circuit reliability evaluation are given in Table 5-1.

Table 5-1. Design parameters of pixel circuit for electrical reliability evaluation.

	2-T pixel circuit	4-T pixel circuit
TFT size	T1: 7 μm /5+5 μm T2 :12μm /5+5 μm	T1: 7 μm /5+5 μm T2: 7 μm /5+5 μm T3: 10 μm /5+5 μm T4: 12 μm /5+5 μm
C_{ST} (fF)	600	600

From the experimental results, it is significant that the current-driven pixel electrode circuit is far more stable than the conventional voltage-driven 2-T pixel that was characterized in Chap. 4. It is easy to perceive the contrast of I_{OLED} stability between 2-T and 4-T pixels, as shown in Fig. 5-8. The I_{OLED} of 2-T pixel decayed from initial current of 10 μA to 7 μA, almost 30% variation over a BTS time of 12 hours. Nevertheless the I_{OLED} of 4-T pixel was almost constant during the BTS experiment. As discussed sec. 5-2, the T4 gate voltage equal to data line voltage V_{DATA} was adjusted automatically according to the V_{TH} variation. Since the T4 was stressed due to the constant data current, the T4 V_{TH} increased as time went on. Consequently, the V_{DATA} was increased to compensate the V_{TH} degradation and maintain the OLED current. From Fig. 5-8., the V_{DATA} of 4-T pixel increased from 5.05 to 5.7 V during the BTS experiment. Based on Eq. 5-3 and assuming V_{OLED}=0V,

the corresponding V_{TH} shift of 0.65 V can be calculated.

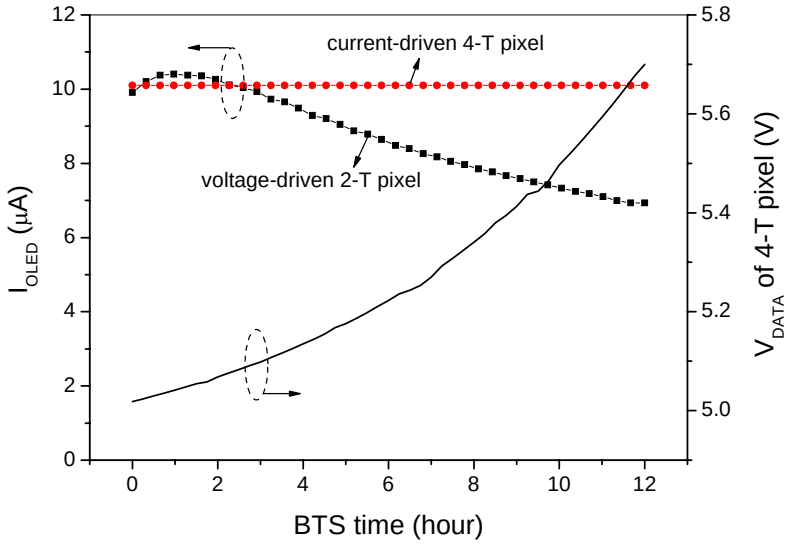


Fig. 5-8. Impact of BTS on the 2-T and 4-T pixel electrode circuit characteristics.

The 4-T pixel electrode circuit had been adopted in a fabricated 2.2" AM-OLED prototype of QCIF+ resolution. In Fig. 5-9(a), a constant data current is supplied to entire pixels and the whole panel view reveals that the random luminance fluctuations due to the V_{TH} variation are compensated, resulting in apparently smoother image. Although the 4-T pixel electrode circuit is capable of improving the luminance uniformity, the decrease of aperture ratio resulting from the complicated circuitry and wire routing is evident. In the fabricated panel, the aperture ratio of 4-T pixel is about 37% so that the driving current should be larger for an adequate luminance, in contrast to 2-T pixel of larger aperture ratio. Consequently, the power consumption of the current-driven AM-OLED is larger.

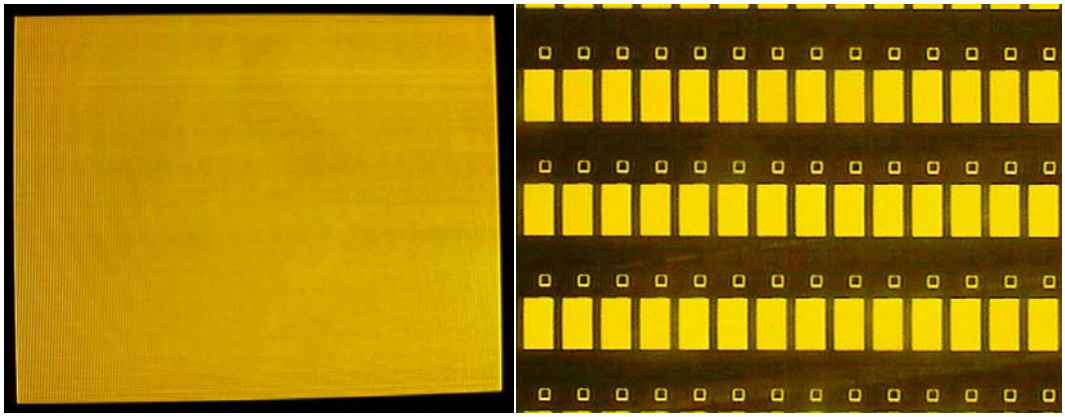


Fig. 5-9. (a) Photograph of the fabricated 2.2” QCIF AM-OLED display panel with current-driven 4-T pixel circuit. (b) Microscopic view of the AM-OLED pixels.

5.4 AM-OLED with integrated current-type data driver

According to the above experiments, the current driving scheme is the most promising candidate among several pixel-driving methods to improve luminance uniformity. However the current driving scheme still suffers a serious drawback that a highly accurate current-type data driver is required. While such driving accuracy might be externally supplied, for example, drivers fabricated by crystal-Si MOSFETs that offer high uniformity in current/voltage characteristics, the use of such drivers would increase programming time further because of the increase in floating load-capacitance induced by the connection between the data drivers and the display panel. Besides, the various OLED materials with different characteristics result in varieties of data drivers. Customizing the current-type c-Si drivers for specific OLED is contributive to achieve high performance AM-OLED, yet increasing the manufacturing cost. What is needed, then, is to integrate high-accuracy current-type data drivers into the AM-OLED substrate with poly-Si TFTs. As a result, in this dissertation we have developed an integrated poly-Si TFT 6-bit current-type data driver.

5.4.1 Current-driven AM-OLED architecture

The interface of AM-OLED panel is fully digital so as to be compatible with most electronic device. The digital input interface can reduce the usage of external driver ICs and is beneficially compatible with most portable electronic device. The system diagram of the current-driven AM-OLED panel, shown in Fig. 5-10., consists of 2 input channels with 6 bits gray scales for RGB video signal.

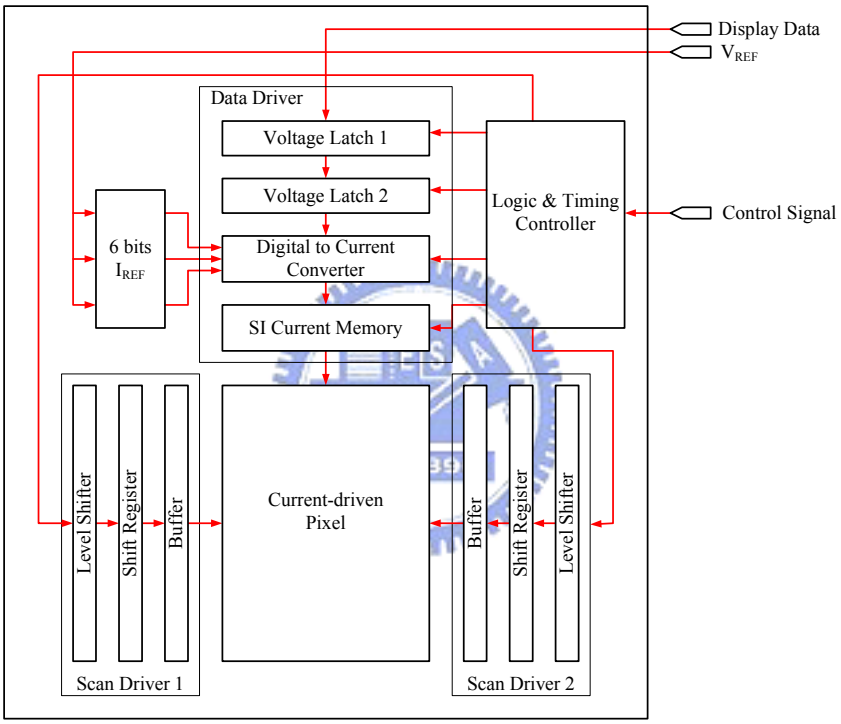


Fig. 5-10. Block diagram of the current-driven AM-OLED display substrate with fully integrated data driver.

The control signal is sent to logic & timing controller to generate the timing signals for each functional circuit. The scan driver which can drive the scan line is composed by buffer, shift register and level shifter. The data driver consists of voltage latch which is used to store to input digital signal for the sake of the serial-to-parallel operation. Digital-to-current converter (DCC) is the key component which can translate the digital signal to current signal. The system features a controllable

reference current that can be adjust by an external signal and generates the different levels of reference currents for respective R, G, B digital-to-current converters. A pair of 176 x 3 high speed switch current memory circuits with serial-in-parallel-out structure can alternately memorize the translated current signal sequentially and send it out to all of the data line one time. The pixel circuits with self-compensation function can achieve the uniform brightness by current signal regardless of threshold voltage variation as discussed above. The key blocks of the current-type data driver will be further detailed along the system signal flow in the following sections.

5.4.2 Reference current generator

Accuracy reference current I_{REF} has to be generated and supplied to the following digital-to-current converter (DCC) to perform the data transforming process. Since the 6-bits DCC produces an analog data current based on the digital image data, six binary weighted reference current signals are needed for each DCC. Two sets of I_{REF} generators are implemented in each display panel and each of them is schematically shown in Fig. 5-11. One I_{REF} generator is in charge of the lower 3 bits corresponding gray scales from 0 to 31 and the other is responsible for the higher 3 bits for gray scales from 32 to 63. In the I_{REF} generator, every TFT operates in the saturation region where V_{GS} of all TFTs are equal. According to the binary weighted number of TFTs, the I_{REF} generator distributes a set of scaling currents by mirroring a reference current supplied from an external driver. With the current mirror configuration, it is admirable to completely avoid characteristic deviations during fabrication and device aging. It should be noted that the I_{REF} generator is immune from the programming time problem caused by parasitic capacitance, because the magnitude of either reference current or generated currents are constant. Moreover, this circuit requires only one

current source when even the number of gray levels is increased.

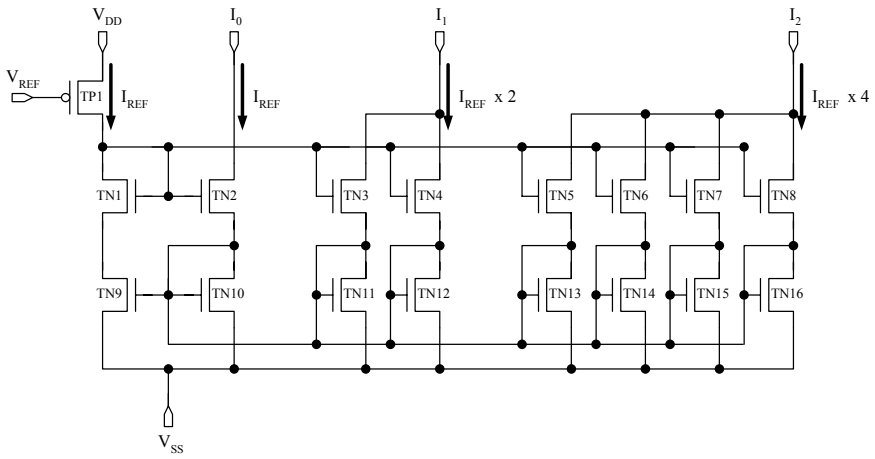


Fig. 5-11. Schematic diagram of reference current generator.

5.4.3 High performance current memory

The switch current memory has been widely used in digital-to-analog converter and analog sampled-data signal processing applications [8][9], since they exhibit superior tolerance to device parameter variations. One of the fundamental factors limiting an accuracy of the switch current (SI) memory is the charge injection occurring when the transistor turns off [10]. The amount of charge a TFT carries in its channel when the gate voltage applied can be expressed as

$$Q_{ch} \approx W \cdot L \cdot C_{OX} \left(V_{GS} - V_{TH} \right) \qquad \text{Eq. 5-13}$$

As the TFT turns off, this charge is released from the channel to the source and drain terminals and affects the voltage at both these terminals. The voltage offset appears as a nonlinear term at source and drain terminals because Q_{ch} is interrelated to the source and drain voltages. The accuracy of SI memory depends upon how to protect the critical gate voltage because the variation of gate voltage can lead to a different reproduced current from the input current. The low sensitivity to the charge injection mechanism of SI memory can be realized by several methods such as:

1) the usage of complementary switch for the partial cancellation of the charge injection.
2) the usage of large capacitance for the reduction of the voltage offset at critical node.

The first method eliminates the charge injection in terms of the carriers that cancels each other due to the opposite polarities (such as those from n-channel and p-channel TFTs in the complementary switch). However the required additional clock signals increases the amount of connecting wire and control logic as well as complicates the control system. Besides, the parasitic capacitance of connecting wire may induce the clock signals miss-alignment and lose the capability of charge injection cancellation. The other is to increase the storage capacitance to restrain the effect of the charge injection. Nevertheless, the larger storage capacitance requires more charging time to establish the gate voltage during the sampling period, consequently, decreasing the operating frequency.

In this dissertation, a current mirror based SI memory restraining charge injection with one control signal is proposed and designed. The experiment results of SI memory implementation using poly-Si TFT process are also presented.

5.4.3.1 Circuit description

Proposed SI memory designed with current mirror is capable of protecting the critical gate voltage against charge injection. In SI memor circuit, the TFT T0, T1 and T2 build the current mirror, and T3, T4 and T5 act as the switches, as shown in Fig. 5-12. Two capacitors, C_{ST1} and C_{ST2}, are used as storage capacitors. The proposed SI memory operates in two mode: sampling and reproducing.

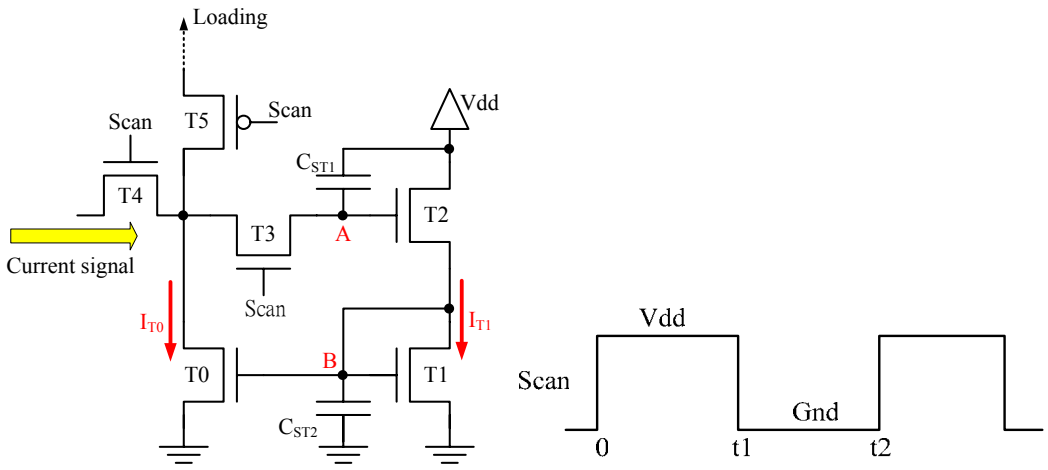


Fig. 5-12. Schematic diagram of proposed SI memory. The circuit samples the current signal in the interval $0 < t < t_1$. The circuit reproduces the sampled current in the interval $t_1 < t < t_2$.

1) Sampling mode (Scan = Vdd): The SI memory is connected to external current source by T4. The drain-to-gate voltage of T2 is adjusted roughly to generate the current I_{T1}. Then I_{T1} sets the the gate voltage of T0 to an appropriate value for generating the current I_{T0} as the same as the input current.

2) Reproduction period (Scan = ground): The SI memory is connected to the loading by T5 and has a capability of sinking the approximately equivalent current from the loading. T1, T2, and T3 make contribution to functionally protect the critical gate voltage of the SI memory. As the scan signal turns off transistor T3, thereby, the circuit is driven into reproducing mode. The charge carriers stored in the channel of T3 is released and redistributes to the gate of T2 (node A). Therefore, the charge carriers injecting into the storage capacitor results in the gate voltage variation of T2 (ΔV_A). A parameter $g_m \cdot V_{GS}$, with the transconductance g_m defined in saturation region as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \left(2I_d \cdot C_{OX} \cdot \mu \cdot \frac{W}{L} \right)^{1/2} \qquad \text{Eq. 5-14}$$

is one of the important parameters of the TFT in the voltage-controlled curent source circuit. The current I_{T1} deviates from the input current due to the gate voltage variation of T2 (ΔV_A) of $g_{m2} \cdot \Delta V_A$ as shown in Eq. 5-15, where g_{m2} is transconductance of T2.

$$\Delta I_{T1} = g_{m2} \cdot \Delta V_A \qquad \text{Eq. 5-15}$$

The current I_{T1} through T1 is changed by charge injection mechanism so that the voltage at node B is also altered as follow

$$\Delta V_B = \frac{\Delta I_{T1}}{g_{m1}} \qquad \text{Eq. 5-16}$$

To combine Eq. 5-15 and Eq. 5-16, the relationship between ΔV_{GS2} and ΔV_B can be expressed as

$$\frac{\Delta V_B}{\Delta V_A} = \frac{g_{m2}}{g_{m1}} = \left(\frac{2I_d \cdot C_{OX2} \cdot \mu_2 \cdot \frac{W_2}{L_2}}{2I_d \cdot C_{OX1} \cdot \mu_1 \cdot \frac{W_1}{L_1}} \right)^{1/2} \qquad \text{Eq. 5-17}$$

As long as T1 and T2 are locally matched, Eq. 5-17 can be simplified as

$$\frac{\Delta V_B}{\Delta V_A} = \left(\frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \right)^{1/2} \qquad \text{Eq. 5-18}$$

The ratio of ΔV_B to ΔV_A observed from the theoretical analysis is only dependent upon the geometric size of TFT. At such condition, W/L ratio of T1 should be enlarged to allow $\Delta V_B/\Delta V_A$ as small as possible. Thus the charge injection mechanism cannot directly affect the critical gate voltage so that the proposed SI memory can effectively achieve the accurate reproducing current by optimizing the size of TFT. Therefore, not only the small capacitance is acceptable for the proposed SI memory design, but the response time of the SI memory is also improved by reducing the size

of storage capacitance.

5.4.3.2 Experiment

The prototype of the proposed SI memory has been designed and evaluated by taking advantage of the simulation program Synopsis H-SPICE with the Rensselaer Polytechnic Institute (RPI) Troy, NY, poly-Si TFT model [11][12]. Table 5-2 lists the parameters used in designing the SI memory. Besides, the laser annealing poly-Si TFT technology is used to fabricate the proposed SI memory shown in Fig. 5-13(a).

Table 5-2. Parameters for SI memory design.

Device	
W/L for T0, T2, T3, T4, T5 (μm)	7/5
W/L for T1 (μm)	7/5, 15/5, 30/5, 50/5
Loading circuit	Pixel liked active loading
Cs (fF)	100, 200, 400, 800
μ_n (cm^2/V-sec)	77.4
μ_p (cm^2/V-sec)	85
Supply Signal	
Vdd, logic-High (V)	10
Ground, logic-Low (V)	0
Input current (μA)	0.1 ~ 12

The dirct measurement of critical gate voltage of SI memory has severe limitation due to the small storage capacitor of 100 fF. The parastic capacitance of measurement probe, usually several pico-farad, greatly affects the measurement accuracy of the probed node when the falling rate of the critical voltage is high. An additional unit gain operation amplifier can be used to circumvent the problem and to be a better monitor of critical gate voltage. The operation amplier possesses the excellent driving

capability to track the input voltage precisely, therefore, suitable for the interface with measurement system. The pixel-liked circuit is designed as an active loading for SI memory. The entire measurement system diagram is shown schematically in Fig. 5-13(b).

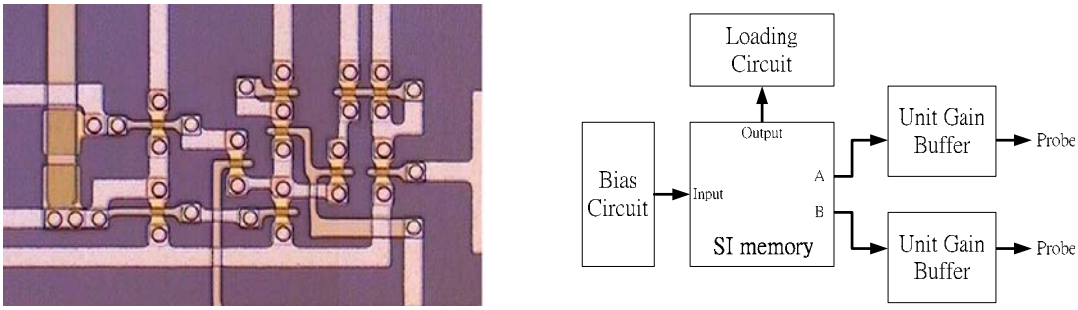


Fig. 5-13. (a) Photograph of porposed SI memory fabricated by LTPS-TFT process. (b) Diagram of SI memory measurement system.

The critical gate node B isolated from switch T3 in proposed SI memory is not perturbed by charge injection directly, as previously discussed. Furthermore,

$$\frac{\Delta V_B}{\Delta V_A} = \left(\frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \right)^{1/2} \qquad \text{Eq. 5-18}$$

indicates that the increase of geometric size of T1 is beneficial for reducing the critical gate voltage error without using large capacitance. The characteristics of voltage error versus input current with different size of T1 were measured and are illustrated in Fig. 5-14. It is evident that the minor critical gate voltage error is achieved by increasing T1 size from 7 to 50 μm. Moreover, large storage capacitor still shows great resistance to charge injection, as confirmed in Fig. 5-15. However, the critical gate voltage error still increases as the input current becomes smaller, as shown in Figs. 5-14 and 5-15. As a result, transistors T1 and T2 driven in sub-threshold region of weak current are

more sensitive to the charge injection.

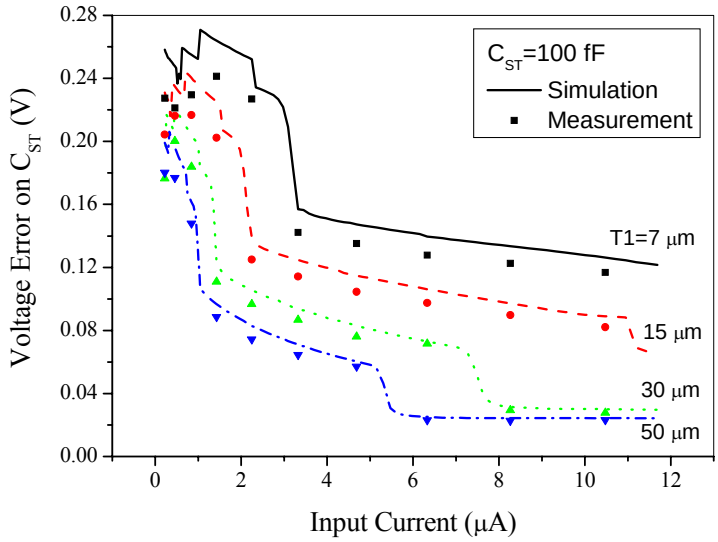


Fig. 5-14. Voltage error at node B in proposed SI memory with different T1 geometric size.

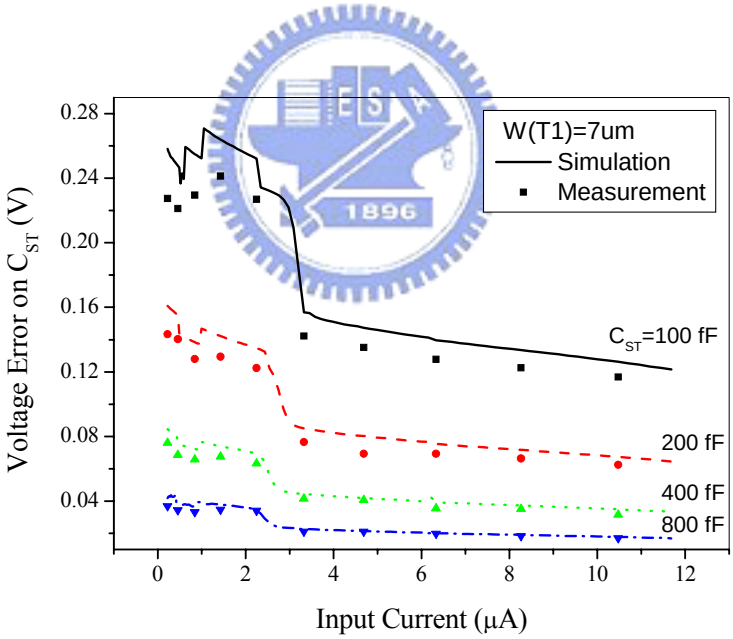


Fig. 5-15. Voltage error at node B in proposed SI memory with different capacitance.

The conventional SI memory is also implemented with poly-Si TFT process for the comparison of the influence of charge injection with proposed SI memory. The critical gate voltage error at node B for each SI memory was measured in the same

testing condition. Noticeable charge injection casued voltage error can be seen in measurement reults of the conventional SI memory, as shown in Fig. 5-16. The voltage error in the conventional SI memory is around 0.4 to 0.5 V when using a capacitor of 100 fF. By contrast, the voltage error in proposed SI memory with the same capacitance is of less than 0.25 V, almost one half smaller than that of the conventional SI memory. The capacitor of at least 400 fF is necessary to reduce the charge injection induced voltage error less than 0.2 V in the conventional SI memory, therefore, limits the response time of the SI memory.

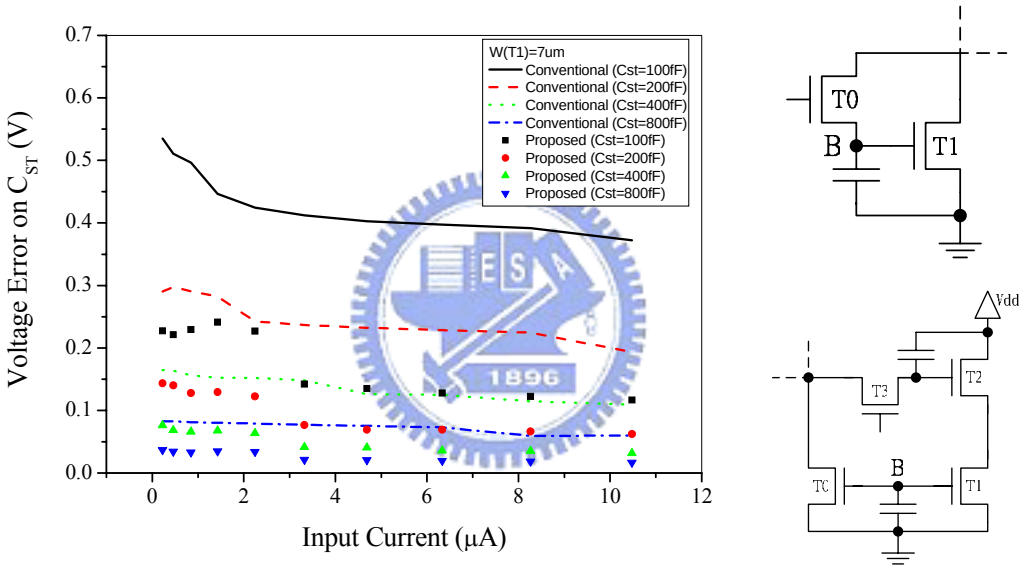


Fig. 5-16. Measured voltage error at node B in both conventional and proposed SI memories with W/L ratio of 7/5.

Critical gate voltage error of less than 0.1 V can be achieved by means of increasing the W/L ratio of T1 up to 30/5 in proposed SI memory with capacitance of 100 fF, as plotted in Fig. 5-17. However, the capacitance of conventional SI memory should be raised to 800 fF so as to accomplish the equivalent voltage error. The above data confirms that the proposed SI memory reveals outstanding resistance to the effect of charge injection even under the usage of the capacitance of 100 fF.

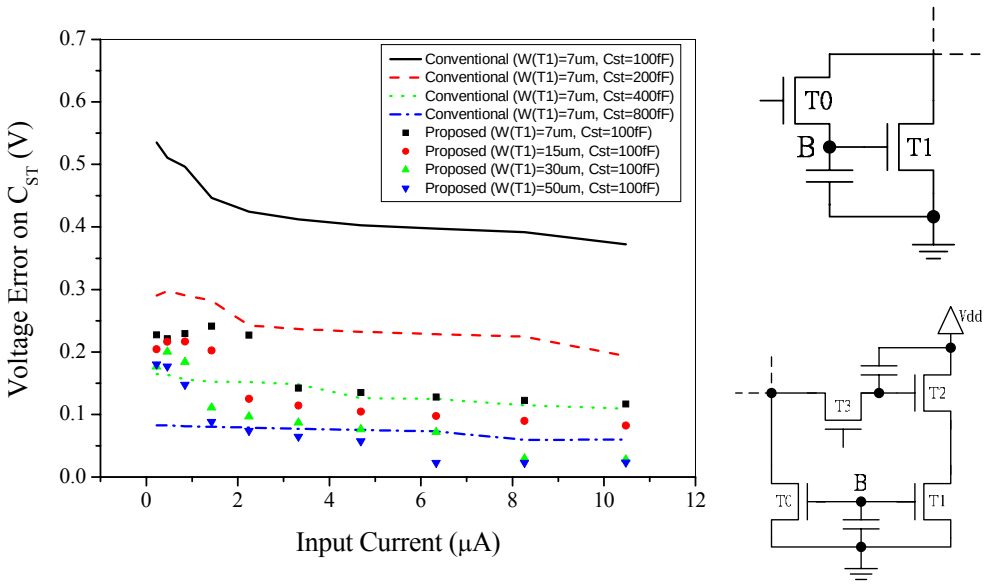


Fig. 5-17. Measured voltage error at node B in both conventional and proposed SI memories.

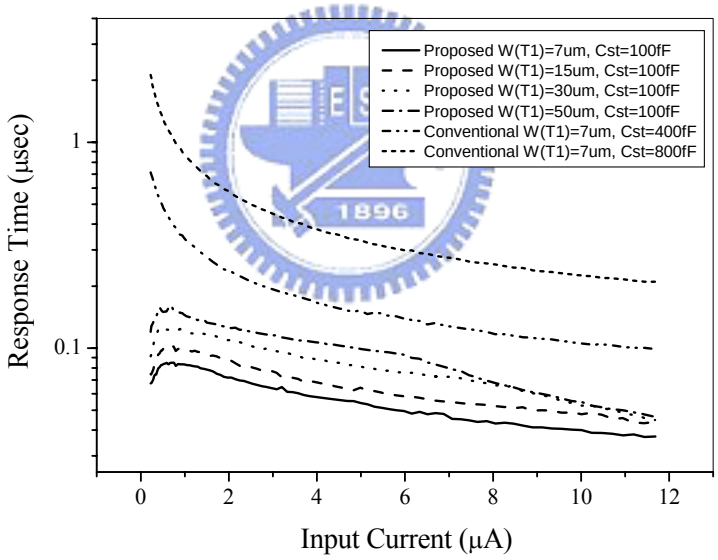


Fig. 5-18. Simulation results of response time of both SI memory.

The response time of both conventional and proposed SI memory is evaluated by SPICE program as the isolated critical gate node is difficult to detect directly, as revealed in Fig. 5-18. The response time of proposed SI memory with capacitance of 100 fF is lower than 0.16 μsas the width of T1 varies from 7 to 50 μm. The aforementioned results indicate that the capacitance of more than 400 fF is requisite

for the approximate voltage error in the conventional SI memory. Thus, the larger capacitance results in the response time of more than 0.7 μs, a factor of 4 times higher than that of proposed SI memory.

The experimental results of both conventional SI memory and proposed SI memory are summarized in Table 5-3. The large capacitance of 800 fF in conventional SI memory merely achieves the equivalent voltage error of 0.1 V as that of proposed SI memory with 100 fF capacitance and W/L ratio of 30/5, nevertheless, at the expense of a factor of 4 increase in the response time of proposed SI memory. However, the area consumption of the proposed SI memory is approximately 1.2 times larger that that of the conventional SI memory due to the usage of 5 TFTs and 2 capacitors. Besides, the power consumption of proposed SI memory is in a factor of three higher than that of conventional SI memory on account of the constant current conducted in T1 and T2 in proposed SI memory.

Table 5-3. Comparison of conventional and proposed SI memory with equivalent voltage error of 0.1 V.

	Conventional SI memory	Proposed SI memory
Required capacitance (fF)	800	100
W/L of T1 (μm/μm)	7/5	30/5
Response time (μsec)	> 0.7	0.13
Layout area (μm^2)	7500	9200
Power consumption at 15k Hz operating freqneucy (mW)	23	68

5.4.4 Digital-to-current converter

The most important part of the integrated current-type data driver is the

digital-to-current converter which is composed by a reference current generator and six proposed switch current memories connected in parallel for 6-bits gray scale of R, G, and B originals. To settle at the speeds required for high resolution applications, the reference currents must be settled to the SI memories in DCC within the time period associated with the maximum video sample signal. To achieve such speeds at low current levels, the proposed SI current memory is used to configure the DCC circuit. Each SI current memory is controlled by 1-bit digital data signal from a voltage latch, the previous stage in integrated data driver. The operation of the DCC schematically shown in Fig. 5-19 is described as following.

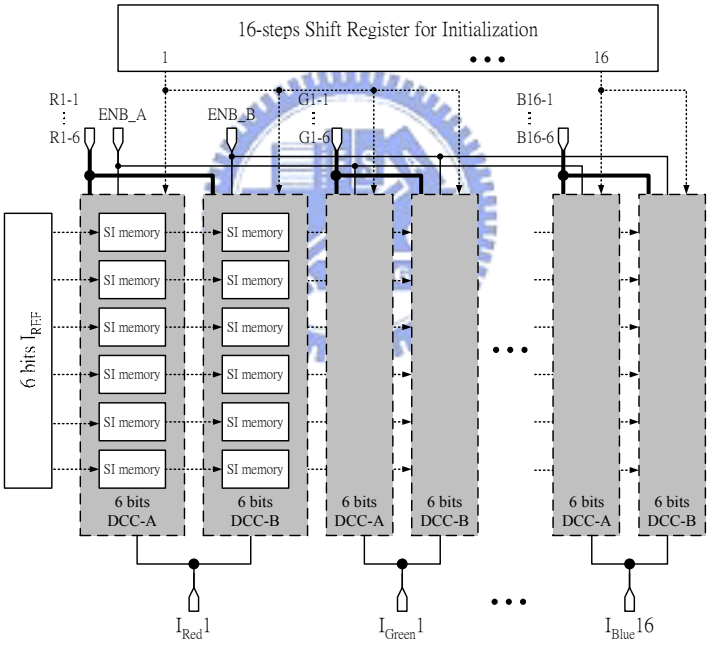


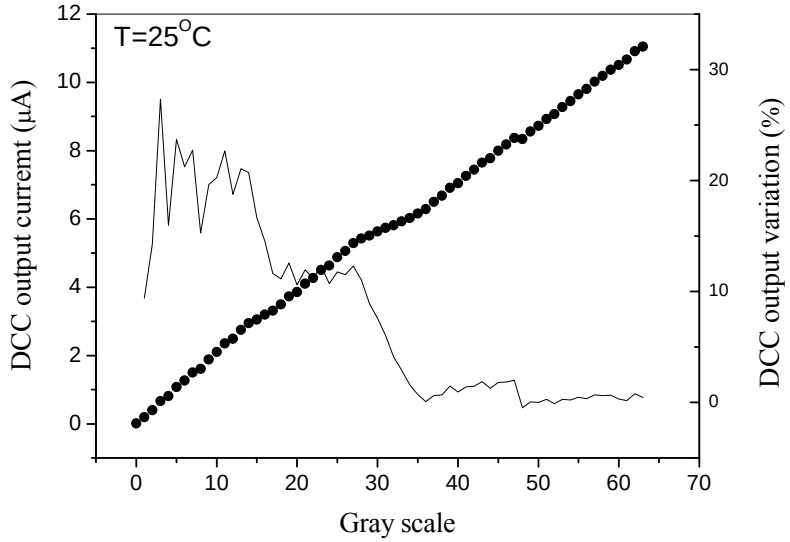
Fig. 5-19. Block diagram of digital-to-current converter.

Before converting the data, six SI memories in each DCC receive and memorize the binary weighted current signals of 2^0, 2^1, 2^2, … 2^5 times the reference current from the I_{REF} generator. The 6-bits voltage latch receives 6-bits digital display data signals from external application system then outputs the data to DCC. Each bit of digital display data of HIGH can activate the corresponding SI memory cell which already stored the

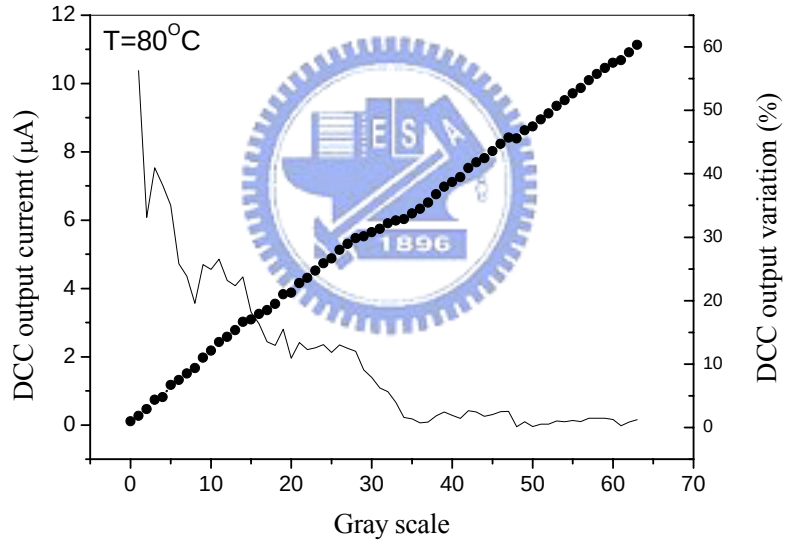
binary weighted current. The selected SI memories reproduce its stored current signals and in the event the total amount of output current of DCC is the sum of selected current signals. Therefore, the digital voltages have been converted to analog currents.

Two sets of DCCs (DCC-A and DCC-B) are used in the data driver to carry out the pipeline data processing. Because the DCC should be refreshed to memorize the reference currents after converting the data prior to the next data processing, the pipeline configuration of DCC is advantageous to accelerate the processing speed. While one set of DCCs, e.g. DCC-A, is converting the input data signals, the other set, DCC-B, can simultaneously export the converted analog current to the next stage of the circuit in data driver. These two different operations for each set of DCCs are performed alternately every scan period.

The test keys of digital-to-current converter have experimentally fabricated by the poly-Si TFT technology. Its measured output characteristics at room temperature and 80ºC are shown in Fig. 5-20. The output current value of the DCC increases from 0 to 11 μA as the value of gray-scale increases, which indicates 6-bits monotony for the output current. The output current deviations were calculated according to the original design values where the current step is 0.18 μA (11 μA divided by 64 gray scales). The output current deviation is higher than 10% when the DCC was operating in a low gray scale region and as the gray scale increases, the deviation can be reduced. The higher deviation at a low gray scale is due to the device geometric size mismatch. Since the equivalent TFT width for a least significant bit (LSB) in I_{REF} generator is relatively smaller than that for other bits, the mismatch can significantly influence the output current.



(a)



(b)

Fig. 5-20. Measured output current of DCC and its variation are as a function of digital gray scale signals at (a) 25ºC and (b) 80ºC.

Nevertheless, the equivalent TFT sizes for other bits in I_{REF} generator are larger so that the DCC is immune to the output current variation in a high gray scale region. As the operating temperature increases, the output current associated with gray scales still shows a good linearity. However, the current deviation in a low gray scale region is

higher than 50%. It is expected that an increase the field-effect mobility as a result of high device temperature can lead to a serious sensitivity to the device size mismatch.

5.5 Design verification

The complete operation of this integrated current driving system was verified after depositing OLED materials onto a substrate fabricated by poly-Si TFT technology. The photograph of a 2.2 inch TFT substrate with QCIF+ resolution (176 x RGB x 220) is shown in Fig. 5-21.

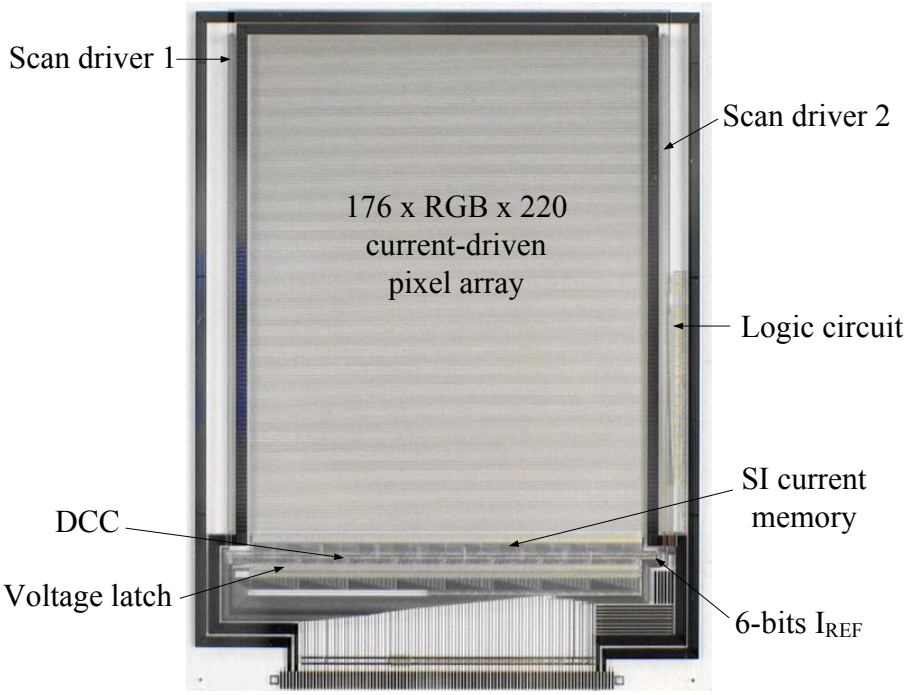


Fig. 5-21. Photograph of glass substrate with integrated data and scan drivers and current-driven pixel array.

A high work function ITO electrode was deposited onto the substrate as an anode contact for OLED. Since available states of OLED materials are less than 5 eV, a thin layer of copper phthalocyanine (CuPc) was used to facilitate the injection of holes by presenting a low energy barrier. Next, a layer of naphtha-phenyl-benzidene (NPB)

was deposited to form a hole transporting layer (HTL). An emitting layer followed, often consisting of tris-(8-hydroxyquiniline) aluminum (Alq_3) doped with a fluorescent dye such as Coumarin 540 for generating R. G. and B three primary colors. For patterning the emitting layer, a shadows mask was required to assist in depositing the R, G, B materials onto the corresponding pixel areas. An additional layer of Alq_3 serving as the electron transporting layer (ETL) was deposited in sequence. Finally, low-work-function cathode metal completed the thin film stack as an electron injector.

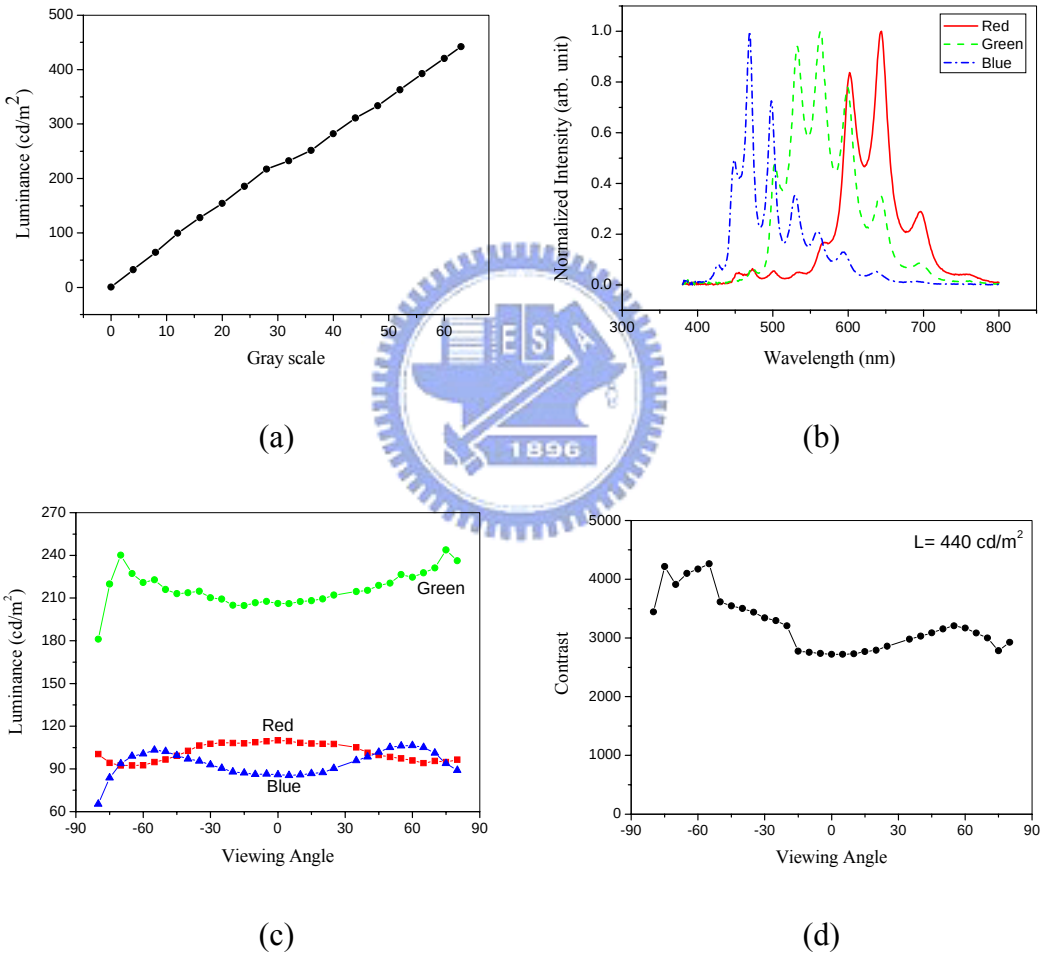


Fig. 5-22. Optical performance of fabricated current-driven AM-OLED. (a) Display luminance as a function of gray scales. (b) Display spectral response. (c) Display luminance versus viewing angle. (d) Display contrast ratio as a function of viewing angle.

To verify the optical performance, the AM-OLED was configured in the QCIF+ resolution and 60 Hz frame rate. The pattern is an all-white flat field. The luminance

of the OLED, recorded by a GmbH Conoscope providing direct readout, varies linearly with input digital signals as seen in Fig. 5-22(a). The peak brightness of 440 cd/m^2 can be achieved under operation voltage less than 15 volts. The spectral response shown in Fig. 5-22(b), reveals a color gamut that is adequate for general display applications. The luminance and contrast ratio versus the viewing angle are shown in Figs. 5-22(c) and 5-22(d). Exactly as a self-emission device, the AM-OLED display possesses a remarkably wide viewing angle as well as a superior contrast ratio of higher than 2500 in dark environment.

Fig. 5-23. A color photograph taken directly from the current-driven AM-OLED display panel.

Operation of the entire current-driven AM-OLED has been verified through successful performance in an actual display application as shown in Fig. 5-23. Besides, pixel to pixel luminance variation is almost invisible in this display so that the proposed integrated current-driven circuits including pixel and drivers are capable of achieving an extremely uniform luminance. Specifications of this AM-OLED are

summarized in Table 5-4.

Table 5- 4. AM-OLED display specifications.

Display size	2.2 inch diagonal
Resolution	QCIF+, 176xRGBx220
Pixel pitch	198μm x 198μm
Gray scale	6 bits
Input data	Digital RGB signals
Peak luminance	> 400 cd/m^2
CIE coordinate	R (0.591, 0.364) G (0.412, 0.542) B (0.204, 0.272)
Contrast ratio	> 2500:1 in dark

5.6 Summary

Design and implementation of current driven AM-OLED with fully integrated data drivers are described and the measurement results of such the panel fabricated with poly-Si TFT technology are presented. In the integrated current type driving system, the SI memory operates with only one control signal and has a capability to improve the output current accuracy by suppressing the influence of charge injection. Moreover, fast response time is achieved by the capacitance of small size without sacrificing the output accuracy. The features, such as fast response time and high accuracy of output current, favor the applications of the proposed SI memory in driver circuits of current driving active-matrix OLED panels. The digital-to-current converter with the new-designed SI memory is capable of generating desired analog current signals for current-driven pixel circuit regardless of the operation temperature and device aging. The expensive current-type driver ICs are no longer needed due to the fully integrated data drivers which can also provide a digital interface to increase

the design flexibility. The measured display performance shows that the current-driven AM-OLED is superior in high uniformity of display luminance to meet the requirements of high performance display applications.

Reference

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Chapter 6

Current-Scaling Pixel Electrode Circuit for AM-OLED

6.1 Introduction

To modulate the OLED current, two approaches have been often used. In the first approach, a voltage signal is used to directly control the driving current of two-TFT pixel electrode circuit. Unfortunately, in this pixel configuration, non-negligible TFT characteristic variations (threshold voltage and field-effect mobility shifts) due to the manufacturing process variation and to the device aging can result in non-uniform luminance over the display area. Current driving schemes with four-TFT pixel electrode circuit has been demonstrated in previous chapter as another approach to drive AM-OLED, whereby the current signal provided by external driver modulates directly the pixel electrode circuits. The four-TFT circuits can not only provide a continuous excitation to OLED, but at the same time can also compensate for the TFT threshold voltage variation.

Although the current driving scheme improves the display luminance uniformity, a large timing delay can be observed at a low data current that is due to combination of a high OLED efficiency and charging of a large interconnect parasitic capacitances. For example, a current of 70 nA is sufficient to achieve luminance of 100 cd/m^2 when an OLED with efficiency of 20 cd/A or higher is used. However, for such small current, an interconnect parasitic capacitance of about 10 pF needs more than 150 μsec to build up a sufficient voltage level. This charging time is much larger than 30 μsec, that is needed for a display with VGA (640 x RGB x 480) resolution

operated at 60 Hz. To reduce the programming time delay, the pixel electrode circuits based on an adjustable TFTs geometric ratio with the current scaling function have been proposed [1][2]. One example of such circuit is current mirror type pixel electrode circuit, as shown in Fig. 6-1(a), where a high data-to-OLED-current ratio can only be achieved for a large geometric ratio of T4 to T3, yet, significantly limit the pixel electrode aperture ratio. A possible solution to this problem is top emission OLED structure in which a nearly entire pixel area can be used as light-emitting region [3]. In general, the pixel aperture ratio should not be influenced by the size of TFT and the complexity of pixel electrode circuit. This is especially true for high resolution displays.

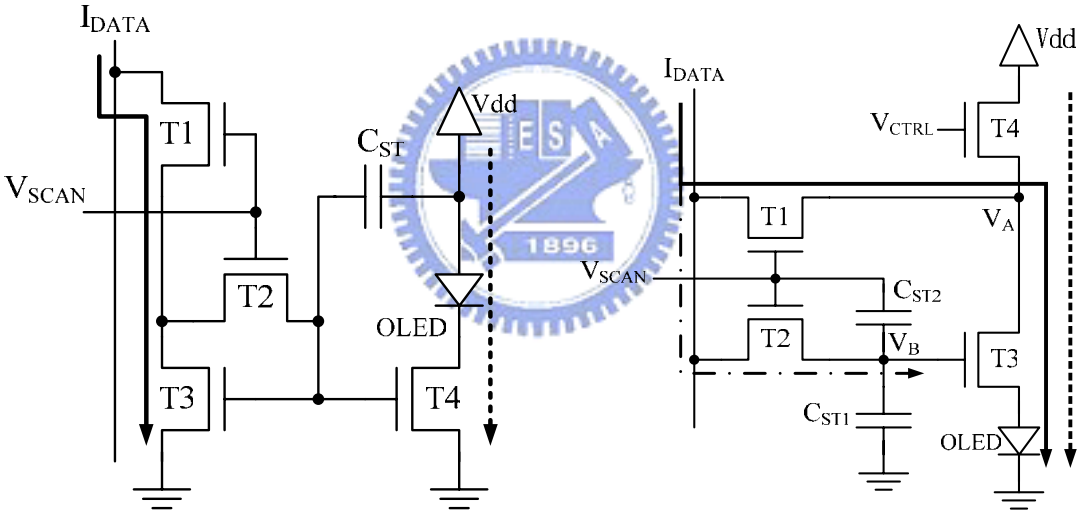


Fig. 6-1. Schematic diagrams of current driven pixel circuits with (a) conventional current mirror and (b) cascade structure of storage capacitors.

In this dissertation, we present an improved current driven pixel circuit based on poly-Si TFT technology with the current scaling function. A cascade structure of storage capacitors is proposed here to achieve a high data-to-OLED-current ratio without increasing TFTs size in comparison to conventional current mirror pixel circuit, shown in Fig. 6-1(a). The proposed pixel electrode circuit can also compensate

for poly-Si TFT threshold voltage variation so that uniform display luminance can be expected. First we describe the structure and discuss the operation principles of pixel electrode circuit. The parameters used for circuit simulation are discussed in Section III. The simulation results and circuit performance are discussed in Section IV, with conclusion presented in Section V.

6.2 Proposed pixel electrode circuit

The proposed current driven pixel electrode circuit consists of three switching TFTs (T1, T2, T4), one driving TFT (T3) and two storage capacitors (C_{ST1}, C_{ST2}) connected between a scan line and ground with a cascade structure, as shown in Fig. 6-1(b). The operation of the circuit is controlled by four external terminals: V_{SCAN}, V_{CTRL}, I_{DATA} and ground. The signals of V_{SCAN}, V_{CTRL}, and I_{DATA} are supplied by external drivers while the cathode of OLED is grounded. It should be noticed that to simplify the circuit analysis, one node of C_{ST1} connected to the ground is adopted. In practice, the ground electrode of C_{ST1} can be connected to the Vdd line in order to reduce number of lines. The operation of this pixel electrode circuit is described as follow:

During the ON-state, the scan line signal V_{SCAN} turns on the switching transistors T1 and T2. During this period, a data current signal I_{DATA} passes through T1 and T3 to OLED, shown as the solid line in Fig. 6-1(b), and sets the voltage at the T3 drain electrode (nodes A). At the same time, the voltage at the T3 gate electrode (node B) is set by I_{DATA} passing through T2 (dash line). The control signal V_{CTRL} turns T4 off to ensure that no current flows through T4. Consequently, the ideal OLED current in ON-state should be equivalent to I_{DATA}. Since the T3 drain and gate electrodes are at the same potential, T3 will operate in the deep saturation region, e.g., $V_{DS} > V_{GS}-V_{TH}$

(threshold voltage) and the V_A and V_B voltages at both nodes are determined automatically according to Eq. 6-1.

$$I_{DATA} = \frac{1}{2} \cdot \mu_{FE} \cdot C_{OX} \cdot \frac{W_3}{L_3} \cdot (V_{GS} - V_{TH})^2 \qquad \text{Eq. 6-1}$$

where μ_{FE}, C_{OX}, W_3 and L_3 are field-effect mobility, oxide capacitance, width and length of TFT(T3), respectively. If T3 threshold voltage changes and if this change is not higher than V_{SCAN} amplitude, the T3 gate voltage, $V_{B\text{-}ON}$, will be adjusted accordingly to ensure the identical I_{DATA} in ON-state. Therefore, $V_{B\text{-}ON}$ is always adjusted to keep I_{DATA} at about the same value regardless of poly-Si TFT threshold voltage. The $V_{B\text{-}ON}$ will also be stored in both C_{ST1} and C_{ST2} and the voltage across C_{ST2} is V_{SCAN}-$V_{B\text{-}ON}$.

When the pixel changes from ON- to OFF-state, V_{SCAN} turns off T1 and T2 and V_{CTRL} simultaneously turns on T4. Because C_{ST2} is connected between the scan line and the node B to form a cascade structure with C_{ST1}, V_{SCAN} change from high to ground state will reduce $V_{B\text{-}ON}$ to $V_{B\text{-}OFF}$ due to the feed-through effect of the capacitors. $V_{B\text{-}OFF}$ can be derived from the charge conversation theory, and is given by Eq. 6-2, in which ΔV_{SCAN} and $C_{OV\text{-}T2}$ are an amplitude of V_{SCAN} (=$V_{SCAN\text{-}ON}$ − $V_{SCAN\text{-}OFF}$) and the overlap capacitance of T2, respectively.

$$V_{B-OFF} = V_{B-ON} - \Delta V_{SCAN} \cdot \frac{C_{ST2} \parallel C_{OV-T2}}{C_{ST1} + C_{ST2} \parallel C_{OV-T2}} \qquad \text{Eq. 6-2}$$

A reduced T3 gate voltage, $V_{B\text{-}OFF}$, will be hold in C_{ST1} and C_{ST2} and it continuously will turn on T3 during this period. Since the overdrive voltage of T4 (=V_{CTRL}-V_A-V_{TH}) is lower than Vdd-V_A, the T4 is working in saturation region. In order to ensure that the V_A is similar to Vdd and the T3 is operating in the deep saturation region, the width of T4 should be large enough to reduce the turn-on resistance of T4. A current smaller than I_{DATA} , shown as the dash line in Fig. 6-1(b), will be generated by $V_{B\text{-}OFF}$

and will pass through T4 and T3 to OLED. Consequently, the OLED current in OFF-state, $I_{OLED\text{-}OFF}$, will be smaller than I_{DATA}.

Since the T3 gate voltage decreases from $V_{B\text{-}ON}$ to $V_{B\text{-}OFF}$, the OLED driving current is scale-down from ON- to OFF-state by the storage capacitor cascade structure. The quantity of voltage drop, shown as $\Delta V_{SCAN} \cdot C_{ST2}/(C_{ST1}+C_{ST2})$ in

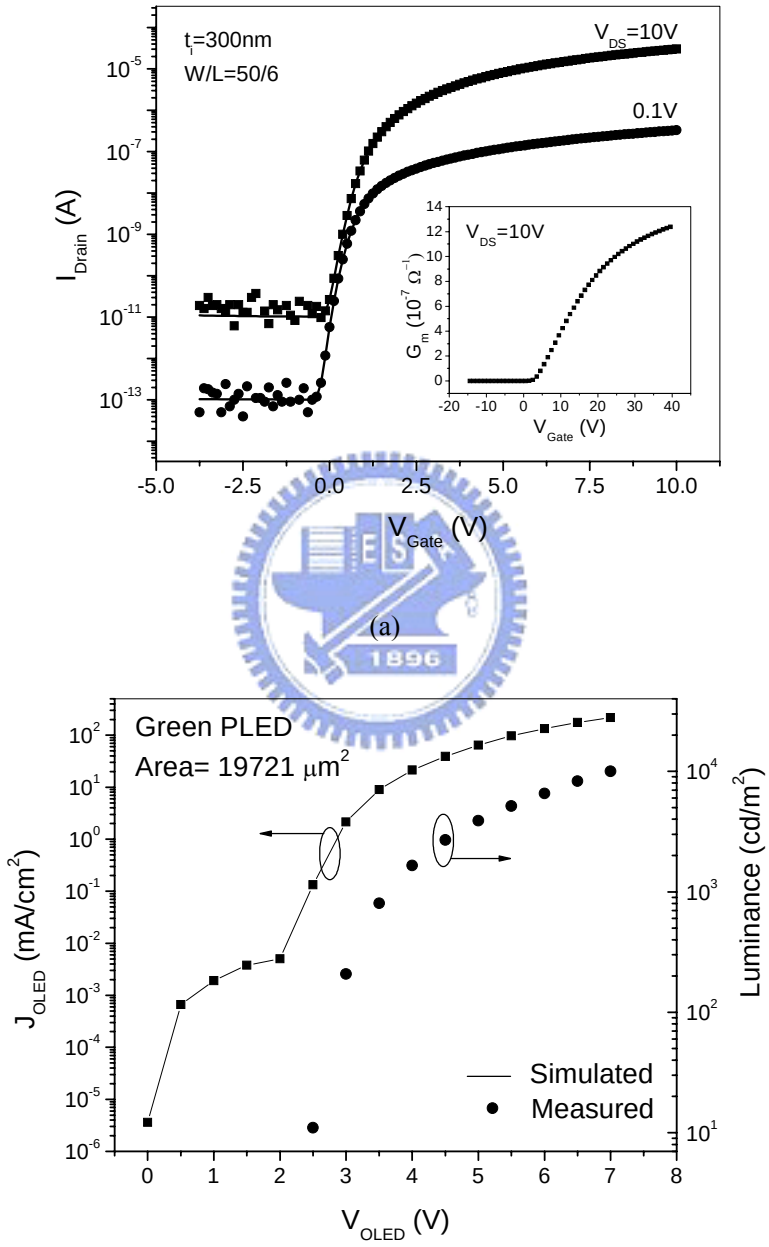
$$V_{B-OFF} = V_{B-ON} - \Delta V_{SCAN} \cdot \frac{C_{ST2} \parallel C_{OV-T2}}{C_{ST1} + C_{ST2} \parallel C_{OV-T2}} \qquad \text{Eq. 6-2,}$$

will increase with increasing ΔV_{SCAN} and C_{ST2} values and will lead to a smaller $I_{OLED\text{-}OFF}$. In other words, the scale-down ratio, $R_{SCALE}=I_{OLED\text{-}ON}/I_{OLED\text{-}OFF}$, is related to both the size of C_{ST2} and to ΔV_{SCAN}. Therefore it is expected that a larger C_{ST2} will result in larger R_{SCALE}. Consequently, when a very large data current I_{DATA} is used to charge the pixel electrode and to shorten the pixel programming time, at the same time, a smaller driving current $I_{OLED\text{-}OFF}$ can be achieved for lower gray scales.

6.3 Parameter extraction and pixel electrode circuit design

Synopsis H-SPICE simulation tool with the Rensselaer Polytechnic Institute (RPI) Troy, NY, poly-Si TFT model [4][5] was used to evaluate the proposed pixel electrode circuit. The poly-Si TFT parameters developed within our group were used in this simulation [6][7]. The transfer characteristics (I_D-V_{GS}, drain current versus gate-to-source voltage) of poly-Si TFT are shown in Fig. 6-2 and its transconductance is given in the insert. To simulate the behavior of OLED the conventional semiconductor diode model, with the parameters extracted for organic polymer light-emitting device (PLED) fabricated in our laboratory, was used. The opto-properties of PLED are shown in Fig. 6-2 and were described elsewhere [8]. In the pixel design, a C_{ST1} with the fixed size of 2.5 pF was used and C_{ST2} size was

varied from 210 to 625 fF to achieve different C_{ST2}/C_{ST1} ratios. Since T2 works as a switch in this circuit, its size can be smaller in comparison with other TFTs. Based on our own experience, we conclude that a high-performance poly-Si TFT with μ_{FE} higher than 1.5 cm^2/V-sec is essential for future poly-Si TFT pixel electrode circuit.



(b)

Fig. 6-2. (a) Transfer characteristics of poly-Si TFT. The transconductance versus gate voltage is shown in insert. (b) An example of measured PLED current density and brightness variation with supplied voltages.

The poly-Si TFT with lower μ_{FE} will need a higher driving voltage and larger geometric size to achieve an adequate OLED driving current level. Then, increased display power consumption and reduced pixel aperture ratio, when light is emitted through the substrate, are expected. In addition, it is expected that a higher performance TFT will have better electrical stability over the time. The poly-Si TFTs and OLED parameters used for this pixel electrode circuit simulation are given in Table 6-1. The parameters used in pixel circuit simulation..

Table 6-1. The parameters used in pixel circuit simulation.

Device parameters for TFT	
W/L (T_1, T_3, T_4) (μm)	150/6
W/L (T_2) (μm)	50/6
V_{TH} (V)	2
μ_{FE} (cm^2/V-sec)	1.9
C_{OV} (nF/m)	0.2
I_{OFF} (pA)	0.1
C_{ST1} (pF)	2.5
C_{ST2} (fF)	210~625
Device parameters for OLED	
n	31
R_S (Ω)	20
I_S (A)	8×10^{-5}
C_{OLED} (pF)	3
Supplied signals	
V_{SCAN} (V)	0~35
V_{CTRL} (V)	0~35
Vdd (V)	35
I_{DATA} (μA)	0~5
Times (mSec)	
t_{ON}	0.33
t_{OFF}	33

6.4 Simulation results and discussion

6.4.1 Current scaling ratio

Since $I_{OLED\text{-}ON}$ (=I_{DATA}) is larger than $I_{OLED\text{-}OFF}$ by a factor of R_{SCALE}, the average OLED current (I_{AVG}) for the pixel electrode circuit must be properly defined:

$$I_{AVG} = \frac{I_{OLED-ON} \cdot t_{ON} + I_{OLED-OFF} \cdot t_{OFF}}{t_{ON} + t_{OFF}} \qquad \text{Eq. 6-3}$$

Where t_{ON} and t_{OFF} denote the select and deselect periods during the frame time, respectively.

Since the $I_{OLED\text{-}ON}$=$I_{OLED\text{-}OFF}$·R_{SCALE}, Eq. 3 can be written as:

$$I_{AVG} = I_{OLED-OFF} \cdot \left[\frac{R_{SCALE} \cdot t_{ON} + t_{OFF}}{t_{ON} + t_{OFF}} \right] \qquad \text{Eq. 6-4}$$

From this equation, an accurate I_{AVG} can be calculated for various combinations of $I_{OLED\text{-}OFF}$ and R_{SCALE} to satisfy the display requirements for different gray scales. In order to display low gray scales, not only a low $I_{OLED\text{-}OFF}$ but also a high $I_{OLED\text{-}ON}$ is needed to control both a low display luminance and a fast programming speed at the same time. Combination of a low $I_{OLED\text{-}OFF}$ and a large R_{SCALE} can be used to satisfy such this display requirement. For higher gray scales, a high $I_{OLED\text{-}ON}$ is not needed since a high $I_{OLED\text{-}OFF}$ can be achieved. Therefore, a combination of a large $I_{OLED\text{-}OFF}$ and a low R_{SCALE} is appropriate to display high gray scales.

Since the scale-down ratio (R_{SCALE}=$I_{OLED\text{-}ON}$/$I_{OLED\text{-}OFF}$) will affect the performance of the proposed pixel electrode circuit, it is important to evaluate its evolution with the I_{DATA} (=$I_{OLED\text{-}ON}$) and C_{ST2}/C_{ST1}. The variation of R_{SCALE} as a function of I_{DATA} is shown in Fig. 6-3(a), where we can conclude that when C_{ST2}/C_{ST1}=1/12, R_{SCALE} decreases from 210 to 1.5 as I_{DATA} increases from 0.1 to 10 μA. In this specific case, since $V_{B\text{-}ON}$ at a high gray scale is larger than that at a low gray scale, it is expected that a large I_{DATA} will pass through T3. And a fixed voltage

drop induced by $\Delta V_{SCAN} \cdot C_{ST2}/(C_{ST1}+C_{ST2})$ is relatively small in comparison to $V_{B\text{-}ON}$, hence data current drop is expected to be small.

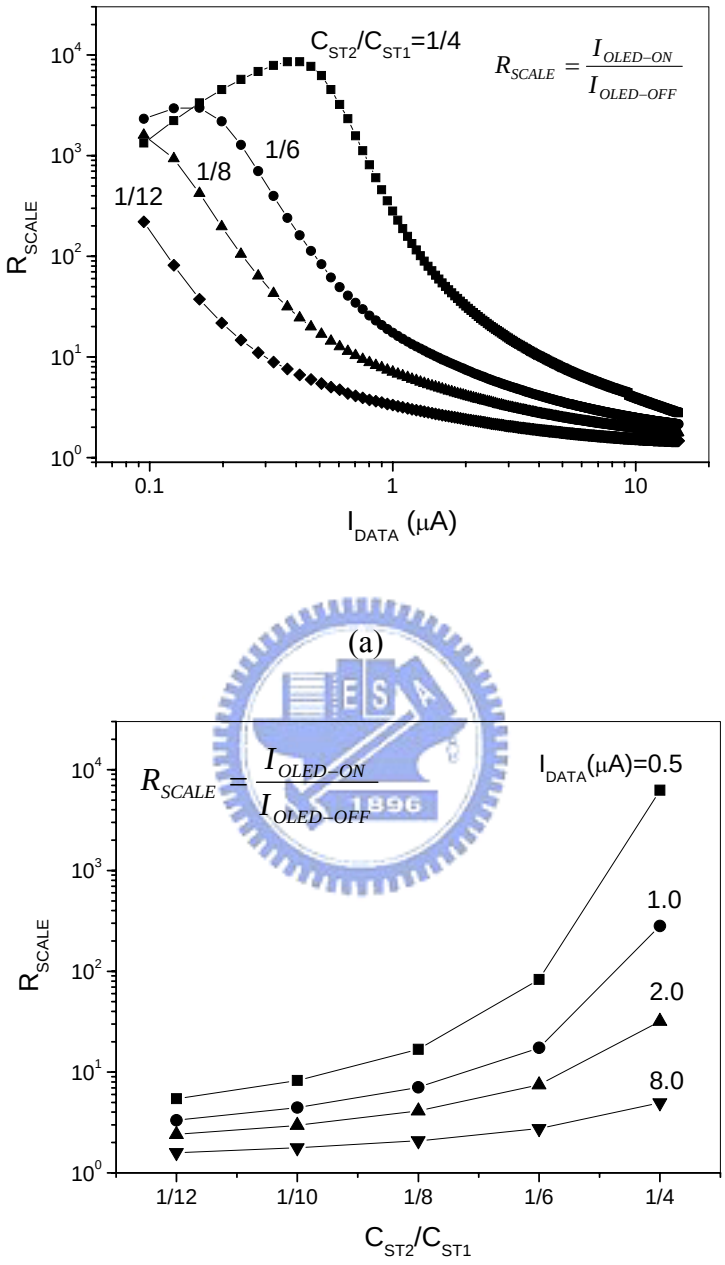


Fig. 6-3. Variation of the scale-down ratio versus (a) data current and (b) ratio of storage capacitances.

In the other words, a fixed voltage drop can dramatically affect $V_{B\text{-}ON}$ at low gray scales where $V_{B\text{-}ON}$ is small. Therefore, a desirable high R_{SCALE} at low gray scales and

a low R_{SCALE} at high gray scales can be achieved by proposed pixel electrode circuit. The variation of R_{SCALE} with the C_{ST2}/C_{ST1} is as shown in Fig. 6-3 (b); which was derived from Fig. 6-3 (a). It should be mentioned that in Eq. 6-2, a large C_{ST2}/C_{ST1} ratio can induce a large V_B offset between pixel ON- and OFF-state. Consequently, V_B decrease will result in the scale-down of the data current and in a high R_{SCALE}. The simulation results show that when I_{DATA} is fixed, R_{SCALE} increases when C_{ST2} increases from 210 to 625 fF, corresponding to an increase of C_{ST2}/C_{ST1} from 1/12 to 1/4. Fig. 6-3(b) also demonstrates that when a smaller I_{DATA} is used, a higher R_{SCALE} can be achieved with the constant C_{ST2}/C_{ST1}.

The current-scaling function is performed so that the large programming current can be reduced to an appropriate value when the pixel operates from the ON- to the OFF-state. In ON-state, the $I_{OLED\text{-}ON}$ (=I_{DATA}) are identical in not only the conventional but also the proposed pixel electrode circuits because the external driver directly controls the current, as shown in Fig. 6-4(a). When pixels work in OFF-state, the proposed pixel circuit reveals superior current-scaling ability in comparison with the conventional current-driven pixel electrode circuit which just ideally keeps the $I_{OLED\text{-}OFF}$ equivalent to $I_{OLED\text{-}ON}$, as shown in Fig. 6-4(b). It should be noticed that the $I_{OLED\text{-}OFF}$ versus I_{DATA} of the conventional pixel circuit changes from linear to curved behavior due to the charge injection phenomenon. This charge injection can occur when the gate voltage is removed, and when the charge carriers in the T2 channel are released and redistributed into the drain and source electrodes. The carrier redistribution will alter the voltages at both nodes. Therefore, the charge injection from T2 causes the $I_{OLED\text{-}OFF}$ slightly deviating from $I_{OLED\text{-}ON}$.

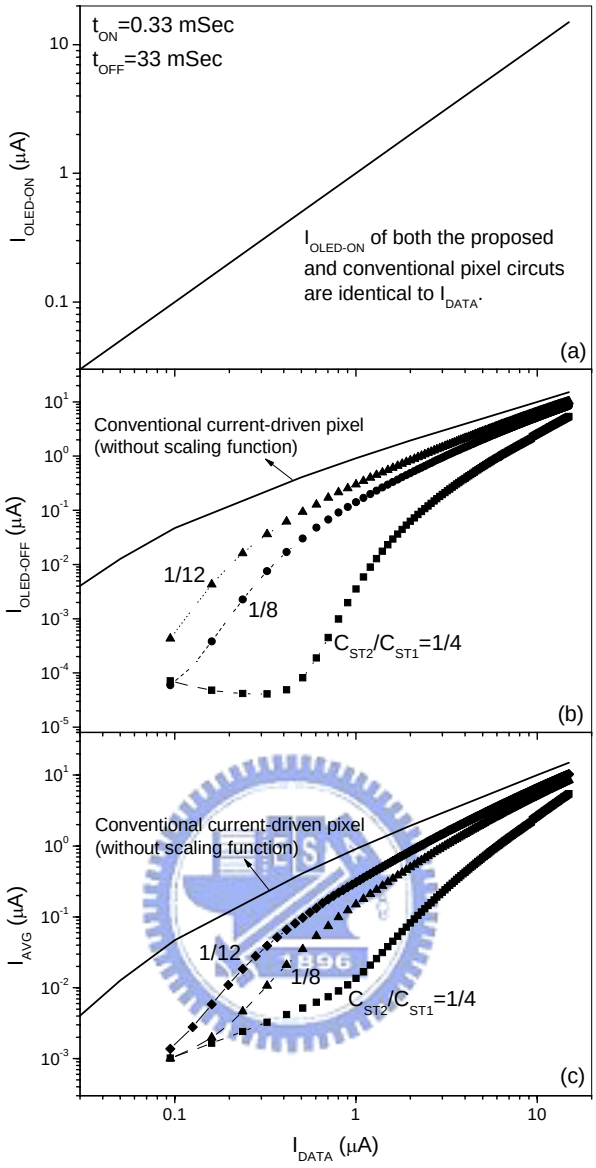


Fig. 6-4. Variation of the $I_{OLED\text{-}ON}$, $I_{OLED\text{-}OFF}$ and I_{AVG} during one frame period versus I_{DATA} (=$I_{OLED\text{-}ON}$) at various C_{ST2}/C_{ST1} ratio.

From Fig. 6-4(b), it is obvious that the large C_{ST2}/C_{ST1} results in significant decrease of the $I_{OLED\text{-}OFF}$. Moreover, since the OFF-state period is much longer than ON-state, the small $I_{OLED\text{-}OFF}$ in OFF-state can further reduce the I_{AVG} even if the $I_{OLED\text{-}ON}$ is large. Using Eq. 6-3, the plots of I_{AVG} versus I_{DATA} (=$I_{OLED\text{-}ON}$) in one frame period (t_{ON} + t_{OFF}) with C_{ST2}/C_{ST1} ratios as a parameter are shown in Fig. 6-4(c). For example, the proposed pixel electrode circuit can generate I_{AVG} ranging from 1 nA

to 5 μA with I_{DATA} ranging from 0.1 to 10 μA. By contrast, the I_{AVG} of conventional pixel electrode circuit is almost equal to I_{DATA}. In other words, a very small I_{AVG} can only be achieved by the I_{DATA} having a similar magnitude. From Fig. 6-4, it is evident that I_{DATA} larger than I_{AVG} can be used to program the proposed pixel circuit in ON-state without increasing the poly-Si TFTs geometric size. Hence using an additional C_{ST2} to form a cascade capacitors structure, a large R_{SCALE} can be achieved and a high I_{DATA} can be used to accelerate the pixel circuit programming in ON-state.

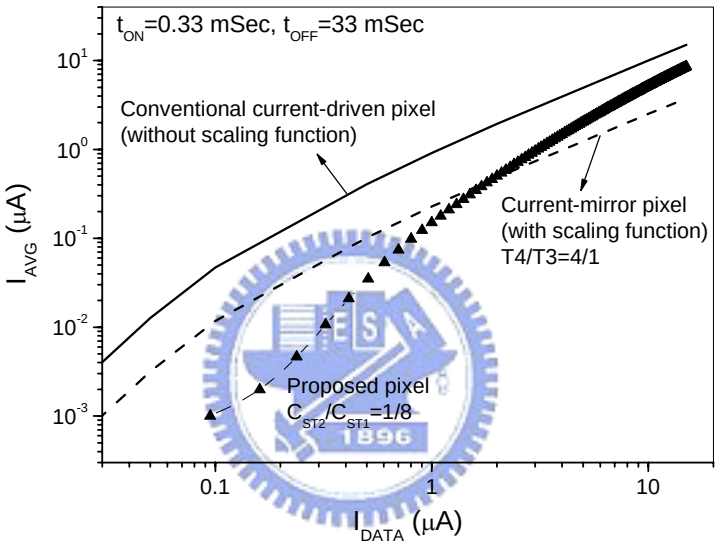


Fig. 6-5. Comparison of I_{AVG} as a function of I_{DATA} among conventional current-driven, current-mirror, and proposed pixels.

To demonstrate the proposed pixel electrode circuit outstanding current scaling function in comparison with both the conventional current-driven and current-mirror pixels, I_{AVG} as a function of I_{DATA} for each pixel electrode circuit was shown in Fig. 6-5. Although the current–mirror pixel is able to scale down I_{DATA}, the scale-down ratio R_{SCALE} is constant in the whole range of I_{DATA}. In current-mirror pixel, a large I_{DATA} for high gray scales will result in a high power consumption due to the fixed scale-down ratio. In addition, to achieve the current scaling function, a larger driving

TFT T4 needed in current-mirror pixel will substantially reduce the pixel electrode aperture ratio. From Fig. 6-5, we can conclude that with the I_{DATA} ranging from 0.1 to 10 μA, our proposed pixel circuit can achieve I_{AVG} ranging from 1 nA to 5 μA, which represents much wide range in comparison with the conventional current-driven pixel (0.05 to 10 μA) and the current-mirror pixel (0.01 to 2.5 μA). Therefore, the proposed pixel circuit can yield not only a high I_{DATA} and a high R_{SCALE} for the low gray scales, but also reasonable I_{DATA} for a high gray scale to avoid large display power consumption.

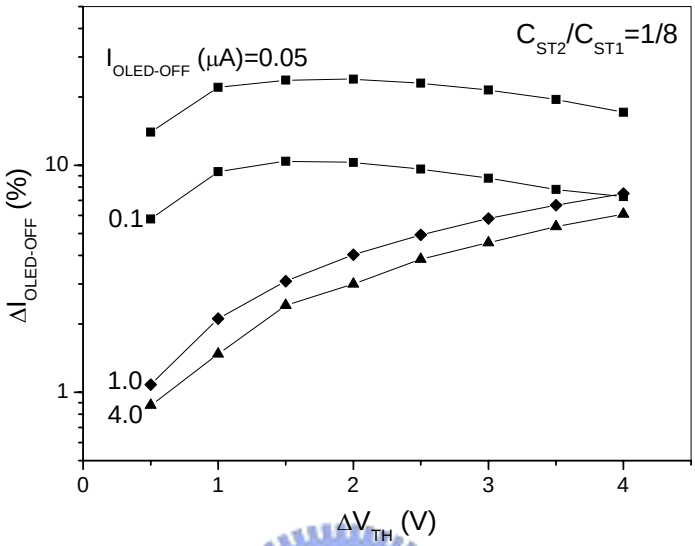
6.4.2 Influence of threshold voltage variation

To investigate the influence of V_{TH} variations of T3 and T4 on pixel circuit performance, various threshold voltage deviations (ΔV_{TH}=V_{TH}(after stress)-V_{TH}(initial)), based on the experimental results reported [7] have been used in pixel circuit simulation. Since the $I_{OLED\text{-}ON}$ (=I_{DATA}) is not affected by ΔV_{TH} and the $I_{OLED\text{-}OFF}$ is related to I_{AVG} through Eq. 6-4, the variation of $I_{OLED\text{-}OFF}$ with the TFT threshold voltage is used to estimate the influence of ΔV_{TH} on pixel circuit operation. For C_{ST2}/C_{ST1}=1/8, the variation of the $I_{OLED\text{-}OFF}$ with ΔV_{TH} can be calculated:

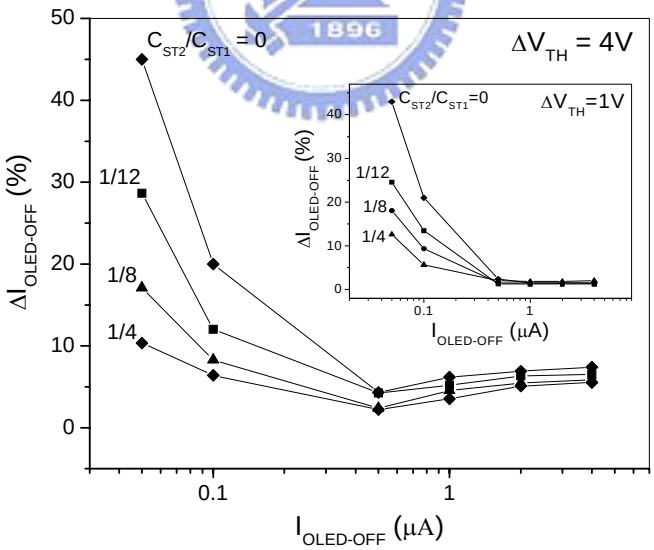
$$\Delta I_{OLED-OFF} = \frac{I_{OLED-OFF}(\Delta V_{TH}) - I_{OLED-OFF}(\Delta V_{TH}=0)}{I_{OLED-OFF}(\Delta V_{TH}=0)} \qquad \text{Eq. 6-5}$$

The variation of $\Delta I_{OLED\text{-}OFF}$ as a function of ΔV_{TH} is shown in Fig. 6-6(a). Following the increase of ΔV_{TH}, $\Delta I_{OLED\text{-}OFF}$ gradually increases from around 1 to 6% when $I_{OLED\text{-}OFF}$ is higher than 1.0 μA. The $\Delta I_{OLED\text{-}OFF}$ up to 6% at ΔV_{TH} of 4V can be reached. This is due to turn-on resistance of T4 and channel length modulation of T3. In ideal case, $I_{OLED\text{-}OFF}$ of T3 operating in saturation mode is independent of drain voltage V_A. However, in practice, the TFTs are impacted by the channel length modulation and the drain voltage variation can only slightly affect $I_{OLED\text{-}OFF}$. Since the

turn-on resistance of T4 changes with the ΔV_{TH} increase, the T3 can suffer a serious drain voltage offset ΔV_A between ON- and OFF-state so that the $I_{OLED\text{-}OFF}$ can be changed.



(a)



(b)

Fig. 6-6. (a)Variation of $\Delta I_{OLED\text{-}OFF}$ as function of TFT threshold voltage shift. (b) $\Delta I_{OLED\text{-}OFF}$ versus OLED current during display operation OFF-state for different C_{ST2}/C_{ST1} and ΔV_{TH}=4V. The data for ΔV_{TH}=1V is shown in insert.

In other words, an increase of $I_{OLED\text{-}OFF}$ with a high T4 turn-on resistance can lead to a decrease of V_A and consequently can result in a large $\Delta I_{OLED\text{-}OFF}$, Fig. 6-6(b). In order to suppress the effect of T4 ΔV_{TH}, a higher V_{CTRL} or T4 with a larger width can be used to reduce the turn-on resistance of T4. However, an additional voltage signal can increase the complexity of peripheral drivers and a larger T4 can slightly decrease the pixel aperture ratio for bottom light-emission OLED structure.

Substantial increase of $\Delta I_{OLED\text{-}OFF}$ when $I_{OLED\text{-}OFF}$ is lower than 100 nA is due to the influence of charge injection of switching T2 on $V_{B\text{-}ON}$. Since a small $V_{B\text{-}ON}$ will result from a low driving current $I_{OLED\text{-}ON}$ at low gray scales, the charge carrier released from T2, when T2 is turn-off, can reduce the $V_{B\text{-}ON}$. Therefore, $V_{B\text{-}ON}$ can be modified by not only a voltage drop induced by cascade structure of C_{ST1} and C_{ST2} but also by a charge injection from T2. In addition, the V_{TH} shift of all TFTs can lead to a higher sensitivity of $V_{B\text{-}ON}$ to the charge injection from T2. Therefore, large storage capacitor is needed to eliminate the effect of T2 charge injection. As shown in Fig. 6-6(b), when large C_{ST2}/C_{ST1} is used, a significant reduction of $\Delta I_{OLED\text{-}OFF}$ at low gray scales is observed in comparison to C_{ST2}/C_{ST1}=0. From our data shown in Fig. 6-4(b) and Fig. 6-6(b), we can conclude that a large C_{ST2}/C_{ST1} can achieve a high R_{SCALE} as well as a small $\Delta I_{OLED\text{-}OFF}$.

6.4.3 Effects of device spatial mismatch and temperature

Mismatch of TFT geometric size and its operating temperature can affect the stability of scale-down ratio R_{SCALE}. The TFT size mismatch usually can result from device fabrication processes such as over-etching and alignment errors. The heat generated by non-emissive recombination of electron and hole in OLED can also increase substrate temperature, thus, alter the electrical performance of TFTs.

According to Eq. 6-1 and Eq. 6-2, the OLED current in OFF-state can be given as:

$$I_{OLED-OFF} = \beta(V_{GS} - V_{TH} - V_{offset})^2 = \beta\left(\sqrt{\frac{I_{OLED-ON}}{\beta}} - V_{offset}\right)^2 \quad \text{Eq. 6-6}$$

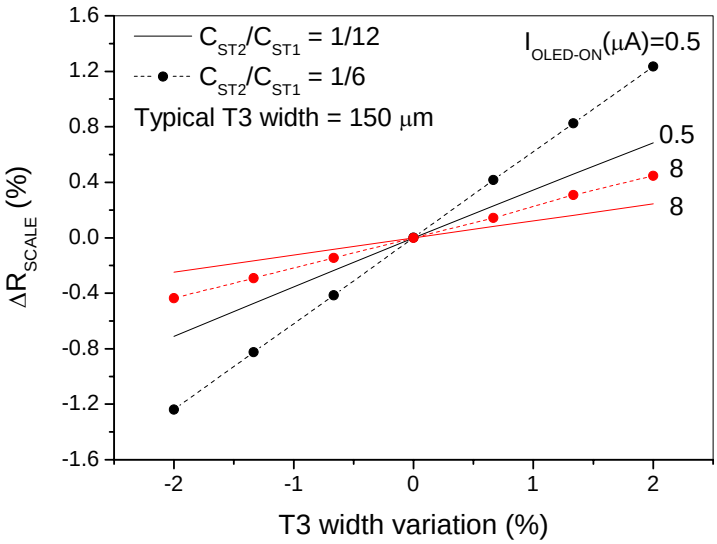
where $\beta = \frac{1}{2}\mu_{FE}C_{OX}\frac{W_3}{L_3}$, $V_{offset} = \Delta V_{SCAN}\frac{C_{ST2} \parallel C_{OV-T2}}{C_{ST1} + C_{ST2} \parallel C_{OV-T2}}$.

Eq. 6-6 can be re-written as

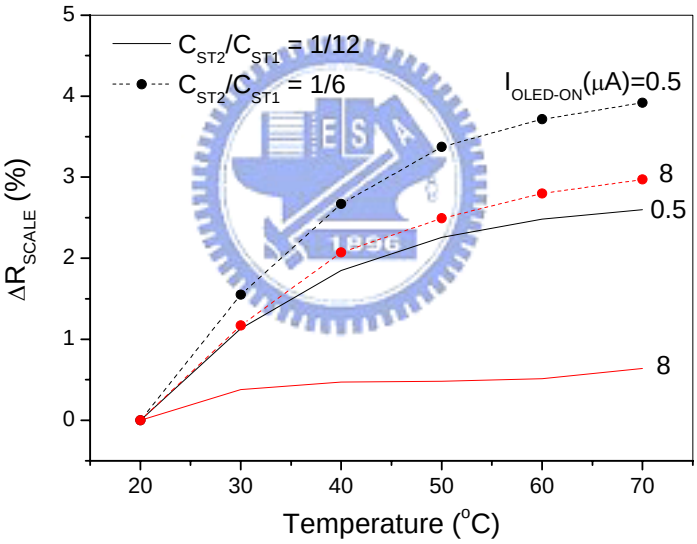
$$I_{OLED-OFF} = I_{OLED-ON} - 2\sqrt{\beta \cdot I_{OLED-ON}} \cdot V_{offset} + \beta \cdot V_{offset}^2 \quad \text{Eq. 6-7}$$

It should be noted that β in the second and third terms of Eq. 6-7 is temperature and mismatch sensitive, hence the $I_{OLED-OFF}$ will be influenced by temperature, resulting in variation of R_{SCALE}. Fig. 8(a) shows the variation of R_{SCALE} with T3 size (W_3/L_3) mismatch. The R_{SCALE} changes by ±1.2% as the T3 width varies from 147 to 153 μm, corresponding to ±2% deviation. Also according to Eq. 6-7, a higher offset voltage V_{offset} value, associated with a large C_{ST2}/C_{ST1} ratio, will introduce greater scale-down ratio deviation ΔR_{SCALE}, as shown in Fig. 6-7(a). Finally, the ΔR_{SCALE} in a high gray scale is not as large as that in a low gray scale because a high driving current can reduce its sensitivity to the geometric size mismatch.

Since the field-effect mobility μ_{FE} can be affected by device temperature, it is expected that β in Eq. 6-6 will also have temperature dependence [9][10]. The temperature increasing from 20 to 70 ºC will result in a higher field-effect mobility thus giving a rise in ΔR_{SCALE}, as shown in Fig. 6-7(b). Also a higher V_{offset} due to a larger C_{ST2}/C_{ST1} ratio can cause an increase of ΔR_{SCALE} not only in a high gray scale ($I_{OLED-ON}$=8 μA) but also in a low gray scale ($I_{OLED-ON}$=0.5 μA) regions. It should be mentioned that as the driving current increases, ΔR_{SCALE} becomes smaller as a result of low temperature sensitivity achieved by a larger $I_{OLED-ON}$.



(a)



(b)

Fig. 6-7. (a) Variation of R_{SCALE} as a function of T3 width variation. (b) Influence of operation temperature upon R_{SCALE}.

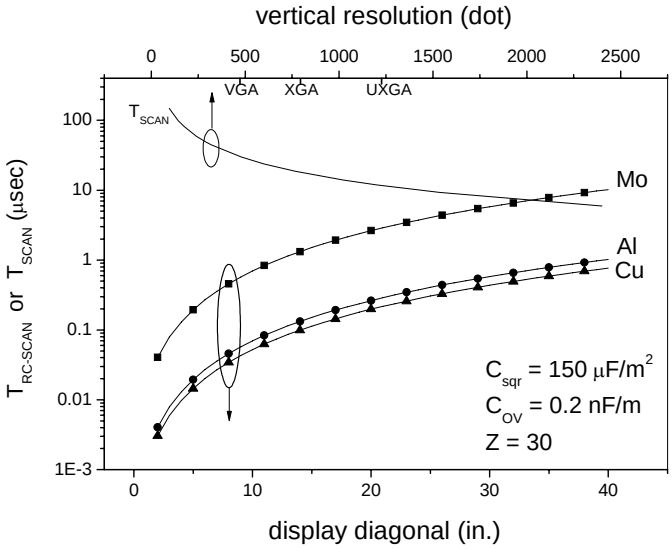
6.4.4 Scan line delay in high resolution display

The key factor to realize a large size and a high resolution display is to overcome the long resistance-capacitance (RC) time constant of the bus lines of which the resistance and capacitance are proportional to the size and the resolution of display

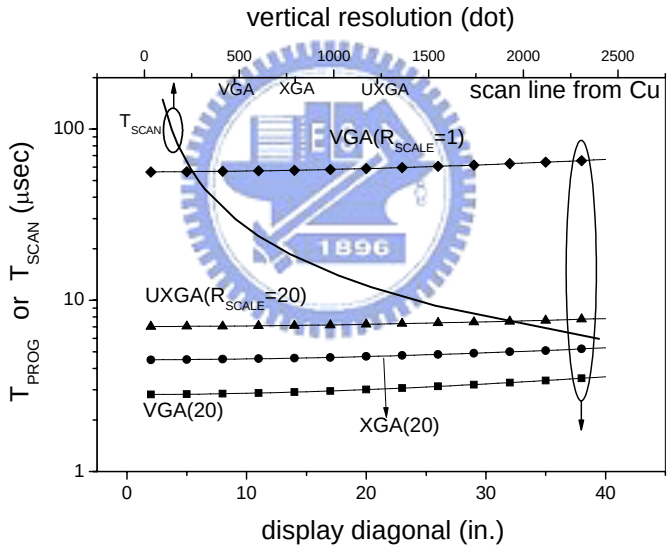
panel. A large RC time constant can cause cross-talk and flicker effects due to the insufficient pixel charging across the large display area. Since the bus line resistance is due to intrinsic resistance of bus lines materials and capacitance is associated with overlap capacitance of intersections and TFTs, the RC time constant of scan line $T_{RC\text{-}SCAN}$ can approximately be estimated by following equation:

$$\begin{aligned} T_{RC-SCAN} &= (N_H \cdot R_{PIXEL}) \cdot (N_H \cdot C_{PIXEL}) \\ &= [N_H \cdot R_{\square} \cdot Z] \cdot \left[N_H \cdot C_{\square} (\frac{H}{N_H \cdot Z})^2 + N_H \cdot C_{OV} \cdot \frac{H}{N_H \cdot Z} \right] \\ &= \frac{R_{\square} \cdot C_{\square} \cdot H^2}{Z} + N_H \cdot C_{OV} \cdot R_{\square} \cdot H \end{aligned} \qquad \text{Eq. 6-8}$$

where H, N_H, $C\square$, $R\square$, Z and C_{OV} are display width, horizontal resolution, capacitance per meter square, sheet resistance, pixel pitch to bus line width ratio and TFT gate-to-drain/source overlap capacitance. According to Eq. 6-8, it is expected that a larger panel size and a higher display resolution will cause a longer $T_{RC\text{-}SCAN}$ which can affect the data programming precision. For $C\square$=150 μF/m^2, C_{OV}= 0.2 nF/m, and Z=30, $T_{RC\text{-}SCAN}$ as a function of display diagonal was calculated for UXGA resolution and for different metallurgy, e.g. copper ($R\square$=0.075 Ω/sqr), aluminum (0.1 Ω/sqr) and molybdenum (1.0 Ω/sqr), Fig. 6-8(a). The scan pulse width T_{SCAN} shown as the solid line in Fig. 6-8(a) is also evaluated for 60 Hz frame rate and for different vertical resolutions. In general, T_{SCAN} should be ten times larger than $T_{RC\text{-}SCAN}$ to prevent the data programming error. Therefore, based on this simple calculation, a high-resistance material such as molybdenum will limit the display size to about 12 inch with UXGA resolution. A low-resistance material such as aluminum or copper is capable of reducing $T_{RC\text{-}SCAN}$ in large size display up to 35 inch or higher to acceptable value.



(a)



(b)

Fig. 6-8. (a) Dependence of scan line RC time constant ($T_{RC\text{-}SCAN}$) on display diagonal and the relationship between scan pulse width (T_{SCAN}) and resolution. (b) Data programming time (T_{PROG}) as a function of panel resolution with a scan line made from Cu.

For AM-OLED, not only the $T_{RC\text{-}SCAN}$ but also the data programming time (T_{DATA}) is important. T_{DATA} is directly related to the data line capacitance C_{DATA}, storage

capacitance C_{ST} and the programming current I_{DATA} and can be approximated by the following equation:

$$T_{DATA} = \frac{V_{DATA} \cdot (C_{DATA} + C_{ST})}{I_{DATA}} \cong \frac{V_{DATA} \cdot N_V \cdot C_{\square}}{R_{SCALE} \cdot J_{OLED}} \qquad \text{Eq. 6-9}$$

where $J_{OLED} = \frac{C_n \cdot C_E \cdot \pi \cdot L}{C_V \cdot \eta}$.

Since the C_{ST} is much smaller than C_{DATA}, it can be neglected to simplify the calculation. In Eq. 6-9, V_{DATA} denotes the voltage at C_{ST} generated by the I_{DATA}, and N_V is the vertical resolution which can be obtained from N_H and aspect ratio of display. The constants Cn, C_E, and C_V depend on the refractive index and the emission spectrum of the OLED material. Besides, L is the OLED luminance and η is device quantum efficiency. It should be noted that the T_{DATA} in Eq. 6-9 is independent of the display size, and I_{DATA} is increased when the pixel area is increased to compensate for large C_{DATA} resulting from the increase of display size. In order to compare the proposed pixel electrode circuit with the conventional pixel circuit and to evaluate its performance, T_{PROG} is defined as $T_{RC\text{-}SCAN}$ + T_{DATA} to describe the total time requirement for accurate data programming. Fig. 6-8(b) shows T_{PROG} of proposed pixel as a function of display size for V_{DATA}=5 V, Cn=1.1, C_E=0.44 V^{-1}, C_V=427 lm/W, L=100 cd/m^2, η=5%, C□=150 μF/m^2 and R_{SCALE}=20, along with the T_{PROG} of conventional pixel for R_{SCALE}=1. Without current scaling function (R_{SCALE}=1), a VGA display requires T_{PROG} of 60 ~ 70 μs to charge up the conventional pixel electrode circuit which is two times higher than a specific T_{SCAN} of display with VGA resolution. Therefore, conventional pixel circuit is not applicable for a large size and a high resolution display device. By contrast, the proposed pixel circuit with the current scaling function can reduce the T_{PROG} significantly when a large I_{DATA} is used. Furthermore, as display resolution increases, the T_{PROG} for UXGA resolution

(1600x1200) is of 8 ~ 9 μs which is lower than a specific T_{SCAN} of 10 μs even for display diagonal of 40 inch. In summary, the proposed pixel electrode circuit with cascade storage capacitance and build-in current scaling capability can allow to achieve a high resolution and a large size current-driven AM-OLED.

6.5 Summary

We proposed a pixel electrode circuit based on poly-Si TFT technology and current driving scheme for speeding up the data programming time. We have shown that this circuit can achieve a high current scale-down ratio by a cascade structure of storage capacitors instead of increasing the size of TFT. In the proposed circuit, the ON-state data current of a factor of 10 larger than OLED current in OFF-state can be achieved. In contrast to the conventional current-driven and the current-mirror pixel electrode circuits, our pixel circuit can achieve the widest range of I_{AVG} for I_{DATA} ranging from 0.1 to 10 μA, hence, both the current scaling function and the reasonable power consumption can be easily accomplished without substantially sacrificing the pixel aperture ratio. Furthermore, the threshold voltage variation of all TFT can also be compensated by the proposed circuit. The effects of device geographic size mismatch and temperature increase on pixel electrode circuit have been analyzed, and it has been concluded that they are within acceptable range of operation. The calculation of scan line delay and the required programming time indicated that the proposed pixel shows admirable capability to improve the data programming time. Even though the higher resolution limits the pixel pitch, the proposed pixel can be easily integrated with the top emission OLED without any aperture ratio restriction. Consequently, this new pixel electrode circuit has great potential for applications in a large size, a high resolution poly-Si TFT AM-OLEDs.

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Chapter 7

Functionality testing for AM-OLED

7.1 Introduction

TFT array inspection and yield management are important to ensure the reliability of AMLCD, AMOLED and other active-matrix display applications [1][2]. In-line testing of TFT array in manufacturing processes is beneficial for yield improvement because the faulty TFT array can be repaired or scrapped before encapsulation, and external driver assembly. Likewise, utilizing TFT array testing for failure analysis can detect the location of the faults and identify the categories of faults in TFT array.

In conventional AMLCD industry, several inspection technologies have been developed and applied for TFT array testing: 1) the voltage imaging scheme [7], 2) the electron beam scheme [8], and 3) the charge sensing scheme [9]. The voltage imaging and electron beam schemes can inspect all TFT devices on entire substrate regardless of the circuitry configuration but only a few kinds of faults can be detected. Besides, demands of high stability of the instruments and long working time also limit the performance of them. Although the charge sensing scheme requires a large number of contact pins, direct contact and measurement can perform the speedy functional testing and evaluate more parameters of the TFT than the others.

The conventional AM-OLED pixel circuit does not provide for fully functional testing with charge sensing scheme as the AM-LCD pixel does [10], unless an additional component can be added-in. We propose the modified pixel circuit with cooperating charge sensing scheme to measure the characteristics of TFT and detect

defects. The proposed TFT array testing scheme is simulated and demonstrated to be a good tool for managing the yield of the array process of AM-OLED's.

7.2 Full function testing for AM-OLED pixels

7.2.1 Schematic of pixel circuit

A conventional 2-transistor (2-T) pixel circuit, in which the transistor T_{SW} acts as a switch and the transistor T_{DV} controls the driving current of the pixel, is encircled by dash line in Fig. 7-1(a). Following TFT array processes, organic material is deposited onto the substrate by evaporation or ink-jet printing processes to form the OLED, denoted by the diode symbol in Fig. 7-1.

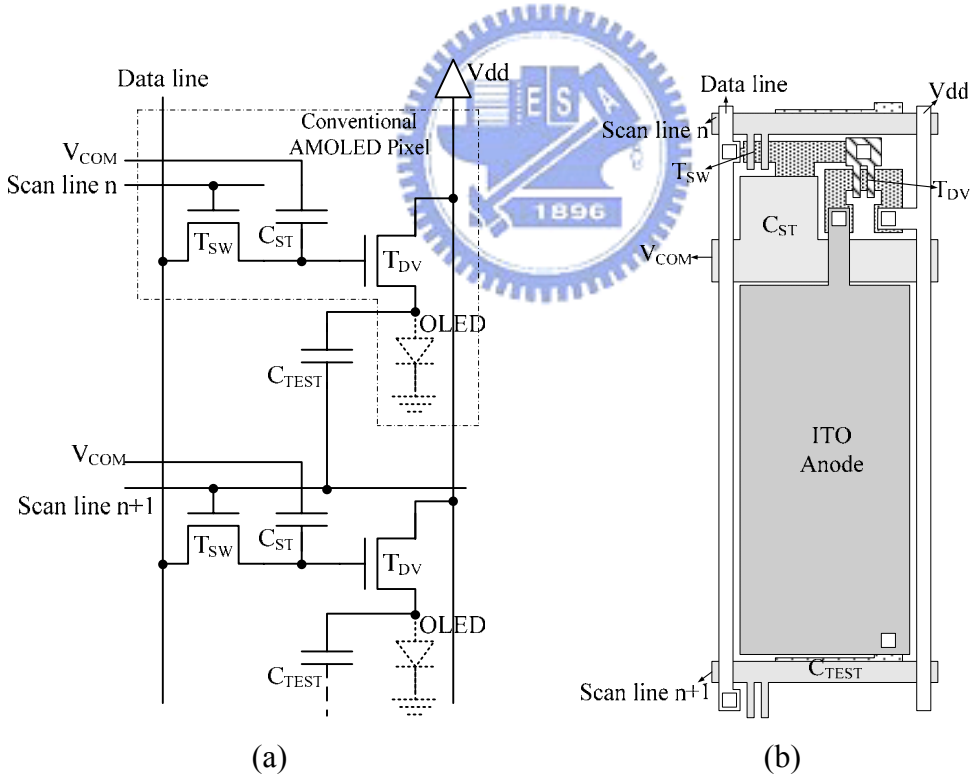

Fig. 7-1. (a) 2-T pixel circuit for AM-OLED TFT array testing and (b)layout view of the modified pixel circuit.

However, before the OLED process is performed, the ITO anode of each pixel circuit

is in a floating state so that not only the source voltage of T_{DV} can not be confirmed, but also no path is available for conducting the driving current. The incomplete pixel circuits limit the testability of the TFT array.

A Capacitor-on-Gate (COG) structure which forms an additional testing capacitor (C_{TEST}) is proposed to improve the testability of the AM-OLED pixel electrode circuits. This C_{TEST} ensures the circuit completeness and prevents the floating status of anode before OLED material deposited onto the TFT array. One electrode of C_{TEST} is connected to the source of T_{DV}, and the other is connected to the scan line, as schematically shown in Fig. 7-1 (a). The function of pixel as well as the characteristics of T_{DV} can be examined by utilizing this C_{TEST}. A layout example of 2-T pixel electrode circuit with proposed COG structure is drawn in Fig. 7-1(b) where shows that an additional C_{TEST} is drawn below the scan line electrode, consequently, no much additional area is needed to form the C_{TEST}.

7.2.2 Detection circuit & operation of functional testing

The pixel, functioning like a sample and hold circuit, is driven to sample analog data and store them until the following sampling period. Also, by connecting the pixel to a detection circuit, the stored data can be retrieved. The principle that underlies the proposed charge sensing scheme is to write and read the charges of the pixel. An operational amplifier, configured as an integrator, is used as a detection circuit to receive the charges from the pixel. The detection circuit constructed by an integrator with virtual ground configuration can maintain the voltage of 0V at the input of detection circuit while the testing is performed. T_{SW} and T_{DC} in the pixel circuit must be examined individually because of the functional differences. For testing either T_{SW} or T_{DV}, (1) writing, (2) holding and (3) reading periods must be achieved sequentially.

The details of testing approach for T_{SW} and T_{DV} is illustrated in following sections.

7.2.3 Functional testing for T_{SW}

The functions of T_{SW} and C_{ST} in AM-OLED pixel circuit are similar to that in AM-LCD pixel. Since the charge in C_{ST} is directly controlled by data line signal, the detection circuit, in which the switch SW1 is used to initialize the output voltage, is connected to the data line of the pixel through a switch SW2. The simplified equivalent circuit and corresponding waveforms for testing T_{SW} are shown in Figs. 7-2(a) and (b), respectively. In the T_{SW} testing, a constant voltage is supplied to V_{COM} electrode as a reference and Vdd electrode is connected to ground. The operation of pixel circuit is only controlled by data line and scan line.

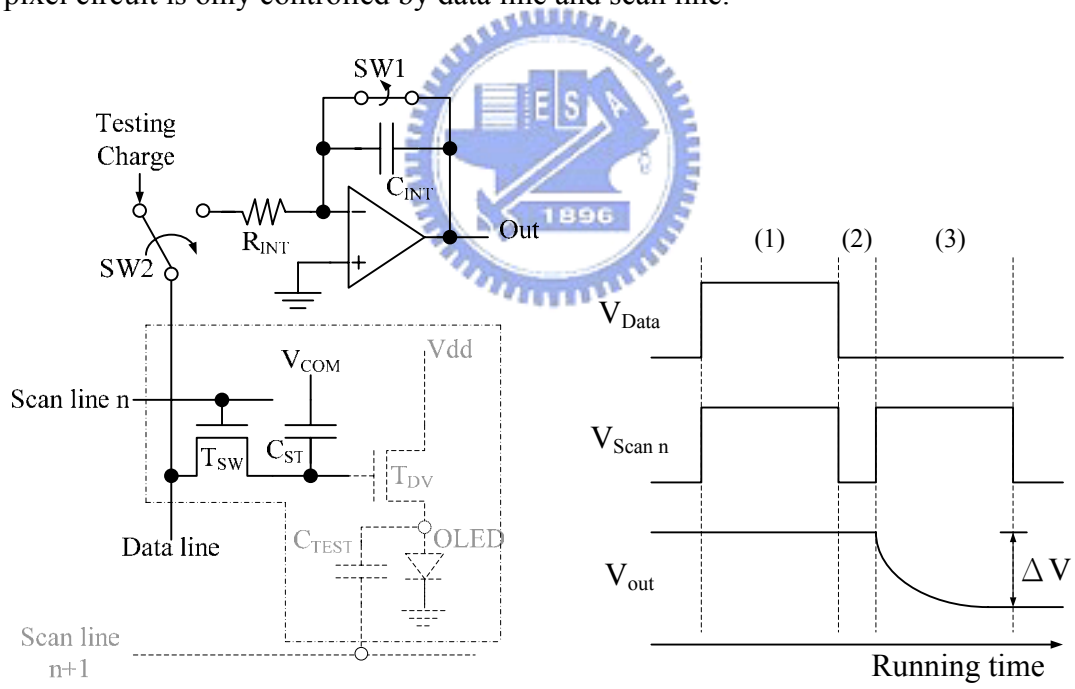

Fig. 7-2. (a) System diagram with charge detection circuit and (b) the timing diagrams for T_{SW} testing. ((1) Writing, (2) holding, and (3) reading period)

When in writing period (1), the signal at scan line n is HIGH to turn on the T_{SW} and the SW2 connects the data line to an external power supply which can provide

testing charge $Q_{ST} = V_{Data} \cdot (C_{ST} \parallel C_{GS-SW})$ to storage capacitor C_{ST} as a positive voltage. In the meanwhile, the SW1 connects the output and negative input of amplifier together to initial the output voltage of 0V. In the following holding period (2), the signal at scan line n becomes LOW to turn off the T_{SW}. When T_{SW} is OFF, the resistance of which must be large enough to prevent significant leakage from C_{ST} to data line. Therefore the charge Q_{ST} is maintained in C_{ST} for the entire holding period.

Now considering the reading period (3), the SW2 switches the data line from power supply to the detection circuit and the SW1 is open to actuate the detection circuit. After that, the scan line signal turns T_{SW} on once again and the charge in C_{ST} is released and redistributed into the detection circuit due to the zero voltage at data line. While collecting the charge Q_{ST} across the feedback capacitor C_{INT}, the detection circuit is still holding the data line at 0V simultaneously, therefore no charge is lost. After the charge is collected, the output voltage of the integrator is decreased by an offset voltage ΔV_{Out}, defined as $\Delta V_{Out} = -Q_{ST} / C_{INT}$, is proportional to the amount of charge Q_{ST} stored in C_{ST}. Therefore, holding more charges in C_{ST} makes the output more negative after detection because of the negatively configured integrator.

7.2.4 Functional testing for T_{DV}

T_{DV} works as a voltage-to-current converter to provide a stable current signal to OLED during whole frame period. Variations of T_{DV} characteristics directly influence output current and result in brightness non-uniformity and inferior image quality. Therefore the functional testing for T_{DV} is more important than T_{SW}. Since T_{DV} is modulated by the voltage signal at storage node and the testing charge is from Vdd electrode, the detection circuit should be connected to Vdd instead of data line and thereby collect the charge in C_{TEST}. The simplified equivalent circuit and

corresponding waveforms for testing T_{DV} are shown in Fig. 7-3(a) and (b), respectively.

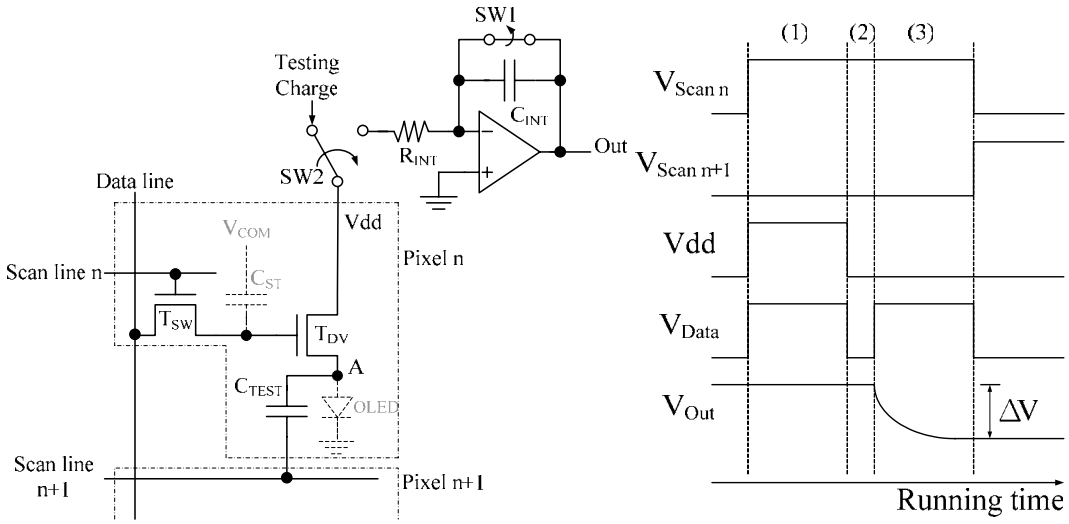

Fig. 7-3. (a) System diagram with charge detection circuit and (b) the timing diagrams for T_{DV} testing. ((1) Writing, (2) holding, and (3) reading period)

During writing period (I), the switch SW1 connects the pixel electrode circuit to V_{TEST} and SW2 connects V_{OUT} to the negative input of operational amplifier to initial the detection circuit. At this time, the output voltage V_{OUT} is 0V. In the meanwhile, the data line signal V_{DATA} turns T_{DV} on and a testing voltage V_{TEST} is stored in C_{TEST} through T_{DV}. According to the charge conservation principle, the charge stored at nodes A and V_{DD} in writing period can be derived as following equations in which C_{GS} and C_{GD} denote the gate-to-drain and gate-to-source parasitic capacitance.

$$Q_{A-I} = (C_{GS-DV} + C_{TEST}) \cdot V_{TEST} - C_{GS-DV} \cdot V_{DATA} - C_{TEST} \cdot V_{SCAN} \quad \text{Eq. 7-1}$$

$$Q_{V_{DD}-I} = (C_{PV} + C_{ST} + C_{GD-DV}) \cdot V_{TEST} - (C_{ST} + C_{GD-DV}) \cdot V_{DATA} \quad \text{Eq. 7-2}$$

In addition to the charged stored in C_{ST}, C_{TEST} and C_{PV}, V_{DATA} can also induce the accumulative electron in the channel of T_{DV}. Therefore the charge held in T_{DV} can be expressed as

$$Q_{DV-I} = -C_{OX} \cdot W_{DV} \cdot L_{DV} \cdot (V_{DATA} - V_{TEST} - V_{TH-DV}) \quad \text{Eq. 7-3}$$

in which C_{OX}, W_2, L_2 and V_{TH2} are the oxide capacitance, width, length and threshold voltage of T_{DV}, respectively.

When pixel electrode circuit changes to the holding period (II), V_{DATA} is low and turns off T_{DV} so that the V_{TEST} is kept in the C_{TEST}. At this time, SW1 switches the pixel electrode circuit to the detection circuit, nevertheless, SW2 still keeps V_{OUT} and negative input of OP-AMP connected together. Because the detection circuit maintains the initial state, the charge Q_{VDD-I} flowing into the detection circuit is removed without disturbing V_{OUT}. It should be taken into account that the charge injection mechanism of T_{DV} will affect the stored charge in C_{TEST} when V_{DATA} changes from high to low. Since the gate voltage is removed so that the channel charge Q_{DV-I} is no longer maintained and will redistribute into the drain and source of T_{DV}. It is assumed that one half of Q_{DV-I} flows into the drain and the other half flows into the source in order to derive equations simply. Moreover, an additional charge induced by C_{ST} at node A and the other half of Q_{DV-I} also flow into detection circuit and is cancelled out. Hence, the charge at V_{DD}, A and TDV in holding period (II) becomes:

$$Q_{A-II} = Q_{A-I} - \frac{1}{2} \cdot C_{OX} \cdot W_{DV} \cdot L_{DV} \cdot (V_{DATA} - V_{TEST} - V_{TH-DV}) \quad \text{Eq. 7-4}$$

$$Q_{V_{DD}-II} = 0 \quad \text{Eq. 7-5}$$

$$Q_{DV-II} = 0 \quad \text{Eq. 7-6}$$

The data line signal V_{DATA} turns on T_{DV} once again as the pixel electrode circuit works in reading period (III) and SW2 is open to enable the charge detection circuit as well. When V_{DATA} changes from low to high, an additional amount of charge will be induced by C_{ST}, C_{gs2} and C_{gd2} at nodes V_{DD} and A, and will result in the non-zero

voltage at V_{DD} and A. However the detection circuit constructed by virtual ground configuration of the integrator maintains the voltage of 0V at the V_{DD} and A while the detection circuit is connected to the pixel electrode circuit. Hence the charge at nodes A and V_{DD} are collected by detection circuit until the voltage at both nodes becomes 0V. After pixel electrode circuit returns to steady state, the charge at V_{DD} and A can be expressed as:

$$Q_{A-III} = -C_{GS-DV} \cdot V_{DATA} - C_{TEST} \cdot V_{SCAN} \quad \text{Eq. 7-7}$$

$$Q_{V_{DD}-III} = -(C_{ST} + C_{GS-DV}) \cdot V_{DATA} \quad \text{Eq. 7-8}$$

Furthermore, the channel charge of T_{DV} is induced again by V_{DATA}, as shown in following equation.

$$Q_{DV-III} = -C_{OX} \cdot W_{DV} \cdot L_{DV} \cdot (V_{DATA} - V_{TEST} - V_{TH-DV}) \quad \text{Eq. 7-9}$$

Since SW2 switches to open before the reading period, the detection circuit starts to collect the charge and an amount of which can be derived from the difference of total amount of charge between holding and reading period.

$$Q_{Total} = (Q_{A-II} + Q_{V_{DD}-II} + Q_{DV-II}) - (Q_{A-III} + Q_{V_{DD}-III} + Q_{DV-III})$$
$$= (C_{ST} + C_{GD-DV})V_{DATA} + (C_{TEST} + C_{GD-DV})V_{DD} + \frac{1}{2} \cdot C_{OX} \cdot W_{DV} \cdot L_{DV} (V_{DATA} + V_{DD} - V_{TH-DV})$$
Eq. 7-10

The output voltage of the integrator is decreased of an offset ΔV_{OUT}, as plotted in Fig. 7-3 after the charge is collected in reading period. ΔV_{OUT}, defined as $\Delta V_{OUT} = -Q_{Total}/C_{INT}$, where C_{INT} is the capacitance used in the integrator, is related to the amount of charge stored in C_{TEST}. The integrator is negatively configured, so holding more charge in C_{TEST} makes the output more negative after detection.

7.3 Simulation results and discussion

7.3.1 Simulation environment

The simulation was performed by Synopsis H-SPICE simulation tool. The characteristics of I_D-V_G of TFT used for simulation are demonstrated in Fig. 7-4(a) in which the subthreshold slope (S.S.) for each curve is listed. In order to imitate the RC loading of the practical panel, the parasitic resistance and capacitance of conducting wires are taken into account, as shown in Fig. 7-4(b). Other parameters, such as geometric size of TFT, mobility, threshold voltage, storage and test capacitance, and driving voltage, are also listed in Table 7-1. In simulation, the ideal operational amplifier with an open loop gain of 10^6 is used to design the charge detection circuit. The resistance R_{INT} and capacitance C_{INT} of charge detection circuit are designed with a value of 100kΩ and 10pF, respectively.

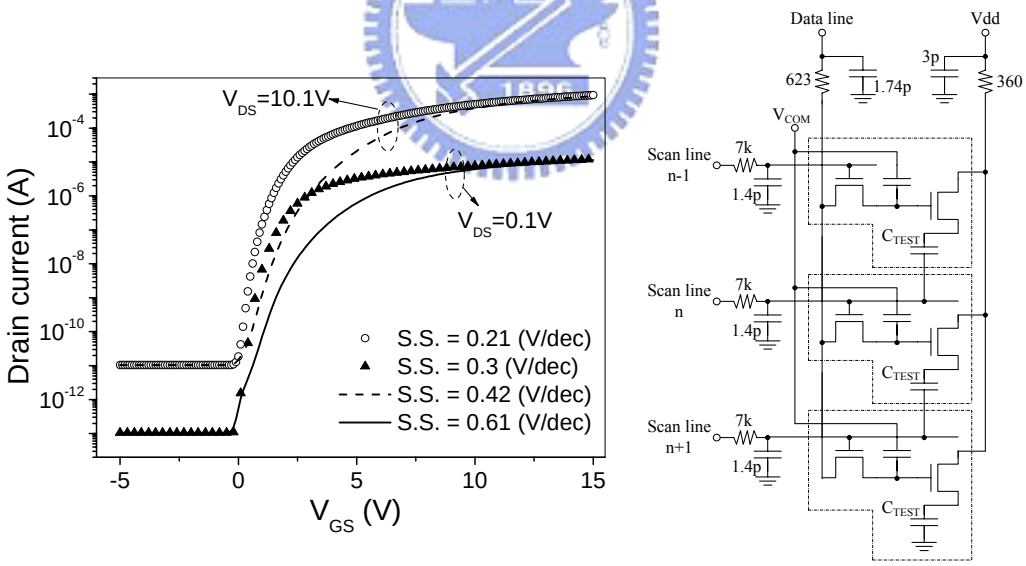

Fig. 7-4. (a) I_D-V_G characteristics of TFTs and (b) the equivalent schematic diagram used for SPICE simulation.

Table 7-1. Parameters used for simulation

Pixel size (um^2)	66 x 198
W/L of T_{SW}(μm)	7/5

W/L of T_{DV}(μm)	10/5 ~ 50/5
V_{th} of N-TFT (V)	1.0
μ of N-TFT (cm^2/s-V)	77.1
C_{ST} (fF)	100 ~ 1000
C_{TEST} (fF)	10 ~ 90
R_{INT} (Ω), C_{INT} (pF)	100k, 10p
R_{para}(Ω), C_{para}(F) of data line	623, 1.74p
R_{para}(Ω), C_{para}(F) of scan line	7000, 1.4p
R_{para}(Ω), C_{para}(F) of Vdd line	360, 3p
V_{Scan} (V)	0, 15
V_{Data} (V)	3 ~ 13
Vdd (V)	0 ~ 15
V_{COM}(V)	15

7.3.2 Results of T_{SW} and T_{DV} testing

The increases of V_{DATA} and C_{ST} result in the corresponding increase of offset voltage when testing the T_{SW}, as shown in Fig. 7-5. As the above discussion, the offset is proportional to Q_{ST}/C_{INT}, consequently, the more charges can be stored in C_{ST}, the larger offset voltage is measured. The geometric size of T_{DV} also affects the offset voltage while testing T_{SW}, as shown in the inset of Fig. 7-5. The V_{DATA} written into C_{ST} can induce the channel of T_{DV} and result in an additional parasitic capacitance C_{DV}. The stored charges can be written as:

$$Q_{ST}' = (C_{ST} \parallel C_{GD-SW} + C_{DV}) \cdot V_{DATA} \qquad \text{Eq. 7-11}$$

Therefore, the larger the geometric size of T_{DV} is, the larger offset voltage can be detected. As a result of the ground shorted to the V_{DD} electrode, various size of C_{TEST} does not affect the offset voltage in T_{SW} testing because no charge is stored in C_{TEST}.

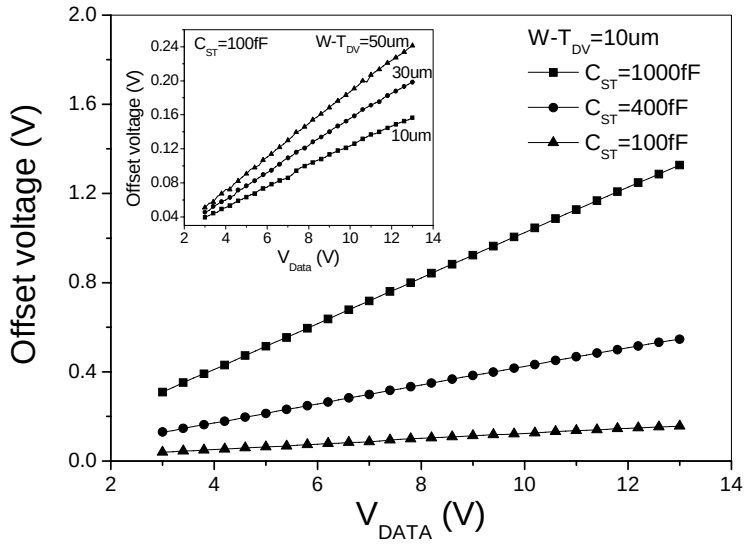

Fig. 7-5. Offset voltage versus data voltage at different storage capacitance C_{ST} in T_{SW} testing. The inset shows the effect of width of T_{DV} ($W\text{-}T_{DV}$) in T_{SW} testing.

The function of T_{DV} can also be inspected by writing and reading the charges in C_{TEST} with proposed testing scheme. The testing charges are written into C_{TEST} through the V_{DD} electrode, and the ON-OFF state of T_{DV} is controlled directly by a digital data signal of 13v and 0v. The simulation result plotted in Fig. 7- 6 demonstrates that the additional C_{TEST} actually improves the testability of T_{DV}. On the other hand, the offset voltage is less than that of T_{SW} testing because of the small C_{TEST} which can minimize the delay of scan line signal. In contrast, the offset voltage can not be detected in the pixel without C_{TEST} even though the T_{DV} is functioning perfectly in simulation.

The offset voltage in T_{DV} testing is also related to the geometric size of T_{DV}. The larger size of T_{DV} leads to larger parasitic capacitance C_{DV} and keeps an additional amount of charge within it. At C_{TEST} of 30fF, increase of the size of T_{DV} results in the shift of the simulated curve, as shown in the inset of Fig. 7- 6, consequently implying that the digital V_{DATA} in T_{DV} testing induces the constant C_{DV} as the width of T_{DV} is

fixed regardless of the V_{DD} voltage.

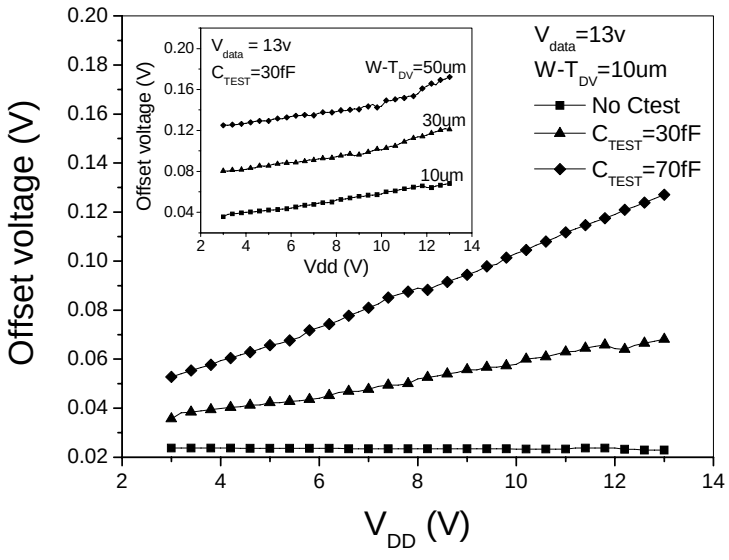

Fig. 7- 6. Offset voltage versus V_{DD} voltage at different C_{TEST} in T_{DV} testing. The inset shows the effect of width of T_{DV} varied from 10 to 50um in T_{DV} testing.

7.3.3 Threshold voltage, leakage current, and subthreshold slope

Data collected by the charge detection circuit can be used to evaluate the characteristics such as threshold voltage and leakage current of the pixel with specific driving conditions. Leakage current induced by process variations causes the charge in C_{ST} leak out even though the T_{SW} is turn-off, ultimately, affecting the gray level of pixel. In the above discussion, the write-in data are hold in storage capacitance for a certain period between the writing and reading process. The write-in data voltage probably decreases during the holding period due to the leakage current of T_{SW}. The degree of leakage current of T_{SW} can be monitored by the offset voltage with various holding period T_{hold}, as expressed in Eq. 7-12.

$$\Delta V = {Q_{ST}}' - I_{leak} \cdot T_{hold} / C_{INT} \qquad \text{Eq. 7-12}$$

The simulation is conditioned by connecting an ideal current source of 10p to 1nA

between source/drain nodes of T_{SW} to simulate the leakage current. The simulation result reveals that the longer holding time is performed, the smaller offset voltage can be detected, as shown in Fig. 7-7.

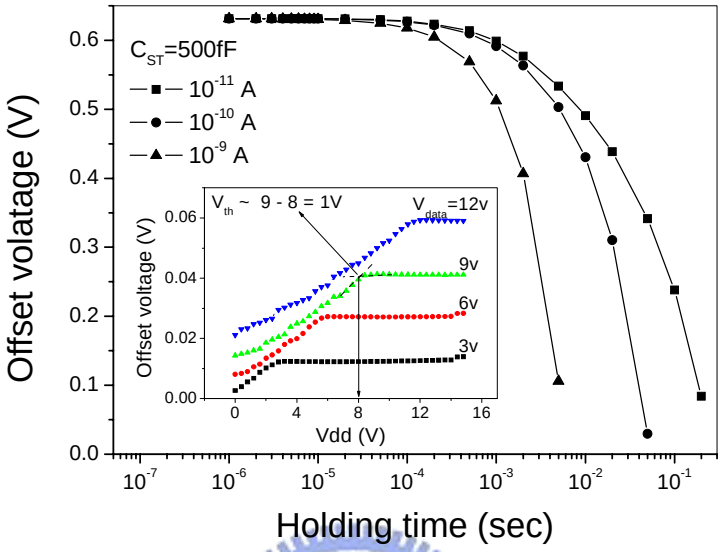

Fig. 7-7. Offset voltage versus holding time at leakage current varied from 10^{-11} to 10^{-9}A in T_{SW} testing. The inset demonstrates the transfer curve of TFT for V_{th} evaluation.

For the panel operation, T_{DV} is used to convert the voltage into current hence the variation of the threshold voltage of T_{DV} must be sufficiently small to ensure the uniform brightness. When testing T_{DV}, the transfer characteristic of T_{DV}, plotted in the inset of Fig. 7-7, can be derived by scanning various voltages to both the data line and the V_{DD} electrode and measuring the offset voltage in turn. The simulated offset voltage curve is similar to the transfer curve of an ideal MOSFET device. The linear region of the simulated offset voltage curve can be distinguished from the saturation region. Therefore, the threshold voltage can be simply derived from the intersection of two asymptotes. The threshold voltage obtained by this functional testing scheme is an approximated value due to numerous parasitic resistance and capacitance, yet, can

be used to monitor the threshold variation in large.

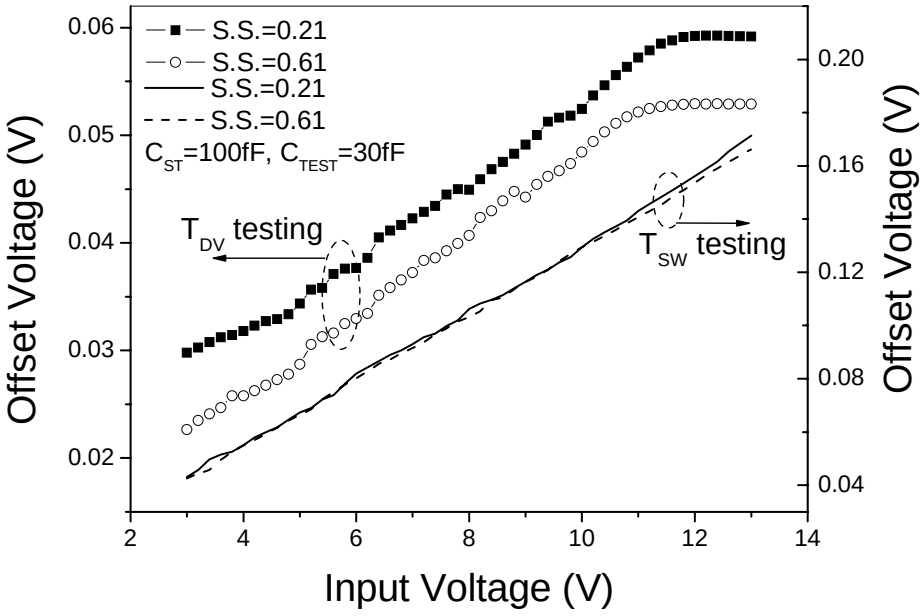

Fig. 7-8. Offset voltage versus input voltage at different subthreshold swing (S.S.) from 0.21 to 0.61 V/dec in T_{DV} and T_{SW} testing.

An important parameter, subthreshold slope (S.S.), indicates how effectively the TFT can be turned off when gate to source voltage is decreased below threshold voltage. In TFT process, the increase of grain boundary trap densities or the random grain size and orientation makes the subthreshold slope increase. Usually, the variation of subthreshold slope can be used to monitor the uniformity of characteristics of TFT. In the proposed pixel circuit, a significant influence of subthreshold slope can be found while performing the pixel testing. A decrease of offset voltage of about 5mV in T_{DV} testing is shown in Fig. 7-8 when subthreshold slope varies from 0.21 to 0.61 V/dec. The reason is that large subthreshold slope attributed to the increase of grain boundary trap densities results in the weak inversion in channel region of TFT, thus the less charge can be retrieved. However, in T_{SW} testing, the decrease of offset voltage is not evident because the channel charge

difference is caused by the negligible variation of subthreshold slope. On the other hand, in T_{DV} testing, the small C_{TEST} is beneficial to observe the effect of subthreshold slope as well as the uniformity of characteristics of T_{DV}.

7.4 Issues of time constant and aperture ratio

The additional C_{TEST} directly increases the resistance-capacitance (RC) time constant T_{RC} of the scan line and decreases the aperture ratio of the pixel, even though the C_{TEST} can enhance the testability of T_{DV}. Although C_{TEST} is geometrically formed below the scan line, as shown in Fig. 7-1(b), the contact hole that connects C_{TEST} to ITO occupies an extra area of 200 um^2, consequently, slightly decreases the aperture ratio from 43.1% to 41.4%.

In order to evaluate the T_{RC} of the scan line, the parasitic resistance and capacitance of a scan line per pixel (R_{scan}, C_{scan}) are set to be 13.2Ω and 2.6fF, respectively for the pixel without C_{TEST}. In the proposed pixel circuit, C_{scan} increases from 2.6 to 72.6fF as C_{TEST} of 10, 30, 50, and 70fF are used. Besides, the frame rate of 30Hz is used to calculate the turn-on period of the scan line ($T_{scan\text{-}on}$) for the comparison between T_{RC} and $T_{scan\text{-}on}$.

T_{RC} is much smaller than $T_{scan\text{-}on}$ for the conventional panel without C_{TEST}. Even though in high resolution such as 1280xRGBx1024 (SXGA), T_{RC} is merely 1.55% of $T_{scan\text{-}on}$, as shown in Fig. 7-9. However, T_{RC} is increased when the proposed pixel is implemented into a panel. For example, in the resolution such as 480xRGBx360, C_{TEST} of 70fF increases T_{RC} to 1.98us, 28 times larger than that of conventional panel. However, T_{RC} to $T_{scan\text{-}on}$ ratio of 2.15% is still smaller than 5% which is a generally acknowledged limitation in display panel design. In other words, from small to moderate resolution, C_{TEST} can be useful for testability enhancement without seriously

impacting on the programming time of the signal. Unfortunately, if the dot resolution is from VGA to SXGA, T_{RC} is dramatically increased by C_{TEST} of 70fF from 3.53 to 14.13us, almost 5.1 to 43.4% of $T_{scan\text{-}on}$. The long T_{RC} results in slow switching behavior of T_{SW} as well as inaccurate data write-in. In order to reduce T_{RC}, an intuitive approach is to use a small C_{TEST} in the pixel circuit, however, the accuracy of charge detection is limited.

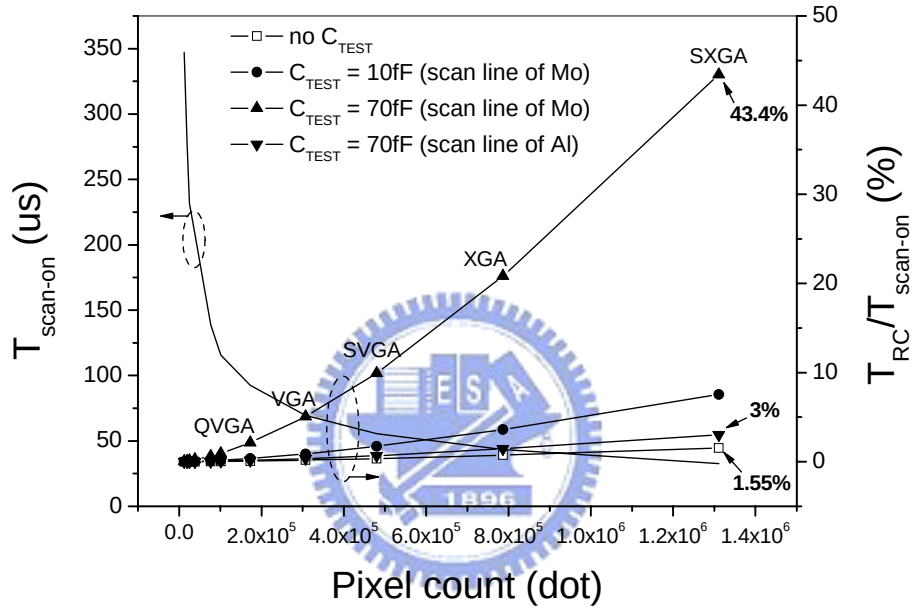

Fig. 7-9. $T_{scan\text{-}on}$ and $T_{RC}/T_{scan\text{-}on}$ versus dot resolution of display panel.

Using high conductivity material such as aluminum to fabricate the scan line instead of molybdenum is another approach to reduce T_{RC}. The sheet resistance of aluminum is 70m Ω/square, merely 7% of that of molybdenum. In contrast with molybdenum, the scan line made by aluminum can achieve the lower R_{scan} of 0.924Ω in proposed dimension. T_{RC} to $T_{scan\text{-}on}$ ratio as a function of dot resolution with aluminum scan line is also plotted in Fig. 7-9. Evidentially, the scan line of aluminum dramatically reduces the T_{RC} to $T_{scan\text{-}on}$ ratio to 3% even in SXGA resolution. Therefore, C_{TEST} of up to 70fF can still be utilized to ensure the accuracy of TFT array

inspection.

7.5 Summary

An effective charge sensing scheme and corresponding pixel circuit were designed to enhance the testability of TFT array of AM-OLED. By using an additional C_{TEST}, the function of all devices such as TFT and storage capacitance can be examined with electrical signal before the OLED process is performed. The proposed functional testing scheme can be performed without any mechanical motion during testing, and an in-situ measurement can be taken in real time with high stability. Two side effects: an increase of RC time constant can be restrained by using aluminum as bus line material; while the reduction of aperture ratio is within acceptable for operation. The simulated and calculated results presented herein including leakage, time constant, and threshold voltage, are useful in identifying the causes of array defects on the panels in situ. Furthermore, the array testing can be integrated into the in-line process as a batch job.

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Chapter 8

Conclusion

Active-matrix organic light emitting displays with integrated driver circuits using polysilicon thin-film transistor technology have demonstrated the capability for being the next generation display applications. In conjunction with the usage of thermal evaporation or ink-jet printing technologies to fabricate OLED pixel elements, it is possible to achieve thin, compact, lightweight, wide-viewing angle, fast response, flexible and yet low cost full color AM-OLED displays.

Unlike AM-LCDs, the organic EL elements for AM-OLEDs are current driven devices. Since the nature of the fabrication process of poly-Si TFT, variations of the TFT electrical characteristics, such as threshold voltage and mobility, over the entire substrate area is unavoidable. Besides, the native parasitic resistance of electrodes can result in a voltage drop as the OLED driving current passing through the addressing electrodes. Consequently, these characteristic and voltage variations cause a large steady state output current error and non-uniform pixel luminance. In this dissertation, we have successfully developed several key driving and testing schemes to improve the display image quality and the functionality evaluations. The characteristics of pixels and driving circuits were taken into consideration for optimizing the display performance, such as the charge injection, parasitic RC time delay and device degradation, etc. Additionally, from this thesis research, the fabrication processes of poly-Si TFT and OLED were utilized for realizing the AM-OLED panel with proposed electronic circuits and components. Most of all, these driving schemes and components greatly improve the display performance of AM-OLED displays and manufacturing yield control, thus, offering more appealing and competitive

AM-OLED's.

8.1 AC driving scheme for voltage driven AM-OLED

A two-transistor pixel electrode circuit driven by voltage signal for AM-OLED's is more attractive because of its high aperture ratio and compatibility with AM-LCD driver technology. Even though the parasitic resistance of addressing wire can lead to a voltage drop as the OLED current passing through it, our proposed voltage type AC driving scheme shows a significant improvement in the display luminance. By using an AC voltage at OLED cathode, the voltage drop at the addressing wire can be easily compensated without modifying the pixel circuit structure.

The normalized luminance of all measured regions of AM-OLED panel was well above 91.6%, for a various duty cycle of the flashing period from 20% to 80% shown experimentally. In contrast, the AM-OLED panel with conventional DC driving scheme shows lower luminance uniformity, due to luminance decays from surrounding to the central area. The lowest luminance measured at the central display region was of only 74.54% of the highest luminance at the surrounding area. Although a higher driving current is needed in the AC driving scheme, the treatment of reversed bias voltage can accelerate the recovery from degradation and lead to an improvement in the J-V characteristics and device lifetime of the OLED. In other words, the higher driving current may degrade OLED performance rapidly, however, the AC driving scheme with proper reversed bias voltage, can alleviate the OLED material degradation.

8.2 Current driven AM-OLED with fully integrated driver

In order to achieve multiple grayscales, circuit designers and process engineers

must address the issue of non-uniform pixel brightness over the display area caused by the non-uniform spatial distribution of threshold voltage in the driving transistor of pixel circuit. In this dissertation, we focus on certain methods and techniques used in designing poly-Si TFT pixel driver circuits to minimize the effect of threshold voltage variation on the display luminance. The key concern in design of current driven pixel circuit is to ensure that the OLED is driven with a specified input current not only during the OLED is addressed but also during the rest of the frame period as well when the OLED is not being addressed. Here we have designed, fabricated, and analyzed a current-driven four-transistor pixel electrode circuit based on poly-Si TFT technology for AM-OLED's. The pixel circuit proposed here is able to reduce the effect of spatial variation of TFT threshold voltage in comparison with traditional voltage driven pixel circuits. Experimental results indicated that continuous pixel electrode excitation with constant current signal can be achieved during more than 12 hours Bias-Temperature-Stress experiment. The pixel electrode circuits showed an excellent electrical stability that no output current variation was observed even when a large TFT threshold voltage shift was measured.

For the sake of system integration, we also designed and implemented several key components of current driving circuits with poly-Si TFT technology, including current memory cell, reference current generator, and digital-to-current converter. The current memory circuit can operate with a high accuracy in a weak current range and the effect of the charge injection is reduced significantly by employing a cascade current mirror structure. The circuit operation does not need complex clock signals and large storage capacitance, thus, facilitating the circuit implementation and minimizing the required layout area. Furthermore, these improvements have been achieved without requiring any critical geometric matching of TFTs. Even though the

power consumption of the proposed current memory is inferior to those of the conventional current memory, the features, such as fast response time and high accuracy of output current, favor the applications of the proposed current memory in driver circuits of current driving AM-OLED's.

In addition to the current memory circuit, the proposed DCC with reference current generator can prevent random characteristic variations in all the transistors of the current source cell by utilizing the external reference current signal and yield accuracy current signals under various driving conditions. By means of the adjustable TFT geometric size, the DCC permits us to flexibly and precisely design the required current signals corresponding to the gray scale of AM-OLED's without using external current-type peripheral drivers, hence, resulting in notable reduction of input contact pins and fabrication cost. The proposed design methodology has been applied to the design and optimization of a 6-bit DCC integrated in an AM-OLED substrate. The opto-electrical characteristics of AM-OLED with above mentioned driver circuitries reveal that the current driving scheme is capable of enhancing the display luminance uniformity. Moreover, the fully integrated data driver circuits not only provide a digital interface which is compatible with AM-LCD but also reducing the usage of current-type external drivers, thus, possibly lower fabrication complexity and cost.

8.3 Current scaling pixel electrode circuit

Current driving scheme with four-transistor pixel electrode circuits can not only provide a continuous excitation to OLED, but also compensate for the TFT threshold voltage variation at the same time. Although the current driving scheme improves the display luminance uniformity, a large timing delay can be observed in low current driving condition. Due to combination of a high OLED efficiency and large

interconnect parasitic capacitance, a long data programming time is required as rendering a low gray-scale image. In this work, a new AM-OLED pixel electrode circuit employing a cascade capacitance structure to achieve current scaling function is proposed and verified by HSPICE simulation. This pixel design, which consists of four poly-Si TFTs and two capacitors, scales down the OLED current more effectively without sacrificing the pixel aperture ratio, so as to guarantee a speedy data programming time, compared with the conventional current mirror structure.

The modified pixel electrode circuit shows outstanding current scaling function in comparison with both the conventional current-driven and current-mirror pixels. Although the current–mirror pixel is able to scale down the data current, the scale-down ratio is fixed. Besides, a large data current for high gray scales will result in high power consumption due to this fixed scale-down ratio. In addition, to achieve the current scaling function, a larger driving TFT needed in current-mirror pixel can substantially reduce the pixel electrode aperture ratio. From the simulated results, we can conclude that with the data current ranging from 0.1 to 10 μA, our proposed pixel circuit can achieve the widest OLED current ranging from 1 nA to 5 μA. By contrast, the conventional current-driven pixel and the current-mirror pixel can merely achieve the OLED current from 0.05 to 10 μA and from 0.01 to 2.5 μA, respectively. Therefore, the proposed pixel circuit can yield not only a high data current and a high scaling ratio for the low gray scales, but also reasonable data current for a high gray scale to avoid large display power consumption. Furthermore, the proposed pixel circuit also compensates for the non-uniformity of electrical characteristics of poly-Si TFTs, such as the threshold voltage and mobility.

8.4 Functionality testing for AM-OLED

In the past few years, several AM-OLED pixel electrode circuits with complex driving schemes have been proposed to improve the luminance uniformity. However, there is no effective testing method proposed to evaluate the functionalities of the pixel circuits. In this work, the capacitor-on-gate structure has been proposed and applied to the AM-OLED pixel circuit to improve the testability. By utilizing the proposed charge sensing scheme, TFT array can be investigated and evaluated immediately after fabrication processes and again after the display has been deposited with OLED materials. It can also be used to verify array designs and perform failure analysis.

Among all kinds of OLED pixel circuits, the pixels are not complete before the OLED process is performed because the ITO anode of each pixel circuit is in a floating state. Hence the source voltage of driving TFT can not be confirmed and no path is available for conducting the driving current as well. The incomplete pixel circuits limit the testability of the pixel electrode circuits of TFT array. Our capacitor-on-gate structure can improve the testability of the AM-OLED pixel electrode circuits and ensures the circuit functions to prevent the floating status of anode before OLED material deposited onto the TFT array. This additional capacitor is below the scan line electrode, consequently, no additional pixel area is required. Using the adequate control signals, an amount of testing charge can be supplied to each component in the pixel circuit including switching TFT, driving TFT, and then stored in the storage capacitor and additional testing capacitor. By sensing the testing charge, these components can be inspected completely so that the pixel circuit functionality can be evaluated. In addition to the pixel functionality, the characteristics of switching and driving TFTs, for example, threshold voltage, leakage current, and

sub-threshold slope, can be roughly measured. Although the scan line RC delay is increased due to the additional testing capacitor, the scan line of low resistance materials is beneficial to reduce the RC time constant. For instance, high conductivity material such as aluminum ($R_{\square}$=70m Ω/square) instead of molybdenum ($R_{\square}$=1 Ω/square) for the scan line is capable of significantly reducing the RC time delay of scan line. Therefore, the additional testing capacitor can still be utilized to ensure the TFT array inspection.

8.5 Future work

Conventional AM-LCD pixel circuit utilizes a voltage signal supplied from data line to control the LC cell for modulation of light transmission. OLED is a current-driven device, hence, the AM-OLED pixel circuit has to convert the voltage signal into current. Although the transmissive and the reflective structures can be integrated in AM-LCD pixel, a backlight is essential as a light source, yet at the expense of increase of the display module size and power consumption. In the case of AM-OLED's, self-emitting characteristic exceptionally enhances the contrast ratio, viewing angle and the reduction of module thickness. Nevertheless, in the bright environment, a high driving current is required to maintain the AM-OLED visibility, consequently increasing the power consumption and degrading the reliability. In this dissertation, we propose a novel pixel circuit and structure by combining an OLED and a reflective LCD with active-matrix array to form a novel transflective display to improve the power consumption.

8.5.1 Hybrid AM-OLED with reflective LCD

The new hybrid pixel circuit is composed of a switching TFT T_{SW}, driving TFT

T_{DV}, and storage capacitor C_{ST}, and controlled by four signals: data, scan V_{AC}, and Vdd. The symbols C_{LC} and diode denote the LC cell and OLED, respectively, as shown in Fig. 8-1. Pixel circuit combined LC cell and OLED control function. (a) schematic and (b) layout.. The difference of the proposed pixel circuit is that two electrodes: Al(LC) and ITO(OLED) are used separately to control the LC and OLED. The Al(LC) electrode which controls the LC cell is connected to storage node A and also works as a reflector. The other ITO(OLED) electrode functioning as OLED anode is formed at the source of T_{DV}. The OLED common cathode is connected to an external driver by a switch SW. An AC power supply V_{AC} is adjusted to certain voltage according to the corresponding display mode.

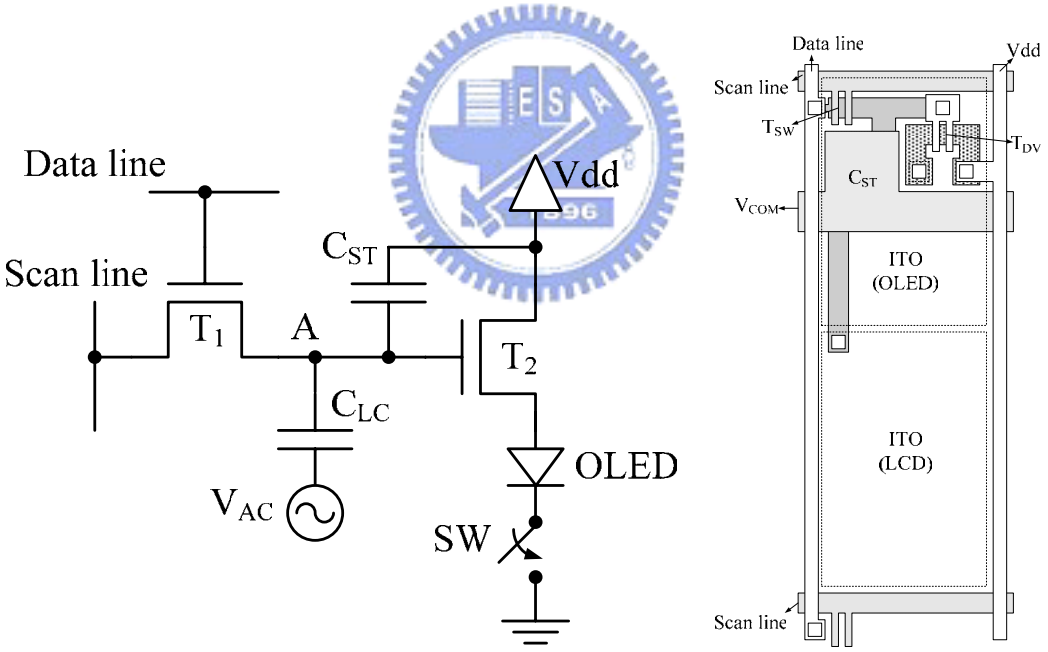

Fig. 8-1. Pixel circuit combined LC cell and OLED control function. (a) schematic and (b) layout.

In the AM-LCD mode, the function of voltage-to-current transformation should be disabled so that the equivalent pixel circuit is identical to the conventional

AM-LCD pixel. At this time, the SW disconnects the OLED cathode from ground and Vdd is set to 0 V. Therefore, the ineffective T_{DV} becomes a small capacitance and can be neglected by comparison to large storage capacitance C_{ST}. An alternately inverse electric field which prevents LC cell from ionizing can be achieved by V_{AC}. Consequently, the normal operation of AM-LCD can be achieved with the display data stored in C_{ST} regardless of T_{DV}. In the AM-OLED mode, the SW connects the OLED cathode to the ground and Vdd is set to a high voltage. By means of normally white LC material, V_{AC} changed to a high voltage can drive the LC cell into black state to decease the reflection. The voltage signal from data line is used to modulate the T_{DV} to generate an adequate current for OLED.

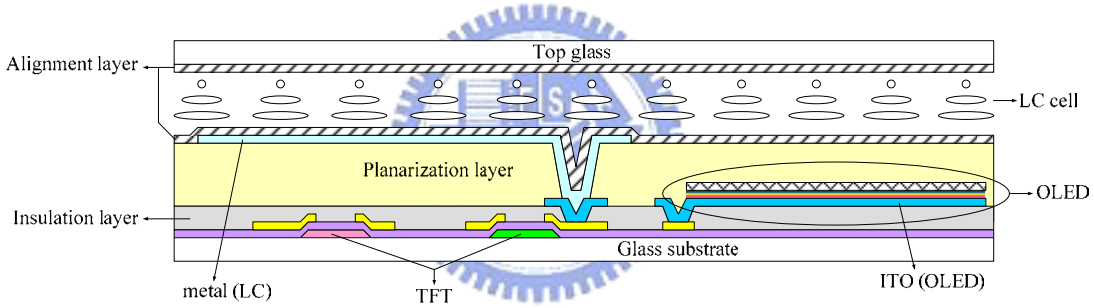

Fig. 8-2. Cross-section view of proposed transflective AM-LCD+OLED pixel circuit.

In order to fabricate this LCD+OLED pixel circuit, some processes should be added or modified. First, the conventional amorphous TFT with bottom-gate stagger structure is fabricated on glass substrate, as shown in Fig. 8-2. Since the traditional organic planarization layer will be deposited after OLED process, silicon nitride or silicon oxide will be used as an insulation layer after pattering the data lines instead of the organic planarization material. The ITO anode is pattered following the insulation layer to form the light emitting area of OLED, then the OLED material and transparent common cathode are fabricated. It should be noted that the transparent common cathode might be deposited with shadow mask because the common cathode

is not allowed to contact the via which is reserved for Al(LC) electrode. Besides, the conventional wet-etching process can not be used to pattern the common cathode since the OLED material is much easily damaged by the chemicals.

The organic planarization material with 2~3 μm thickness is used as a preservation layer to protect the OLED. The organic planarization layer should be baked to reduce the residual moisture and oxygen to prevent from the lifetime degradation of OLED. After via definition, aluminum is deposited and patterned to form the reflective electrode Al(LC) for LC cell. The rubbing process is applied on both the bottom and top glass substrates to provide an alignment layer to control the pre-tilt angle of LC cell. Finally, the LC material will be injected into the panel after assembling the top and bottom glasses.

The proposed pixel circuit combines the self-emitting OLED and reflective LCD to yield a novel transflective display system. By means of the reflective LCD part, the high display visibility at outdoor can be easily achieved so that the OLED can be turn-off to reduce the power consumption and device degradation. When the display used in low ambient light environment, the OLED part can substitute the LCD to provide the brightly colored, high contrast display images. The additional processes needed are being worked out. Besides, several process issues should be considered to avoid the OLED degradation.