A 2.45/5.2 GHz Image Rejection Mixer With New Dual-Band Active Notch Filter

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***Abstract*—A 2.45/5.2 GHz dual-band Gilbert downconversion mixer with image rejection function is presented, which is implemented using the 0.18 μm CMOS technology. The proposed differential dual-band image rejection circuitry is employed for the 2.45/5.2 GHz WLAN application to effectively diminish the dc power consumption and complexity of circuit design compared to the traditional Hartley or Weaver architectures. Moreover, the cross-connected pair consisted of NMOS and PMOS transistors in the proposed notch filter will further ameliorate the image rejection capability. The IC prototype achieves conversion gain of $10.5/11$ dB, IIP3 of $-4.9/-5.2$ dBm for $\mathrm{RF} = 2.45/5.2$ GHz and $\mathrm{IF} = 500$ MHz while the image rejection ratio is better than 36/45 dB in the whole operation bandwidth.**

***Index Terms*—Complementary metal oxide semiconductor (CMOS), dual-band Gilbert mixer, image rejection.**

I. Introduction

RECENTLY, wireless communication has developed the demand for low-cost and low-power RF circuits, which can support multi-band operation in a single chip, such as the IEEE 802.11a/b/g wireless local area network (WLAN) dual-band system. Conventional design strategies have adopted different single-band transceiver circuits in parallel for different frequency bands [1]. However, it is unavoidable to result in a high implementation cost because of the large chip area and an increased chip current dissipation simultaneously. In order to improve the above-mentioned drawbacks, a dual-band mixer has demonstrated the feasibility to take the place of the conventional structure for dual-band application [2].

In addition, the suppression of the image signal is an essential requisite for the RF receiver design. Generally, the dual-band image rejection mixer can be achieved by either Hartley or Weaver architecture, but the image rejection characteristic is restricted due to the magnitude mismatch and phase error of the quadrature signal. On the other hand, the required dual-band mixer with quadrature signal generator for dual-band operation will further increase the complication of the circuit implementation, which is undesired for low-cost and low-power application. In this letter, we adopt the differential, dual-band, third-order, active notch filter to attenuate the dual-band image signal while maintaining a superior in-band performance and achieve smaller chip area and dc power consumption than previous circuits [3]–[6].

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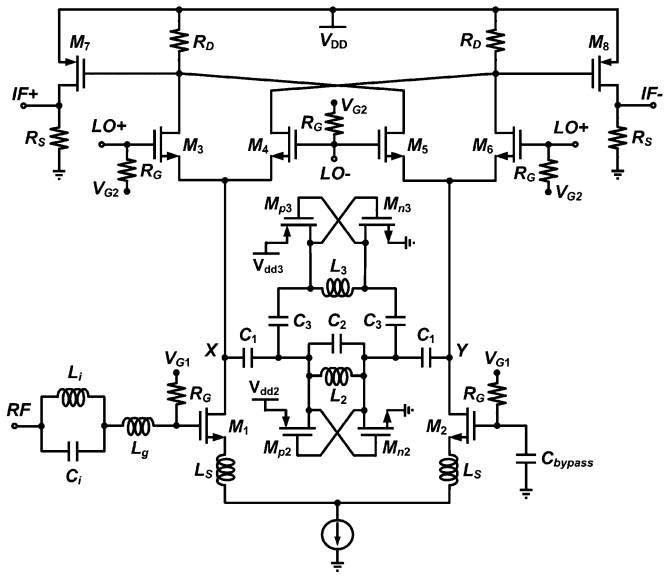

Fig. 1. Complete schematics of the proposed dual-band image rejection mixer.

II. Circuit Design and Analysis

The proposed dual-band image rejection mixer fabricated by 0.18 μm TSMC CMOS process is shown in Fig. 1 with the target dual-band frequencies at 2.4–2.48 and 5.15–5.35 GHz. The common-source differential pair (M_1 and M_2) with one of the inputs grounded by a capacitor can be regarded as a single-ended to differential balun. By appropriately adjusting the bias voltage V_{G1}, a better conversion gain of mixer with minor second order harmonic behavior can be acquired [7]. In addition, the proposed mixer adopts a source-degenerated amplifier with a dual-band input network (L_i, C_i, L_g) to achieve a 50 Ω match at 2.45 and 5.2 GHz. The circuitry in between nodes X and Y is the proposed dual-band active notch filter to be discussed below.

Fig. 2 shows a third-order notch filter, which can provide low and high impedance at the image and wanted frequencies, respectively to effectively attenuate the image signal without deteriorating the in-band performance [8]. In this letter, a differential dual-band image suppression circuitry based on the third-order notch filter topology is proposed and shown in Fig. 3(a). In the following analyses, we utilize the half circuit in Fig. 3(b) to facilitate the discussions. It is obvious that the parallel L-C section is inductive and capacitive at low and high frequencies, respectively; however, it is reversed for the series L-C section. If the resonance frequency is appropriately designed, the

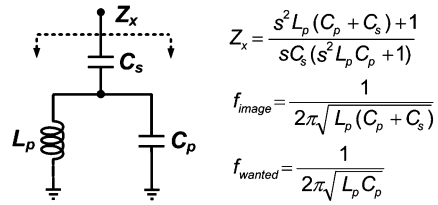

Fig. 2. Third-order notch filter reported in [8].

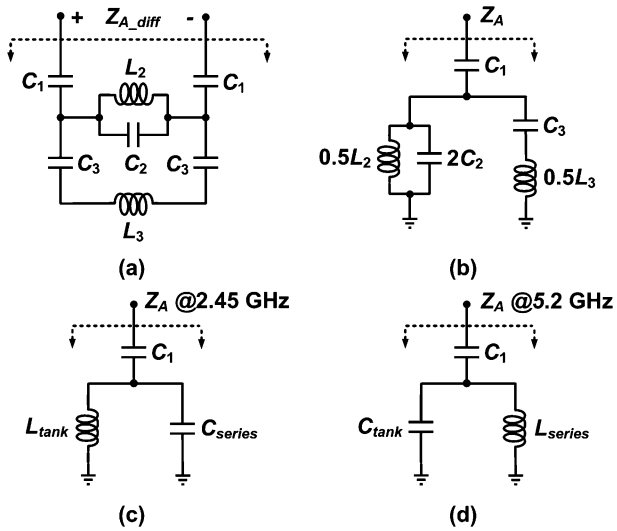

Fig. 3. (a) Proposed differential dual-band third-order notch filter. (b) The half circuit of (a). (c) Equivalent circuit at low frequency. (d) Equivalent circuit at high frequency.

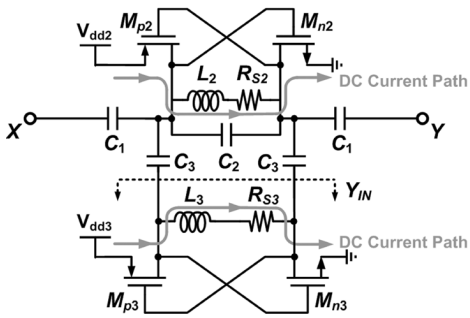

Fig. 4. Poposed differential dual-band notch filter with the negative-resistance cells consisted of NMOS and PMOS transistors.

$0.5L_2-2C_2$ and $C_3-0.5L_3$ circuit in Fig. 3(b) at low frequency such as 2.45 GHz can be equal to an inductor $L_{\rm tank}$ and a capacitor $C_{\rm series}$ shown in Fig. 3(c). Similarly, Fig. 3(d) can be acquired and comprehended by the above ratiocination. As a consequence, the proposed circuitry turns out to be the third-order notch filter in Fig. 2 at low and high frequencies simultaneously. After a straightforward derivation, the input impedance of the filter is given by

$$Z_A = \frac{s^4 0.25B(C_1 + 2C_2) - s^2(0.5L_2C_1 + A) + 1}{sC_1[s^4 0.5BC_2 - s^2 A + 1]} \quad (1)$$

where $A = L_2C_2 + 0.5L_2C_3 + 0.5L_3C_3$, $B = L_2L_3C_3$, from which two zeros and two poles can be obtained in the positive

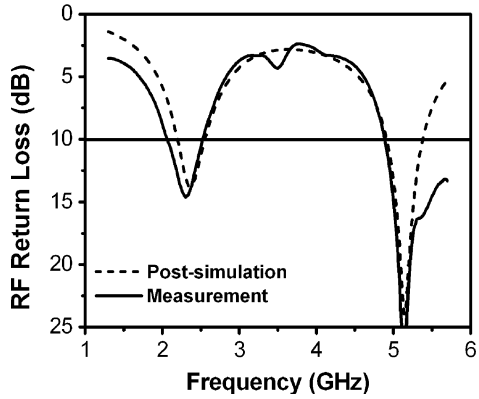

Fig. 5. Measured and simulated RF return loss of the proposed mixer.

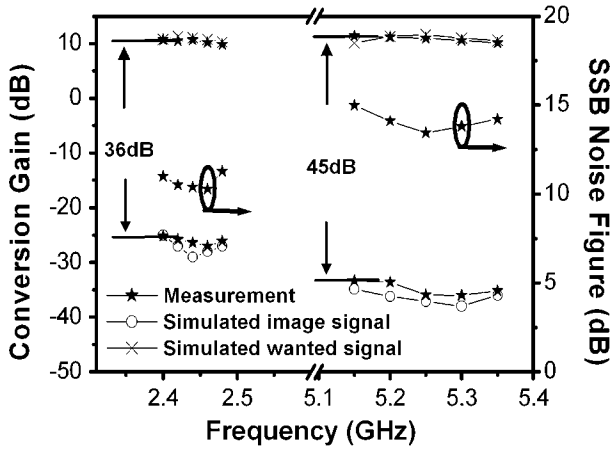

Fig. 6. Conversion gain and noise figure of the proposed mixer.

frequency domain to provide low impedance at dual image frequencies and high impedance at dual wanted frequencies, respectively.

The proposed differential dual-band third-order notch filter can be utilized for the 2.45/5.2 GHz WLAN application. However, it should be taken into account that the maximum attenuation of the image rejection filter is restricted by the series resistance of on-chip inductor. To overcome this limitation, the negative-resistance cell by using cross-coupled transistors can be employed to improve the Q value of on-chip inductor. In this study, the cross-connected pair consisted of NMOS and PMOS transistors as a negative conductance generator is used and shown in Fig. 4. Power consumption and the usage of inductors can be cut in half compared to the traditional approach while providing the same negative conductance. The dc current path will be provided by the on-chip inductor and the impedance $Y_{\rm IN}$ can be expressed as

$$Y_{\rm IN} \approx \frac{1}{j\omega L_3} + j\left(\frac{C_{\rm gsn3}C_{\rm gsp3}}{C_{\rm gsn3} + C_{\rm gsp3}}\right) + \frac{R_{S3}}{(\omega L_3)^2} - \frac{g_{\rm mn3}g_{\rm mp3}}{g_{\rm mn3} + g_{\rm mp3}}. \quad (2)$$

As can be seen in (2), sufficient negative resistance can be generated to eliminate R_{S3} by adjusting the bias voltage $V_{\rm dd}$ since the $g_{mn,p}$ is proportional to the current of transistors. Moreover,

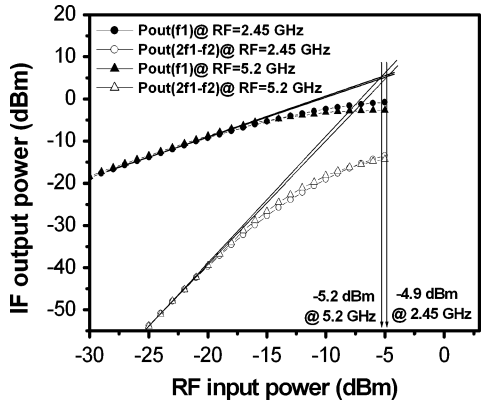

Fig. 7. Measured results of fundamental output power and IM3 for the proposed mixer with RF input frequency spacing of 10 MHz.

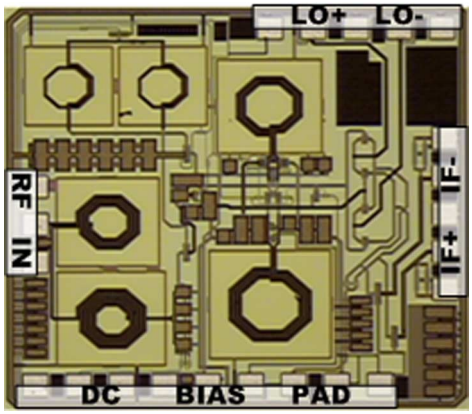

Fig. 8. Microphotograph of the mixer. Die area is 1.07×1.07 mm^2.

TABLE I
COMPARISON WITH PREVIOUS WORKS

Item	This work	[2]	[3]	[4]	[5]	[6]
RF (GHz)	5.2/2.45	8/4	5.2	5.25	5.7/5.2	5.7/2.4
Gain (dB)	11/10.5	-14/-8	11	14	18.5/20	8/9
IP_{1dB} (dBm)	-16/-17	-	-17	-18	-15/-15	-13/-11
IRR (dB)	45/36	N/A	40	40	44/48 *	40/40
NF_{SSB} (dB)	13/10	-	-	7.9	-	25/23
P_{diss} (mW)	10	81	150	58	-	126
Area (mm^2)	1.2	2	7.5	4	5	4
Tech.	0.18μm CMOS	0.18μm CMOS	2μm GaInP/ GaAs HBT	0.18μm CMOS	2μm GaInP/ GaAs HBT	0.18μm CMOS

* only at 5.7 and 5.2 GHz, not in the whole operation bandwidth

the externally controlled and adjustable bias voltages Vdd2 and Vdd3 are required in order to compensate for the process variation and temperature.

III. MEASURED RESULTS

The dual-band mixer chip with image rejection function was mounted on an FR4 test board for the measurement and the dc power dissipation was 10 mW. The simulated and measured results of input return loss are better than 10 dB in the operation bandwidth as depicted in Fig. 5. And as shown in Fig. 6, the measured conversion gain at $\mathrm{RF} = 2.45/5.2$ GHz is $10.5/11$ dB for $\mathrm{IF} = 500$ MHz and $\mathrm{LO} = 1.95/4.7$ GHz. The maximum image rejection is 37 dB and 47 dB respectively. The measured minimum single sideband noise figure at $\mathrm{RF} = 2.45/5.2$ GHz is about 10/13 dB. The two-tone test with 10 MHz tone separation was performed using two Agilent 83640B signal generators and an Agilent 8564EC spectrum analyzer. The measured results of input-referred 1 dB compression point ($\mathrm{IP}_{1\,\mathrm{dB}}$) and input-referred third-order intercept point (IIP3) are depicted in Fig. 7. The values of the measured $\mathrm{IP}_{1\,\mathrm{dB}}$ and IIP3 are $-17/-16$ dBm and $-4.9/-5.2$ dBm when $\mathrm{RF} = 2.45/5.2$ GHz. A die microphotograph of the mixer proposed is shown in Fig. 8 with die area including pads of 1.07×1.07 mm^2. The presented mixer is compared with recently published mixers and summarized in Table I.

IV. CONCLUSION

A 2.45/5.2 GHz image rejection mixer with differential dual-band third-order notch filter has been fabricated and designed. The suppression of about 36/45 dB at the image frequencies can be achieved without worsening the in-band characteristics. In this letter, the dc power consumption and chip area are smaller than the literature presented in [3]–[6] due to the reduction in the complexity of image rejection circuit mechanism.

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