CHAPTER 1

Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In recent years, low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have attracted much attention because they have been used very successfully for active matrix displays, such as active matrix liquid crystal displays (AMLCDs) [1.1]-[1.7] and active matrix organic light emitting displays (AMOLEDs) [1.8]-[1.14]. Expect large area displays, poly-Si TFTs have been applied into some memory device such dynamics random access memories (DRAMs) [1.15], static random access memories (SRAMs) [1.16], and have great potential for 3-dimention ICs' applications [1.17],[1.18].

Compared to conventional a-Si TFTs, the field-effect-mobility of poly-Si TFTs is much higher. Higher field-effect-mobility means transistor can provide higher driving current. The higher driving currents can allow the pixel-switching element TFT's dimension shrinkage, resulting higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. Besides, the superior mobility performance allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry on the same glass substrate, which brings the era of system-on-glass (SOG) that will include a memory, central processing unit (CPU), and display.

. The process complexity can be greatly simplified and manufacturing cost can be

substantially reduced. The ability of fabricating high-performance LTPS TFTs enables their use in a wide range of new applications. Therefore, there is great interest in improving the performance of LTPS TFTs.

In comparison with signal-crystalline silicon, poly-Si suffers many grain boundary defects and intra-grain defects. The order of poly-Si grain size is about 0.1μm. At present, when poly-Si TFTs are used in LCD applications, the minimum feature size is typically much larger than 10μm and therefore a large number of grain boundaries (GBs) are present in the channel. Electrons are scattered at the grain boundaries or trapped by the interface states, leading to lower mobility than in single crystal silicon. Much effort has been made to increase the performance of LTPS TFTs [1.19]-[1.21]. Crystallization of a-Si thin films has been considered the most critical process for fabricating high-performance LTPS TFTs. Among various crystallization technologies, excimer laser crystallization has become the mainstream technology for mass production of flat panel displays (FPDs) because of high throughput, low temperature process compatible with glass substrate, and formation of high-quality poly-Si [1.22].

From the viewpoint of device technologies, various structural improvements, such as offset gate [1.23],[1.24], lightly doped drain (LDD) [1.25],[1.26], multi-gate structure [1.27], and gate-overlapped LDD [1.28]-[1.30] have been proposed. Most of these structures effectively reduce the electric field near the drain junction. Consequently, the anomalous leakage current and kink current of poly-Si TFTs can be effectively reduced accompanying with a promotion of reliability in poly-Si TFTs.

In summary, it is expected that the poly-Si TFTs will becomes increasingly important in future technology, especially when the 3-D circuit integration and SOP era is coming. There are lots of interesting and important topics that are worthy to be researched.

1.2 Electrical Characteristics of LTPS TFTs

Because poly-Si is rich in grain boundary defects as well as intra-grain defects, which lead to degradation in device performance, the electrical characteristics of poly-Si TFTs are much inferior to those of single-crystalline silicon (c-Si) counterparts. This includes higher threshold voltage, lower mobility and higher leakage current.

For n-channel poly-Si TFTs, electron trap centers have an electrical effect similar to that of acceptor-type impurities[1.31]. Generally, the threshold voltage is determined by total charge in the depletion layer near the surface. Therefore, the channel of devices posses more defects simply require larger gate voltage in order to fill the greater number of traps before the device can turn on. Higher threshold voltage implies more defects existing in poly-Si thin-film.

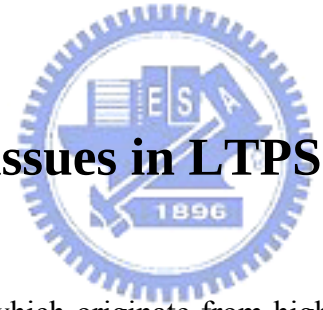
Carrier mobility is degraded because a large number of electronic charges trapped at grain boundaries form the potential barriers, which deteriorate carrier transport in poly-Si. Besides, scattering with charge-trapping centers also degrades carrier mobility.

The anomalous high leakage current is also found in poly-Si TFTs, and the leakage current of LTPS TFT has typically be 5 to10 times larger than that of a-Si TFT and 25 to 50 times worse than c-Si. The dominant leakage current mechanism is the field emission via the traps by high electric field near drain junction [1.32]-[1.34].

The floating-body architecture and charge trapping by defect states results in serious avalanche induced effects in poly-Si TFTs [1.35]. Due to impact ionization occurring in the high electric field region at the drain end of the channel, hole are injected into the floating body forcing further electron injection from the source, and then collected by the drain. This added drain current augments impact ionization which, in turn, forward biases the floating body harder, thereby causing a regenerative action which leads to a premature breakdown. As

a result, the output characteristics exhibit an anomalous current increase in the saturation regime, and such a phenomenon is often called “kink” effect [1.36].

It can be seen that the defect traps place a profound influence on electrical characteristics of poly-Si TFTs. Thus, the most effective approach to improve the performance of poly-Si TFTs is to reduce the defect traps by promoting the quality of poly-Si thin films. Besides, by means of modifying the architecture of poly-Si TFTs to reduced kink effect and leakage current is also important. They include light doped drain (LDD), offset gate structure and gate-overlapped lightly doped drain (GOLDD), etc. Recently, a study on the influence of lateral electric field on anomalous leakage current and kink effect of poly-Si TFT has been reported [1.37],[1.38]. It was found that the high lateral electric field at the channel/drain junction can be effectively reduced by use of a thick drain but thin channel structure.

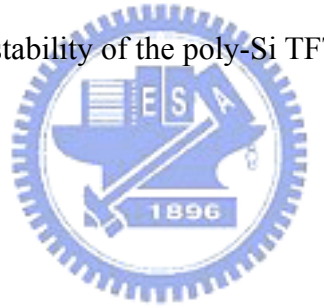


1.3 Reliability issues in LTPS TFTs

The hot-carrier effects which originate from high electric field near the drain junction have been widely investigated in MOSFETs. Due to inferior grain structure, the reliability issue is more essential in LTPS TFTs. Conduction carriers can obtain energy from the high electric field and become “hot”. And then these high-energy carriers can easily break weak Si-Si or Si-H bond existing in poly-Si, creating lots of defect states and oxide trapped charges. Serious degradation can be generated in the hot carrier operation mode (typically Vd>>Vg>Vth), and the degree of degradation depends on the strength of electric field, that is, the energy of the hot carriers. It is already known that the application of high drain voltage and relatively high gate voltage (hot-carrier condition) decreases the maximum transconductance $g_{m\ \max}$ and causes the variation of turn-on voltage V_{ON} [1.39]. The degradation of $g_{m\ \max}$ and V_{ON} variation during stress application is greatly important for

circuit designers in order to integrate TFTs in flat-panel display. Generally, the electric-field-relief TFT structures can reduce the hot carrier degradation, such as LDD, offset drain, and gate-overlapped LDD.

Besides, self-heating effect has also been reported to be another degradation mechanism when poly-Si TFTs were fabricated on poor thermal-conducting substrate, especially for larger width TFTs and/or small length TFTs [1.40]-[1.42]. The threshold voltage, subthreshold swing, on-current and off-current are all degraded by the self-heating effect, which resulted from the high current stress. This was attributed to the state creation caused by self-heating occurring along the overall channel. Self-heating effect is related with thermal conductivity and power dissipation [1.43]. Therefore, the structure to release Joule heat, such as a heat buffer layer with higher thermal conductivity under the channel or with divided channel patterns, can improve stability of the poly-Si TFTs effectively [1.44].



1.4 Motivation

In order to make LTPS TFTs suitable for advanced circuits, besides the improvement of performance of LTPS TFTs, the improvement of reliability is also significant. Therefore, reliability testing and understanding of reliability mechanisms become more and more necessary.

The instability mechanisms of LTPS TFTs under DC (direct current) bias stress have been widely discussed. However, up to now, the reliability of LTPS TFTs under AC (alternating current) bias stress has been paid much less attention. First, in practice, the LTPS TFTs used as switching elements for AMLCDs are operated in an AC mode, thus AC stress is much closer to real operational condition than conventional DC stress testing. Then, unlike pixel TFTs, the TFTs in driver circuits are subjected to high-frequency voltage pulses. In the

SOP, different circuits will require the different operating frequencies. Last, for the power consumption consideration, CMOS technology is necessary for the driving circuits, therefore the reliability for n- and p-channel LTPS TFTs are very important. Therefore, it is extremely important to understand the degradation mechanisms of p- and n-channel LTPS TFTs under AC bias stress.

In this study, the threshold voltage and mobility shifts of p- and n-channel LTPS TFTs under various AC stress conditions, including frequencies, amplitudes, falling/rising times, and duty ratios, were discussed to verify the degradation mechanism under AC bias stress.

1.5 Thesis Organization

In this thesis, the phenomena and mechanisms of device degradation are studied for n- and p-channel low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) by electrical AC stress.

In chapter 2, experimental procedures will be introduced, including the fabrication of LTPS TFTs, setup of measurement equipment, and measurement methods. Besides, the methods of the electrical parameter extraction will be introduced. In the end, there will be a review of stability mechanisms under AC stress.

In chapter 3, the degradation phenomena and instability mechanism of p-channel LTPS TFTs were investigated in detail under different AC stress region with various frequencies, rising/falling times, and base voltages. The DC stress was also performed to compare with AC stress. Hot-carrier induced degradation mechanism in p-channel LTPS TFTs under AC stress was proposed.

In chapter 4, the degradation phenomena and instability mechanism of n-channel LTPS TFTs were investigated in detail under different AC stress region with various frequencies,

falling times, and base voltages. The DC stress was also performed to analyze the observed degradation phenomena under AC stress. Besides, the simulation was also performed. By analyzing the degradation behaviors with electrical measurement and simulation, the instability mechanisms of LTPS TFTs under AC stress were identified.

Finally, summary and conclusions are given in chapter 5.

CHAPTER 2

Experimental Procedures and Review of Instability Mechanisms under AC stress

2.1 Procedures of Fabrication of LTPS TFTs

The low-temperature poly-silicon thin film transistors (LTPS TFTs) used in the experiment were the conventional top-gate structure and fabricated on the glass substrates. The cross-section views of p- and n-channel LTPS TFTs are shown in Fig. 2-1 and Fig. 2-2, respectively. The basic process flow is described as follows. First, the buffer oxide and a-Si:H films were deposited on glass substrates by the PECVD system. Then, XeCl excimer laser was used to crystallize a-Si:H film followed with poly-Si active area definition. Subsequently, gate insulator was deposited by PECVD. The thickness of gate oxide is 1000Å. Next, the metal gate formation and source/drain doping were performed. Dopant activation and hydrogenation was carried out after interlayer dielectric deposition. Finally, contact holes formation and metallization were performed to complete fabrication work. The lightly doped drain (LDD) structure was used in the n-channel TFTs to enhance hot carrier endurance. The width/length of the TFT was 20 μm/6 μm. The TFTs of the same dimension will be used for reliability testing in the chapter 3 and 4.

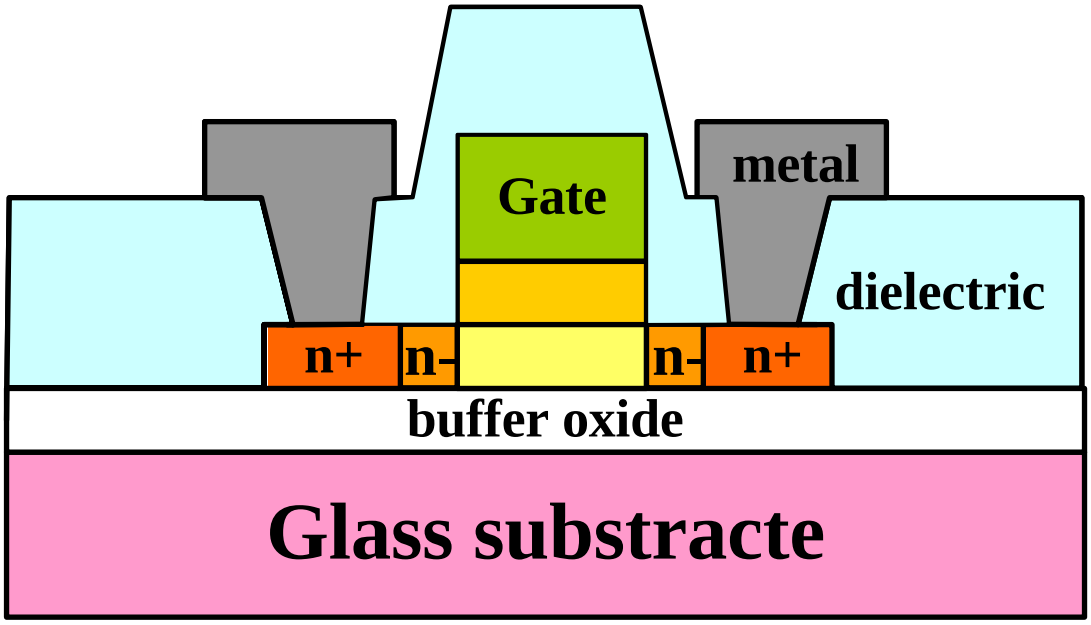


Fig. 2-1 The cross-section views of n-channel LTPS TFTs with LDD structure

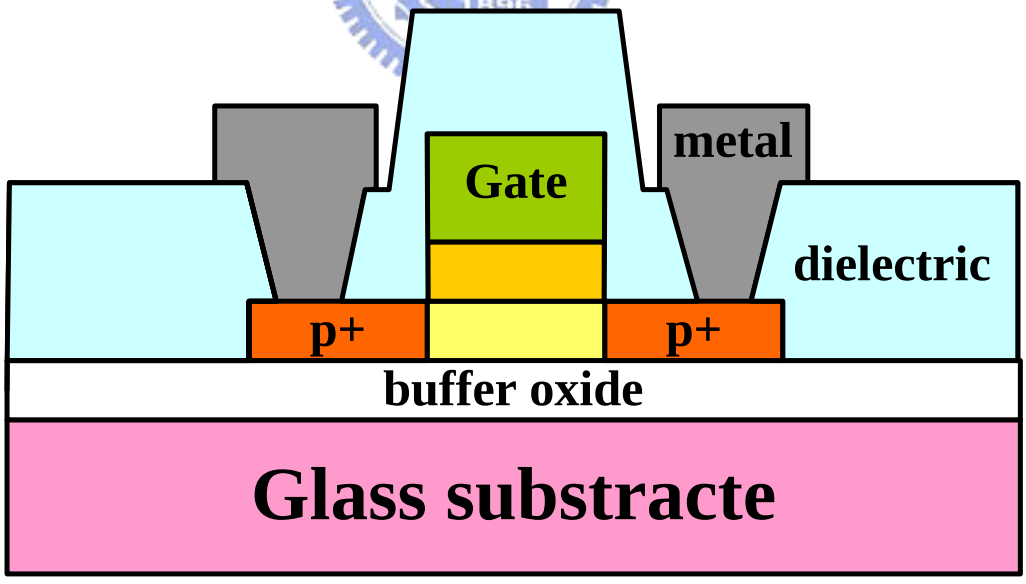


Fig. 2-2 The cross-section views of p-channel LTPS TFTs

2.2 Setup of Measurement Equipment and Extraction of the electrical parameters

2.2.1 Configuration of the Measurement Equipments

The measurement equipments used in this study consist of HP 4156C precise semiconductor parameter analyzer, HP41501A pulse generator and HP 16440A SMU/PGU selector. The HP41501A is used to generate the AC pulse signal, including pulse amplitude, frequency, and duty ratio to stress poly-Si TFTs. After AC signal stress, the TFT is measured by HP4156C to extract the electrical parameter, including threshold voltage, subthreshold swing, and mobility. Fig. 2-3 illustrates the diagram of the bias stress measurement equipments.

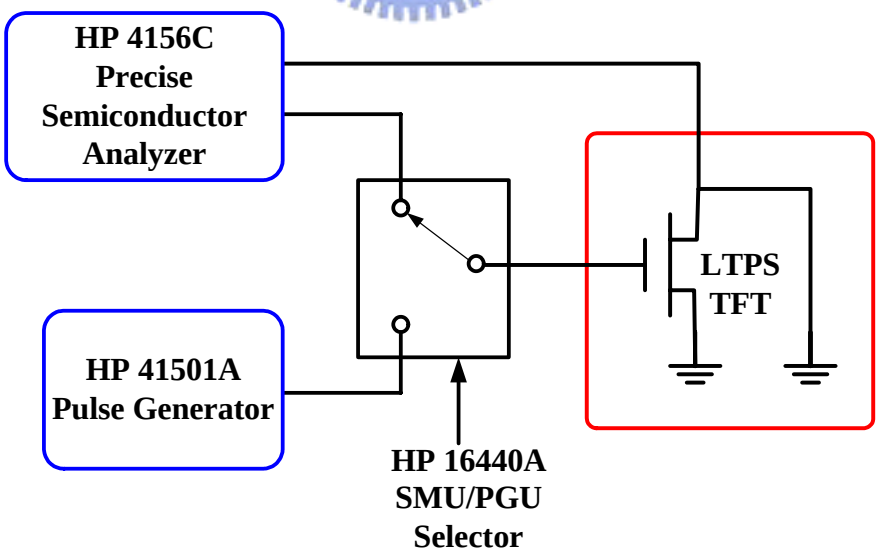


Fig. 2-3 Measurement configuration for the p-channel poly-Si TFT

2.2.2 Waveform of the AC Signal

The AC signal used in this study consists of signal amplitudes, frequencies, and duty ratios. We can adjust these parameters and then perform various stress conditions on the gate electrode to realize the instability of LTPS TFTs under different swing regions. Fig. 2-4 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is given as follow:

$$t_c = t_{vp} + t_f + t_{vb} + t_r \tag{2.1}$$

$$f = 1/\, t_c \tag{2.2}$$

$$D.R. = (t_{vp} + t_r)/\, t_c \tag{2.3}$$

Where t_c is the signal period, f is the signal frequency and $D.R.$ is the duty ratio.

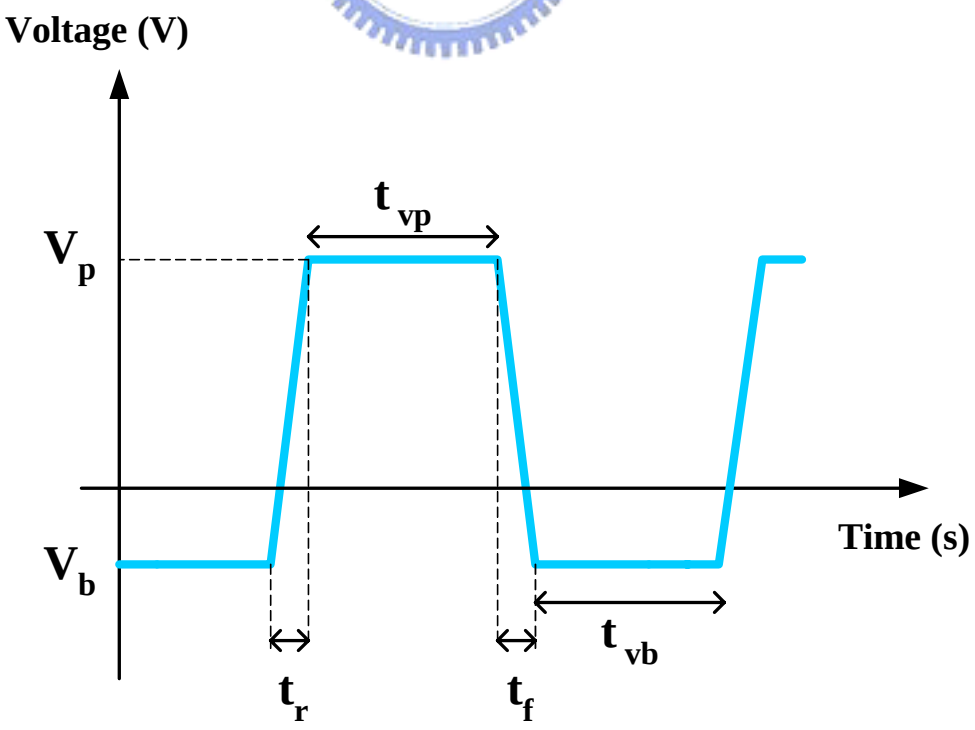


Fig. 2-4 Waveform and definition of the AC signal

In the waveform of AC signal, V_p is defined as the peak voltage, while V_b is defined as the base voltage. The frequency (f) is equal to $1/t_c$, where the t_c is the signal period and the duty ratio is defined as eq.(2.3) where t_{vp}, t_{vb}, t_f, t_r is the time of peak voltage, the time of base voltage, the falling time, the rising time, respectively, and the sum of t_{vp}, t_{vb}, t_f, t_r is equal to t_c.

2.2.3 Measurement Methods

HP 4156C precise semiconductor parameter analyzer was used to perform the stress measurement on the TFTs and extract the transfer characteristics after DC bias stress. Besides, combining the HP41501A pulse generator with HP 4156C precise semiconductor parameter analyzer, the stress measurement were performed on the TFTs and the transfer characteristics were extracted after AC bias stress.

Both of the DC and AC bias stress measurements were performed up to 1000s and interrupted at a specific time to measure the transfer curves at the drain-to-source voltage (V_{ds}) of 0.1V (in linear region). At last, the electrical characteristics of poly-Si TFTs were extracted by an HP 4156C electrical analyzer.

2.2.4 Extraction of Device Electrical Parameters

The methods of the typical electrical parameter extraction will be introduced in the following, including threshold voltage, field-effect mobility, subthreshold swing, on-current, and leakage current.

2.2.4.1 Determination of the Threshold Voltage (V_{th})

The method to determine the threshold voltage in this thesis is the constant drain current method, which is adopted in most studies of TFTs. The threshold voltage is defined as the gate voltage which yields a normalized drain current (i.e. the threshold current). Typically, the threshold current is specified as 10nA at $|V_{ds}|$=0.1V in most papers to extract the threshold voltage.

2.2.4.2 Determination of the Field Effect Mobility (μ_{FE})

The field effect mobility (μ_{EF}) is determined from the transconductance gm at low drain bias. The transfer characteristics of poly-Si TFTs can be derived by a gradual channel approximation. The relation can be expressed as

$$I_d = \mu_{FE} C_{ox} \frac{W}{L}[(V_{gs} - V_{th})V_d - \frac{1}{2}V_d{}^2] \quad (2.1)$$

Where

C*ox* is the gate oxide capacitance per unit area,

W is channel width,

L is channel length, and

V*th* is the threshold voltage.

The transconductance is defined as

$$g_m = \left.\frac{\partial Id}{\partial Vg}\right|_{Vd=const.} = \mu_{FE} \frac{W}{L} C_{ox} V_d \quad (2.2)$$

Therefore, the field effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox} W V_d} g_m \quad (2.3)$$

2.2.4.3 Determination of the Subthreshold Swing (*SS*)

Subthreshold swing is a measure of the efficacy of the gate potential to modulating drain current. It is defined as the amount of gate voltage to increase and/or decrease drain current by one order of magnitude. It can be shown that the expression for *SS* is given by

$$SS = \frac{\partial V_g}{\partial(\log I_d)} \tag{2.4}$$

Clearly, the smaller the value of *SS*, the better the transistor is as a switch. A small value of *SS* means a small change in the input bias can modulate the output current considerably.

2.2.4.4 Determination of the On-Current (I_{on}) and Off-Current (I_{off})

Ion is an indicator of driving ability. A high Ion enable TFTs to provide sufficiently high drive current, which results in shorter pixel capacitance charging time and high aperture ratio. A low Ioff enable TFTs to hold the current during off-stage, which results in high aperture ratio. In this thesis, the on current is specified by the maximum drain current at $|V_{ds}|$=5V and $|V_{gs}|$=20V, while the off current is specified by the minimum drain current at $|V_{ds}|$=5V.

2.3 Variation of Experimental Electrical Parameters

In MOSFETs, electrical parameters such as threshold voltage, transconductance, and subthreshold swing depend on oxide trapped charges and interface states [2.1],[2.2]. However, in poly-Si TFTs, not only the carrier injected into gate oxide and the interface state generation but also state generation in the grain boundaries /intra-grain, should be considered to clarify the degradation mechanism. The deep traps existing in grain boundaries have been demonstrated to affect mainly threshold voltage and much less g_m [2.3]-[2.6]. On the contrary, tail states from grain regions in the interface and/or from grain boundaries mainly contribute to the decrease of g_m [2.3],[2.4],[2.6]. The subthreshold slope depends mainly on intra-grain traps distributed uniformly inside the poly-Si film and also on the deep interface states [2.7]. Therefore, poly-Si TFTs degradation can be clarified by analyzing the variation of electrical parameter after stress. These points are summarized on the Table 2-1.

Table 2-1 Variation of electrical parameters and the corresponding possible degradation mechanics

Electrical parameters after stressing	**Mainly depending on**
Δgm	● interface state generation ● state generation in the grain boundaries(tail states)
ΔVth	● charges injected into gate oxide ● interface state generation (deep states) ● state generation in the grain boundaries (deep states)
ΔS	● intra-grain defect density generation (bulk states) ● interface state generation (deep state)

2.4 Review of Instability Mechanisms under AC stress

Toyota et al. also proposed that mobile carriers are able to follow the transient variation of gate voltage while the electrons trapped in the midgap state aren't [2.8]. Besides, Uraoka et al. attributed the dominant ac degradation mechanism to hot electrons generated by trapped electrons exposed to the high electric field and gain energy from the electric field during ac stress [2.9]. The mechanism was analyzed by using a picosecond emission microscope and a device simulation to examine the transient current experimentally and theoretically, respectively.

The degradation model under ac stress is described as follow. When the gate voltage is high, the electrons gather to form a channel shown in Fig. 2-5(a). When the gate voltage drops, the electrons in the channel move rapidly to the source and drain shown in Fig. 2-5(b). Some of the trapped electrons are exposed to the high electric field and grain energy from the field. Hot electrons are generated at this moment and form electron traps shown in Fig. 2-5(c), and a density of state (DOS) in tail edge of poly-Si is increased by the hot electrons.

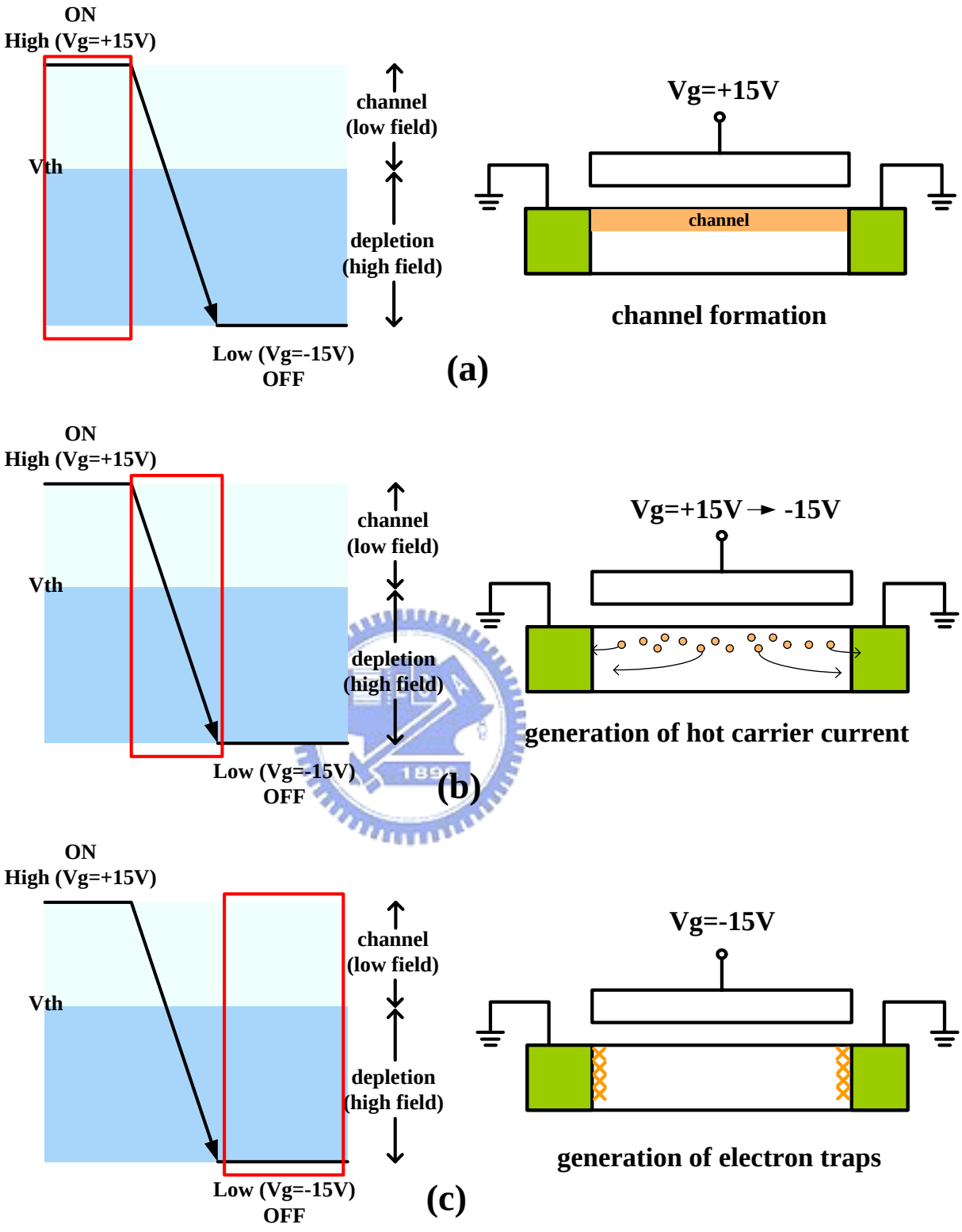


Fig. 2-5 A schematic diagram for degradation model of the poly-Si TFT

CHAPTER 3

Instability of Low-Temperature poly-Si p-channel Thin-Film Transistors under AC Gate Bias Stress

3.1 Introduction

Hot carrier effect in low-temperature poly-Si thin film transistors (LTPS TFTs) becomes particularly significant as their dimensions are reduced [3.1]. Several works have pointed out that the instability of polysilicon TFTs is more serious than that of single-crystalline silicon MOSFETs after electrical stress [3.2]-[3.4]. The lower stability of polysilicon TFTs is due to the high density of intra-grain and grain boundary defects, the poor properties of the gate insulator and the poor polysilicon/oxide interface [3.5]-[3.7]. The instability of n-channel polysilicon TFTs was explained by different degradation mechanisms, such as defect state generation in the polysilicon film, hot-carrier induced interface state generation and charge trapping in the gate insulator [3.4],[3.8]-[3.11]. Until now, the stability of p-channel polysilicon TFTs has not been investigated as much as n-channel polysilicon TFTs. Furthermore, little work was investigated on the stability of short-channel polysilicon TFTs under ac stress [3.12].

In this chapter, the mechanism of device degradation under ac stress of different operating region will be discussed. The threshold voltage shifts and the mobility changes of LTPS TFTs under various conditions, including frequency, rising/falling time, and amplitude,

are discussed. The fabrication of LTPS TFTs, measurement methods and sequences are provided. Then, by varying various stress conditions (i.e. signal frequency, rising time etc.), the mechanism of device degradation under ac stress of different swing region will be proposed and identified.

3.2 Measurement Methods and Sequences

The experiment was divided into two parts. One is AC (alternating current) stress, and the other is DC (direct current) stress.

Under AC stress, pulse voltage was applied to the gate electrode and source and drain were grounded, which is shown in Fig. 3-1(a). A rectangular pulse was used with various frequencies, rising/falling times and duty ratios to investigate the device degradation under different operating regions. The signal frequencies ranged from 20kHz to 500kHz, and rising times ranged from 100ns to 500ns. The pulse swing region was separated into two parts; one was the ON region, and the other was the OFF region as shown in Fig. 3-1(b). The ON region means the pulse swing over threshold voltage where the channel region was formed. The OFF region means pulse swing under threshold voltage where the channel region was fully depleted. The HP41501A pulse generator and HP 4156C precise semiconductor parameter analyzer were used to perform the stress measurement on the TFTs and extract the transfer characteristics after AC bias stress.

Under DC stress, the stress gate voltage were -4V, -8V, -12V, and –16V, respectively, with a fixed drain voltage of –16V. HP 4156C precise semiconductor parameter analyzer was used to perform the stress measurement on the TFTs and extract the transfer characteristics

after DC bias stress.

Both of the DC and AC bias stress measurements were performed up to 1000s and interrupted at a specific time to measure the transfer curves at the drain-to-source voltage (V_{ds}) of 0.1V (in linear region). At last, the electrical characteristics of poly-Si TFTs were extracted by an HP 4156C electrical analyzer. The field effect mobility is extracted from maximum transconductance in the linear region of I_d -V_g characteristics at $|V_{ds}|$=0.1V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of I_d = (W/L) x 10^{-8} A at $|V_{ds}|$ = 0.1V. The Vth shift is defined as the difference between V_{th2} and V_{th1}, where V_{th1} is the threshold voltage before stress and V_{th2} is the threshold voltage after stress.

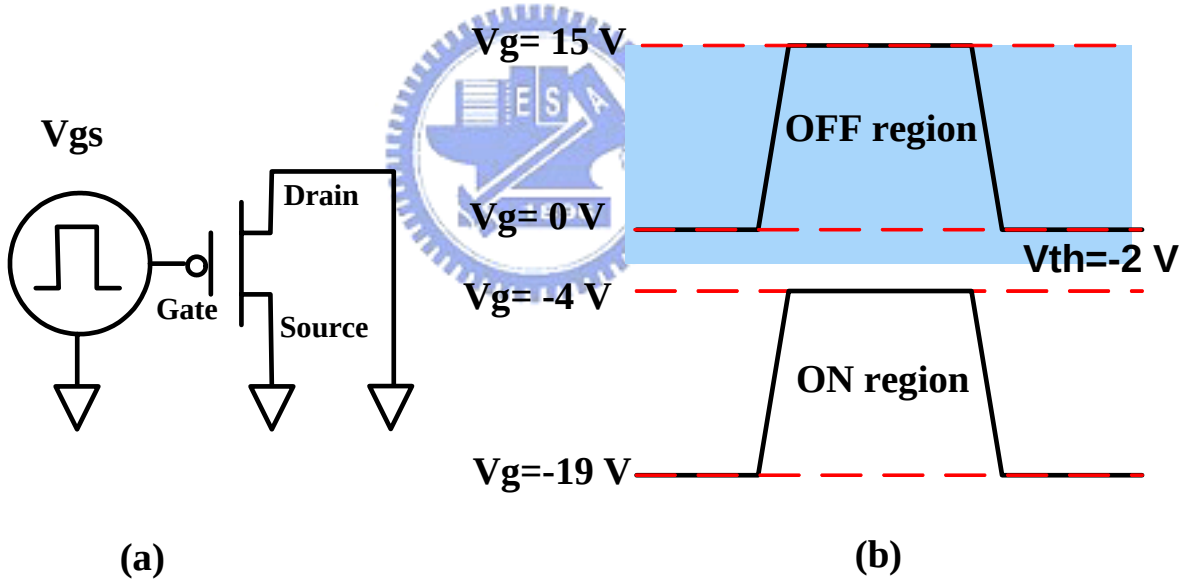


Fig. 3-1(a) Stress configuration (b) The swing region was separated into the ON and OFF regions.

3.3 Experimental Results and Discussion

3.3.1 Degradation under AC stress

3.3.1.1 Frequency Dependence

To compare the device degradation of the ON region stress with the OFF region stress, various frequencies range from 20 kHz to 500 kHz were applied at a fixed $t_r = t_f$ =100ns and the experimental results will be discussed in detail.

Fig. 3-2 to Fig. 3-4 illustrate the comparison of the degree of the mobility variation under ON and OFF region stress of different signal frequencies. The mobility variation is expressed as the ratio of degraded mobility (μ_f) to initial mobility (μ_i). The device degradation in our work means the variation of electrical parameters in LTPS TFTs after stress. Device degradation under the OFF region stress was larger than the ON region stress. There is no difference of the results between the high and low frequencies from the mobility degradation (μ_f/μ_i).

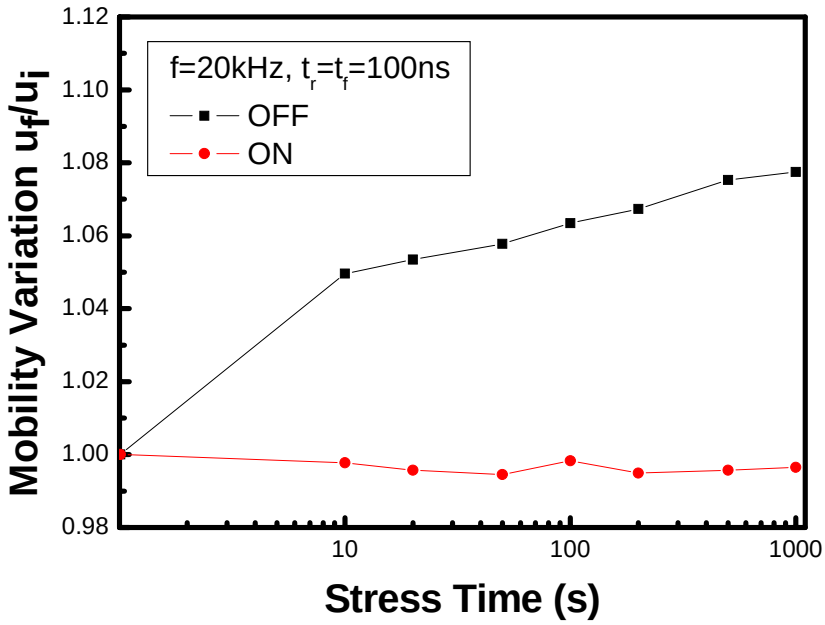


Fig. 3-2 Comparison of the degree of the mobility variation under ON region and OFF region at frequency of 20 kHz.

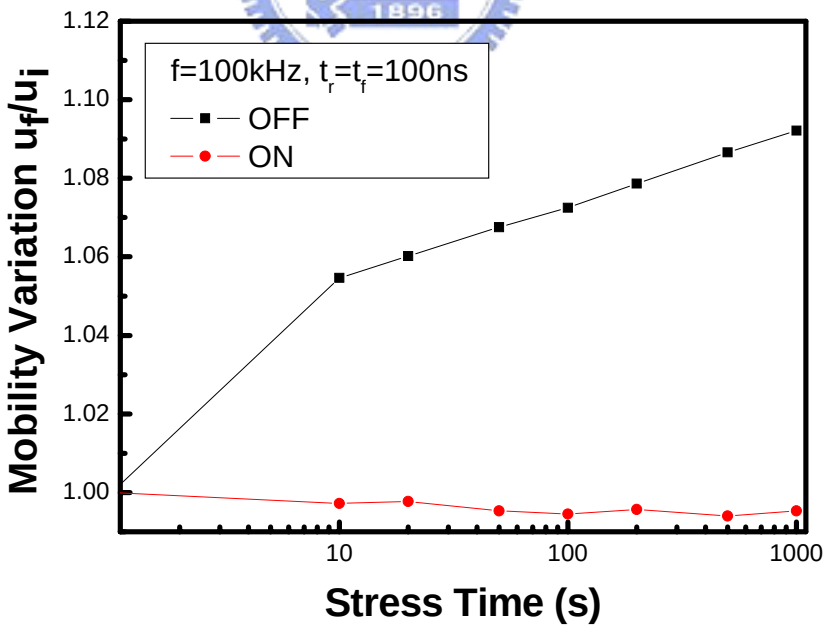


Fig. 3-3 Comparison of the degree of the mobility variation under ON region and OFF region at frequency of 100 kHz.

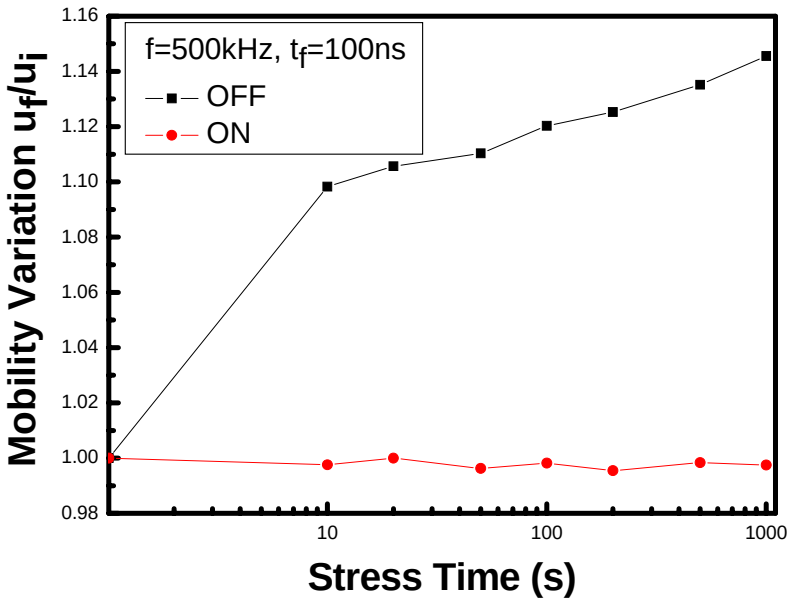


Fig. 3-4 Comparison of the degree of the mobility variation under ON region and OFF region at frequency of 500 kHz.

The mobility variation under the ON and OFF regions at various frequencies was shown in Fig. 3-5. The degradation under the OFF region was enhanced by the increase of frequency, while that under the ON region one was independent of the frequency. The degradation under the ON region was small, however, that under the OFF region was large. Fig. 3-6 indicates the mobility variation of poly-Si TFTs stressed at various signal frequencies. The degradation of poly-Si TFTs shows frequency dependence under OFF region stress, but is almost constant under ON region stress. Fig. 3-7 shows the transfer characteristics (Id-Vg) for the poly-Si TFT before and after 1000s OFF region stress. It can be observed that the mobility and on current were increased, while the leakage current and absolute value of threshold voltage (|Vth|) were decreased. Fig. 3-8 shows the transfer characteristics (Id-Vg) for the poly-Si TFT before and after 1000s ON region stress. The electrical characteristics of poly-Si TFT under ON region stress are nearly unchanged.

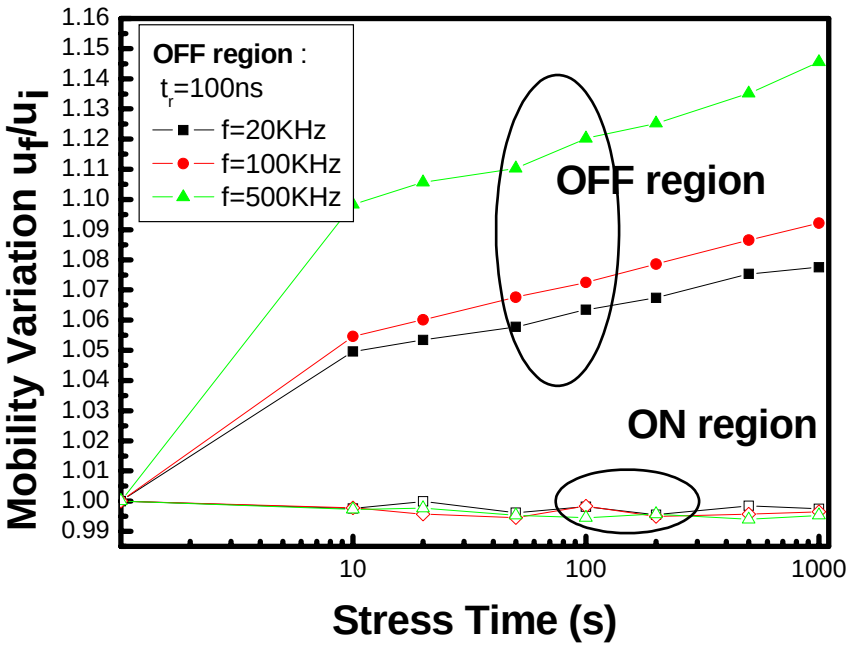


Fig. 3-5 Dependence of swing region on the mobility variation

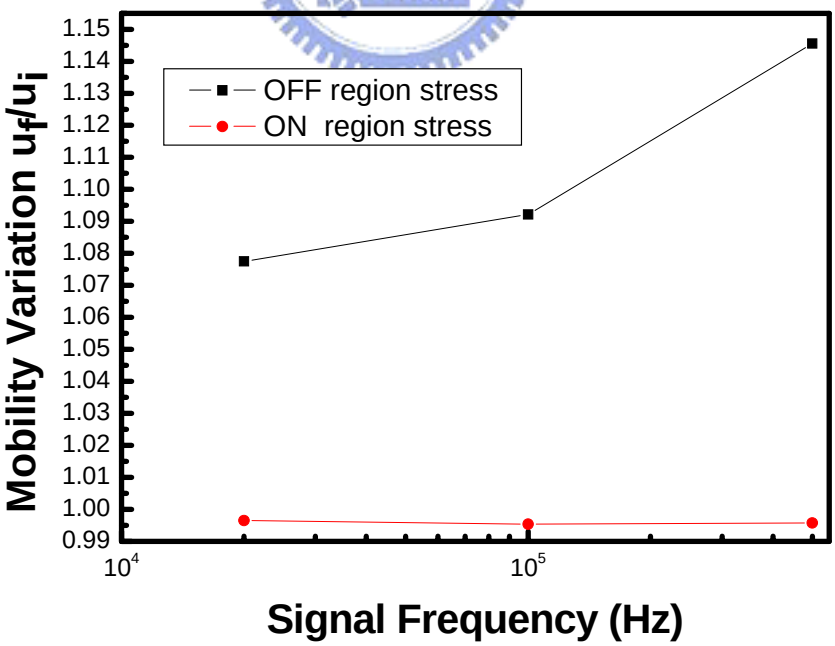


Fig. 3-6 Frequency dependence of the mobility variation for poly-Si TFTs under ON and OFF region stresses

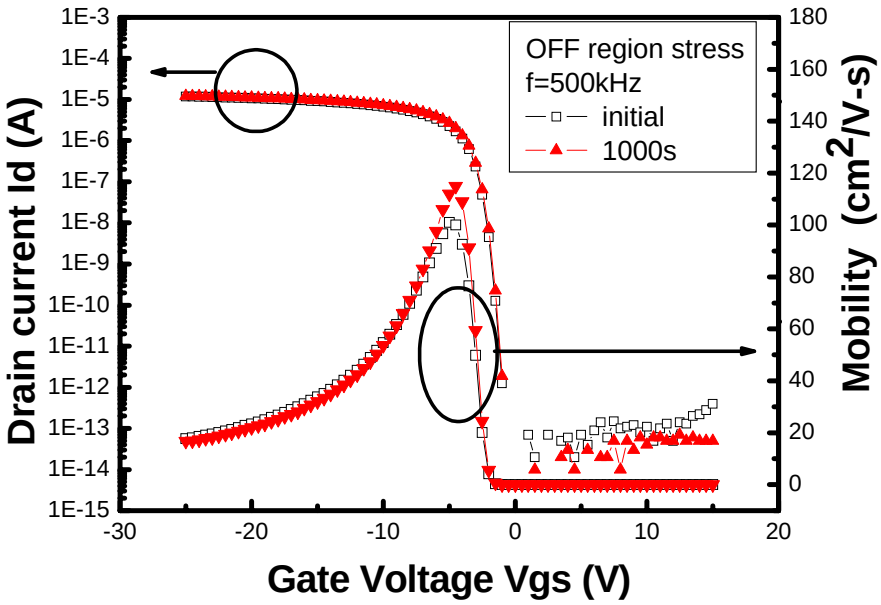


Fig. 3-7 Degradation of p-channel TFT after OFF region stress at frequency of 500 kHz. With stress time increasing, on current and mobility were increased, while the leakage current and |Vth| were decreased.

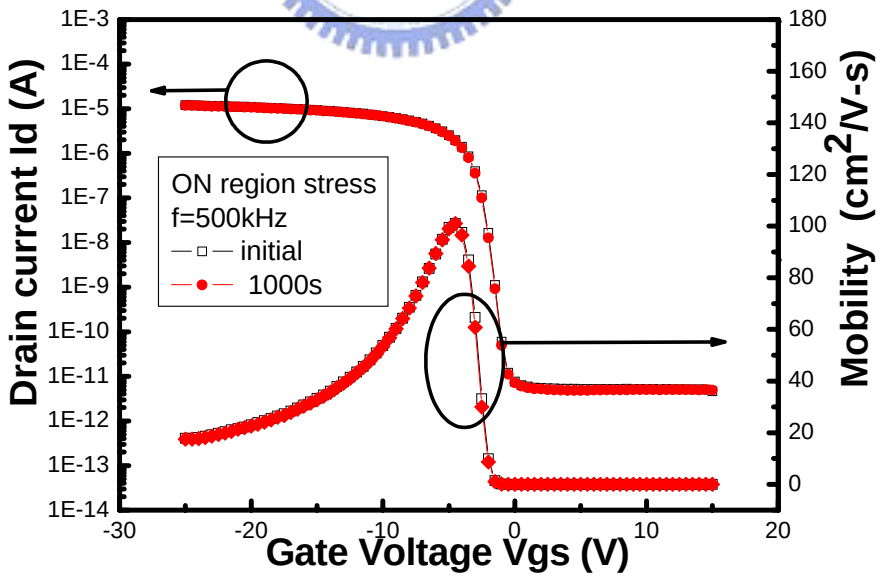
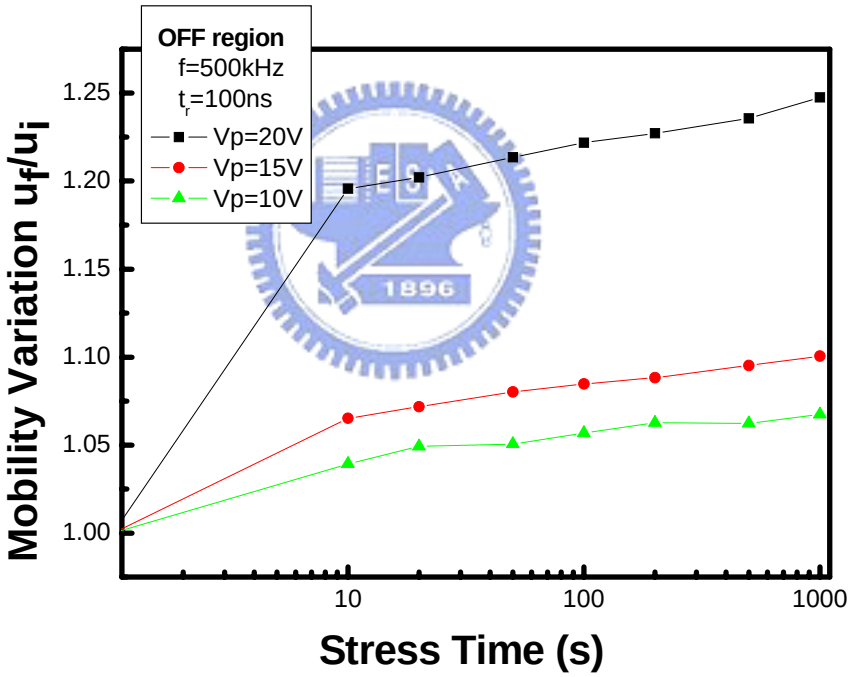


Fig. 3-8 Degradation of p-channel TFT after ON region stress at frequency of 500 kHz. With stress time increasing, drain current and mobility were nearly unchanged.

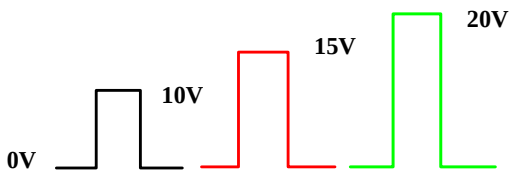
Due to almost unchanged electrical parameters after ON region stress, only the degradation under OFF region stress will be discussed in the following two sections.

3.3.1.2 Peak Voltage Dependence

Internal electrical field under OFF region stress was larger when operating at a larger peak voltage (i.e. a larger amplitude). Therefore, it can be expected that the degradation is severer under larger peak voltage. The result was shown Fig. 3-9.



(a)



(b)

Fig. 3-9 (a) Peak voltage dependence on the device degradation under OFF region stress at frequency of 500kHz (b) Three rectangular pulses with different peak voltages

3.3.1.3 Rising time dependence

Fig. 3-10 shows the rising time dependence on the mobility variation at frequency of 500 kHz and falling time of 100 ns. The degradation is enhanced by the decrease in the rising time.

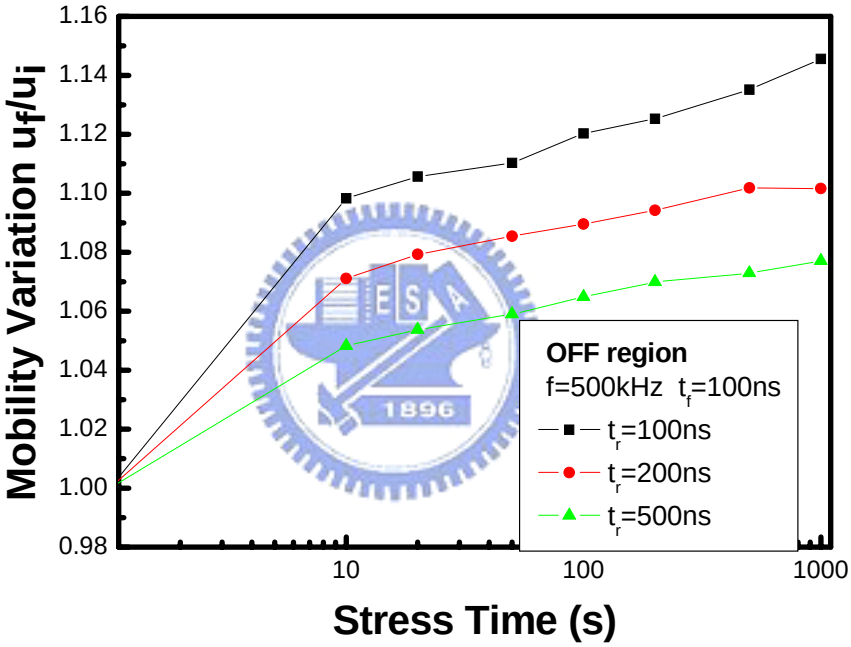


Fig. 3-10 Rising time dependence on the mobility variation.

In addition, the duty ratio and falling time effect were also been investigated. Fig. 3-11 shows the mobility variation versus stress time with various duty ratios (D.R.) and falling times (tf). It was observed that the degradation is independent of duty ratio and falling times. It means that only when the rising time period (i.e. the device is turning off) will the device

performance be affected. Due to duty ratio independence, it can be inferred that the duration of peak voltage, i.e. Vg=15, does not enhance the degradation. Fig. 3-12 shows almost unchanged mobility after stress at Vg=15V and Vd=Vs=0V. That is to say, the duration of peak voltage has little effect on the device performance, which is quite different from amorphous silicon thin film transistors [3.13]. Compared to falling time effect, rising time has much greater effect upon the device degradation. This is due to the depletion of carrier in the channel, when the gate pulse falls.

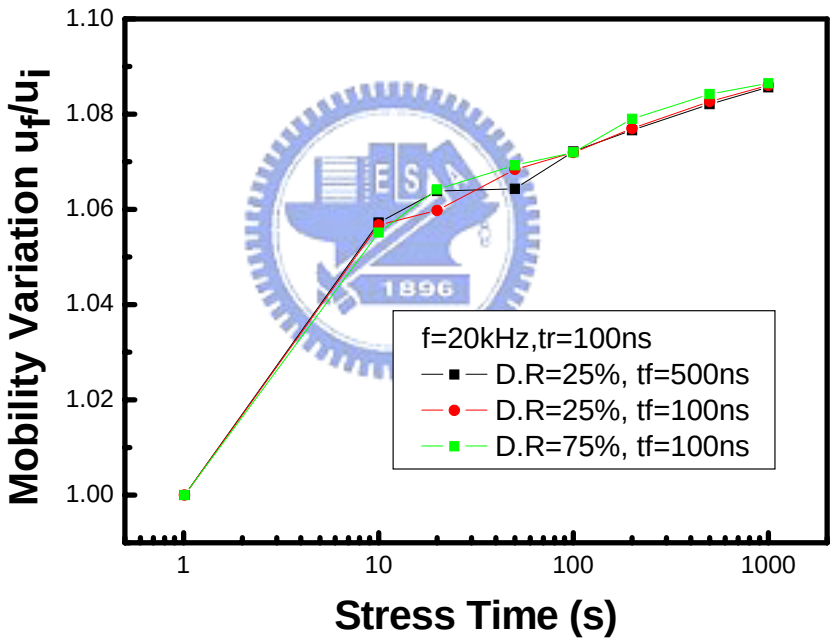


Fig. 3-11 Mobility variation versus stress time with various duty ratios (D.R.) and falling times (tf).

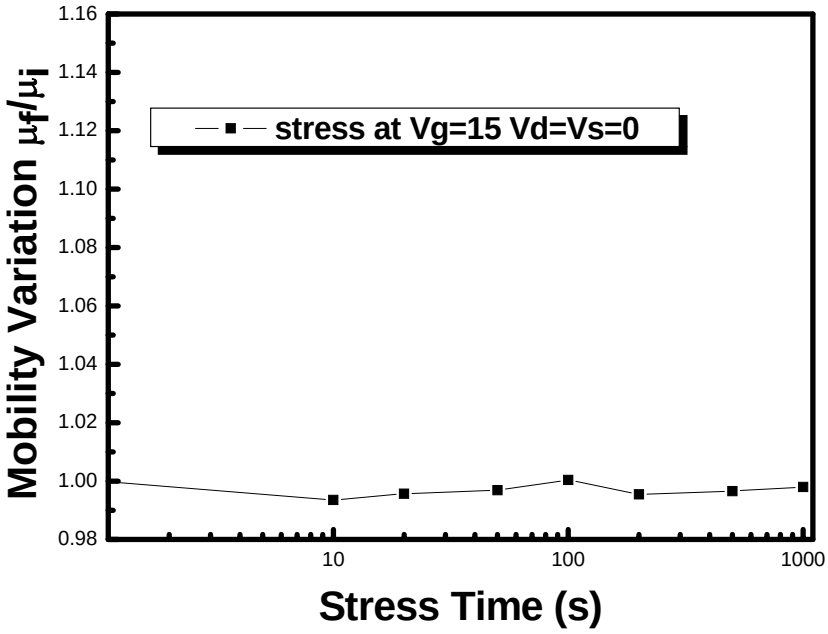


Fig. 3-12 Mobility variation versus stress time after stressing at Vg=15V and Vd=Vs=0V.

3.3.2 Hot-carrier-induced degradation in p-channel low-temperature poly-Si TFTs (LTPS TFTs)

The degradation of threshold voltage (Vth), mobility (μ), and on/off current ratio in p-channel MOSFET's is dependent on hot-carrier stress conditions [3.8], [3.14], [3.15]. In other words, these electrical parameters can be either increased or decreased after particular bias stress. The same phenomenon of device degradation can be observed in p-channel TFTs [3.16], [3.17]. The shifts of the electrical parameters show different behaviors under strong and weak current saturation stress owing to different degradation mechanisms.

P-channel LTPS TFTs were stressed at a fixed drain voltage (Vd=-16V) over the entire

range of device saturation, i.e. 0<|Vg|<|Vd|. Two different device degradation behaviors were observed in Fig. 3-13. Under strong current saturation (i.e. small |Vg|), the threshold voltage is improved, while degraded under weak current saturation (i.e. large |Vg|).

Under strong saturation current stress, mobility has a positive shift with time, which was shown in Fig. 3-14. Similarly to the threshold voltage, mobility has an opposite shift after weak saturation current stress, which was shown in Fig. 3-15.

Under strong current saturation, hot electrons are pulled into the gate oxide near the drain region. The trapped electrons produce an electric field which reenforces the gate-field line near the interface. As a consequence, the energy band bends deeper, mobile hole density increases. Therefore, mobility (μ) should increase and Vth shift should increase. The reason is in agreement with the effective short channel effect, i.e., hot-electron-induced punchthrough effect [3.18]. Fig. 3-16 illustrates the schematic diagram of hot-electron injection induced channel shortening.

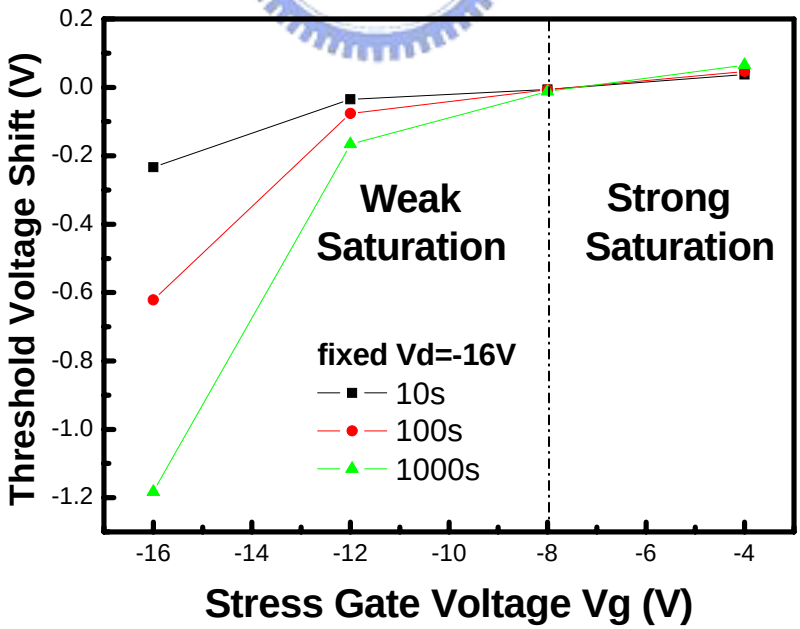


Fig. 3-13 Threshold voltage shift versus gate voltage for fixed Vd=-16V at different stress times.

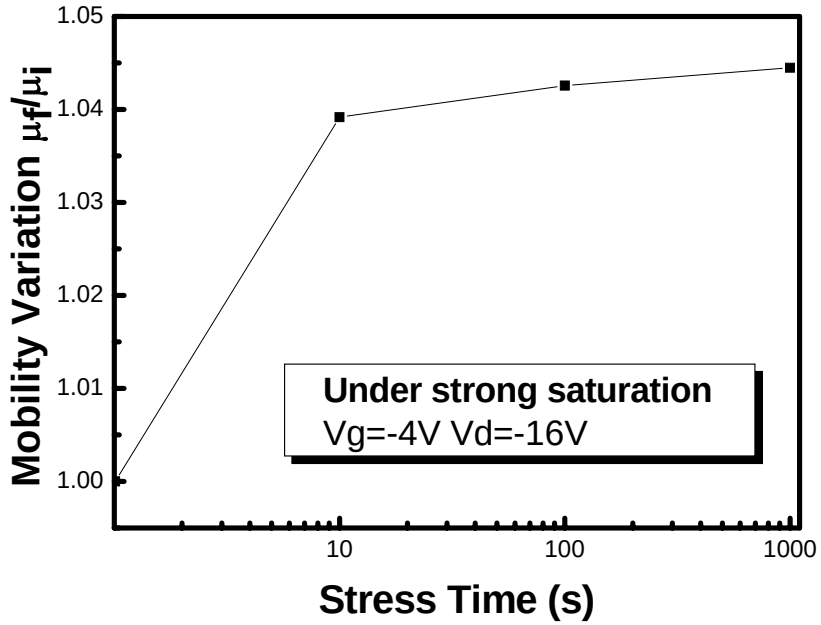


Fig. 3-14 Mobility variation versus stress time under strong saturation: Vg= -4V and Vd= -16V

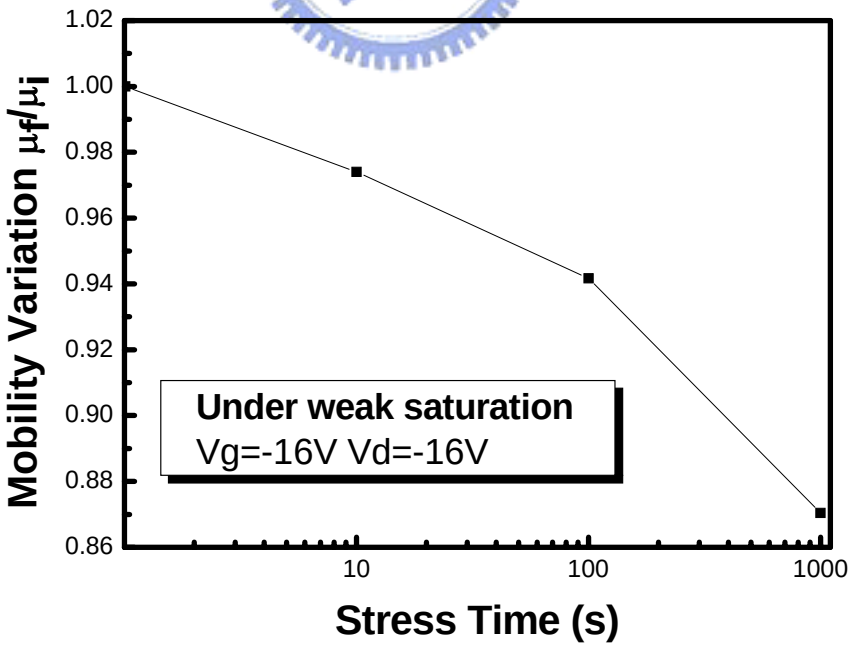


Fig. 3-15 Mobility variation versus stress time under weak saturation： Vg= -16V and Vd= -16V

Under weak current saturation, high vertical electric field in the channel causes holes trapped in gate oxide near the drain region [3.14]. The trapping of hot hole as well as the generation of donor-type interface states gives rise to degraded electrical characteristics exactly opposite to that of hot electrons, which results in the degradation of the threshold voltage and the mobility.

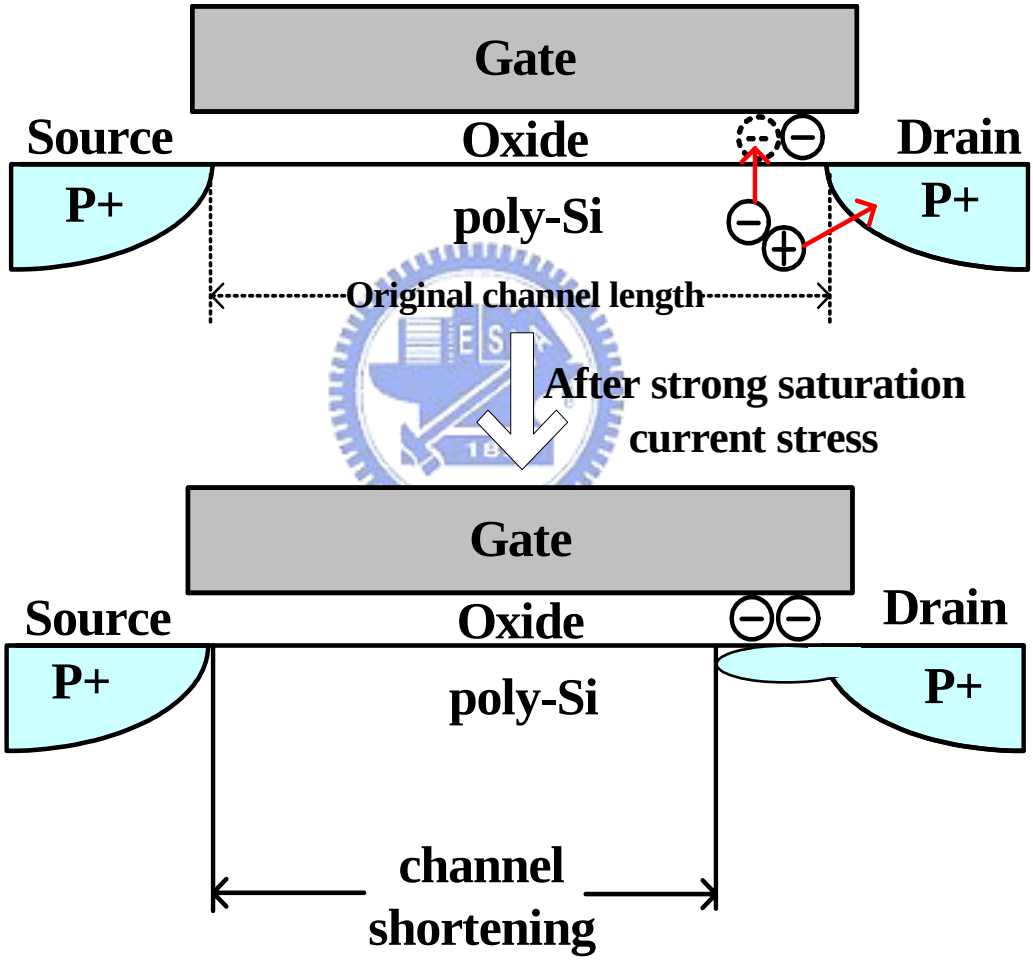


Fig. 3-16 Schematic diagram illustrating a hot-electron injection

3.3.3 Correlating AC stress with hot-carrier stress

Fig. 3-17 shows the mobility variation and threshold voltage shift versus stress time after OFF region stress at frequency of 500 kHz. From Fig. 3-17 and Fig. 3-18, it can be found that the degradation phenomena were the same with those under DC strong saturation current stress. First of all, the mobility and threshold voltage have been observed to increase with the accumulation of the stress time of AC OFF region stress as well as the DC strong saturation current stress. And then, mobility was increased rapidly before the first 10 seconds and gradually after 10 seconds of OFF region stress. Last, the slope of the threshold shift vs. stress time was nearly the same shown in Fig. 3-18.

These degradation phenomena imply that the degradation mechanism under OFF region stress might be the same with those under strong saturation current stress. As mentioned in section 3.3.2, hot electrons inject into gate oxide near the drain oxide, which results in effective short channel effect. It also means that the OFF region stress induced internal electrical field is large near the drain and/or source end just like strong saturation current stress.

As to mobility shift, which shows different power-time dependence with different slopes from 0 to 10s and from 10s to 1000s, it can be explained by the decreased lateral electrical field. When hot electrons inject into gate oxide, these negative charges would screen the electrical field from gate to drain. Therefore, the decreased lateral electrical field alleviates the high-field-induced degradation effect.

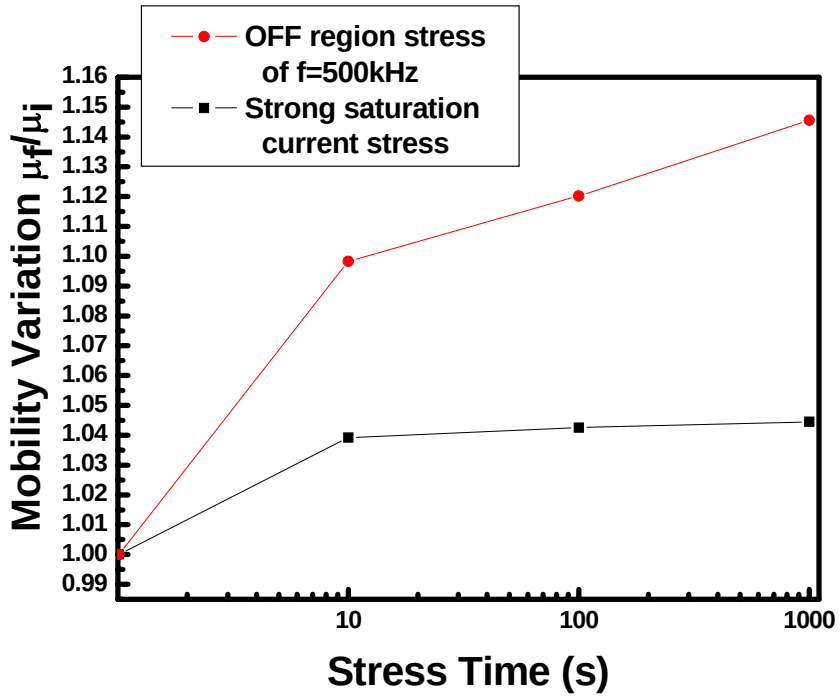


Fig. 3-17 Mobility variation versus stress time after OFF region stress and strong saturation current stress.

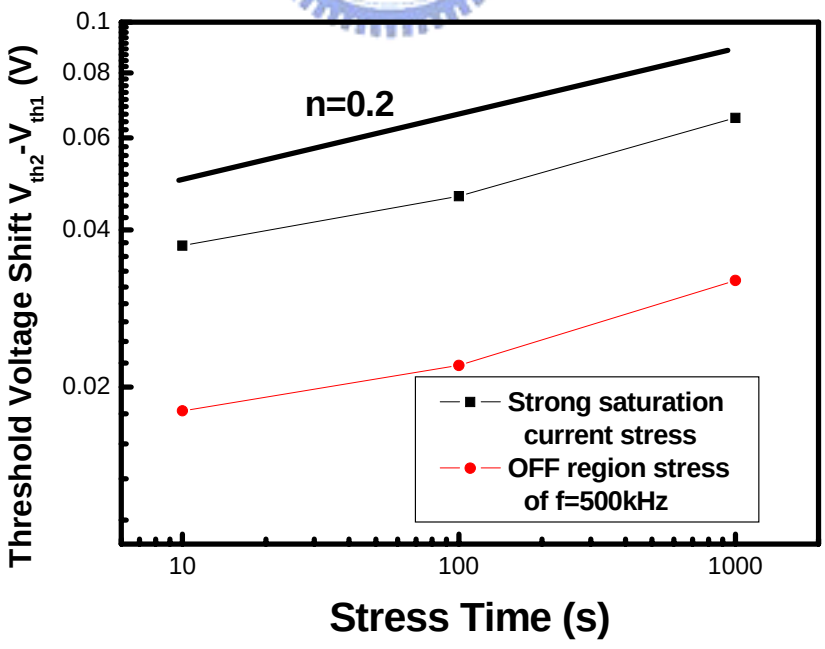


Fig. 3-18 Threshold voltage shift versus stress time under strong saturation current stress and OFF region stress

It was also noticed that the threshold voltage shift exhibits a power-time dependent law of the form: V_{th1}-V_{th2} = At^n with n=0.1~0.2. In bulk-Si MOSFETs, the threshold voltage (△Vth) has been found to follow a power-time dependent law with the form of △Vth= At^n, where A is a constant and the exponent n=0.1-0.7. It has been shown that an exponent of around 0.1-0.3 is due to carrier trapping in the gate oxide. An exponent n of around 0.4-0.7 correspond to interface state generation at Si/gate oxide interface, which is related to the trapping of holes followed by electron capture induced by drain avalanche hot-carrier injection into the gate oxide [3.19]. In addition to the same exponent, the threshold voltage shifts to a positive position. These results indicate that both the degradation mechanisms are caused by the generation of negative charge near the drain and/or source region, which probably due to electron trapping at the gate oxide/poly-Si interface.

The device degradation is nearly unchanged under ON region compared with OFF region stress. In spite of this, it was shown the different degradation phenomena from those under OFF region stress. Fig. 3-19 shows the mobility variation and threshold voltage shift versus stress time after ON region stress. Even though the mobility shift was increased at a certain time, it had a tendency to be decreased approximately. In addition, the threshold voltage was decreased with time. The degradation phenomena under ON region stress were like those under weak saturation current stress (i.e Vg=-8, Vd=-16).

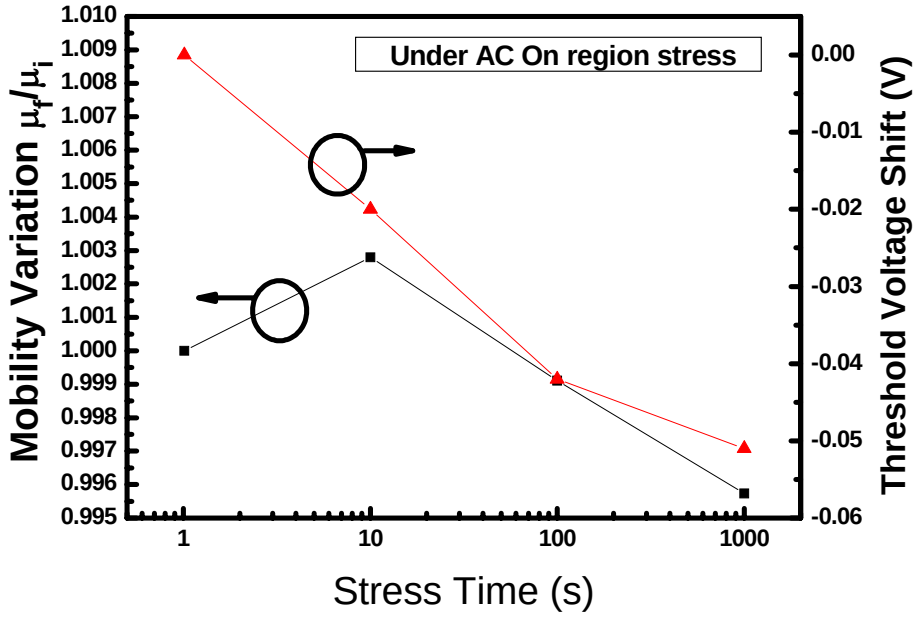


Fig. 3-19 The mobility variation and threshold voltage shift versus stress time after ON region stress

3.4 Summary

The instability of p-channel poly-Si TFTs has been investigated by the ON and OFF region stress, respectively. The degradation under OFF region stress was much severer than that under ON region stress. Beside, the degradation of poly-Si TFTs shows frequency dependence under OFF region stress, but is almost constant under ON region stress. Under OFF region stress, the degradation is enhanced by the increase in frequency and peak voltage and the decrease in rising time. By means of comparison of the electrical degradation, the AC OFF region stress has the similar instability mechanism as the DC strong saturation current one. The instability mechanism is effective short channel effect.

CHAPTER 4

Instability of Low-Temperature poly-Si n-channel Thin-Film Transistors under AC Gate Bias Stress

4.1 Introduction

For realization of a ”system-on-panel (SOP)”, both of the improvement of performance and reliability of the low-temperature poly-silicon thin film transistors (LTPS TFTs) are equally important, since high speed circuits such as processors, memories, drivers, and so on need to be integrated with a pixel array on the same glass or plastic substrate. The electron mobility of the LTPS TFTs is about 100 times larger than that of the amorphous silicon TFTs. Taking advantage of this predominance, poly-Si TFTs are used both as pixel elements and in driver circuits.

Unlike pixel elements, TFTs in driver circuits are subjected to high frequency voltage pulses. Therefore, understanding of the instability mechanism under ac stress becomes increasingly important.

Many studies have been reported for discussing the degradation mechanisms of poly-Si TFTs under dc [1.40]-[1.42], [4.1]-[4.3] and ac stress [2.8]-[2.9], [4.4]. Poly-Si TFTs under on-state dc stress has been shown to cause more significant degradation compared to off-state dc stress [4.1]. On the contrary, under ac stress, the degradation by pulse swing only has tiny

impacts on the ON region. However, that degradation caused by pulse swing has large impacts on the OFF region [2.8].

In this chapter, the mechanism of device degradation under ac stress of different operating region will be investigated. First, the experimental details are provided, including the fabrication of LTPS TFTs, the equipment of measurement system and measuring method. Then, by varying various stress conditions (i.e. signal frequency, falling time), the mechanism of device degradation under ac stress of different swing region will be proposed and identified.

4.2 Measurement Methods and Sequences

Pulse voltage was applied to the gate electrode and source and drain were grounded, which is shown in Fig. 4-1(a). We used a rectangular pulse with duty cycle of 50%, and various frequencies and fall times to investigate the device degradation under different operating regions. The signal frequencies ranged from 5kHz to 500kHz, and falling times ranged from 100ns to 500ns. The pulse swing region was separated into two parts; one was the ON region, and the other was the OFF region as shown in Fig. 4-1(b). The ON region was for the pulse swing over threshold voltage where the channel region was formed. The OFF region was for pulse swing under threshold voltage where the channel region was fully depleted. At last, the electrical characteristics of poly-Si TFTs were characterized by an HP 4156C electrical analyzer. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of I_d = (W/L) x 10^{-8} A at $|V_{ds}|$ = 0.1V. The field effect mobility is extracted from the maximum transconductance in the linear region of I_d-V_g characteristics at $|V_{ds}|$ = 0.1V. The on/off current ratio is specified by the maximum drain current at $|V_{ds}|$ = 5V and $|V_{gs}|$ = 20V over the minimum drain current at $|V_{ds}|$ = 5V.

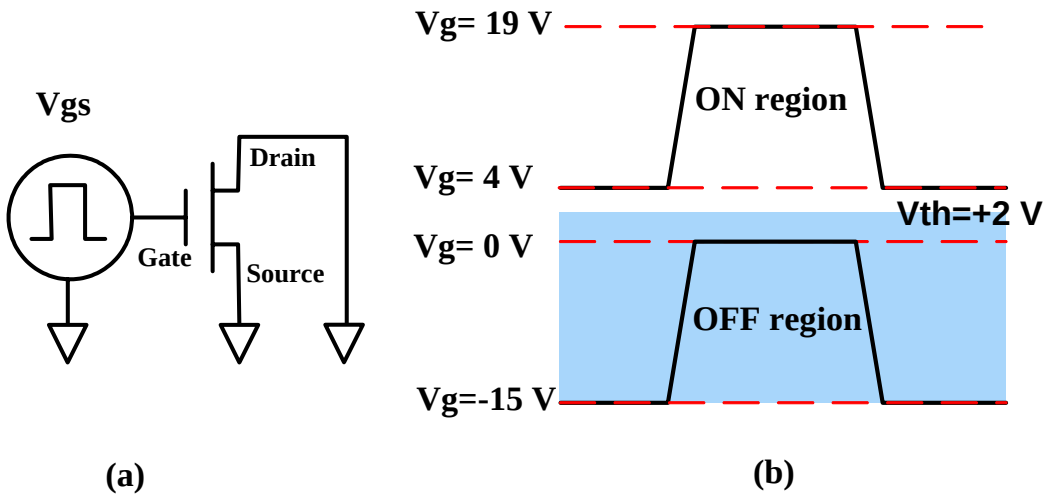


Fig. 4-1 (a) Stress configuration

(b) The swing region was separated into the ON and OFF regions.

4.3 Experimental Results and Discussion

4.3.1 Frequency Dependence

To compare the device degradation of the ON region stress with the OFF region stress, various frequencies from 5 kHz to 500 kHz were applied at a fixed t_f =100ns and the experimental results will be discussed in detail.

Fig. 4-2 to Fig. 4-5 illustrate the comparison of degradation under ON and OFF region stress of different signal frequencies. The mobility variation is expressed as the ratio of degraded mobility (μ_f) to initial mobility (μ_i). The device degradation in our work means the variation of electrical parameters in LTPS TFTs after stress. When the frequencies of 500 kHz and 100 kHz were applied, degradation under the OFF region stress was larger than the ON region stress shown in Fig. 4-2 and Fig. 4-3, while reverse situation can be seen under lower frequencies shown in Fig. 4-4 to Fig. 4-5. It is obvious to see the discrepancy of the results between the high and low frequencies from the mobility degradation (μ_f/μ_i).

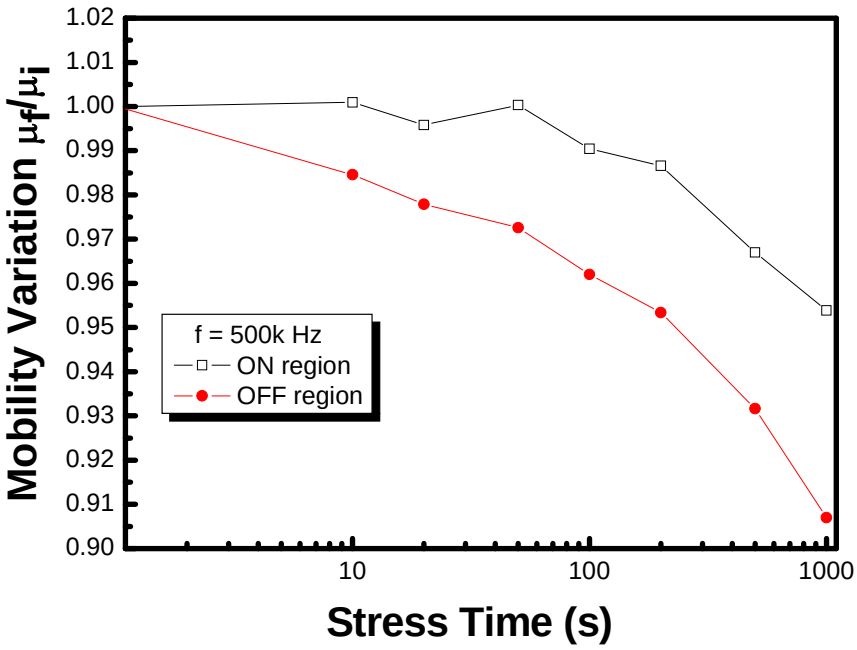


Fig. 4-2 Comparison of the degree of degradation under ON region and OFF region at frequency of 500 kHz and falling time of 100 ns

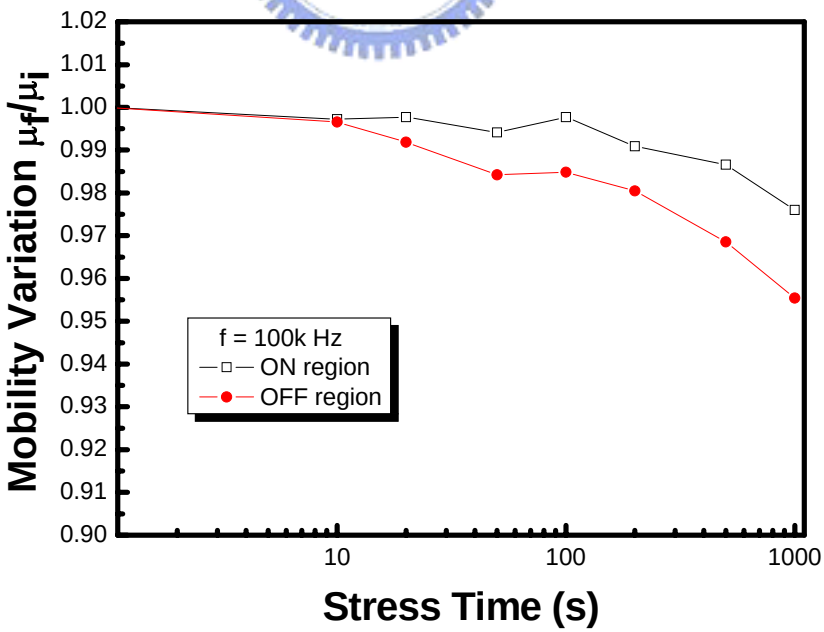


Fig. 4-3 Comparison of the degree of degradation under ON region and OFF region at frequency of 100 kHz and falling time of 100 ns

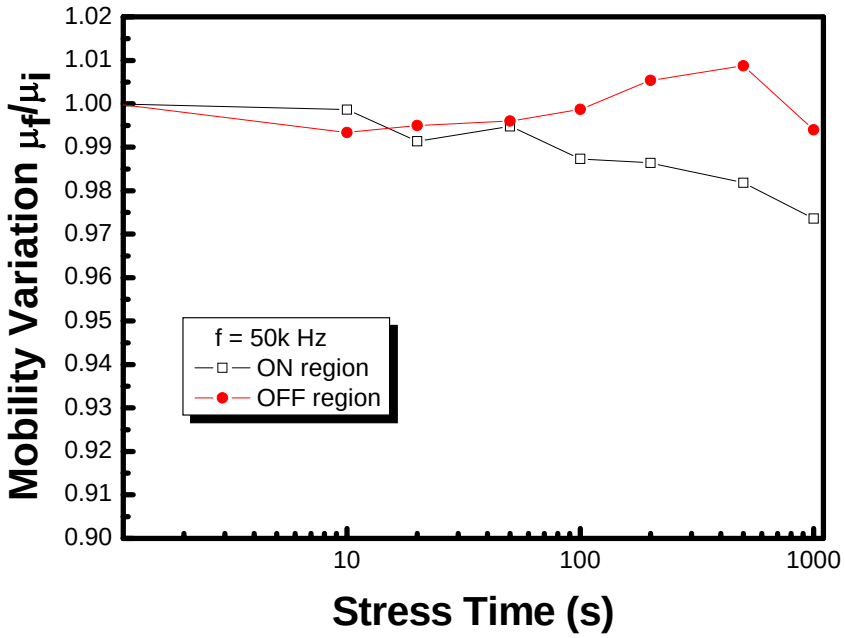


Fig. 4-4 Comparison of the degree of degradation under ON region and OFF region at frequency of 50 kHz and falling time of 100 ns

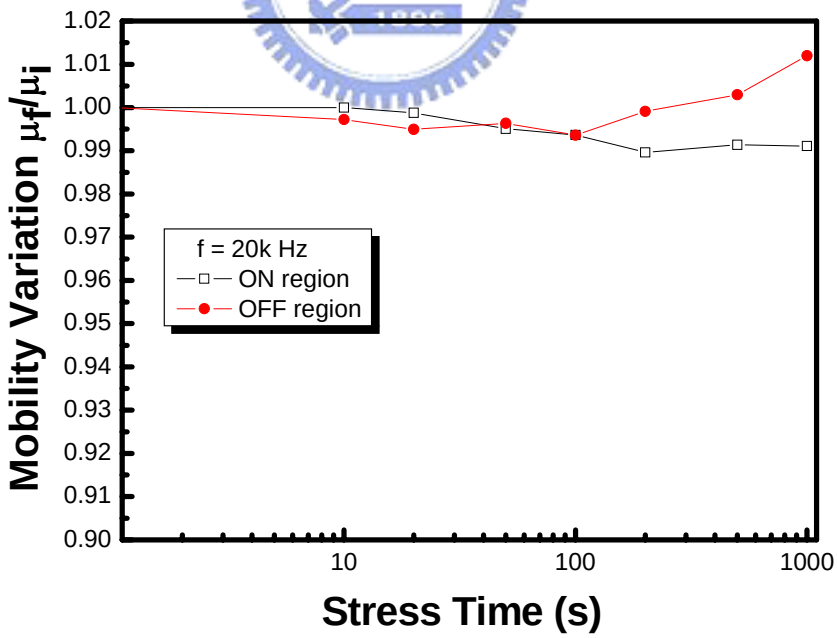


Fig. 4-5 Comparison of the degree of degradation under ON region and OFF region at frequency of 20 kHz and falling time of 100 ns

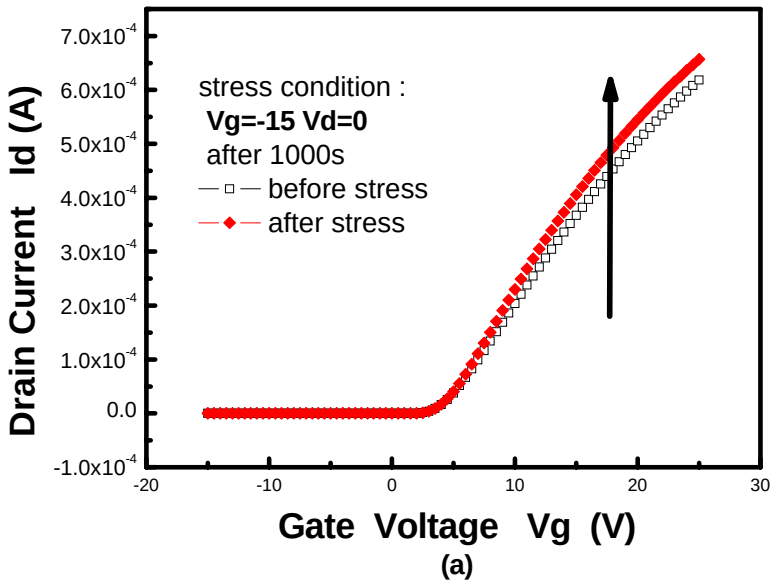
The above experimental data show that the degradation under the OFF region was

smaller than under the ON region with decreasing frequency, which is reverse to the result proposed by Uraoka et al. It deserves to be mentioned that mobility degradation is larger than 1 (i.e. degraded mobility is larger than initial mobility) under lower frequency.

The commonly accepted model for low temperature n-channel polycrystalline silicon TFTs under ac stress is that the trapped electrons, which cannot follow the transient stress of gate voltage, are exposed to high electric field and gain energy from the field. Therefore, hot electrons are generated, resulting in electron traps in poly-Si. It is believed that the device will be degraded by transient stress during the turning off period. As a result of enhancement of mobility under lower frequency, we believed that there must be some physical mechanism to promote the electrical characteristics of the device.

The transfer characteristics in the linear regime before and after application for 1000s under accumulation-mode stress condition：Vg=-15V, Vd=0V were presented in linear and logarithm scale, respectively, which were shown in Fig. 4-6(a) and (b). It can be observed from Fig. 4-6 (a) that on-current was increased and threshold voltage showed a negative shift. In the inset of Fig. 4-6 (b), just as expected, decreased off-current after accumulation-mode stress-bias condition can be observed. Moreover, mobility is also increased after stress as shown in Fig. 4-7. Several important electrical characteristics of TFTs after application for 1000s under accumulation-mode stress condition are summarized in Table 4-1.

Unlike accumulation-mode stress condition, decreased on-current, increased off-current and a positive threshold voltage shift after inversion-mode stress-bias condition can be observed in Fig. 4-8(a) and (b). Besides, mobility is also decreased after stress as shown in Fig. 4-9.



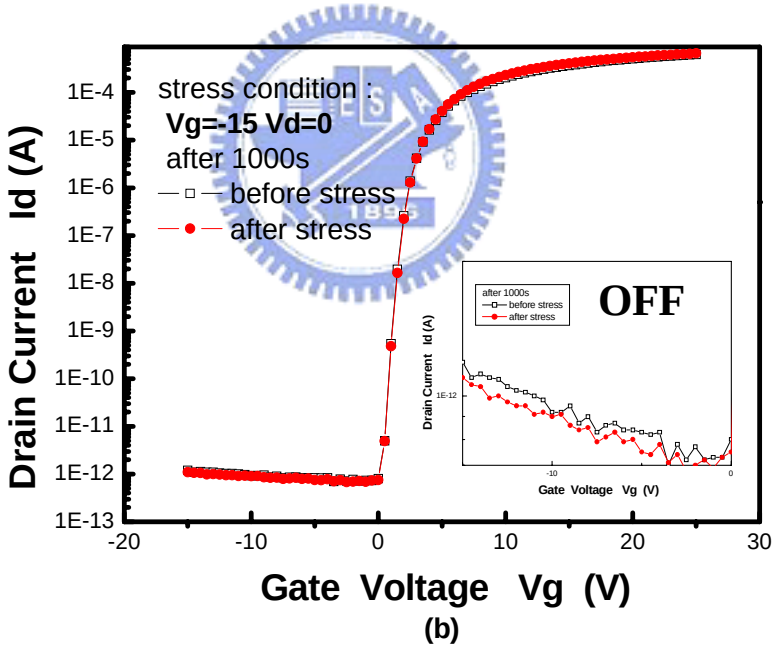


Fig. 4-6 Transfer characteristics in the linear regime of the virgin device and the stressed characteristics at off-state stress-bias condition: Vg=-15V, Vd=0V after 1000s stress time. The measurement was done at Vd of 5V. (a) Drain current in linear scale (b) Drain current in log scale. After the stress, the ON current was increased and leakage current was decreased.

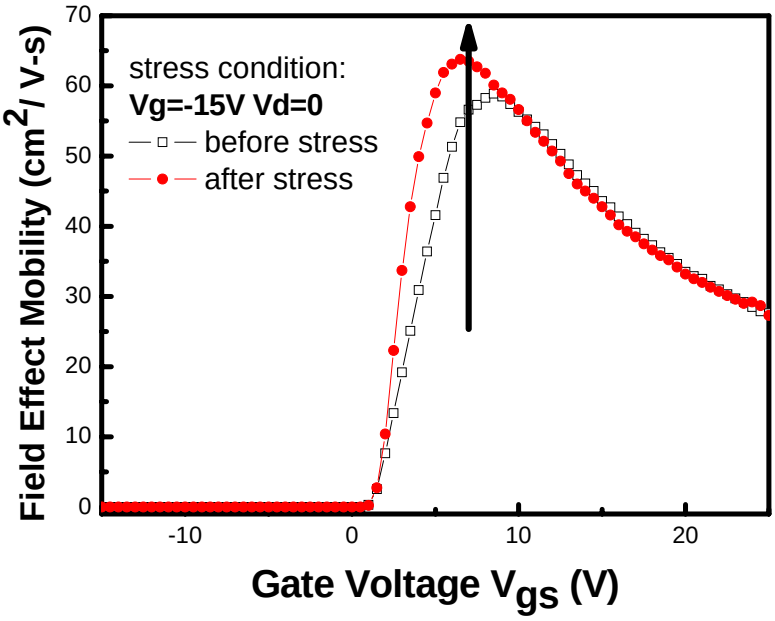
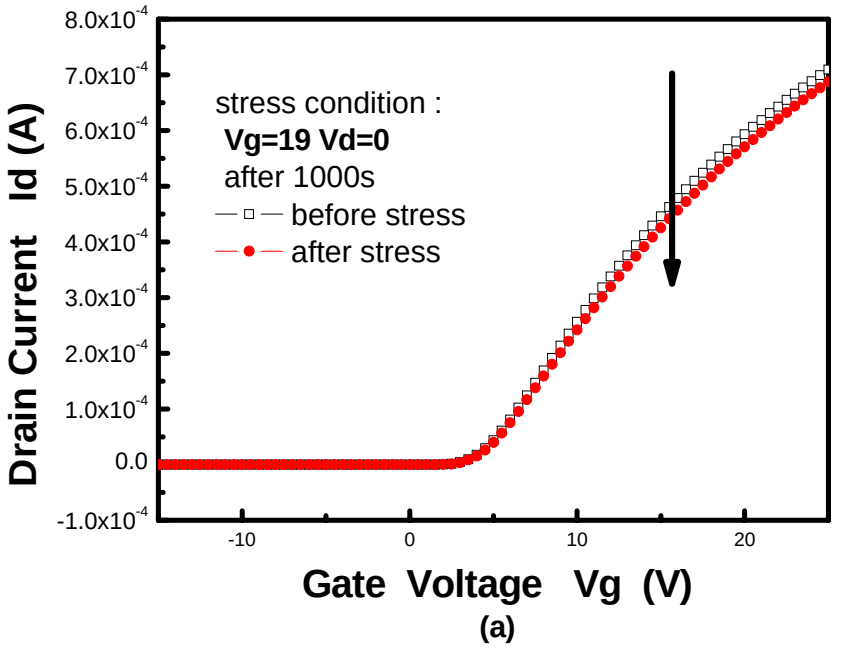


Fig. 4-7 Mobility before and after dc stress of Vg=-15V and Vd=0 for 1000s stress time.

Table 4-1 Measured important electrical characteristics of TFTs after applied for 1000s of accumulation-mode stress-bias condition

Stress Time(s)	Threshold Voltage (V)	Mobility (cm^2/V-s)	Subthreshold Slope (mV/decade)	I_{on}/I_{off} @ V_{ds} = 5V
0	2.057	58.92	276.326	7.22×10^8
10	2.143	58.73	278.880	7.11×10^8
20	2.144	58.84	279.359	7.33×10^8
50	2.171	58.52	282.704	7.56×10^8
100	2.148	58.67	280.682	7.29×10^8
200	2.094	59.40	279.029	7.64×10^8
500	2.017	61.50	280.666	8.02×10^8
1000	2.021	63.83	280.603	7.22×10^8



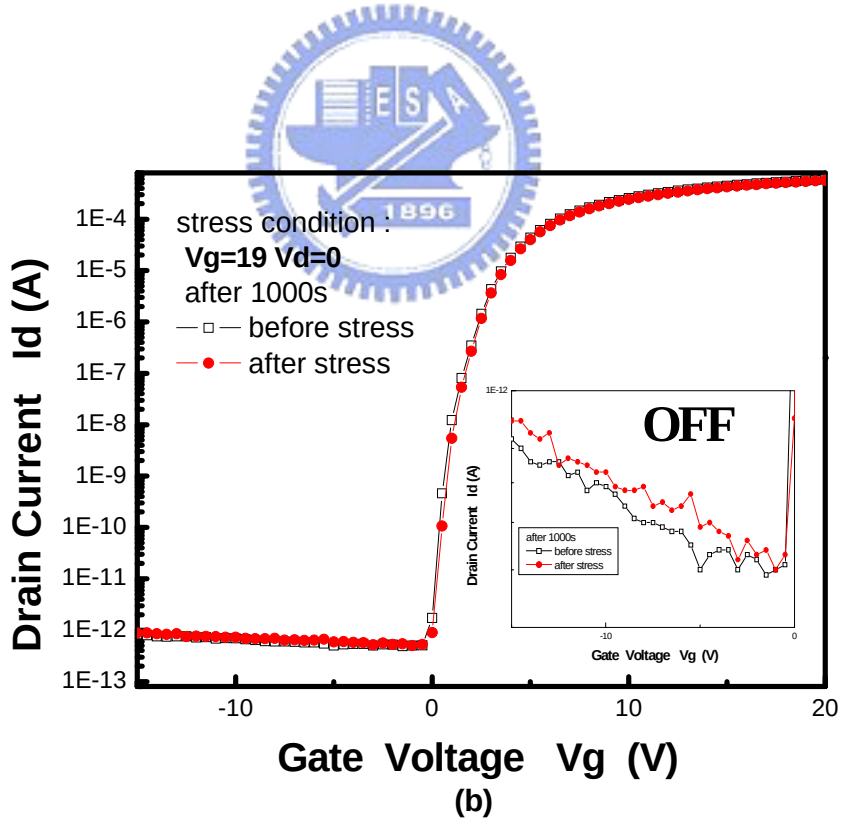


Fig. 4-8 Transfer characteristics in the linear regime of the virgin device and the stressed characteristics at on-state stress-bias condition: Vg=19V, Vd=0V after 1000s stress time. The measurement was done at Vd of 5V. (a) Drain current in linear scale (b) Drain current in log scale. After the stress, the ON current was decreased and leakage current was increased.

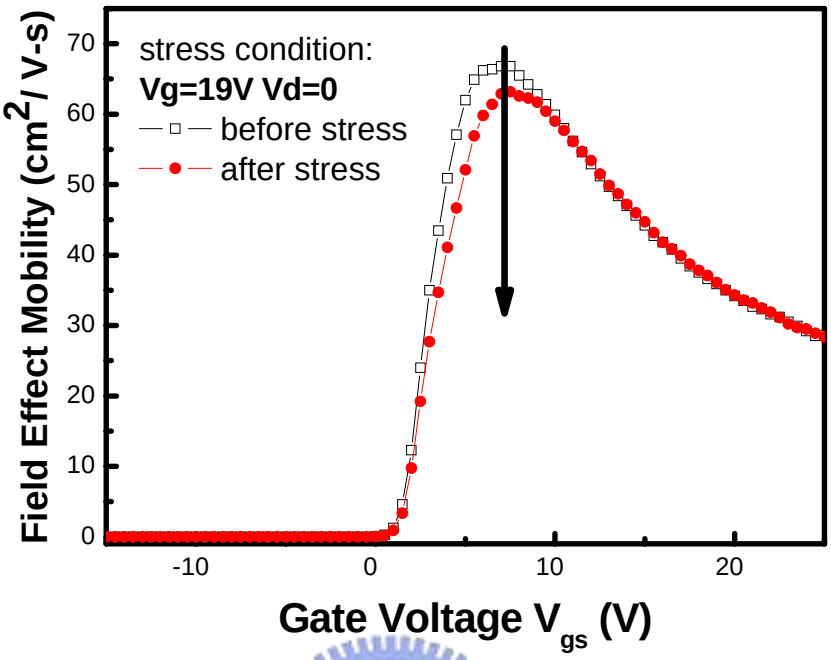


Fig. 4-9 Mobility before and after dc stress of Vg=19V and Vd=0 for 1000s stress time.

4.3.2 Degradation Mechanisms under Accumulation- and Inversion-Mode Stress Condition

4.3.2.1 Degradation Mechanism under Accumulation-Mode Stress Condition

There have been a number of previous investigations into the stability of poly-Si TFTs, and several degradation mechanisms have been characterized. They can be categorized as follows：(1) hot-carrier effects [4.3], [4.5]-[4.7], (2) gate bias trapping effects [4.8]-[4.10], (3)

self-heating effects [1.40]-[1.42], and (4) states creation effects [4.1]. Hot carrier degradation effects in poly-Si TFTs are very similar to those seen for single-Si MOSFETs where a combination of interface state generation and carrier trapping in the oxide is seen. Such effects are only seen at high drain bias (V_D), where carrier can attain sufficient energy from field to be injected into gate oxide. Due to V_D=0 during accumulation-mode stress, hot carrier effects are completely excluded. Besides, there is no current flow through the channel, which the self-heating effect is excluded under this stress condition. The subthreshold slope depends mainly on intra-grain traps distributed uniformly inside the poly-Si film and also on the deep interface states [2.7]. Since there is no significant change of subthreshold slope under this stress condition, states creation effects can also be neglected.

In view of the polarity of electric field, negative threshold voltage shifts for negative bias, which was consistent with charge trapping in the oxide. Increased mobility can be explained in terms of effective short channel effect. Although hole trapping might degrade the device, this effect was screened by the effective short channel effect. As the area of the positive oxide trapped charge is localized near drain and/or source end as shown in Fig. 4-10, has a great impact of reducing threshold voltage. This part of transistor consequently switches on before the rest. At voltages corresponding to the threshold voltage of the transistor, there is already considerable channel charge situated below the damage region. The transistor thus appears, at threshold, as a device with a slightly shorter effective length. This results in an increase in the mobility of the device.

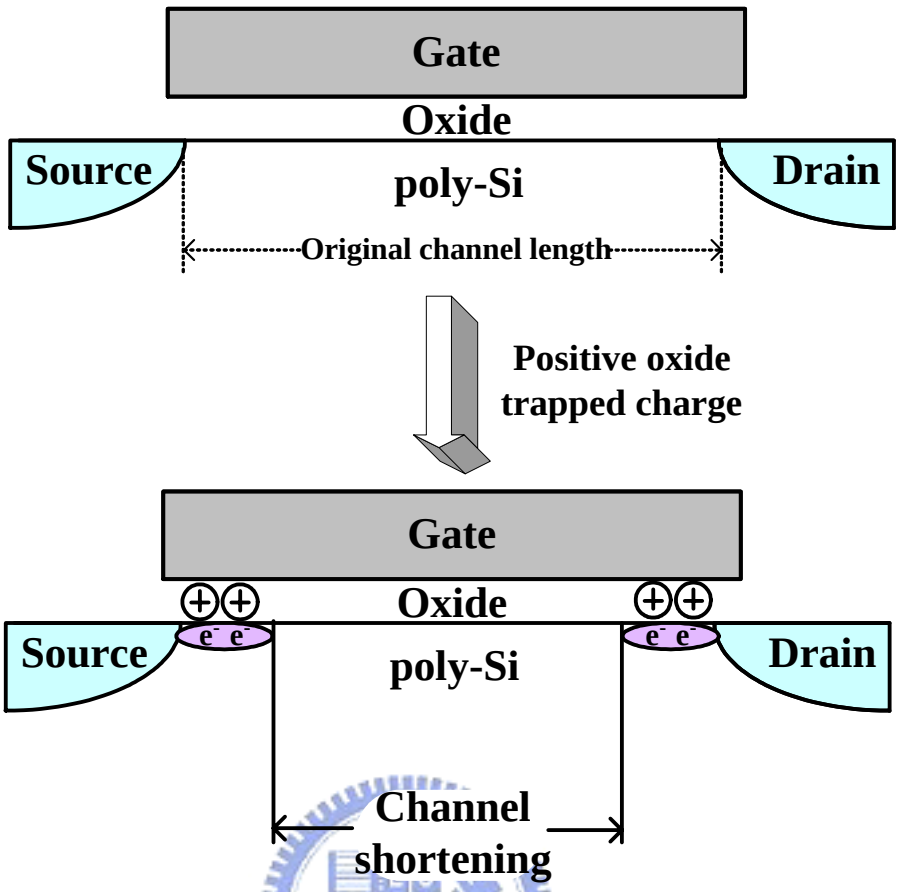


Fig. 4-10 ⊕ denotes positive oxide trapped charge, which results in effective short channel effect.

The mechanism we proposed can be verified by the following measurement. It was found that with more negative gate bias, there is greater degradation, indicating more charge trapping.

The stressed gate voltages (Vg) of –2.5V, –15V and –25V are applied on the devices respectively. The degree of promotion of mobility is highest under gate voltage of –25V, the next is under gate voltage of –15V, and the lowest is under gate voltage of –2.5V. The electrical field from drain to gate is largest when the device is biased at Vg of –25V. Therefore, there are more holes injecting into the oxide, which results in more severe effective short channel effect. The mobility increases more at Vg of –25V than –15V and –2.5V, which is shown in Fig. 4-11. The effect becomes more pronounced for more negative gate bias applied

during accumulation-mode stress.

In addition to changing gate voltage to vary the electric field, drain voltage (Vd) is also changed to vary the electric field from drain to gate. Again, the electrical field from drain to gate is larger when the device is biased at Vd of 5V than 0V. Thus, there are more holes injecting into the oxide, which results in more severe effective short channel effect. The mobility increases more at Vd of 5V than 0V, which is still shown in Fig. 4-11. The effects become more pronounced for higher drain bias applied during electrical stress.

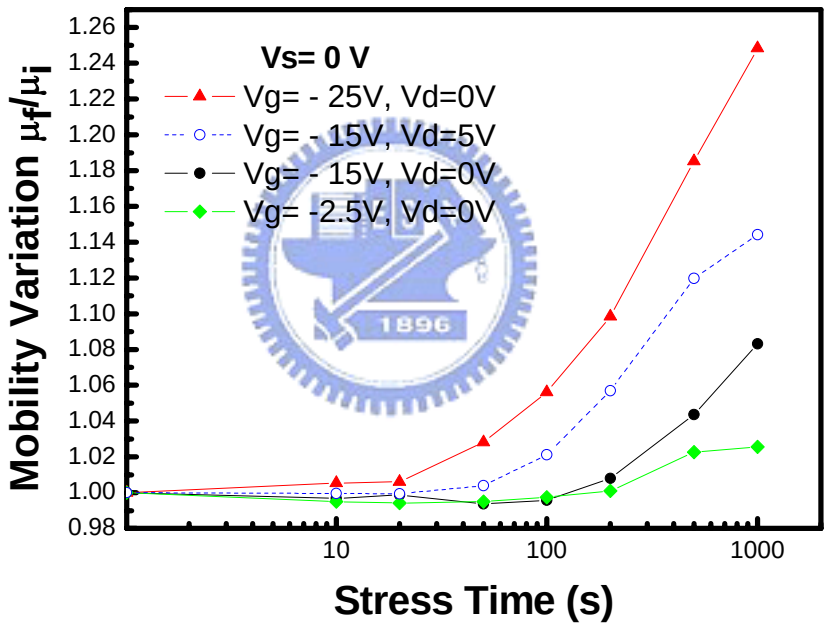


Fig. 4-11 Mobility degradation v.s. stress time under different bias-stress condition

To give further proof, a conventional n-channel SOI with LDD structure was simulated by using ISE simulator. First, the process flow was used as an input. Then, device simulator was used to calculate electrical behavior numerically. The device simulator includes carrier transport models and basic semiconductor equations, etc. At last, 2D graphic was checked and

the concerned device characteristics were extracted.

The device after stressed at Vg=-19 V and Vd=Vs=0 V have been simulated. First, the spatial doping concentration and electrical potential were confirmed. Fig. 4-12 and Fig. 4-13 shows the spatial doping concentration and electrical potential, respectively. The doping concentration is just as expected. In addition, the simulated electrical potential conformed to the stressed condition.

Then, the simulated hole density and electrical field were observed. It can be found that there were more hole density and larger electrical field near the drain and source junctions than in the channel, which were shown in Fig. 4-14, Fig. 4-15.

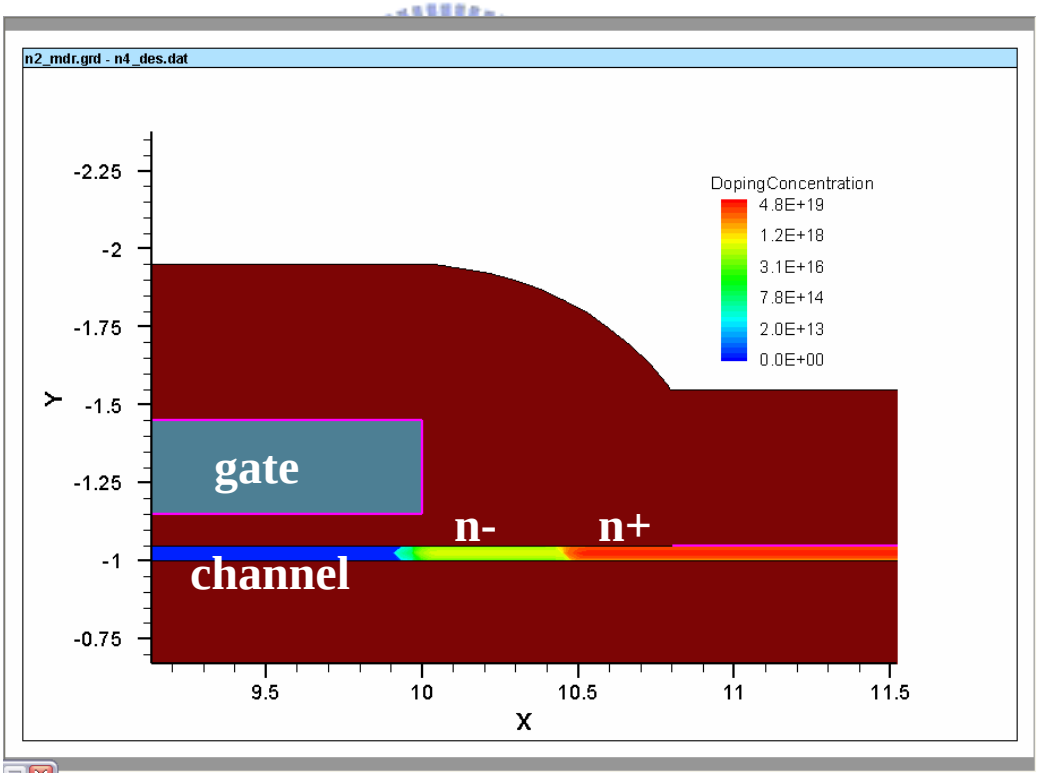


Fig. 4-12 The spatial distribution of doping concentration. Bias stress condition is Vg=-15V, and Vd=Vs=0V

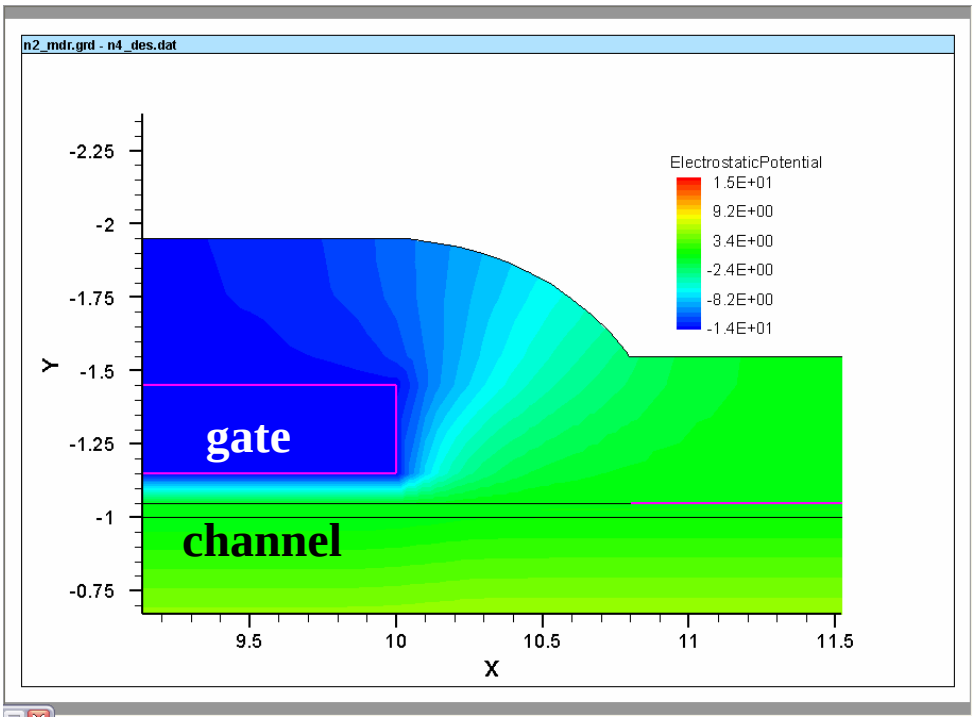


Fig. 4-13 The spatial distribution of electric potential. Bias stress condition is Vg=-15V, and Vd=Vs=0V

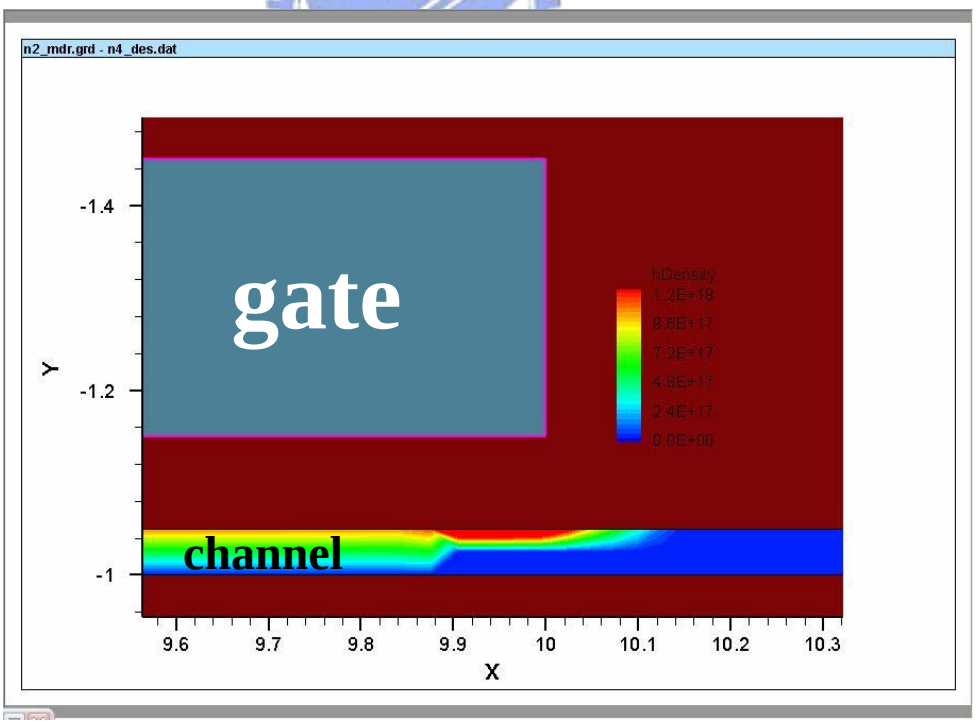


Fig. 4-14 The spatial distribution of hole density. Bias stress condition is Vg=-15V, and Vd=Vs=0V

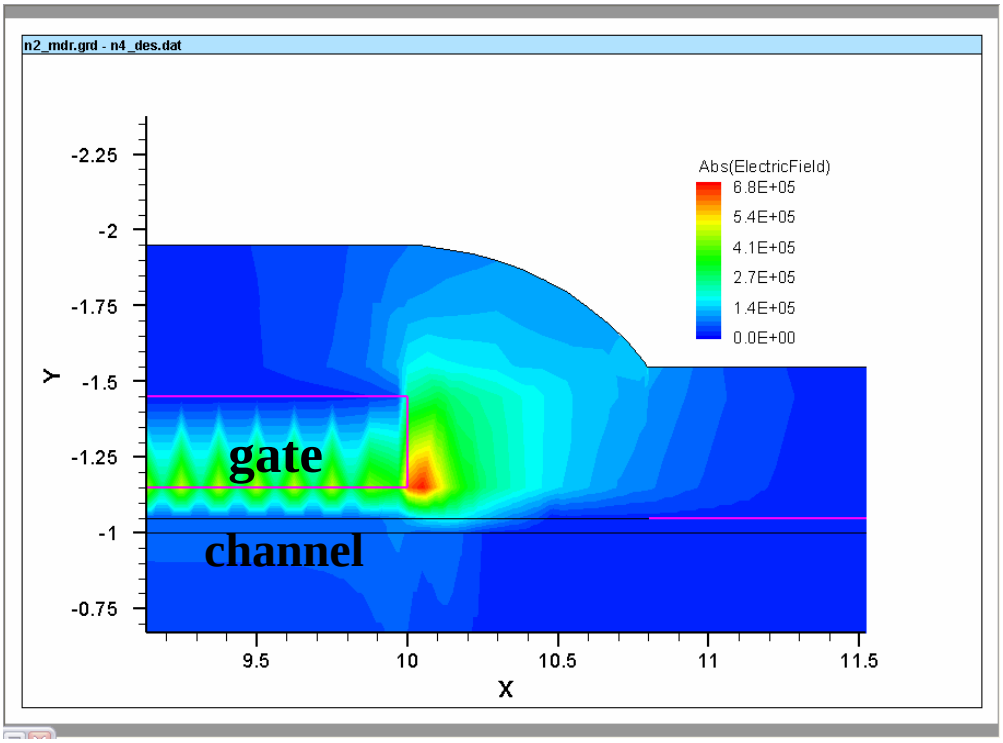


Fig. 4-15 The spatial distribution of electric field. Bias stress condition is Vg=-15V, and Vd=Vs=0V

Fig. 4-16 shows the distribution of lateral E_x, vertical E_y, and the total, $E=(E_x + E_y)^{1/2}$ electrical field, 10nm below the SiO_2/polysilicon interface. Due to reverse-bias at source and drain junctions, a negative electric E_y (i.e. E_y is directed from the polysilicon film to the gate electrode) was induced. A negative electric E_x near the drain end means that E_x is directed from the drain to the channel, while reverse result was observed near the source end.

Fig. 4-17 shows the spatial distribution of hole density and electric field at SiO_2/poly-Si interface. It can be observed that both the spatial distribution of hole density and electric field have two peaks at the source and drain junctions. It was further proved that the positive oxide trapped charges were induced near the source and drain end by these results.

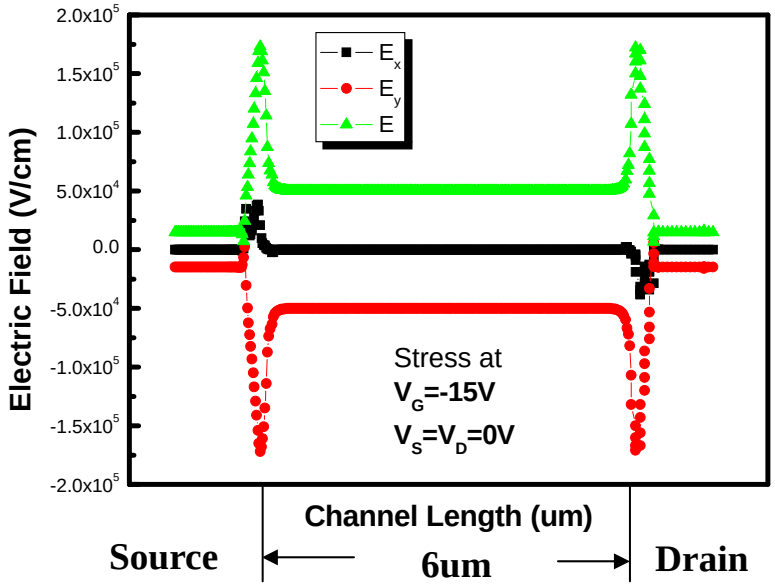


Fig. 4-16 The distribution of lateral E_x, vertical E_y, and the total, $E=(E_x + E_y)^{1/2}$ electrical field, 10nm below the SiO_2/polysilicon interface

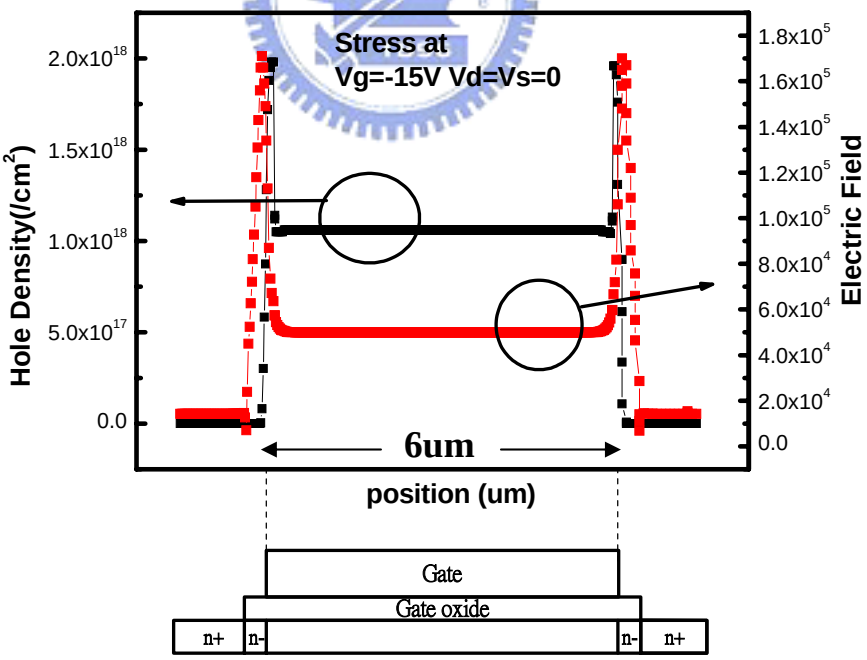


Fig. 4-17 The spatial distribution of hole density and electric field at SiO_2/poly-Si interface under gate bias stress. Bias stress condition is Vg=-15V, and Vd=Vs=0V

4.3.2.2 Degradation Mechanism under Inversion-Mode Stress Condition

Threshold voltage shifts for positive bias, which was consistent with electron trapping in the oxide in view of the polarity of electric field. The oxide trapped electrons give rise to a potential barrier for carrier transport in the channel and defect in bulk polysilicon or interface state, which deteriorates the performance of LTPS TFTs. It is obvious that the electrical performance of TFTs is degraded under such stress condition shown in Fig. 4-18. Several electrical characteristics of TFTs after application for 1000s of accumulation-mode stress-bias condition are summarized in Table 4-2.

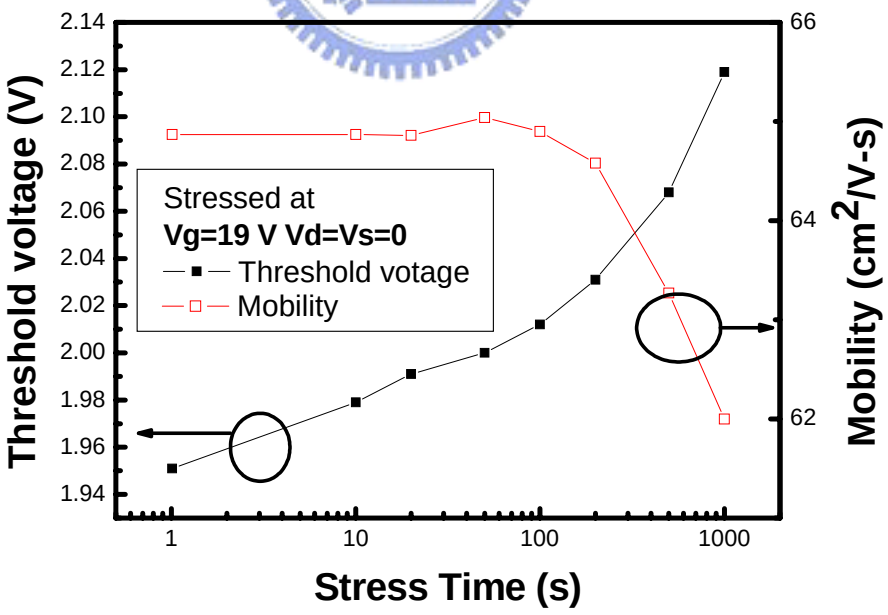


Fig. 4-18 The evolution of threshold voltage and mobility with stress time

Table 4-2 Measured electrical characteristics of TFTs after application for 1000s of accumulation-mode stress-bias condition

Stress Time(s)	Threshold Voltage (V)	Mobility (cm^2/V-s)	Subthreshold Slope (mV/decade)
0	1.951	64.87	259.581
10	1.979	64.87	253.457
20	1.991	64.86	248.582
50	2	65.04	251.652
100	2.012	64.90	254.297
200	2.031	64.58	252.496
500	2.068	63.27	253.280
1000	2.119	62.00	254.596

As device degradations are caused by opposite polarity of charges, each stress condition will have its own degradation behavior. It can be found that both dc inversion-state stress and ac ON region stress degrade the devices. Thus, no matter how low the frequency is, the device will be degraded with time under ON region stress.

4.3.3 Dependence of the Number of Pulse Repetitions under Accumulation-mode Stress

Fig. 4-19 shows dependence of degradation of the number of pulse repetitions. All lines didn't follow the universal curve. There are two curves in the figure. One is degraded with time no matter frequency is high or not, and the other seems to be recovered and even

promoted with time under lower frequency. Table 4-3 shows the dependence of frequency on accumulation-mode stress time. Fixing the falling time (t_f =100ns), the lower the frequency is, longer the accumulation-mode stress time is. Therefore, the accumulation-mode stress is more remarkable with decreasing frequency.

The evidence shows that the device is affected by dc accumulation-mode stress under lower frequency.

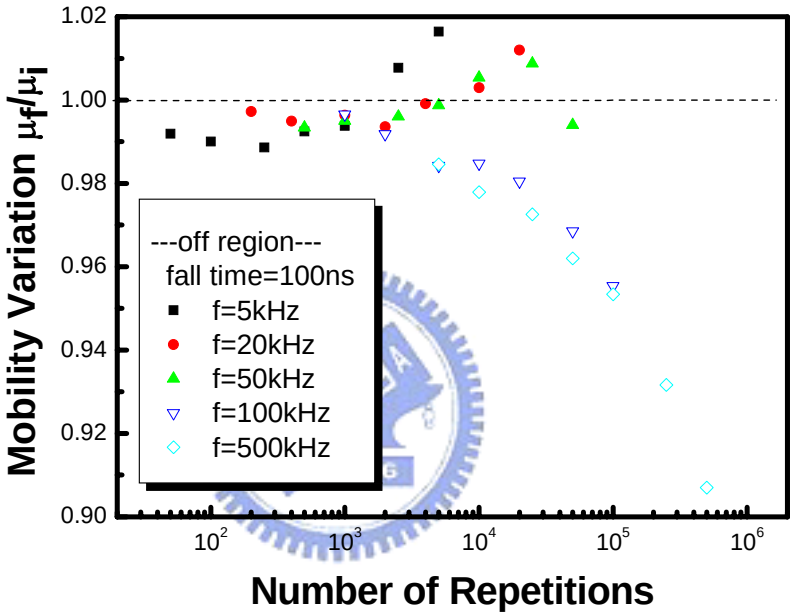


Fig. 4-19 Dependence of the number of pulse repetitions as a parameter of frequency

Table 4-3 The dependence of frequency on accumulation-mode stress time

Frequency (kHz)	Accumulation-mode stress time (μs)
5	99.9
20	24.9
50	9.9
100	4.9
500	0.9

4.3.4 Falling Time Dependence under accumulation-mode stress

Fig. 4-20 illustrates the dependence of degradation on number of repetition as a parameter of fall time and a fixed accumulation-mode stress time of 900ns. As mention in 4.3.1, the accumulation-mode stress also affects the performance of the devices, therefore, accumulation-mode stress time is fixed to attain an objective result.

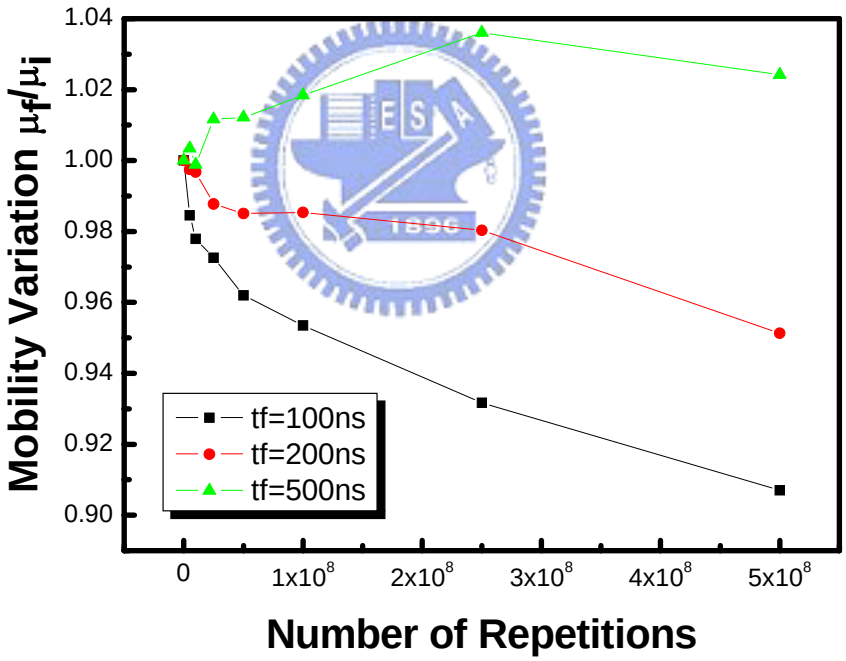


Fig. 4-20 Dependence of degradation on number of repetition as a parameter of falling time

It is obvious that the degree of degradation is less severe under long falling time. Moreover, the characteristics of the device are promoted under even longer fall time (i.e. 500ns).

The device will be less degraded by transient stress without respect to decreasing frequency or increasing falling time. At this time, it is more obvious that the dc accumulation-mode stress can promote the electrical characteristics of the device.

4.3.5 Base Voltage Dependence under accumulation-mode stress

When the gate pulse falls, the internal electrical field increases [2.8]. The device degradation under ac stress of more negative base voltage is more severe due to larger internal electrical field.

Therefore, the effect of accumulation-mode stress is screened when applying more negative base voltage. The result is shown in Fig. 4-21.

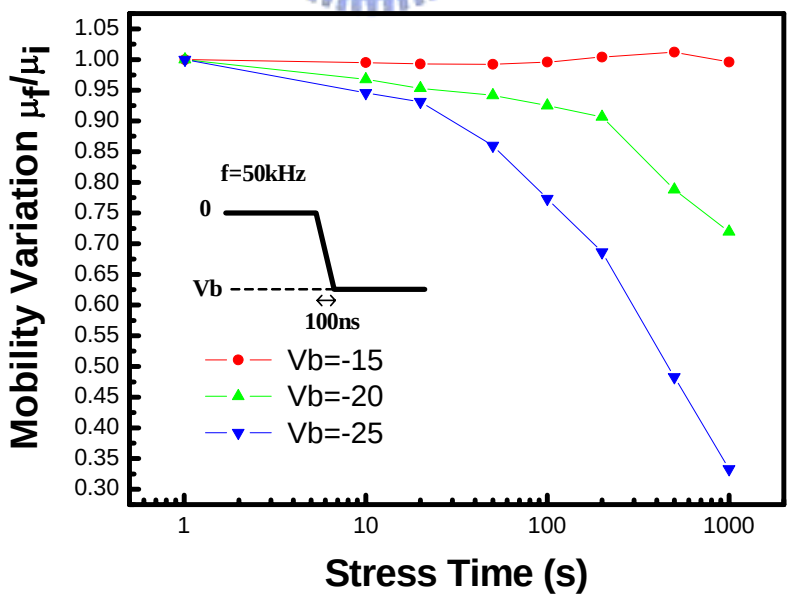


Fig. 4-21 The base voltage dependence on mobility degradation

4.3.6 Comparison of Degradation under Different Stress Condition

Fig. 4-22 shows mobility degradation with stress time under different stress condition. As discussed above, the cause of the mobility degradation under OFF swing region stress is divided into two effects. One is falling time of ac stress, and the other is accumulation-mode stress. The mobility is increased under accumulation-mode stress, while the mobility is degraded with time under OFF swing region stress of high frequency. Therefore, it can be expected that the degree of mobility degradation under lower frequency will lie in between them due to the trade off between two effects. It can also be thought that device is affected by dc accumulation-mode stress under lower frequency.

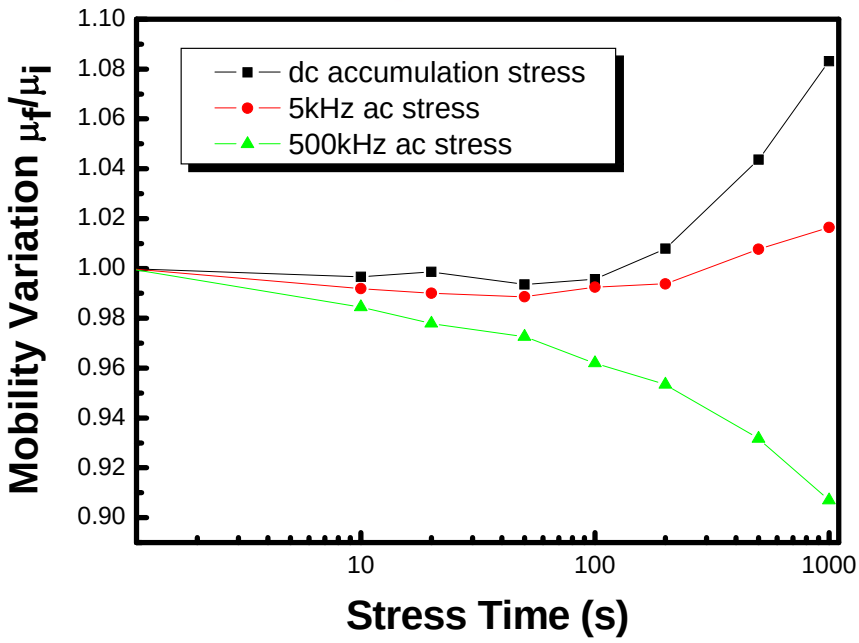


Fig. 4-22 Mobility degradation with stress time under different stress condition.

4.4 Summary

It was found that the mobility is increased under accumulation-mode stress due to positive oxide trapped charge, which results in effective short channel effect, while the reverse result was found under inversion-mode stress. Device simulation has been performed to further prove the mechanism under accumulation-mode stress.

It also found that device degradation under OFF swing region is dislike that under ON swing region. That is, devices degrade under ON swing region stress with time no matter under high or low frequency, while the mobility under OFF swing region stress will degrade less and even promote with time under low frequency or long falling time. Induced effective short channel effect from the accumulation mode stress will be trade-off with the increase of defects at poly-Si film for the falling time of the OFF region in AC stress.

The relationship between the mobility degradation and the repetition number was dependent on the frequencies, besides, the mobility is enhanced under OFF swing region stress of longer falling time. It can be also explained by degradation mechanism mentioned above.

CHAPTER 5

Conclusions

The instability mechanisms and degradation phenomena of p- and n-channel LTPS TFTs were investigated in detail under AC stress of different swing region with various frequencies, rising/falling times, peak/base voltages, and duty ratios.

In p-channel LTPS TFTs, it was found that the degradation under OFF region stress was much severe than that under ON region no matter the frequency is high or not. Beside, the degradation of poly-Si TFTs shows frequency dependence under OFF region stress, but is almost constant under ON region stress. As expected, the degradation is enhanced by the increase in frequency and peak voltage and the decrease in rising time. By means of comparison of the electrical degradation, the AC OFF region stress has the similar instability mechanism as the DC strong saturation current one.

In n-channel LTPS TFTs, it was found that the degradation under OFF region stress was much severe than that under ON region only when the frequency is higher. However, reverse situation can be observed under lower frequencies. It is obvious to see the discrepancy of the results between the high and low frequencies from the mobility degradation. The phenomenon can be ascribed to the effective short channel effect under accumulation-mode stress, which was analyzed by electrical measurement and device simulation. Induced effective short channel effect from the accumulation mode stress will be trade-off with the increase of defects at poly-Si film for the falling time of the OFF region in AC stress. The relationship between the mobility degradation and the repetition number was dependent on the frequencies, besides,

the mobility is enhanced under OFF swing region stress of longer falling time. It can be also explained by degradation mechanism mentioned above.

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