Characteristic Fluctuation Dependence on Discrete Dopant for 16nm SOI FinFETs at Different Temperature

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Abstract

In this paper, we numerically study the discrete-dopant-induced characteristic fluctuations in 16nm silicon-on-insulator (SOI) FinFETs. For devices under different temperature condition, discrete dopants are statistically generated and positioned into the three-dimensional channel region to examine associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". Electrical characteristics' fluctuations are growing worse when the substrate temperature increases, the standard deviation of threshold voltage increases 1.75 times when substrate temperature increases from 300K to 400K for example. This "atomistic" device simulation technique is computationally cost-effective and provides us an insight into the problem of discrete-dopant-induced fluctuation and the relation between the fluctuation and thermal effect.

1 Introduction

Electrical and physical characteristic fluctuation dependence on the random-dopant-number and position for CMOS devices is crucial in nanoelectronics industry [1-2]. Nanometer-scale silicon device with vertical channel structure, such as multiple-gat FinFETs are promising candidates for next generation VLSI devices [3-5]. Experimental and theoretical investigations on the randomness effect on diverse transistor's performance have recently been reported. However, the discrete-dopant-induced characteristic fluctuation for nanoscale FinFETs under different substrate temperature has not been clear explored yet.

In this paper, we for the first time study the characteristic fluctuations simultaneously coupling with device's thermal effect in 16nm SOI FinFETs. The studied SOI FinFET is first quantitatively characterized [3] and the metal gate with a properly selected work function is used instead of the poly gate. The random-dopant-number- and random-dopant-position-induced fluctuations for different characteristics, such as the on/off state currents and the threshold voltage are explored by a three-dimensional

(3D) large scale statistical device simulation technique. This "atomistic" simulation technique is computationally cost-effective and provides us an insight into the problem of temperature-dependent fluctuations. For the 16nm SOI FinFET has same normalized on-state current (I_{on}), the off-state current (I_{off}) varies with discrete-dopant-number and position, but the maximum variation of I_{on} is about 3,000nA/ μ m for the substrate temperature is 300K. However, the amplitude of the variation of the I_{off} current increases three times, shown in Fig. 3(a), when the temperature increases from 300K to 400K. For the same increase of the substrate temperature, the standard deviation of threshold voltage increases 1.75 times, as shown in the inset of Fig 2(a).

2 Simulation and Discussion

All statistically generated discrete dopants, shown in Fig. 1, are incorporated into the large-scale 3D device simulation. A large-scale quantum mechanical transport simulation is performed by solving the 3D density-gradient equation coupling with hydrodynamic model. The computation is performed under our parallel computing system and enables us to quantitatively explore the characteristic fluctuations that induced by the randomness of dopant number and position in the channel region [5]. Figure 1(a) shows 758 discrete dopants randomly distributed in (80nm)³ cube with average concentration of 1.48x10¹⁸cm⁻³. We notice that the dopants vary from 0 to 14, where the average number is 6, within its 125 sub-cubes of (16nm)³, as shown in Figs. 1(c), 1(d), and 1(e). These 125 sub-cubes are equivalently mapped into the SOI FinFET's channel region for the 3D device simulation with discrete dopant, as shown in Fig. 1(b). The thickness of gate oxide is equal to 1.2nm for all devices in this study.

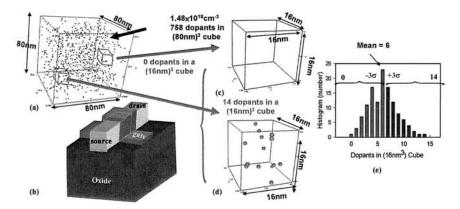


Figure 1: (a) Discrete dopants randomly distributed in $(80\text{nm})^3$ cube with an average concentration of $1.48 \times 10^{18} \text{cm}^{-3}$. (b) A 3D plot of the studied SOI FinFET. Plots of (d), (e) and (f)) show the 758 dopants within the cube and dopants vary from 0 to 14 within its 125 sub-cubes of $(16\text{nm})^3$. These 125 sub-cubes are then equivalently mapped into channel region for dopant position/number-sensitive simulation.

Figure 2(a) shows the threshold voltage (V_{th}) fluctuation of the 16nm SOI FinFET with respect to different substrate temperature (T_{sub}). For a given substrate temperature, the increase of dopant number substantially alters the threshold voltage,

and the random dopant position induced different magnitude of characteristic fluctuation in spite of the same number of dopants. The magnitude of the spreading characteristics is enlarged upon the number of dopants increases. As the substrate temperature increases from 300K to 400K, the threshold voltage is decreased from 0.275V to 0.2V. Without scaling correspondingly, the threshold voltage fluctuation increases from 53mV to 55mV instead. To compare the device with different nominal (i.e., the case of continuously doped) threshold voltage at different substrate temperature, the threshold voltage is normalized with respect to devices' nominal threshold voltage. The inset of Fig. 2(a) shows the standard deviation (S.D.) of the normalized threshold voltage at different substrate temperature. The normalized fluctuation almost doubly increases as substrate temperature increase; the magnitude of S.D. is further enlarged at the higher substrate temperature. Figure 2(b) shows the large-scale statistical computation of the drain current versus the gate voltage (Id-Vg), where the spreading Id-Vg curves reflect the influence of discrete dopant. The significant larger spreading range of Ioff shows the larger fluctuation of Ioff. The variation of the Ion and Ioff versus the number of discrete dopants, are shown in Figs. 2(c) and 2(d).

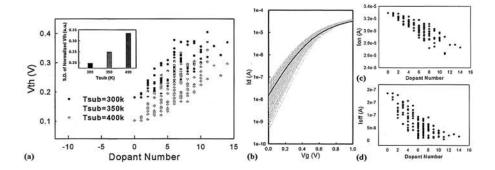


Figure 2: (a) Plot of V_{th} 's fluctuation versus the number of dopants for device at different T_{sub} . The inset shows the S.D. of normalized V_{th} at different T_{sub} . (b) The Id-Vg curves of the 16nm SOI FinFET at $T_{sub} = 300$ K. The red line is the nominal case. Plots of (c) and (d) are the I_{on} and I_{off} 's fluctuation versus the number of dopants.

Figure 3(a) shows the characteristics of $I_{\rm off}$ versus the normalized $I_{\rm on}$ for the 125 discrete-dopant 16nm SOI FinFETs at different substrate temperature. Due to the different nominal $I_{\rm on}$ of devices at different substrate temperature, we normalized the $I_{\rm on}$ with respect to the largest $I_{\rm on}$ at given temperature for a consistent comparison. Figures 3(b) and 3(c) show the studied continuously doped and a selected discretely doped case at a substrate temperature of 300K. Even the $I_{\rm on}$ of the two cases are rather similar, both the on-state potential contour and current density distribution are significantly different, as shown in Figs. 3(b''), 3(c''), and 3(c'''), respectively. Moreover, the off-state potential contours, shown in Figs. 3(b''') and 3(c'''), explains why the amplitude of $I_{\rm off}$'s fluctuations of the discretely doped cases is about one-order larger than the nominal case (the red solid line in Fig. 2(b)).

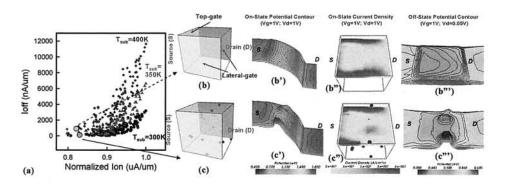


Figure 3: (a) Plot of I_{off} vs. I_{on} of the 125 discrete-dopant 16nm SOI FinFETs at different T_{sub} . Plots of (b) and (c) show the nominal and selected discretely doped cases at $T_{sub} = 300$ K; for similar I_{on} between them, the on-state potential (b') and (c'), and current density (b") and (c") are different. Plots of (b"') and (c"') are the off-state potentials. All cross-sectional plots are extracted at the 1nm below the gate oxide.

3 Conclusions

We have explored the random-dopant effects on the characteristics of 16nm SOI FinFETs using a full-scale 3D "atomistic" simulation technique. The random-dopant-number- and random-dopant-position-induced fluctuations have been estimated for the device under the different substrate temperature. This study provides us an insight into the problem of fluctuation and the relation between the fluctuation and temperature effect.

Acknowledgements

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-95-2221-E-009-336 and Contract NSC-95-2752-E-009-003-PAE, by MoEATU Program, Taiwan, under a 2006-2007 grant, and by the Taiwan Semiconductor Manufacturing Company under a 2006-2007 grant.

References

- S. Roy and A. Asenov, "Where do the dopants go?", Science, vol. 309, pp. 388-390, 2005.
- [2] Y. Li and S.-M. Yu, "Comparison of random-dopant-induced threshold voltage fluctuation in nanoscale single-, double-, and surrounding-gate field-effect transistors". Jpn. J. Appl. Phys., vol. 45, pp. 6860-6865, 2006.
- [3] F.-L. Yang et. al., "35 nm CMOS", Tech. Dig. Symp. VLSI Tech., pp. 104-105, 2002.
- [4] F.-L. Yang et. al., "Strained FIP-SOI (FinFET/FD/PD-SOI) for sub-65 nm CMOS scaling", Tech. Dig. Symp. VLSI Tech., pp. 137-138, 2003.
- [5] Y. Li, H.-M. Chou, and J.-W. Lee, "Investigation of electrical characteristics on surrounding-gate and omega-shaped-gate nanowire FinFETs", IEEE Trans. Nanotech., vol. 4, 510-516, 2005.