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碩 士 論 文

氮化矽快閃記憶元件
可靠性分析量測分析

SONOS Flash EEPROM Reliability Physics and Characterization

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中華民國 九十四 年 六 月

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摘要

本篇論文主要著重於特殊類型 SONOS 快閃式記憶元件之可靠性議題。其中包括重複寫入/抹除之耐久性、寫入狀態之資料保存、抹除狀態之臨界電壓漂移、讀取時之元件擾動。關於可靠性議題方面，抹除狀態資料遺失被觀測到。首先，在一經過多次寫入抹除元件中，抹除狀態之臨界電壓會隨著儲存時間而漂移。此漂移與溫度呈現弱相關。臨界電壓漂移與時間的相依性，可用穿隧波前模型來做完整的描述。此外，在兩位元操作下，有著明顯的讀取擾動效應。而一正電性之氧化層電荷導致通道電子注入之解析模型，被用來闡明此讀取擾動特性。氮化矽層電荷透過氧化層缺陷導致穿隧而造成之資料遺失，在此也被描述。Frenkel-Poole 散失為此最主要的機制。

另外，我們觀測到短時間因寫入動作干擾所引發的可靠性議題，並研究因隨機雜訊所引發之讀取電流不穩定，此一不穩定現象會隨著寫入/抹除次數增加和閘極長度微縮而變差。且利用通道熱電子所寫入之不均勻電荷分佈亦會擴大其效應。憑藉在本篇論文中所提及之氧化層改進方法，此種負面現象將得以舒緩。

SONOS Flash EEPROM Reliability Physics and Characterization

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Abstract.

The reliability issues of two-bit storage nitride flash memory cells including low-V_t state threshold voltage instability, read-disturb, and high-V_t state charge loss will be addressed. Program-state retention loss due to nitride charge escape via oxide trap assisted tunneling is also characterized. Frenkel-Poole emission is found to be the dominant mechanism. In addition, erase-state data loss is explored. An erase-state threshold drift with storage time is observed in a P/E cycled cell. This drift has insignificant temperature dependence. The temporal evolution of the threshold voltage drift can be well described by the tunneling front model. Furthermore, significant read-disturb effect is noticed in two-bit operation. An analytical model based on positive oxide charge assisted channel hot electron injection has been developed to explain the read-disturb behavior. Our study shows that the cell reliability

is strongly dependent on operation methods and process conditions.

Furthermore, program/erase cycling induced random telegraph noise in read current noise is observed. The amplitude of current fluctuation increases with P/E cycle number and with decreasing gate length. Non-uniform charge storage by CHE programming can further enhance read current fluctuation. The improvement of bottom oxide reliability can significantly reduce this effect.

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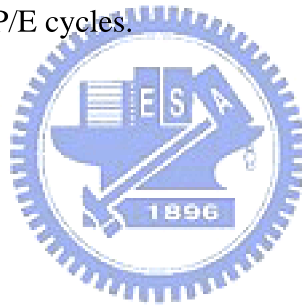


Chapter 1
Introduction

Currently, two major research thrusts in nonvolatile semiconductor memory are underway. One has data stored in a multi-layer gate structure in a field effect transistor and the other takes advantage of electrical polarization of ferroelectric material in a ferroelectric capacitor/transistor [1]. With respect to charge storage devices, there are two kinds of them. (a) Charge Trapping Devices: Charge is stored in traps at the interface of a multi-layer gate structure and/or in the bulk of insulator, such as the metal nitride oxide silicon (MNOS) structure [2], [3]. (b) Floating Gate Devices: Charge is stored in a thin conducting or semiconductor layer or conducting particles sandwiched between insulators [4], [5].

However, since its invention in 1967, the nitride-based nonvolatile memory structures, both MNOS and polysilicon oxide-nitride-oxide silicon (SONOS) [6]-[10], have received limited commercial acceptance due to their employment of ultra-thin dielectric (~20Å) and their non-ideal charge retention characteristics. In conventional SONOS cells, charges are stored uniformly in the nitride layer. This SONOS concept has recently evolved into a two-bit storage cell (NROM).

Recently, the new SONOS flash EEPROM cell has soon gained great attention for their smaller size per bit ($2.5F^2$/bit in Flash, where F is the feature size of the process) [11], [12], less fabrication complexity [13], no drain turn-on and better charge retentivity [14] This SONOS cell is made of a n-channel MOSFET with an oxide-nitride-oxide gate dielectric structure, as shown in Fig.1.1. The major difference between NROM and the conventional SONOS devices [15] is that the bottom oxide is about 60Å [11], which is much thicker than that of SONOS (~20 Å), where direct tunneling is involved for charge transport..

By taking advantage of localized charge storage in the nitride layer above the n^+

source and drain junctions, two-bit per cell operation can be achieved. Channel hot electron injection and band-to-band hot hole injection are utilized for programming and erasing, respectively. Table.1.1 shows the operation bias of program, erase, and read [16].

In this thesis, the reliability issues of the nitride flash cells will be reviewed. Responsible mechanisms and possible solutions will be discussed. Following the introduction, high-V_t state charge loss will be discussed in chapter two. In chapter three, we will discuss low-V_t state reliability issues. We will demonstrate a micro-second transient measurement circuit to investigate program disturb effect. Random telegraph noise induced read current fluctuation will be discussed in chapter four. Finally, we will make a conclusion of this thesis.

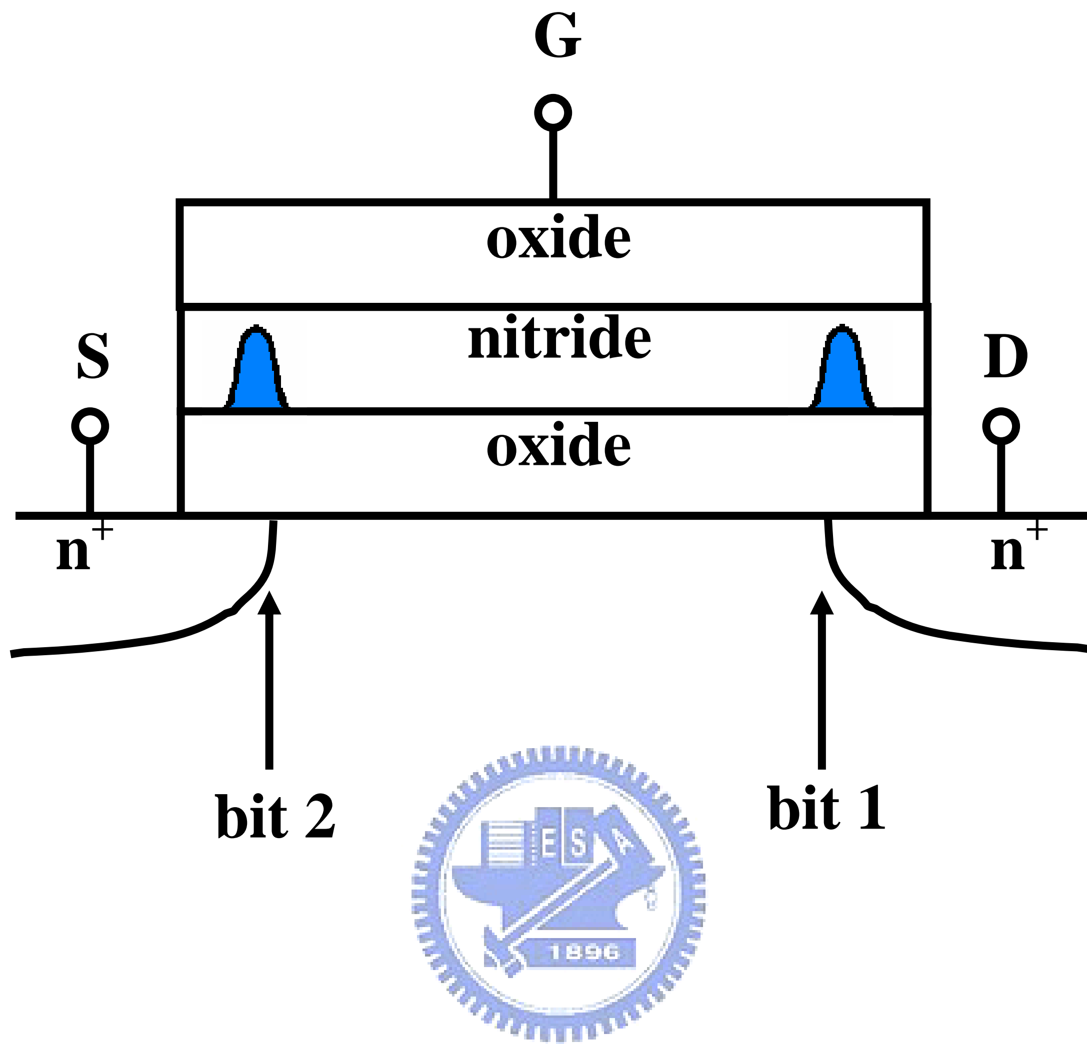


Fig. 1.1 Schematic representation of a SONOS cell and two-bit storage. The shaded area in the nitride layer represents stored charges.

Table.1.1 Suggested bias conditions for MXVAND cell operation.

		Program	Erase	Read
Bit 1	Vg	11V	-3V	2.5V
	Vd	5V	8V	0V
	Vs	0V	0V	>1.5V
Bit 2	Vg	11V	-3V	2.5V
	Vd	0V	0V	>1.5V
	Vs	5V	8V	0V

Chapter 2
High-V_t State Charge Loss

2.1 Introduction

One of the major advantages of the NROM cell, as compared with the floating gate flash EEPROM, is the better retentivity due to localized charge trapping [17]. The retention loss characteristics of the NROM are determined by two factors. (i) oxide charge detrapping (Q_{ox}) [18], and (ii) nitride charge loss (Q_{SiN}) [19]. The amount of created oxide trapped charge is dependent on P/E stress and oxide quality. In this cell, due to a thick bottom oxide, nitride charge escape to the substrate has to go through a two-step process, i.e. electron emission from nitride traps to the nitride conduction band and subsequently escape to the substrate via oxide trap assisted tunneling. Thus, nitride charge loss is also dependent on trap creation in the bottom oxide. Fig. 2.1 shows the retention loss versus P/E number. At low P/E stress, oxide trap creation is minimal and thus charge retention loss is small.

2.2 Oxide Charge Detrapping Mechanism

With respect to oxide charge detrapping, we utilize the so-called tunneling front model [20] to describe the charge detrapping behavior. A tunneling front moving through the oxide with distance/time dependence is given by

$$x_m(t) = (2\beta)^{-1} \cdot \ln(t/t_0) \qquad (2.1)$$

where $x_m(t)$ is the position of the front as a function of time t, β is the tunneling constant, and t_0 is the characteristic tunneling time.

Because of the sharpness of the moving tunneling front, the charge passed by the front can

be considered to be totally detrapped. The amount of charge escaping, ΔQ(t), via tunneling at time t can be approximated by

$$\Delta Q(t) = q\int_0^{x_m(t)} dx \cdot N(x) \tag{2.2}$$

where x is the distance from the Si-SiO_2 interface, q is the electronic charge, and N(x) is the spatial distribution of charged oxide traps. Note that for a uniform trap distribution N_{ox}, a logarithmic time dependence of ΔQ can be derived immediately from Eqs.(2.1) and (2.2), as shown in Eq.(2.3)

$$\Delta Q(t) = \frac{qN_{ox}}{2\beta}\ln(\frac{t}{t_0}) \tag{2.3}$$

According to the simple quantum mechanical two-band, one-electron tunneling theory, we can derive the tunneling parameter β as

$$\beta = \left[\frac{2m^*}{\hbar^2}E_{to}\right]^{1/2} \tag{2.4}$$

where m* is the tunneling effective mass of the trapped charge in oxide and E_{to} is the oxide trap energy. Finally, the threshold voltage shift due to oxide charge escape is

$$\Delta V_{th} = -2.3\frac{\overline{t_{ONO}}}{\varepsilon_{ONO}}\frac{q\hbar N_{OX}}{2\sqrt{2m^* E_{to}}}\log\frac{t}{t_0} \tag{2.5}$$

where t_{ONO} and ε_{ONO} are the equivalent thickness and dielectric constant of the ONO dielectrics, respectively.

2.3 Nitride Charge Retention Loss

2.3.1 Movement of Trapped Nitride Charge

The retention loss occurs either due to charge escape in the vertical direction (vertical retention loss [21]) or due to lateral redistribution of the trapped charge within nitride (lateral retention). Recently, Eitan's group makes efforts to investigate the cause of the charge loss in a NROM-like cell [11]. They claimed that the root cause of the threshold voltage lowering is lateral spread of stored charges since vertical retention is guaranteed by adopting a thick bottom oxide to avoid charge direct tunneling. Their argument is definitely correct in a fresh cell. However, it's not straightforward in a cycled cell due to the presence of oxide trap assisted tunneling.

The lateral distribution of the trapped nitride charge can be deduced at least qualitatively by the dispersion of the threshold voltage versus drain bias. As drain bias increases, the junction depletion region extends further into the channel. The nitride charge above the depletion region is "masked" and does not affect the threshold voltage. Fig. 2.2 shows the measured threshold voltage versus drain bias in a fresh device. To enhance charge movement in the nitride layer, the sample was baked at 85C for 1900 sec. The Vt-Vd after the bake is shown in the figure for a comparison. No significant change is noticed. The result in Fig. 2.2 suggests that lateral movement of the nitride charge is insignificant. We also measured the Vt-Vd in a 100k P/E device (Fig. 2.3). Similarly, lateral movement of the nitride charge is not observed. However, we observe a slight threshold voltage reduction at 85C bake, an evidence of charge loss in the vertical direction. Interestingly, if we applied a negative gate bias of 3V

during bake, a significant threshold voltage decrease is found in Fig. 2.3. From the above findings, we believe that the data retention loss is caused by charge escape in the vertical direction, since the application of a vertical field (Vg=-3V) apparently has a large influence on charge retention capability.

Next, we would like to investigate the influence of vertical field on charge retention loss in program state. Three different gate biases are applied in the retention measurements. Fig.2.4 shows the threshold voltage evolution with retention time in a fresh cell. No charge loss is observed for all three gate biases. The reason is that the bottom oxide in the fresh device is clean. As pointed out earlier, nitride charge loss is improbable without oxide trap assisted tunneling. At low P/E cycles, the bottom oxide plays a blocking role for nitride charge loss. In the 100k P/E device, apparent gate bias dependence of charge retention loss is obtained in Fig.2.5. As a conclusion, vertical retention loss is a dominant mechanism in a P/E cycled cell, which exhibits strong vertical field dependence.

The following measurement provides another evidence to exclude the possibility of lateral movement in the retention loss. Here, we use uniform channel FN injection rather than hot electron injection for programming. In this way, the injected nitride charge has a uniform distribution. The possibility of lateral movement can be ruled out completely in this case. Then, we use GIDL and GISL [22] to monitor the variation of charge in the two ends of the channel during retention measurement. Fig. 2.6 shows the measured result in a fresh cell. The GIDL/GISL are constant in the entire measurement period. In a P/E stressed device (stressed at the drain side), the threshold voltage and GISL still keep unchanged during the measurement, but GIDL decreases with time, as shown in Fig.2.7. The threshold voltage does not change because only the drain side is damaged and charge loss takes place in the drain side. The potential barrier in the channel region is mostly unaffected. Similarly, GISL does

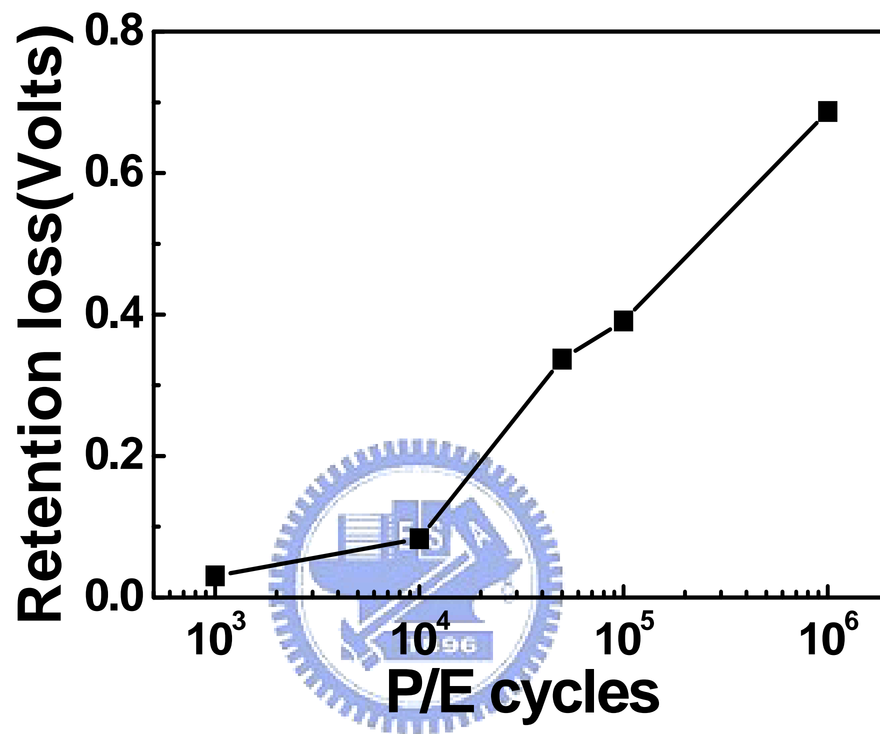


Fig. 2.1 Program-state retention loss versus P/E cycles.

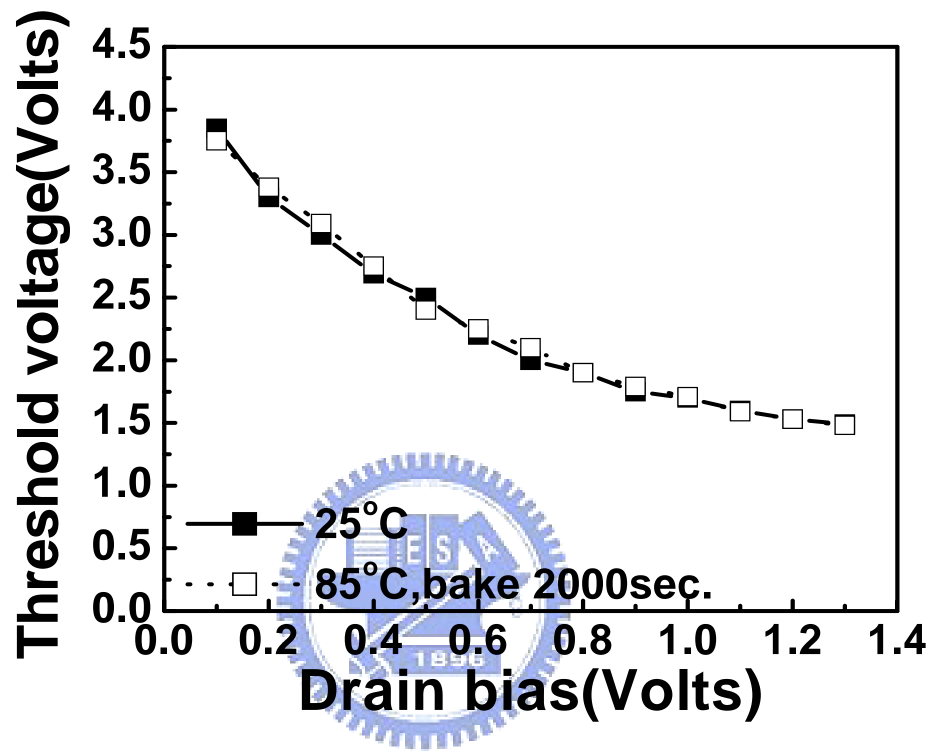


Fig. 2.2 Threshold voltage plotted against drain bias in a fresh device. T=25°C and 85°C.

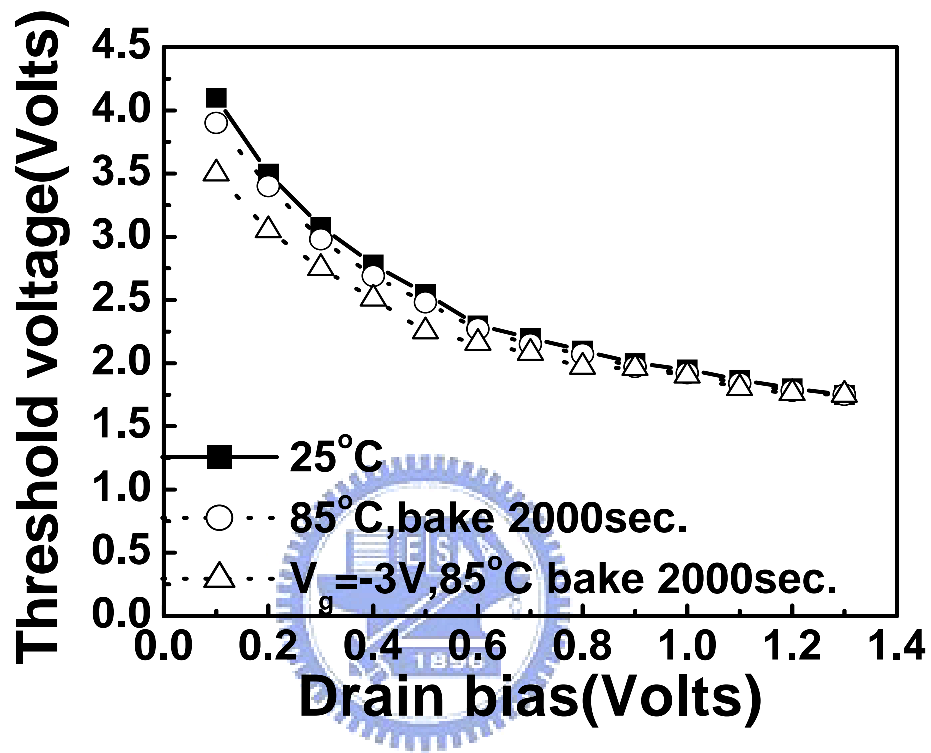


Fig.2.3 Threshold voltage versus drain bias in a 100k P/E cell.

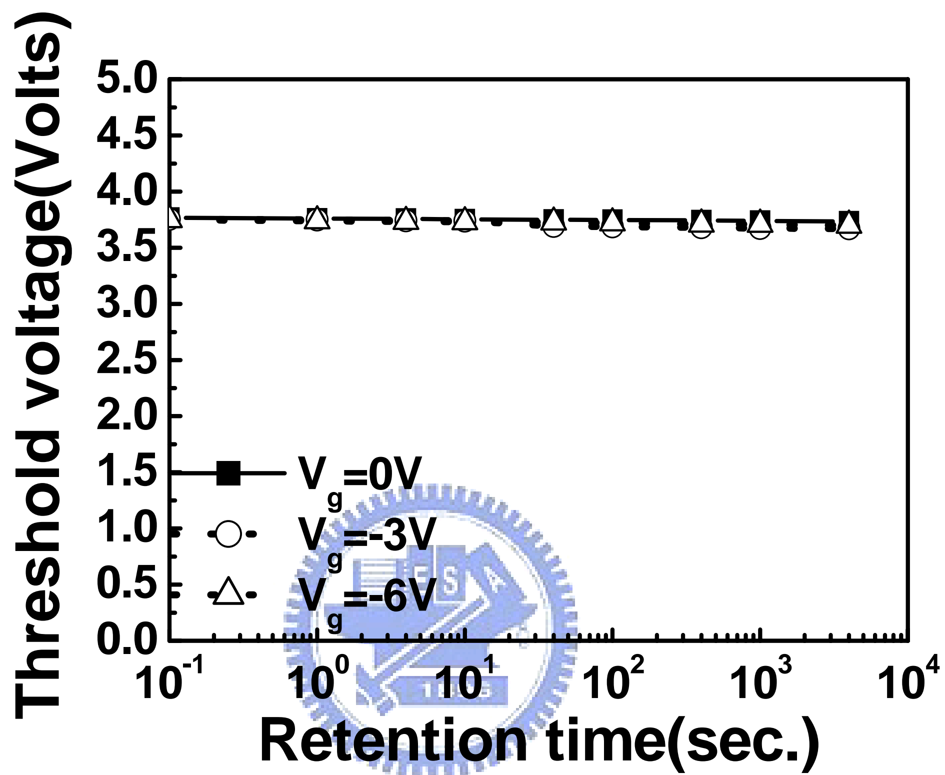


Fig. 2.4 Dependence of threshold voltage on retention time in a fresh cell. Gate bias is 0V, -3V and -6V in retention measurement state.

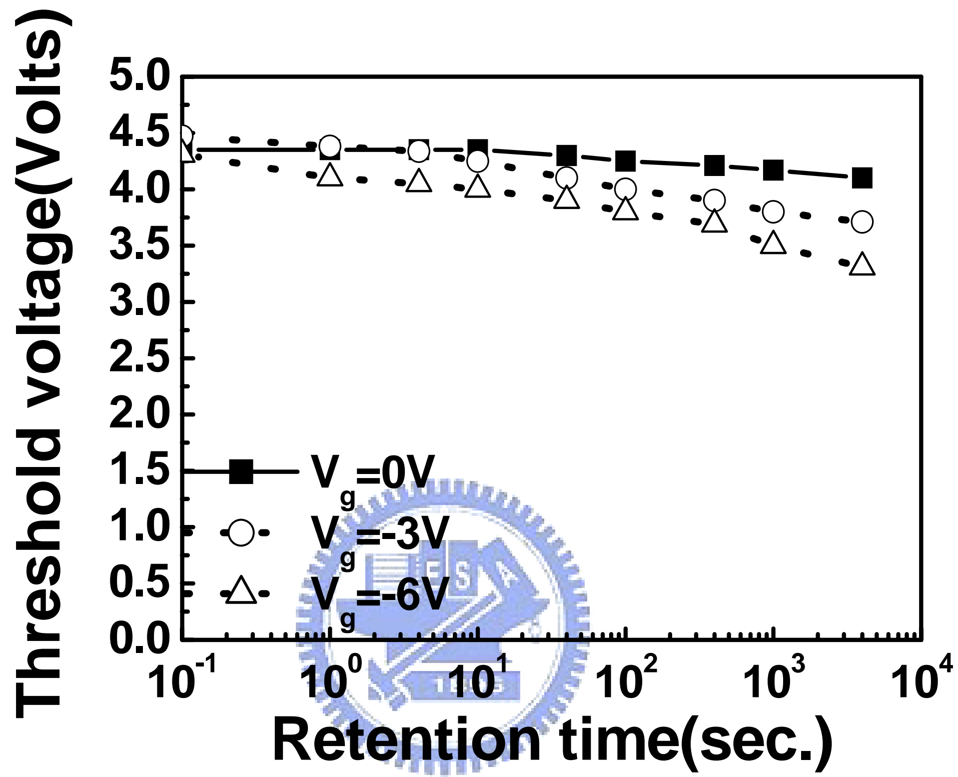


Fig. 2.5 Dependence of threshold voltage on retention time in a 100k P/E device. Retention gate bias is 0V, -3V and -6V.

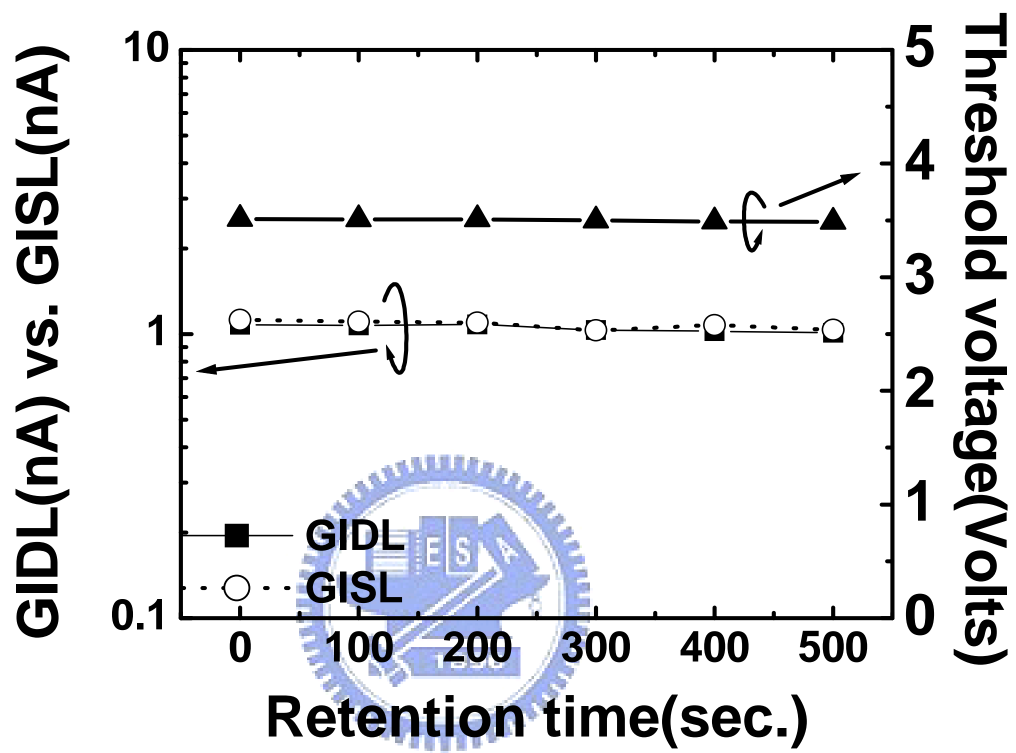


Fig. 2.6 Dependence of GIDL/GISL and threshold voltage on retention time in a fresh device.

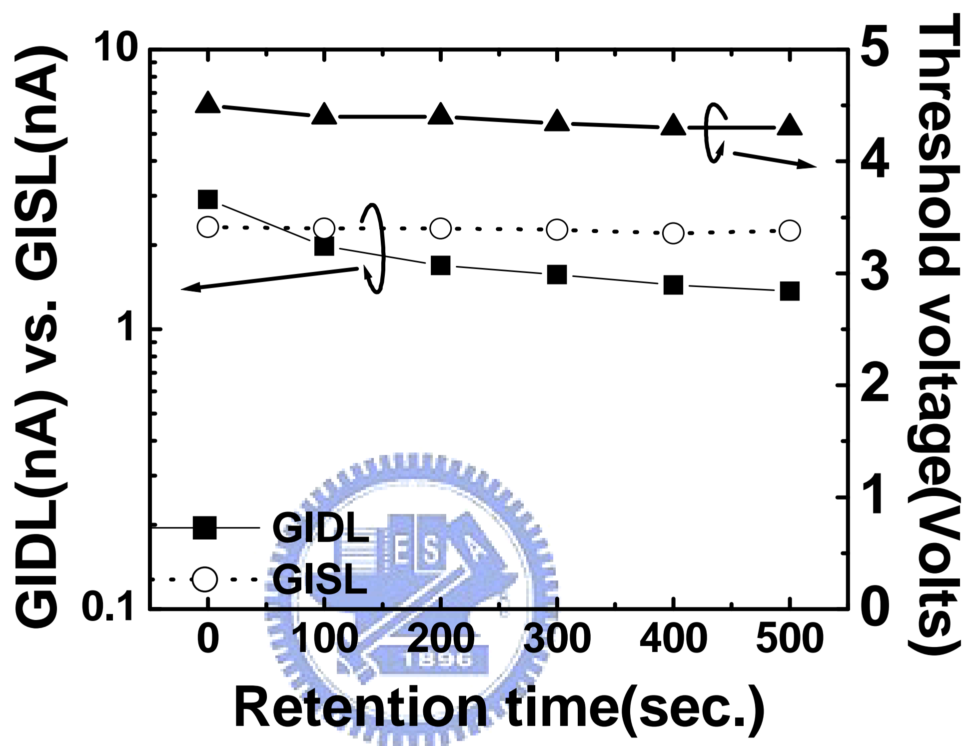


Fig. 2.7 Dependence of GIDL/GISL and threshold voltage on retention time in a 100k P/E device.

not change with time since GISL is affected only by the charge at the source end. This distinctly different feature of GISL and GIDL in Fig. 2.7 implies that the retention loss is correlated with oxide defects created by P/E stress. In summary, there are two factors affecting the nitride charge loss; (1) temperature, and (2) the damage due to cycling stress. Temperature will accelerate trapped charge emission rate but on the other side may cause oxide trap annealing and reduce the retention loss [23].

2.3.2 Data Retention Model

In this section, we will focus on the modeling of nitride charge detrapping processes in a NROM device. In our discussion, it's assumed that blocking oxide is thick enough to prevent any charge loss. All four device terminals are grounded when devices are in the retention mode. The nitride film is initially filled with injected electrons.

Fig.2.8 shows the retention characteristics at different P/E cycles. The cycling number and temperature dependence in Fig.2.8 implies that the stored nitride charge loss is through thermionic-field emission (Frenkel-Poole model [24]) and subsequently oxide trap assisted tunneling [25]. These processes are illustrated in Fig.2.9. The nitride charge emission time can be written below,

$$\tau_N = \tau_0 \exp((\phi_N - q(qE/\pi\varepsilon)^{1/2})/kT) \qquad (2.6)$$

where ϕ_N is the nitride trap energy, E is the electric field in nitride and other variables have their usual definition. The nitride charge emission current and the corresponding V_t shift can be derived as follows,

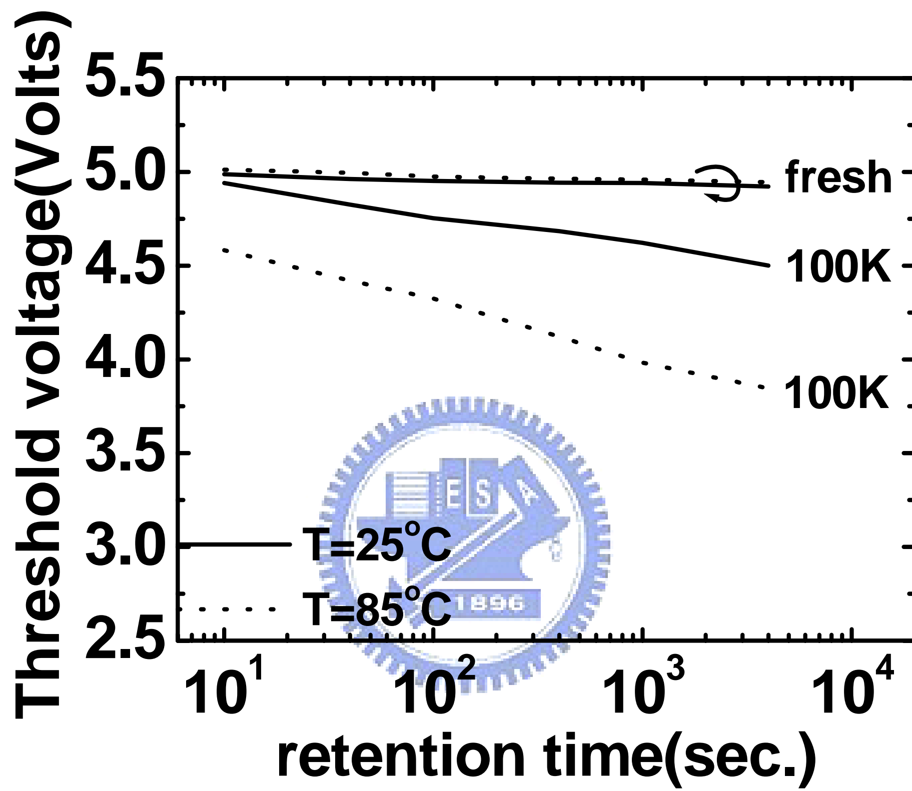


Fig. 2.8 Program-state charge loss characteristics in a fresh and a 100k P/E NROM cells. T=25℃ and 85℃.

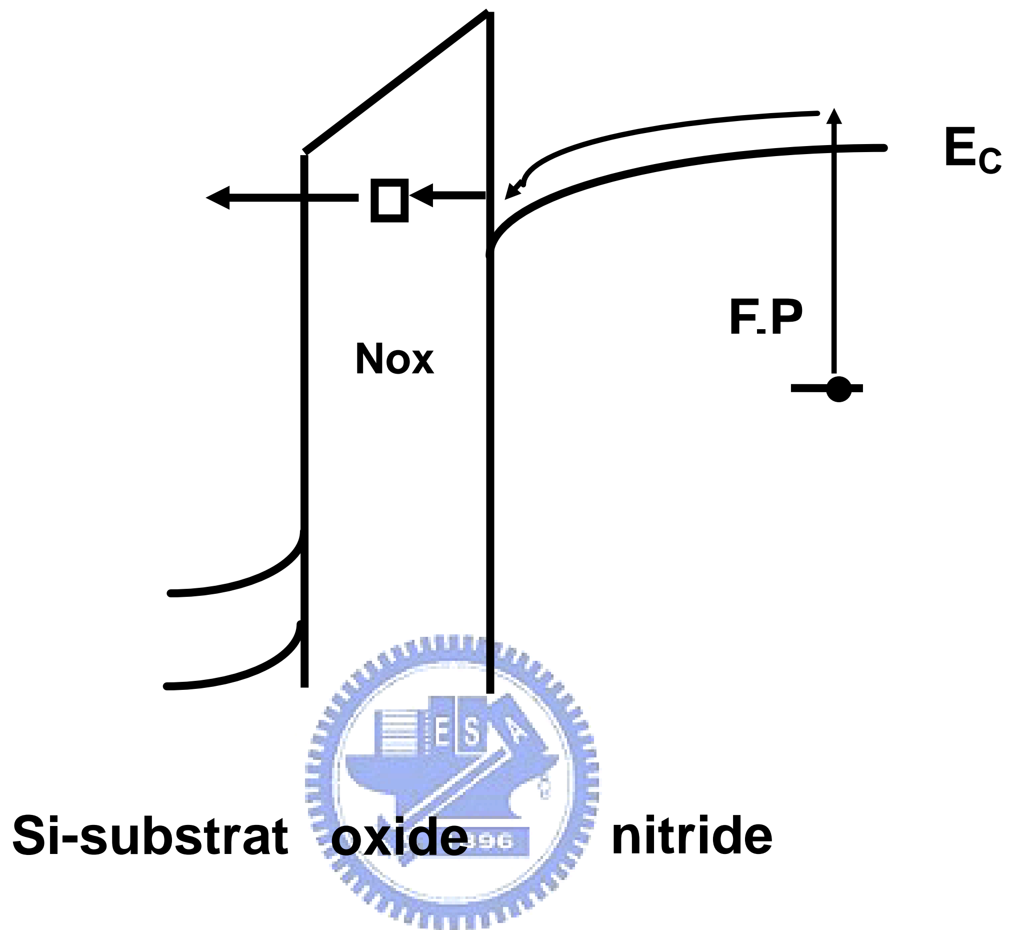


Fig. 2.9 Illustration of stored charge loss by Frenkel -Poole-emission and subsequently oxide trap assisted tunneling.

$$I_N = AQ_N \frac{d\phi_N}{dt} = \frac{AQ_N kT}{t} \qquad (2.7)$$

$$\Delta V_t(t) = \frac{Q_N}{C_{ONO}} [q(\frac{qE}{\pi\varepsilon})^{1/2} + kT \ln(\frac{t}{\tau_0})] \qquad (2.8)$$

where Q_N represents trapped charges in nitride per unit area and per unit trap energy. In the above derivation, we make the following assumptions. First, we assume that at measurement time t all nitride traps with time constants less than t are completely emptied and all other traps are unaffected. Secondly, we assume that nitride trapped charge escape is limited by the FP emission, i.e., trap-assisted tunneling in bottom oxide much faster than the FP emission. This assumption is reasonable in a heavily P/E cycled cell where bottom oxide stress is severe. Third, we assume that emitted nitride charges in a measurement interval from 1 second to 100 seconds (Fig. 2.10) have a uniform distribution in trap energy, i .e. , Q_N a constant . This assumption is also reasonable since the trap energy span in the measurement period is only about kTln(100)~0.12eV. For a constant energy distribution of nitride trapped charges, the nitride charge emission current obeys a 1/t relationship (Eq.(2.7) & Fig. 2.10) and the V_t loss is proportional to the square root of the electric field (Eq.(2.8) & Fig. 2.11).

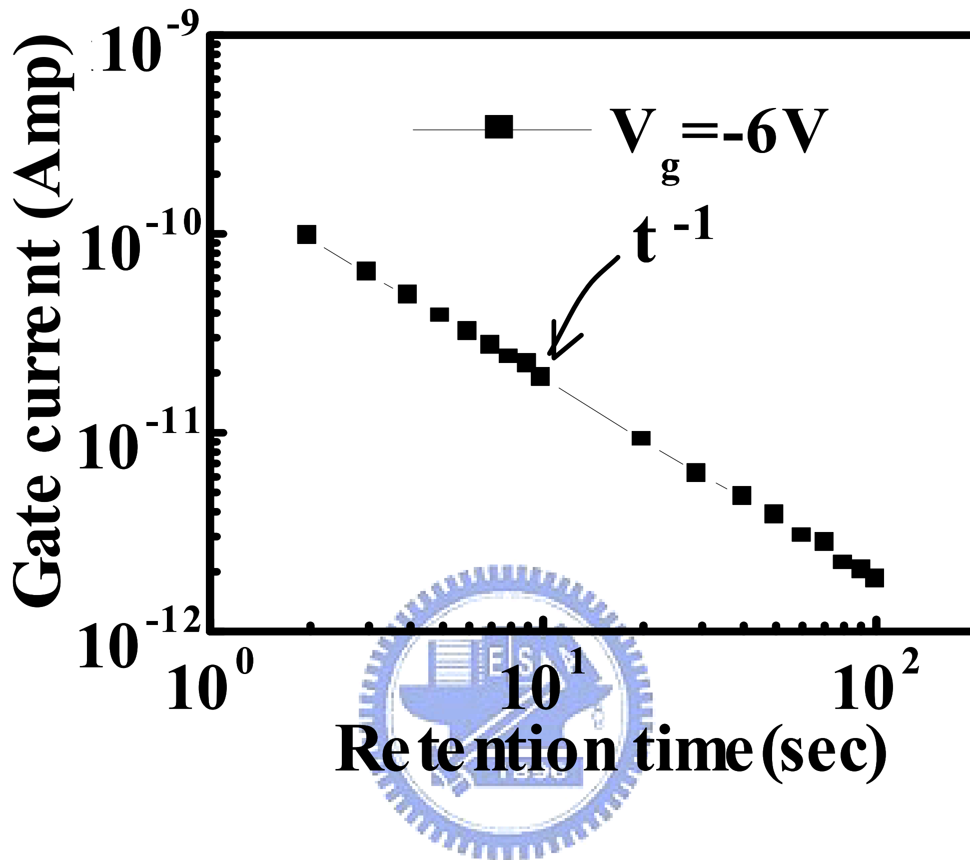


Fig. 2.10 Measured nitride charge detrapping current (I_N) in a large area device at Vg=-6V. The device was subject to FN stress at Vg= -20V for 2000s

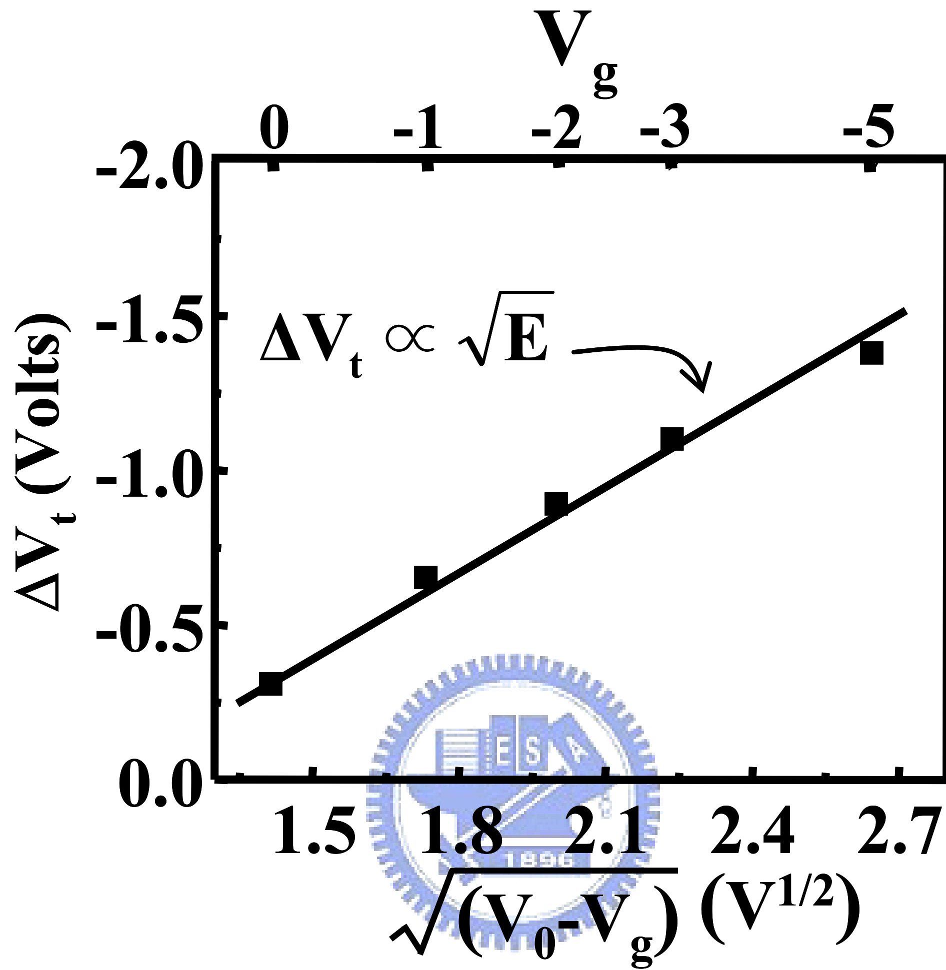


Fig. 2.11 High-V_t state charge loss versus applied gate bias (top axis). The bottom axis corresponds to the square root of the nitride electric field. Vo is the flat-band voltage in high-V_t state.

Chapter 3

Low-V_t State Reliability Issues

3.1 Introduction

In this chapter, we will discuss three erase-state retention loss phenomena, room temperature (RT) threshold voltage drift, read-disturb and over erase. The responsible physical mechanisms will be investigated.

3.2 Room-Temperature Threshold Voltage Drift

3.2.1 Mechanism of Vt Drift

The NROM cell exhibits excellent data retention behavior before P/E cycling. After P/E stress, a positive erase-state V_t drift with a logarithmic time-dependence is observed (Fig. 3.1). This V_t drift does not have temperature dependence. Positive oxide charge tunnel detrapping was proposed [28] to explain this phenomenon. In order to measure positive oxide charge detrapping current directly (Fig. 3.2(a)), large area devices were fabricated with two different ONO processes (A and B). Process B is known to have better oxide endurance. The substrate current (I_b) before and after FN stress was measured in these two samples. According to the hole tunneling front model [29], the post-stress substrate current resulting from positive oxide charge detrapping follows a 1/t time-dependence,

$$I_b(t)=A\frac{Q_{ox}}{\alpha_h}t^{-1} \tag{3.1}$$

$$\alpha_h=4\pi\sqrt{2m\phi_{ox}}/h \tag{3.2}$$

where Q_{ox} is the positive oxide charge density, ϕ_{ox} denotes the energy barrier of positive

trapped charges and A is the area of the device. Fig. 3.2(b) shows the measured pre-stress and post-stress substrate currents versus time. Note that process B exhibits a smaller post-stress substrate current because of less positive oxide charge creation.

Fig. 3.3 shows the measured V_t drift in two 10k P/E cycled cells. By comparing the two ONO processes, a correlation between the V_t drift and I_b is obtained.

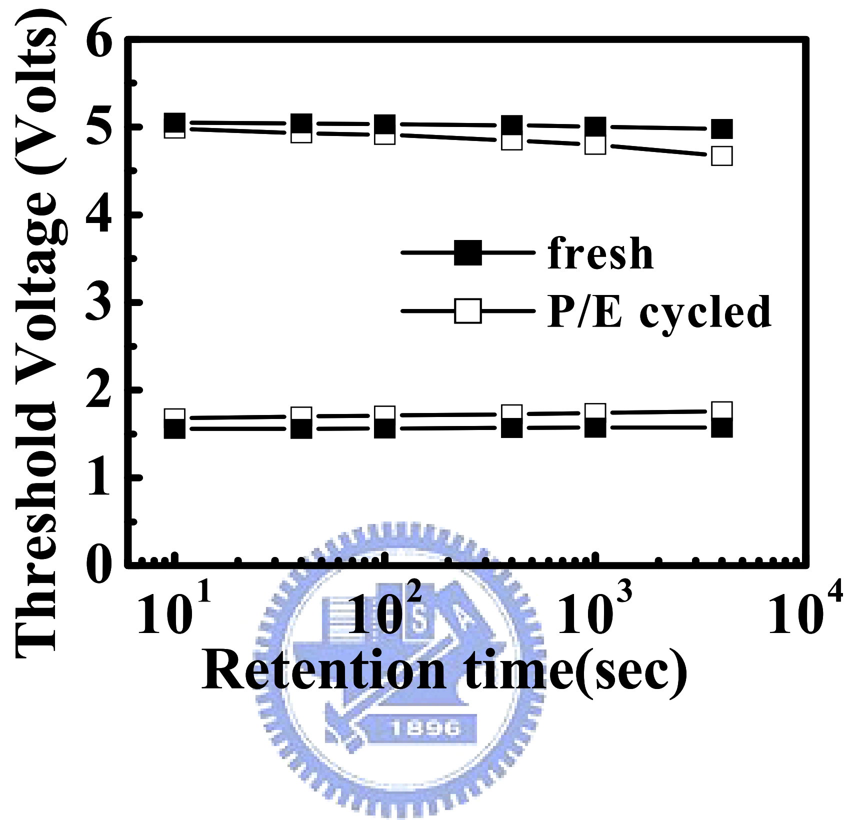
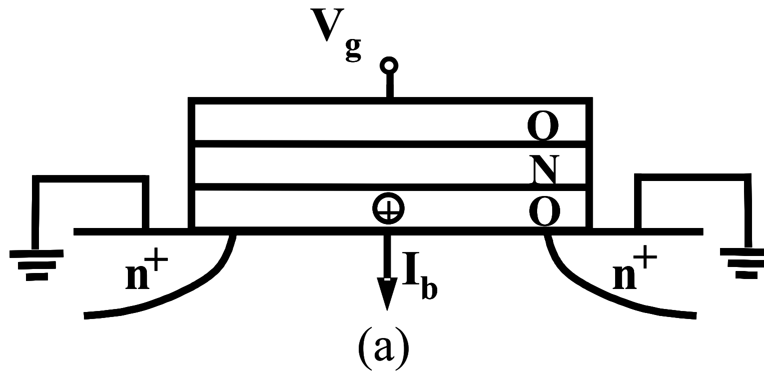
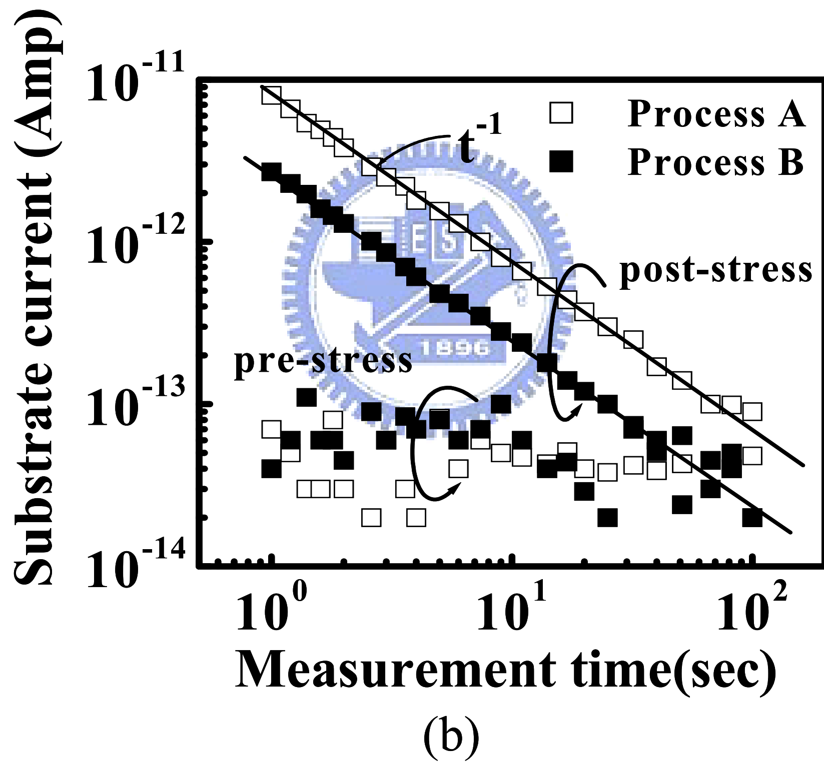


Fig. 3.1 Typical V_t retention characteristics in a fresh and a 100k P/E cycled cell.



(a)



(b)

Fig. 3.2(a) Measurement setup of positive oxide charge detrapping induced substrate current (I_b).

Fig. 3.2(b) Pre-stress and post-stress substrate currents in two large area devices (500 μm × 500 μm). FN stress was at Vg = -18V for 3000s. Substrate current was measured at $Vg=V_{FB}$.

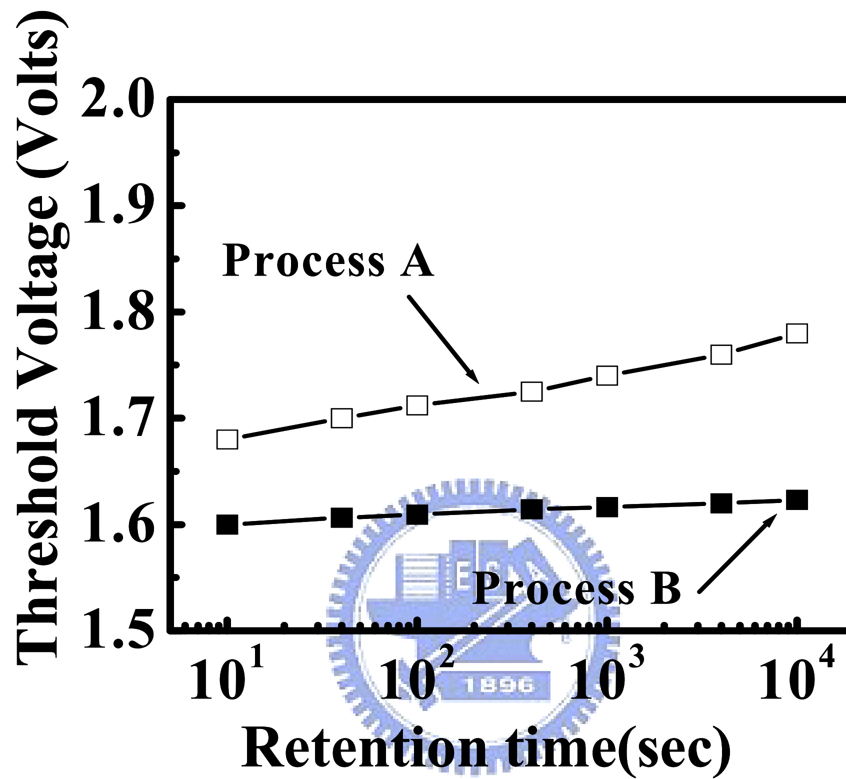


Fig.3.3 Room temperature V_t drift in two 10k P/E cycled NROM cells fabricated with different ONO process. The cell size is Lg =0.5μm and Wg = 0.35μm.

3.2.2 Time Dependence of Vt Drift

To explain the observed time-dependence of the RT drift, the tunneling front model discussed in Chapter 2 is employed. In a P/E stressed device, the trapped hole in the bottom oxide can escape to the substrate via tunneling. Based on the tunneling front model, the threshold voltage shift caused by valence band electron tunneling is illustrated by path A in Fig.3.4

$$\Delta V_{th} = -2.3 \frac{\overline{t_{ONO}}}{\varepsilon_{ONO}} \frac{q\hbar N_{ox}}{2\sqrt{2m^*(\phi_B + E_g)}} \log t \quad (3.3)$$

and the threshold voltage shift caused by conduction band electron tunneling is illustrated by path B in Fig.3.4

$$\Delta V_{th} = -2.3 \frac{\overline{t_{ONO}}}{\varepsilon_{ONO}} \frac{q\hbar N_{ox}}{2\sqrt{2m^*(\phi_B)}} \log t \quad (3.4)$$

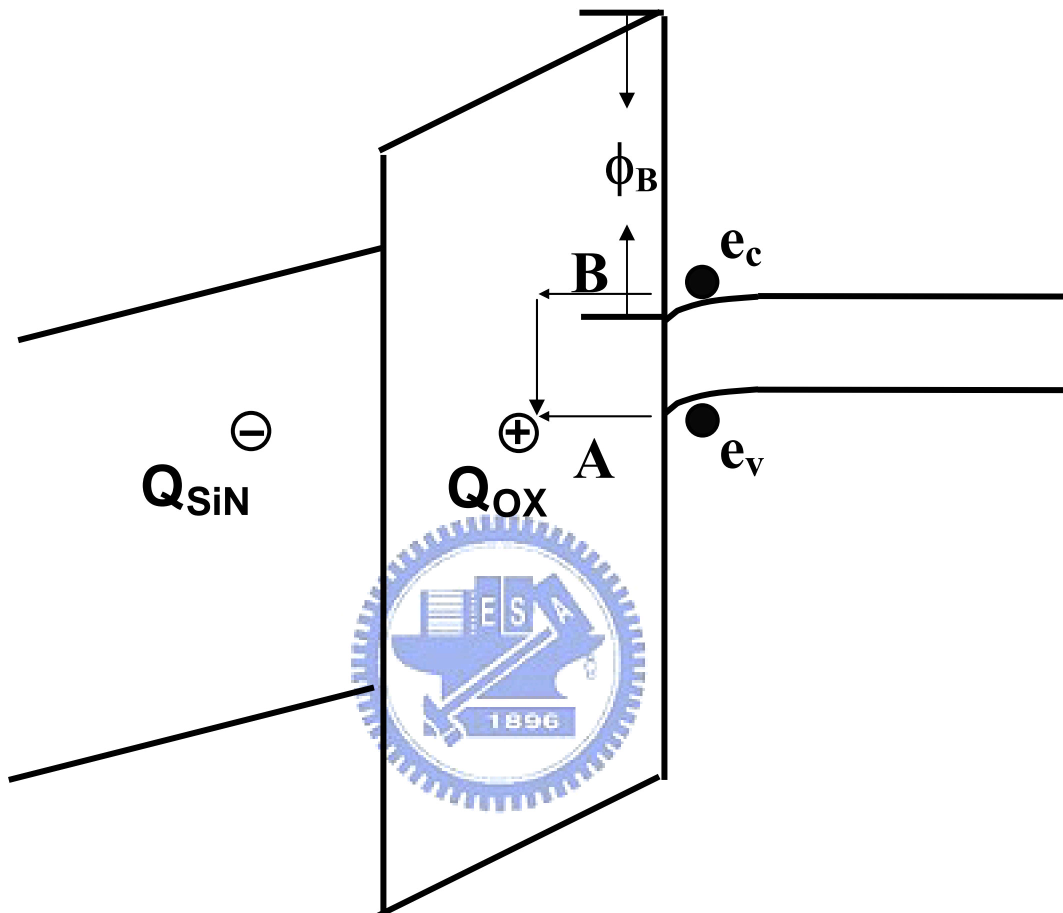


Fig.3.4 Schematic band diagram showing positive oxide charge and negative nitride charge in a 1k P/E cycled device. The electrons in valance band and conduction band can tunnel to recombine with positive oxide charge via path A and path B.

3.3 Read-Disturb Effects in Erase State

3.3.1 Cause of Read-Disturb Effect

Read-disturb effect is twofold. The wordline voltage during read may enhance the RT drift in the neighboring bit. On the other side, the relatively large read bitline voltage may cause channel hot electron injection and result in a significant threshold voltage shift of the neighboring bit. The hot electron injection caused Vt shift follows power-law time-dependence. An analytical model based on positive oxide charge assisted channel hot electron.

3.3.2 Commonality between Vt Drift and Read-Disturb

The RT drift and read-disturb have something in common. We performed RT drift measurement and the read-disturb measurement in the same device sequentially. No matter the RT drift or the read-disturb is measured first, the subsequent read-disturb or RT drift is significantly reduced. From the study in the preceding section, we believe that read-disturb is also related to trapped charge in the bottom oxide.

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3.3.3 Read-Disturb Behavior

At V_g=3.0V, V_d=2.5V, the read-disturb caused Vt shift follows a power-law time dependence (t^n) (Fig. 3.5). Channel electrons can gain sufficient energy from a large electric field to inject into the nitride conduction band and then get trapped in the nitride. In the next section, we will develop the read-disturb model based on the channel hot electron injection into the SiN via positive charge assisted tunneling (PCAT).

3.3.4 PCAT Model in Read-Disturb

The columbic potential of a positive oxide charge acts as a sequential tunneling center. The channel hot electron injection into nitride via PCAT is illustrated in Fig.3.6. I_{cat} is positive charge assisted electron tunneling current.

$$I_{cat} \propto t^{-P}, P = (\frac{m_e \phi_e}{m_h \phi_h})^{1/2} \quad (3.6)$$

The time dependence of the threshold voltage shift from I_{cat} injection is derived in the following.

$$\Delta V_{th} \propto \int I_{cat}(t)dt = \int t^{-P}dt = t^{1-P} = t^n \quad (3.7)$$

It is a general trend in literature to have $m_h \geq m_e$ [29-31] and $\phi_h \geq \phi_e$ [32,20]. Thus the power factor P in Eq.3.6 is expected to be smaller than 1 and the extracted value of P in [33] is about 0.7. In other words, n is about 0.3, which is consistent with our measured result.

Moreover, since the bit-line voltage in reverse read must be sufficiently large to overcome the stored charge of the second bit, hot electron injection during read should be considered. The hot electron read disturb is worsened in a P/E cycled cell because of positive oxide charge enhanced electron injection. Fig. 3.7 shows the V_t shift versus read bit-line voltage in a fresh device and in a 10K P/E cycled NROM cell [34]. The read disturb increases drastically as the read voltage is above 2V. Lower operating temperature and shorter gate length will aggravate hot electron read disturb (Fig. 3.8).

Various methods were proposed [35, 36] to reduce the positive oxide charge enhanced read-disturb.

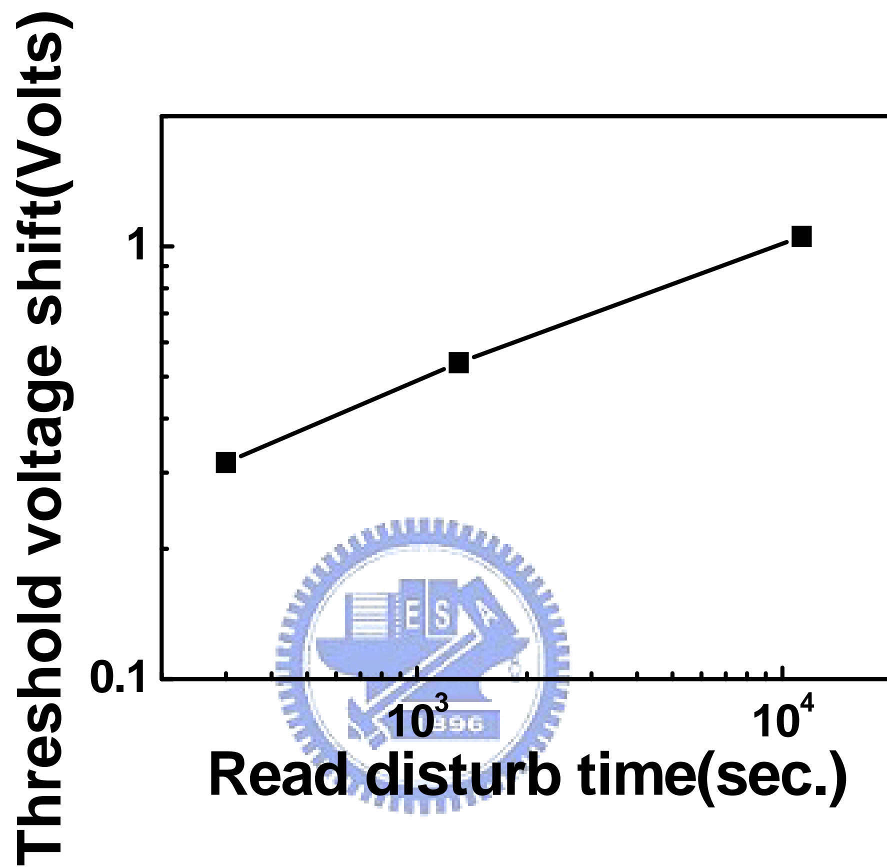


Fig.3.5 Dependence of Vt shift on read-disturb time in a 1k P/E cycled cell. Power-law time dependence (t^n) is obtained. The read bias condition is V_g=3V, V_d=2.5V.

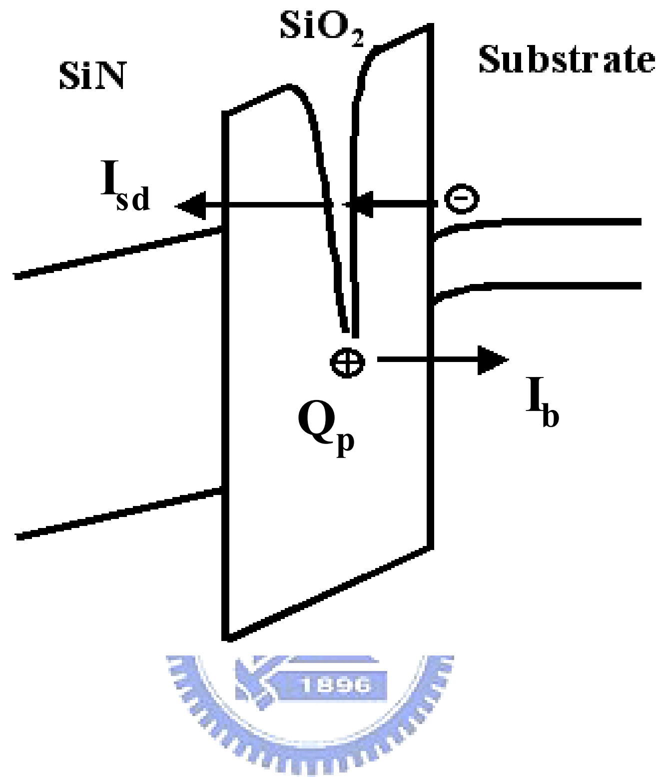


Fig.3.6 Illustration of positive charge assisted electron tunneling current (I_{sd}) in gate disturb.

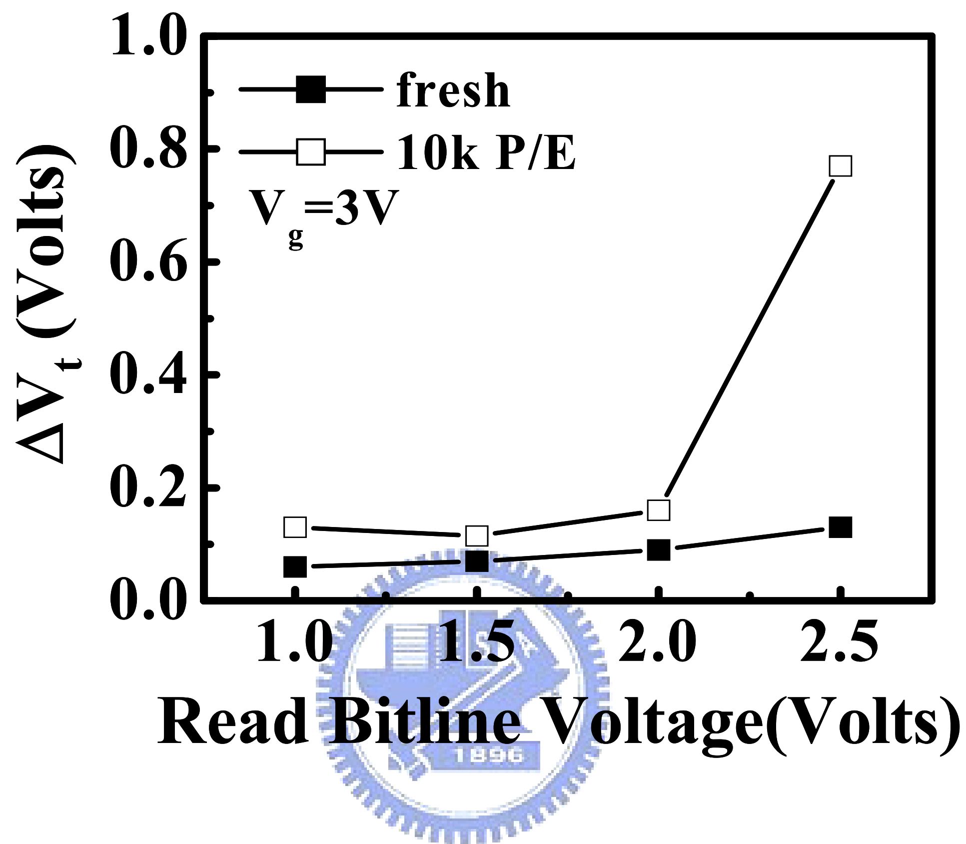


Fig.3.7 Hot carrier read-disturb caused ΔV_t in a fresh cell and in a 10k P/E cycled cell. The disturb time is 10^4s.

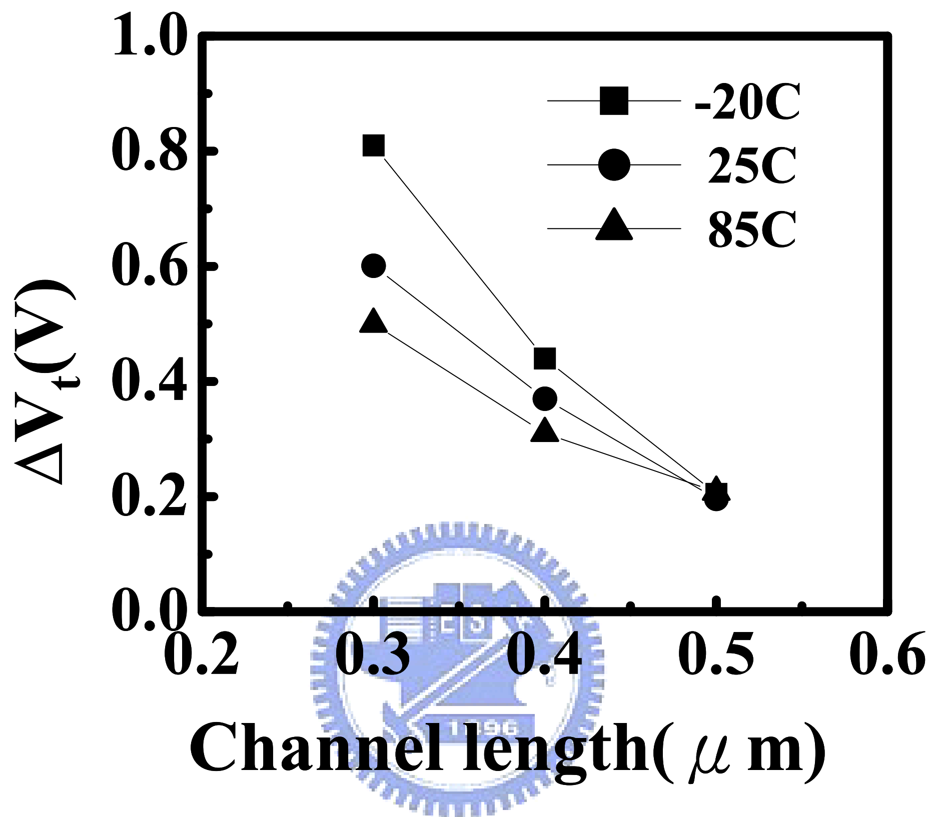


Fig.3.8 Temperature effect on read disturb of 1k P/E cycled cells. Devices with a gate length of 0.5μm, 0.4μm and 0.3μm are characterized. The applied gate and drain biases are 3V and 1.6V, respectively, and the disturb time is 10^4 sec.

3.4 Over-erase

One major reliability concern in a NROM cell comes from the lateral migration of trapped charges in the nitride layer [37]. This effect is more serious in hole accumulation state (erase state) since trapped holes are more mobile than electrons in a nitride [38]. To investigate hole lateral movement in erase state, an extremely strong band-to-band hot hole injection condition is used. As opposed to the RT V_t drift, the over-erased cell shows a negative V_t drift with time (Fig. 3.9). This effect is more significant at higher temperatures and is attributed to trapped hole hopping in the lateral direction [39].

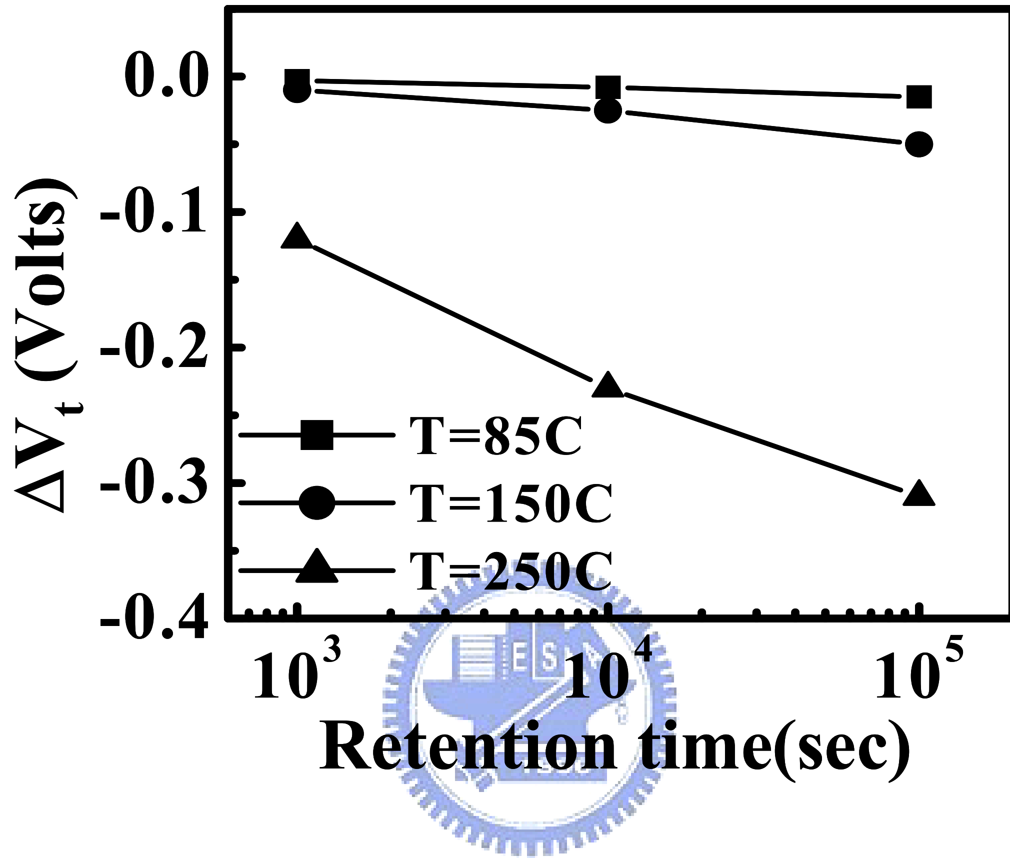


Fig.3.9 The evolution of erase-state V_t with storage time in an over-erased cell. The band-to-band hot hole injection

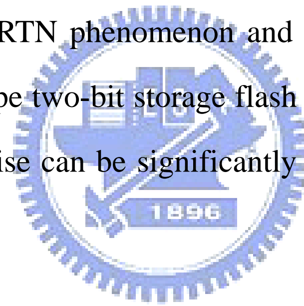
Chapter 4

P/E Cycling Induced Read Current Noise

4.1 Introduction

In this chapter, we investigate P/E cycling induced random telegraph noise (RTN) in non-uniform charge storage nitride flash cells for the first time. The amplitude of RTN increases with P/E cycle number and with decreasing gate length. Non-uniform charge storage by channel hot electron programming can further enhance read current fluctuation. The large amplitude of read current fluctuation implies we must allow for more margins in cell operation and needs careful attention especially in Multi-level cell (MLC) application.

Therefore, to probe the RTN phenomenon and to find the solutions will be an important issue in SONOS type two-bit storage flash memory cells. According to our investigation, read current noise can be significantly reduced by the improvement of bottom oxide reliability.



4.2 Random Telegraph Noise Measurement

The charge transport through a MOSFET device characterized by discrete switching events of the drain current, has often been observed and attributed to the trapping/detrapping of conduction carriers by a single defect near Si/SiO_2 interface [37]-[39]. Different names exist for the phenomenon, like burst noise or Random Telegraph Noise (RTN). Micro-second Transient measurement system for measuring read current noise is shown in Fig. 4.1. This setup can monitor the drain current noise in fixed read bias. The sampling rate in our experiments is 10kHz, which enables the observation of fast transitions of read current with time constant down to 0.1ms, which corresponds to 10^5 reading in each measurement of 10 seconds. The devices used in this work have a gate length of 0.35μm and a gate with from 0.5μm to 0.3μm.

4.3 P/E Cycling Stress

In a P/E cycled cell, the read current fluctuation induced by oxide trap is found to be larger than that in a fresh cell. Fig. 4.2 shows read current fluctuation at program state in a fresh cell, after 1k P/E cycles and after 100k P/E cycles. The cell biased in weak inversion and the read current is near 1μA. The apparent random telegraph noise patterns are observed in a 100k P/E cycled cell while it is undetected in a fresh cell. The RTN rises from the charging/discharging of single oxide trap or multiple oxide traps created by P/E cycling stress [40]. At a low cycle number the RTN exhibits two-level transitions (Fig. 4.2(b)) while at a large cycle number multi-level transitions (4-level) are occasionally observed (Fig. 4.2(c)). These multi-level transitions, superimposed by several independent two-level RTN waveforms, may exhibit a large ΔId and result in a read failure.

The dependence of noise amplitude on read current level is shown in Fig. 4.3. In this measurement, a NROM cell is programmed to different Vt and the reverse read bias is at |Vds|=1.5V and Vgs=4V. The cycle number is 100 that only two-level transitions are obtained. As shown in Fig. 4.3(a), ΔId is found to increase from 0.04μA in a high-Vt cell (1μA read current) to 0.18μA in a low-Vt cell (30μA read current).

4.4 Length Dependence & Non-uniform Vt Effect

The gate length effect on RTN is shown in Fig. 4.4. The read current level is about 1μA. The RTN amplitude with two-level transitions is shown in Fig. 4.4(a), a noticeable increases of ΔI_d with decreasing gate length [41]. A two-dimensional device simulation is performed to calculate the gate length dependence. A similar trend is obtained (Fig. 4.5). Moreover, RTN is found to be further enhanced by localized charge storage. Fig. 4.6 shows the current fluctuations by FN injection and

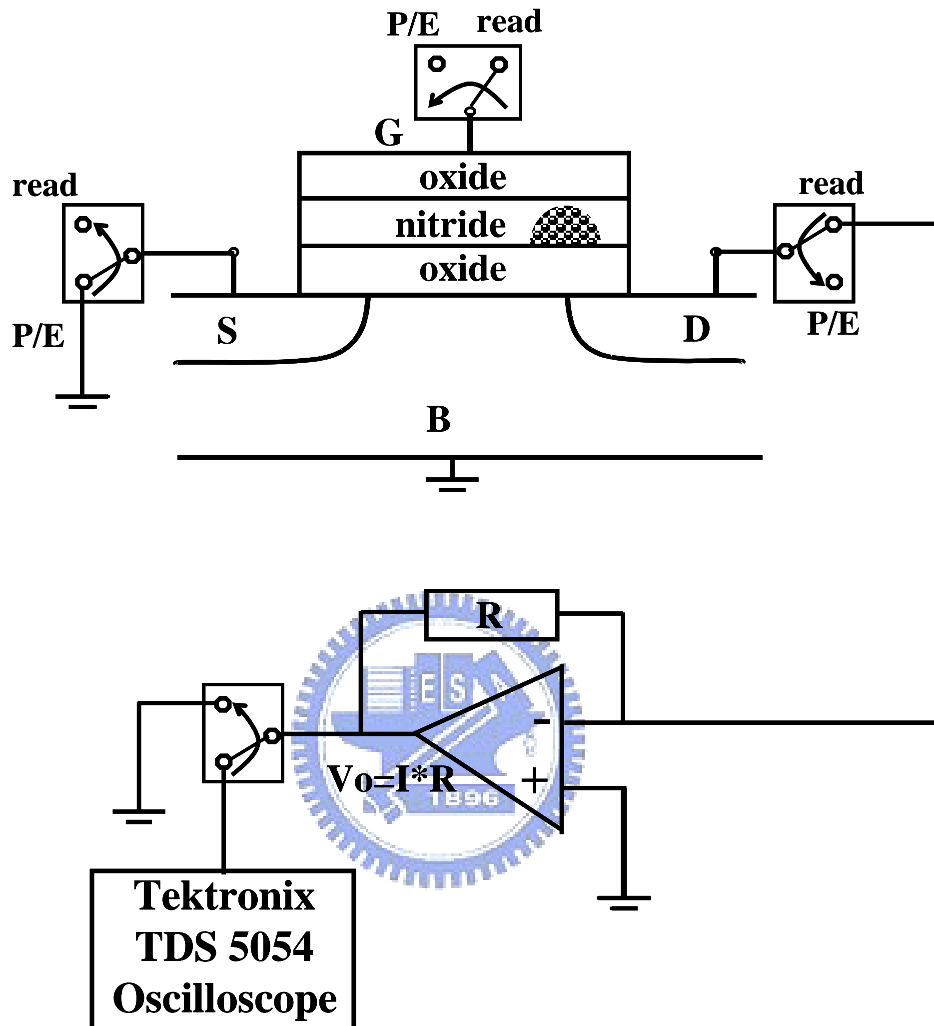


Fig. 4.1 Experimental setup for RTN measurement.

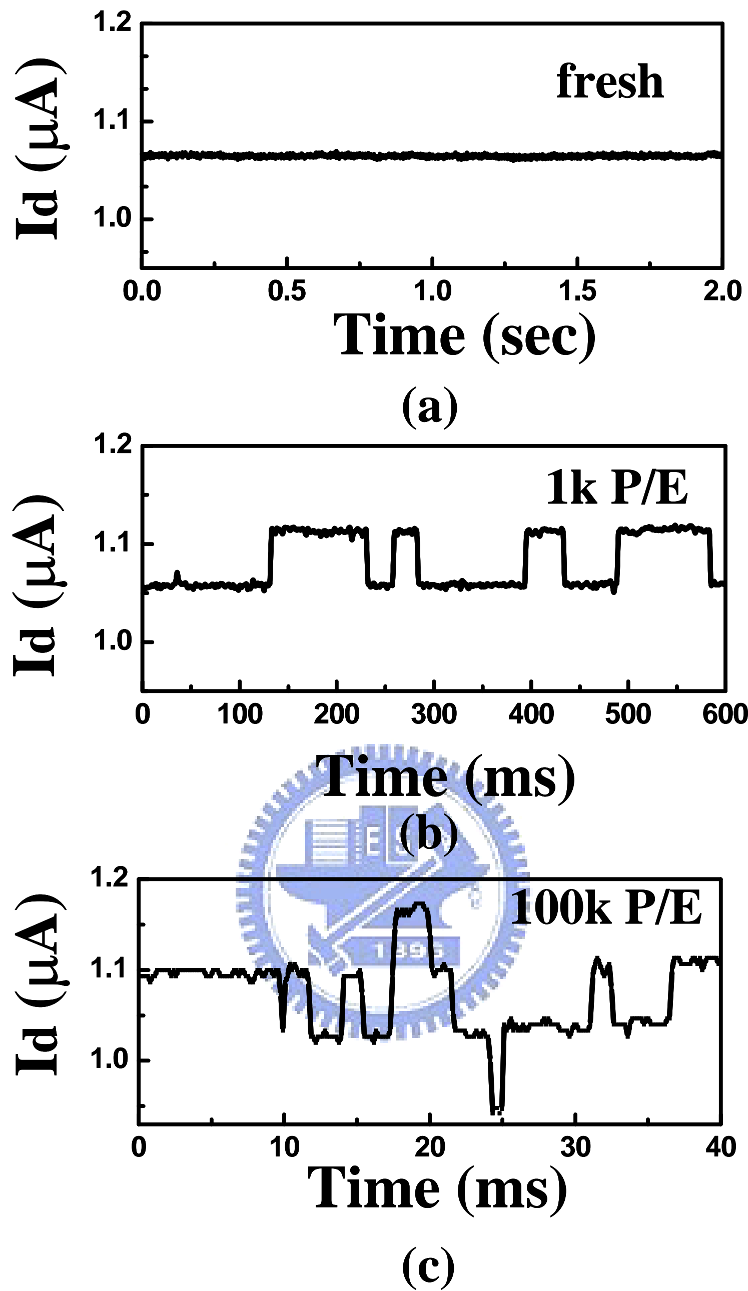
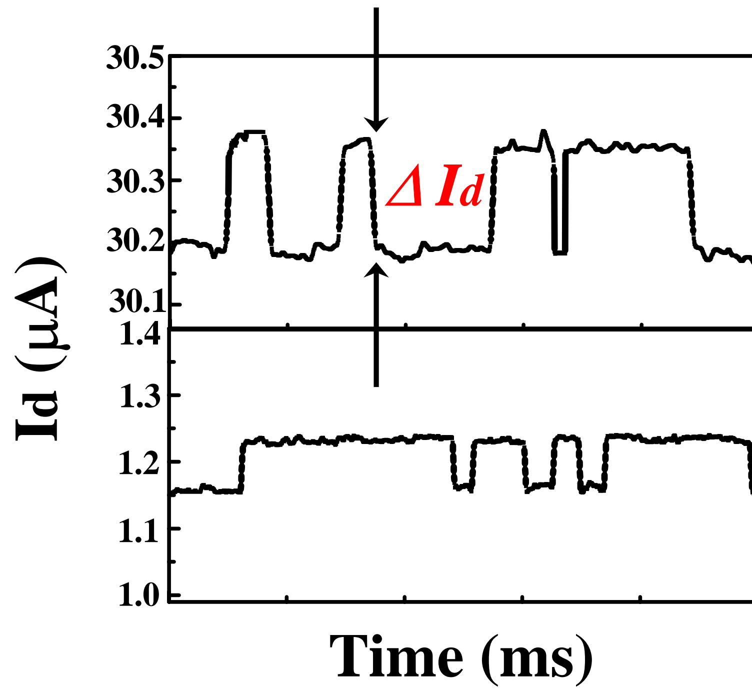
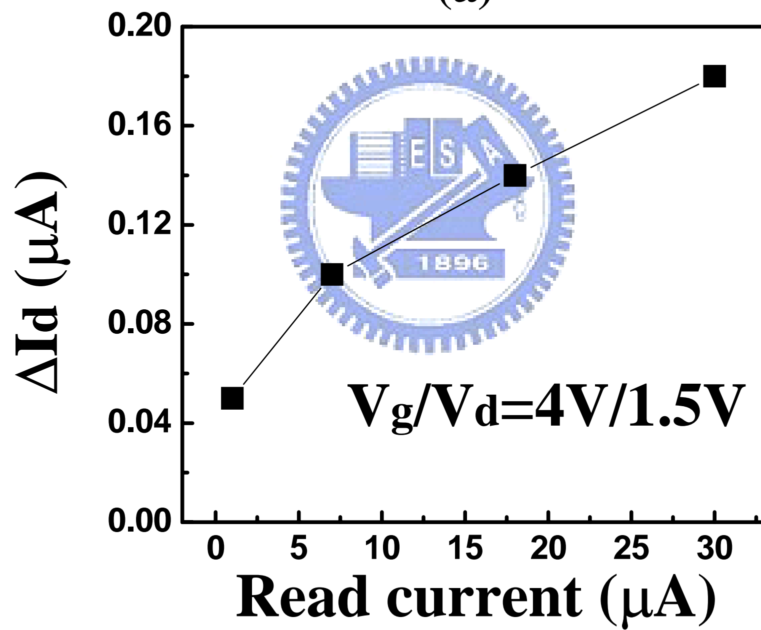


Fig. 4.2 Representative RTN traces in a NROM cell (W/L=0.35μm/0.3μm). (a) fresh, (b) 1k P/E cycles, (c) 100k P/E cycles.



(a)



(b)

Fig. 4.3 (a) Comparison of RTN amplitude in program-state and in erase-state (b) Dependence of ΔId (two-level transition) on read current. The P/E cycle number is 100 P/E. The reverse read bias is V_g=4V, V_s=1.5V and V_d=0V.

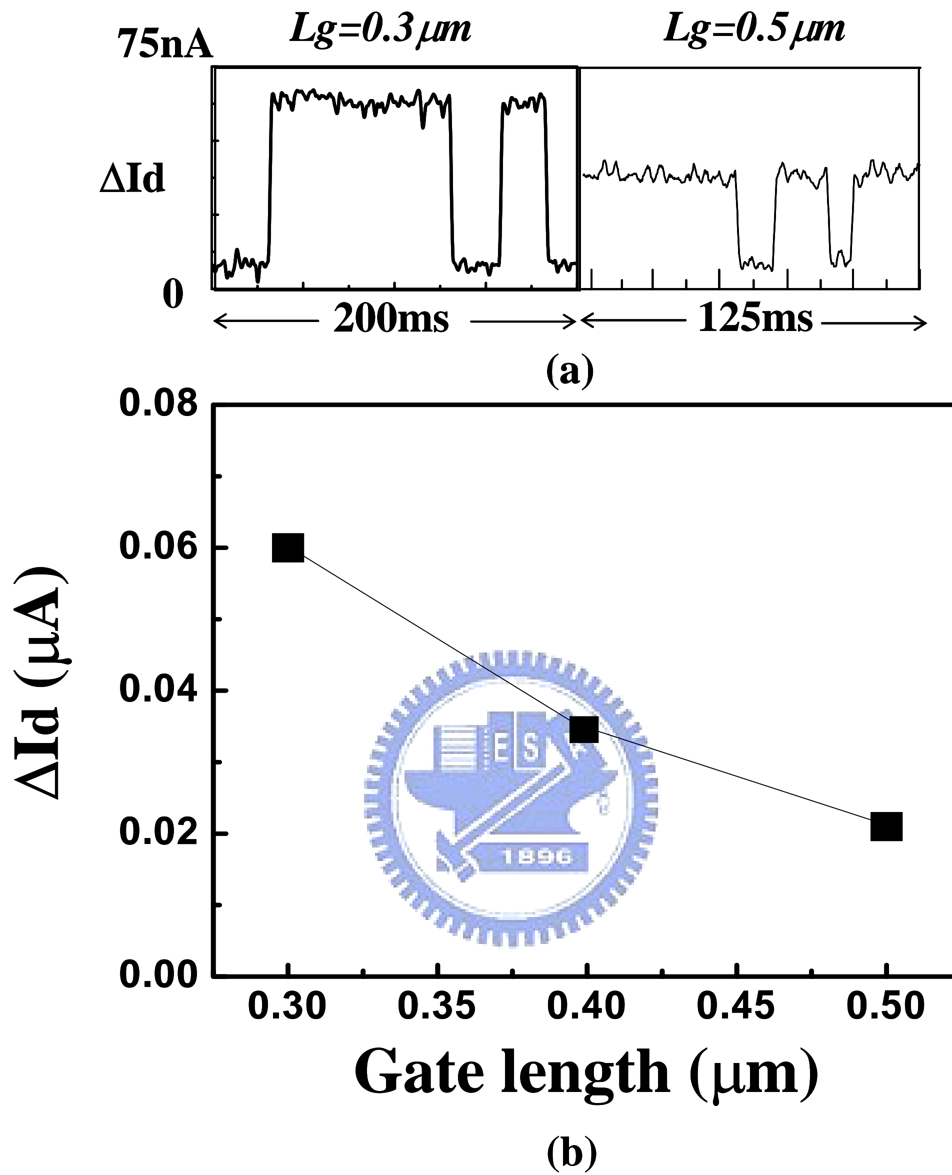


Fig. 4.4 (a) Comparison of RTN amplitude for Lg=0.3μm and 0.5μm. (b) Dependence of ΔId (two-level transition) on gate length. The read current level is about 1μA.

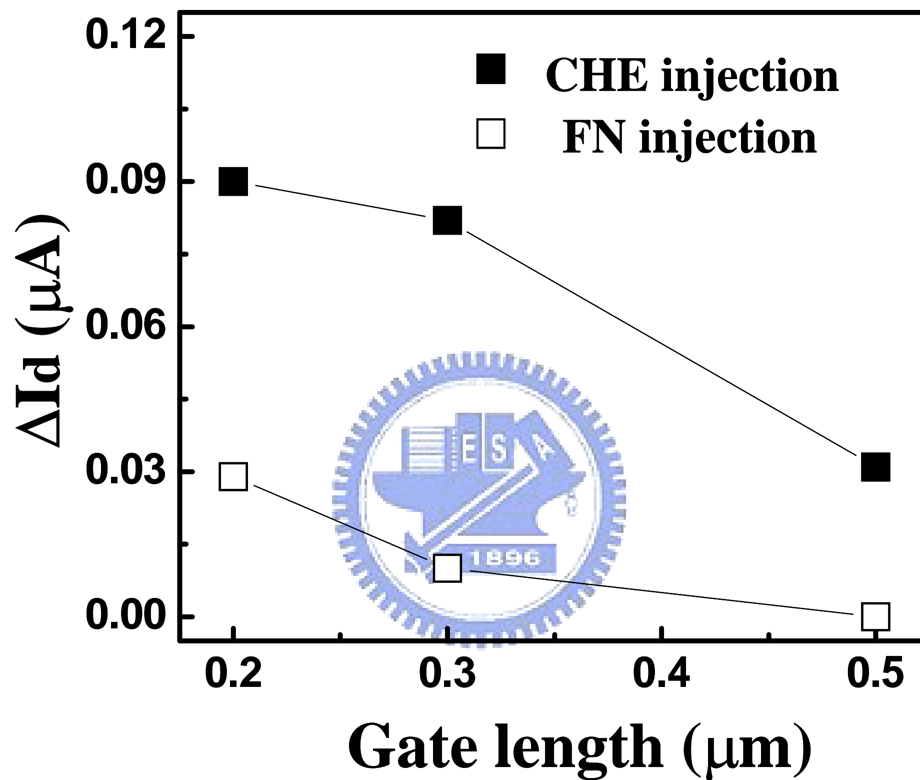


Fig. 4.5 Calculated gate length dependence of two-level RTN amplitude from 2D device simulation. For CHE injection, the trapped charge width is assumed to be 30nm. FN injection has uniform charge storage. The parameters in simulation are not calibrated.

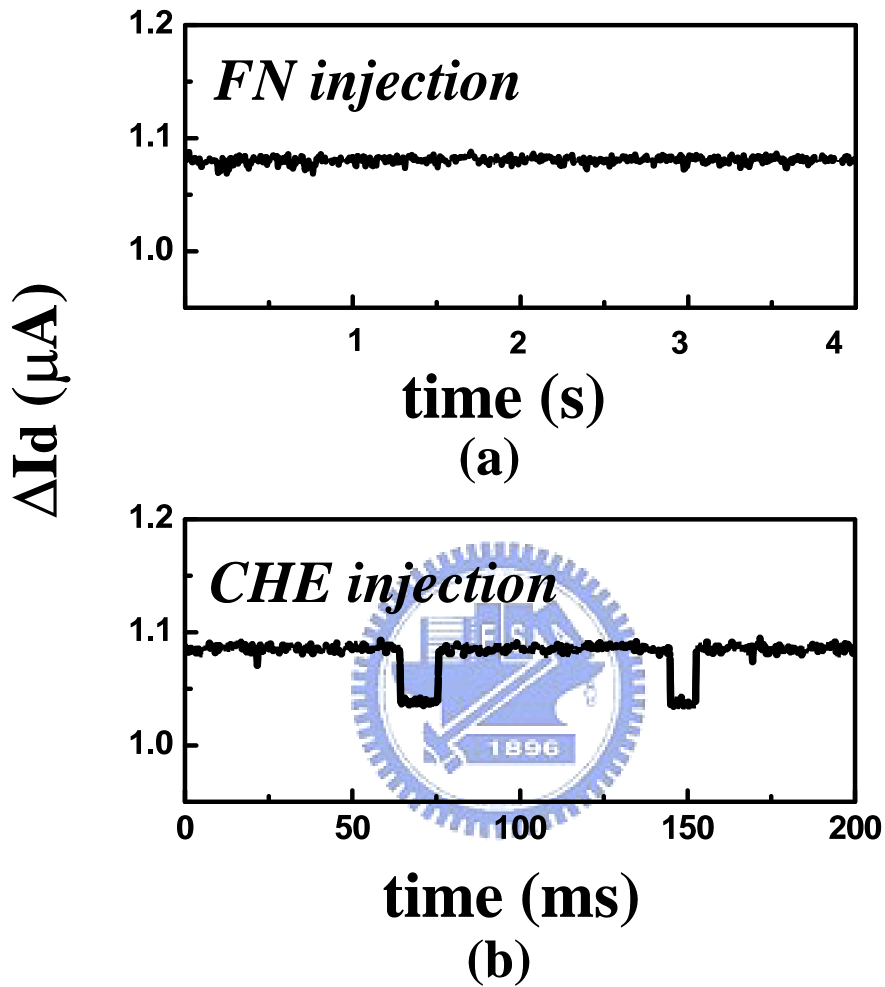


Fig. 4.6 Typical RTN traces for uniform FN injection (a) and channel hot electron injection (b). Both cells have the same P/E stress conditions.

CHE injection, respectively. The two cells experience the same cycling procedure but have different injection conditions in the last programming. In the uniform FN injection cell (Fig. 4.6(a)), RTN is very small or undetectable in a measurement span of 4 seconds. The simulated result in Fig 4.5 also shows that uniform injection yields smaller RTN. Our result here is consistent with earlier work in [42] that non-uniform channel Vt-distribution can increase 1/f noise. Fig 4.7 shows the maximum read current fluctuation and corresponding number of levels in read current in a 0.3μm cell. The read current is about 30μA. ***At 100k P/E cycles, 5-level transitions in read current is noticed and maximum ΔId is ~0.7μA in a sampling space of 10^5 reading.*** RTN with more levels and a large ΔId is still expected as more reading are taken [43].

4.5 Oxide Process Effect

To evaluate bottom oxide process effect on RTN, two different oxide process conditions with a 0.5μm gate length (device A and device B) are used. Device B is known to have better oxide endurance from a charge pumping measurement result (Fig. 4.8(a)) RTN traces in device A and B are shown in Fig. 4.8. Note that device B exhibits smaller amplitude in read current fluctuation. This is because device B has less oxide traps creation and thus the probability of multi-level RTN is much reduced.

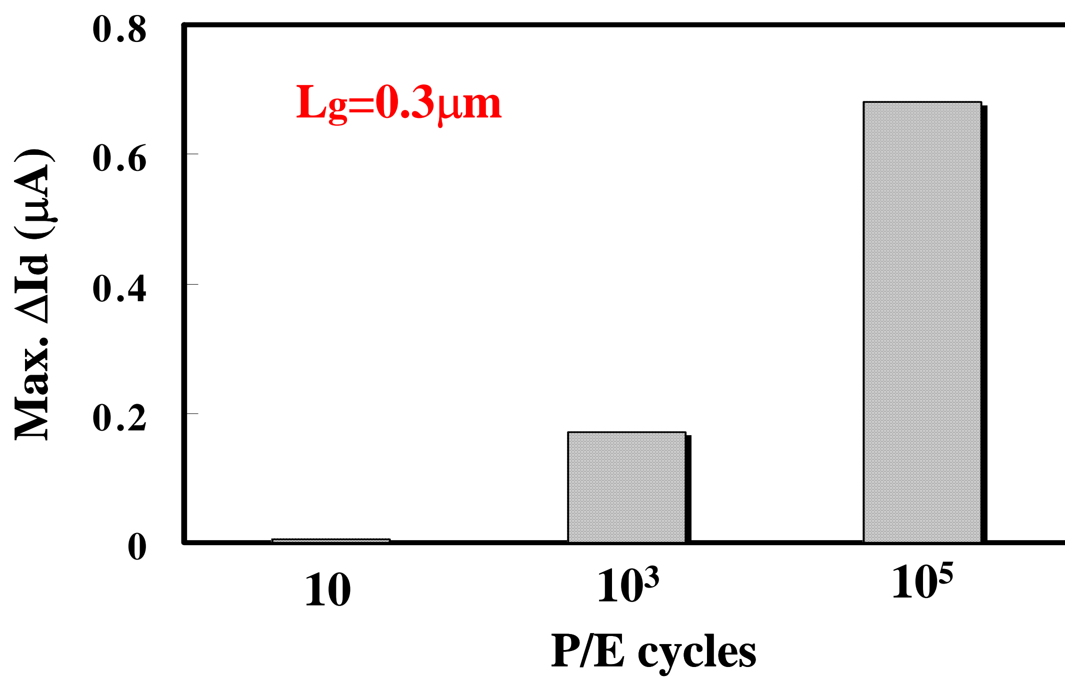


Fig. 4.7 Maximum ΔId observed at a read current of 30μA from multi-level RTN. The sampling size is 10^5 readings.

(a)

NROM	Process A	Process B
ΔIcp(10k)	70pA	40pA

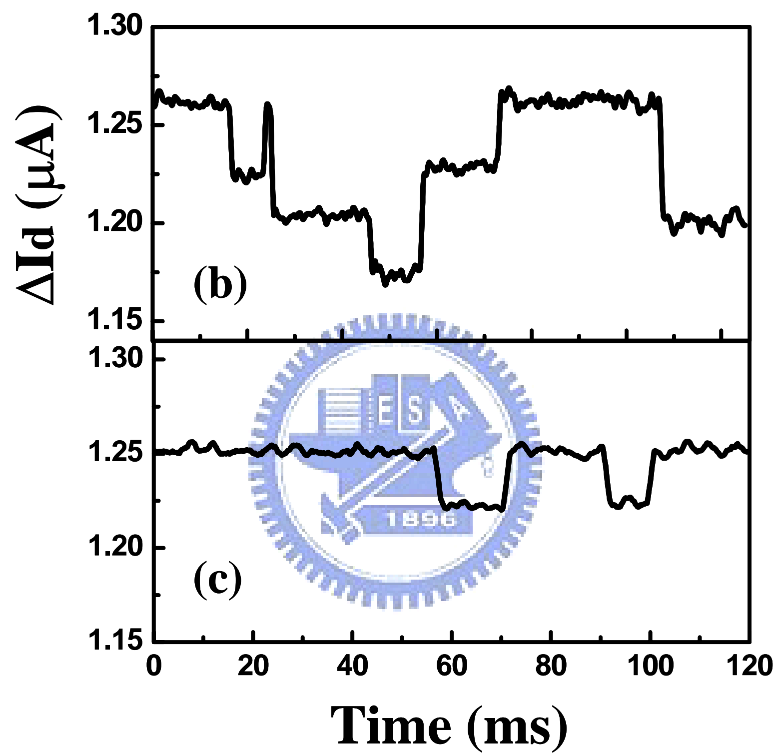


Fig. 4.8 (a) The increment of charge pumping current (I_{cp}) in device A and device B after 10k P/E cycles. (b) RTN traces in Device A after 10k P/E cycles (c) RTN traces in Device B after 10k P/E cycles.

Chapter 5
Conclusion

In low-V_t state, P/E stress created positive oxide charge plays a major role in various reliability issues. ONO process is critical to the improvement of the cell reliability. High-V_t state charge retention in the major nitride flash cells, NROM, is investigated. Our result shows that the electron injection method has large impact on nitride charge retention behavior.

Oxide charge trapping/detrapping induced read current fluctuation is discussed. Read current noise is increased in localized charge storage cells due to non-uniform Vt distribution. As the cycle number increases, the read current instability caused by RTN will become more severe. The improvement of bottom oxide reliability can significantly reduce this effect.

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