矽鍺製程之低漏電流二極體串聯電路
及其在靜電放電防護上之應用

Design on the Low-Leakage-Current Diode String for ESD Protection in SiGe BiCMOS Process

研究生　：吳偉琳　　Student: Woei-Lin Wu

指導教授：柯明道　教授　　Advisor: Prof. Ming-Dou Ker

國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

Submitted to Department of Electronics Engineering & Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao-Tung University
In Partial Fulfillment of the Requirements
for the Degree of
Master
in
Electronics Engineering
April 2005
Hsin-Chu, Taiwan, Republic of China

中華民國九十四年四月

矽鍺製程之低漏電流二極體串聯電路

及其在靜電放電防護上之應用

學生: 吳 偉 琳　　　　　　指導教授: 柯 明 道 教授

國立交通大學

電子工程學系　電子研究所碩士班

摘要

本篇論文主旨在設計適用於矽鍺製程之靜電放電防護電路。所提出的新型電路可以有效地降低二極體串產生的漏電流問題，且具有高的靜電放電防護能力。本篇論文分為三大部分，透過實驗的量測以及理論的推導來驗證所提出的新型設計。

第一部分是在 0.35 微米矽鍺製程中，藉由改變元件結構以及佈局參數來探討二極體與矽鍺異質接面雙極性電晶體之靜電放電防護能力，並利用傳輸線觸波產生器來量測這些元件在高能量電流脈衝注入下的電壓電流特性。此外，也探討在低壓，高壓及高速等不同應用之矽鍺異質接面雙極性電晶體，其靜電放電防護能力。

因為寄生元件的存在，傳統的二極體串將會產生嚴重的基極漏電流問題，尤其是在高溫的狀態下。本論文在第二部份是針對矽鍺製程中設計出新型的二極體，並使用新型的二極體組成低漏電流二極體串聯電路。本設計配合適當的電路技巧可有效地降低二極體串造成的漏電流問題。此外，本設計是利用二極體串在順偏導通狀態下導去靜電放電電流，因此在小的佈局面積下就具有高的靜電放電耐受度。

針對第二部份所提出的低漏電流二極體串聯電路作為靜電放電箝制電路，為了達到此電路具有最低漏電流的目的，第三部分藉由推導此電路寄生元件的特性

方程式以及模擬結果來達到電路設計參數的最佳化，再經由實驗的量測來驗證此結果。本論文更進一步提出第二種新型的二極體串，從理論推導及實驗結果證明其漏電流將更有效地被降低。此外，使用此新型二極體串作為矽鍺異質接面雙極性電晶體之觸發電路也在本論文中被提出與驗證。

在本論文中，已經針對於矽鍺製程中設計出低漏電且高靜電放電耐受度之二極體串聯電路，其適用於積體電路之靜電放電箝制電路。所設計的靜電放電防護電路均已在實際晶片上成功驗證，並有數篇會議論文發表。

Design on the Low-Leakage-Current Diode String for ESD Protection in SiGe BiCMOS Process

Student: Woei-Lin Wu Advisor: Prof. Ming-Dou Ker

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

ABSTRACT

The aim in this thesis is to design the ESD protection circuits in SiGe BiCMOS process. In this design, the leakage current of the diode string can be effectively reduced and a high ESD robustness can be achieved. There are three parts in this thesis.

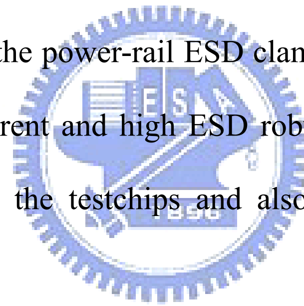
The first part investigates the ESD robustness of the diodes and heterojunction bipolar transistors (HBTs) by different device structures and layout parameters. The transmission line pulse generator (TLPG) is also used to investigate the characteristics of these devices under high-current stress. In addition, the ESD robustness of HBTs for low-voltage, high-voltage, and high-speed applications are also investigated.

For the traditional diode string, the parasitic p-n-p bipolar junction transistor (BJT) devices in the diode string will induce a large leakage current into the substrate, especially under high temperature condition. In the second part, a new diode structure in SiGe process is proposed and low-leakage-current diode string (LLCDS) is formed by this new diode structure. Furthermore, the leakage current of LLCDS can be

effectively reduced by extra circuit design. Because the diode string is designed to sustain the ESD stress under forward-biased condition, a high ESD robustness can be achieved in a small silicon layout area.

In the third part, the optimum design on the circuit to minimize the leakage current of LLCDS as the power-rail ESD clamp circuit is evaluated by calculating the physical formulas of the parasitic devices in the diode string and the simulation results. The experimental results are also performed to verify the simulation results. Furthermore, the second design on the diode string as the power-rail ESD clamp circuit is proposed to further reduce the leakage current. In addition, the power-rail ESD clamp circuit with new diode string as the trigger circuit of HBT is also proposed and verified.

In summary, LLCDS as the power-rail ESD clamp circuit are developed in SiGe process with low leakage current and high ESD robustness. Each of the design has been successfully verified in the testchips and also published in the international conference papers.



誌謝

首先我要感謝我的指導教授柯明道博士，這一年多以來給我的指導和鼓勵。當初剛從電子物理進到電子工程時，被教授要求做研究，常常搞不懂狀況，出錯的次數也比較多，被教授釘的滿頭包，那時候覺得真蠻辛苦的，但是那也是我成長最快的時候。現在回想起來，心中只有感激，而無一絲的埋怨。教授說過:「寧願讓我們在實驗室裡被罵的臭頭，也不要在外面被別人罵。」現在我真的能夠感同身受，體會教授的用心。

首先先感謝我的父母及兄長，有他們的栽培與鼓勵我才能站在這裡，再來感謝實驗室的同學陳穩義與其他學長姐們對我的指導和協助，尤其是張瑋仁學長，對剛進來的我有許多的指導與建議，讓我在實驗室能很快的適應；還有張智毅學長，他一步步的指導我，讓我很多東西從不會到會，在短時間內能盡速的進步達到要求，令我獲益良多。更要感謝工研院內的學長們，尤其是林昆賢學長，陳子平學長，莊哲豪學長與陳世宏學長，讓我在工研院工讀的時期學到許許多多的待人處世，做研究應有的態度與技巧，以及辦各種活動所需注意的事項，讓我在這二年內的工讀生生活過的十分充實，大家在研究與生活上都給了我許多的幫忙和建議，另外要感謝台灣積體電路公司提供取得不易的矽鍺製程，讓我能順利做研究，在此由衷致謝。

另外我還要感謝交大桌球隊的學長姐與學弟們，尤其是在研究所時期，陪我度過情感的低潮期，並且讓我在研究時能適當的紓解壓力，再度面對更多的挑戰，大家的友情真的讓我很感動。

其他要感謝的人還有很多，不可勝數，在此一併謝過。

吳偉琳

九十四年四月

CONTENTS

ABSTRACT (CHINESE) i

ABSTRACT (ENGLISH) iii

ACKNOWLEDGEMENT v

CONTENTS vii

TABLE CAPTIONS viii

FIGURE CAPTIONS ix

Chapter 1 Introduction 1

1.1 MOTIVATION 1
1.2 THESIS ORGANIZATION 2

Chapter 2 Characteristics of ESD Devices in 0.35-μm SiGe BiCMOS Process 4

2.1 INTRODUCTION 4
2.2 TEST STRUCTURE FOR DIODES AND HBTS 5
2.2.1 Diodes 5
2.2.2 HBTs 6
2.3 EXPERIMENTAL RESULTS AND DISCUSSION 7
2.3.1 Diodes 7
2.3.2 HBTs with Different Emitter Lengths 9
2.3.3 HBTs with Different Emitter Widths 10
2.3.4 HBTs with Different Base Resistances 11
2.3.5 HBTs with Different Layout Patterns 12
2.4 CONCLUSION 13

Chapter 3 Low-Leakage-Current Diode String in 0.18-μm SiGe BiCMOS Process and Its Application on

Power-Rail ESD Clamp Circuits 30

3.1 INTRODUCTION 30
3.2 REVIEW ON THE DIODE STRING 32
3.2.1 The Pure Diode String 32
3.2.2 The Modified Diode String to Reduce Leakage Current 32
3.3 LLCDS 33
3.4 MEASUREMENT RESULTS 34
3.5 CONCLUSION 36

Chapter 4 Minimization of Leakage Current in the Diode String in 0.18-μm SiGe BiCMOS Process 45

4.1 INTRODUCTION 45
4.2 DESIGN ON POWER-RAIL ESD CLAMP CIRCUIT 47
4.2.1 Low-Leakage-Current Diode Stinrg (LLCDS) 47
4.2.2 Low-Leakage-Current Diode String 2 (LLCDS2) 49
4.2.3 HBT Triggered by LLCDS 52
4.3 EXPERIMENTAL RESULTS 54
4.4 CONCLUSION 56

Chapter 5 Summary and Future Works 69

5.1 SUMMARY 69
5.2 FUTURE WORKS 70

REFERENCES 71

VITA 73

TABLE CAPTIONS

Table 2.1 ESD robustness of low-voltage SiGe HBT with different base nodes grounded. 29
Table 2.2 ESD robustness of low-voltage SiGe HBT with some emitter and base node grounded...29
Table 4.1 Parameters of devices used in the HSPICE simulation... 68
Table 4.2 Parameters of devices measured from the experimental results................68

FIGURE CAPTIONS

Fig. 2.1 (a) Top view and (b) cross-sectional view of P-well/N-well diode in a SiGe BiCMOS process. 14
Fig. 2.2 (a) Top view and (b) cross-sectional view of varactor (VR) diode in a SiGe BiCMOS process. 15
Fig. 2.3 (a) Top view and (b) cross-sectional view of vertical base-collector (VBC) diode in a SiGe BiCMOS process....................16
Fig. 2.4 The device cross-sectional view of low-voltage SiGe NPN HBT with local collector (LC) implantation....................17
Fig. 2.4 The DC characteristics of these different structure diodes....................17
Fig. 2.6 Breakdown voltage versus diode type when leakage current equals to 1 μA. 18
Fig. 2.7 Comparisons of second breakdown current among the P-well/N-well diode, the VR diode, and the VBC+LC diode with different widths under forward-biased condition. 18
Fig. 2.8 Comparisons of HBM ESD robustness among the P-well/N-well diode, the VR diode, and the VBC+LC diode with different widths under forward-biased condition. 19
Fig. 2.9 Comparison of second breakdown current among the P-well/N-well diode, VR diode, and VBC+LC diode with different widths under reverse-biased condition 19
Fig. 2.10 HBM ESD robustness versus diode length of the VBC diode with the diode width of 40 μm under forward-biased condition. 20
Fig. 2.11 Three types of ESD stress for the SiGe HBT device....................20
Fig. 2.12 The TLP I-V curve of the low-voltage SiGe HBT with different emitter lengths and a fixed emitter width of 0.45 μm under CE stress. 21
Fig. 2.13 HBM ESD robustness versus emitter length of the low-voltage SiGe HBT with emitter width of 0.45 μm. 21
Fig. 2.14 The TLP I-V curve of the high-voltage SiGe HBT with different emitter lengths and a fixed emitter width of 0.45 μm under CE stress. 22
Fig. 2.15 HBM ESD robustness versus emitter length of the high-voltage SiGe HBT with emitter width of 0.45 μm. 22
Fig. 2.16 The TLP I-V curve of the high-speed SiGe HBT with different emitter lengths and a fixed emitter width of 0.45 μm under CE stress. 23
Fig. 2.17 HBM ESD robustness versus emitter length of the high-speed SiGe HBT with emitter width of 0.45 μm. 23
Fig. 2.18 The TLP I-V curve of the low-voltage SiGe HBT with different emitter widths and a fixed emitter length of 30 μm under CE stress. 24
Fig. 2.19 HBM ESD robustness versus emitter width of the low-voltage SiGe HBT with emitter length of 20.3 μm. 24
Fig. 2.20 The TLP I-V curve of the high-voltage SiGe HBT with different emitter widths and a fixed emitter length of 30 μm under CE stress. 25
Fig. 2.21 HBM ESD robustness versus emitter width of the high-voltage SiGe HBT with emitter length of 20.3 μm. 25
Fig. 2.22 The TLP I-V curve of the high-speed SiGe HBT with different emitter widths and a fixed emitter length of 30 μm under CE stress. 26
Fig. 2.23 HBM ESD robustness versus emitter width of the high-speed SiGe HBT

with emitter length of 20.3 μm. 26
Fig. 2.24 The SiGe HBT with multi-finger device structure. Base resistance will increase if the base terminal is not all connected together through the contact on its top...27
Fig. 2.25 The designed high-speed implantation patterns for HBT device. K1 is the standard layout with uni-square shape. K2, K3, K4, and K5 are designed to different shapes for investigation..27
Fig. 2.26 HBM ESD robustness versus high-speed SiGe HBT with different high-speed implantation patterns. 28
Fig. 3.1 The whole-chip ESD protection design with the diode string applied in the power-rail ESD clamp circuit. 38
Fig. 3.2 The cross-sectional view of the pure diode string.......................................38
Fig. 3.3 The cross-sectional view of the n-stage triple-well diode string and its parasitic base-emitter tied p-n-p bipolar transistors......................................39
Fig. 3.4 The top view of triple-well diode structure in 0.18-μm BiCMOS SiGe process. 39
Fig. 3.5 The cross-sectional view of triple-well diode structure in 0.18-μm BiCMOS SiGe process..40
Fig. 3.6 The new proposed diode string with extra bias to the deep N-well to reduce the substrate leakage current...40
Fig. 3.7 The measured I-V curves along the diode string with three diodes in series (N=3) under the bias conditions (Vbias) of deep N-well floating, or biased at 1.8V. 41
Fig. 3.8 The measured I-V curves of the different diode number of the diode string under the bias conditions (Vbias) of deep N-well floating, or biased at 1.8V, at the temperature of 25°C. 41
Fig. 3.9 The relation between the total blocking voltage and the diode number (N) of the diode string under Vbias=1.8V at the different temperatures. 42
Fig. 3.10 The relation between the total blocking voltage and the diode number (N) of the diode string under Vbias floating at the different temperatures. 42
Fig. 3.11 The relation between bias resistance and total leakage current (I_A + Ib) of the diode string with diode number of N=4 and bias condition of Vp=Vb=1.8V, measured at the temperatures of 25°C, 75°C, and 125°C, respectively.....43
Fig. 3.12 The TLP-measured I-V curves of the diode strings with different diode numbers under the bias resistance of 10 kohm.. 43
Fig. 3.13 The dependence of secondary breakdown current (It2) of diode string on the diode number (N) in series..44
Fig. 4.1 The whole-chip ESD protection design with the diode string applied in the power-rail ESD clamp circuit. 58
Fig. 4.2 The cross-sectional view of the conventional diode string. 58
Fig. 4.3 The cross-sectional view of LLCDS in 0.18-μm BiCMOS SiGe. 59
Fig. 4.4 The equivalent circuit of LLCDS in 0.18-μm BiCMOS SiGe. 59
Fig. 4.5 The equivalent circuit of LLCDS2 in 0.18-μm BiCMOS SiGe. 60
Fig. 4.6 The circuit design on HBT triggered by diode for low-voltage power supply. 60
Fig. 4.7 The equivalent circuit of LLCDS applied in another power-rail ESD clamp circuit. 61
Fig. 4.8 The DC characteristics of the conventional diode string at 25°C. 61
Fig. 4.9 The DC characteristics of LLCDS at 25°C. 62
Fig. 4.10 The DC characteristics of LLCDS2 at 25°C. 62

Fig. 4.11 The simulation result of the relationship between bias resistance (R) and total leakage current of LLCDS with diode number of N=4 and bias condition of VDD=1.8V, at the temperatures of 125°C. 63
Fig. 4.12 The relationship between bias resistance (R) and total leakage current of LLCDS with diode number of N=4 and bias condition of VDD=1.8V, measured at the temperatures of 25°C, 75°C, and 125°C, respectively.....63
Fig. 4.13 The simulation result of the relationship between bias resistance (R) and total leakage current of LLCDS2 with diode number of N=4 and bias condition of VDD=1.8V, at the temperatures of 125°C. 64
Fig. 4.14 The relationship between bias resistance (R) and total leakage current of LLCDS2 with diode number of N=4 and bias condition of VDD=1.8V, measured at the temperatures of 25°C, 75°C, and 125°C, respectively.....64
Fig. 4.15 The total leakage current of the conventional diode string, LLCDS and LLCDS2 under 125°C for N=4 and R=10 kohm. 65
Fig. 4.16 The dependence of secondary breakdown current (It2) of the conventional diode string, LLCDS and LLCDS2 on the diode number (N) in series.....65
Fig. 4.17 The relationship between Ro and total leakage current of the HBT triggered by conventional diode string , HBT triggered by LLCDS and HBT triggered by LLCDS2 at bias resistance (R) = 10 kohm under diode number of N=4 and bias condition of VDD=1.8V, measured at the temperatures of 125°C. 66
Fig. 4.18 The TLP I-V curve of the HBT triggered by conventional diode string for N=4, VDD=1.8V, and R=Ro=10 kohm. 66
Fig. 4.19 The TLP I-V curve of the HBT triggered by LLCDS for N=4, VDD=1.8V, and R=Ro=10 kohm...67
Fig. 4.20 The TLP I-V curve of the HBT triggered by LLCDS2 for N=4, VDD=1.8V, and R=Ro=10 kohm...67

Chapter 1
Introduction

1.1 MOTIVATION

In the 1990s a further revolution in bipolar transistor design occurred with the emergence of Silicon-germanium (SiGe) Heterojunction Bipolar Transistors (HBTs). Previously HBTs had only been available in compound semiconductor technologies, such as AlGaAs/GaAs. However, material research showed that a good heterojunction could be obtained if the SiGe layer was thin and the Ge content relatively low. Recently, SiGe HBT has become a key technology for RF applications in giga-bit communication systems. ESD protection in SiGe technology plays an important role in telecommunication system reliability [1]-[5].

In a SiGe BiCMOS process, with the consideration of Giga-Hz input signals, the SiGe HBT can be also used as the on-chip ESD protection device. Therefore, the relation between ESD robustness and layout parameters of SiGe HBT and diodes with different junctions should be characterized to achieve a good enough ESD protection design in such high-speed communication integrated circuits.

For ESD protection design in SiGe BiCMOS process, diode string is a good candidate as the power-rail ESD clamp circuit, because the diode string under forward-biased condition can sustain a very high ESD stress within a smaller chip area. The diode string has been widely used in integrated circuits for ESD protection [1]-[4]. However, a parasitic vertical p-n-p bipolar transistor exists in the conventional P+/N-well diode with the common P-type substrate. This parasitic vertical p-n-p bipolar transistor may cause high leakage current in the diode string [1]-[4], especially

in the high-temperature condition. To overcome the leakage problem, an extra bias to the deep N-well of the diode string with triple-well structure was proposed in this thesis. Although the additional extra bias may cause leakage current into the diode string, the overall leakage current of the diode string can be minimized by a bias resistance. Optimization design on the bias resistance was calculated and derived from the formula. The results of this design are also verified by HSPICE simulation and measured data.

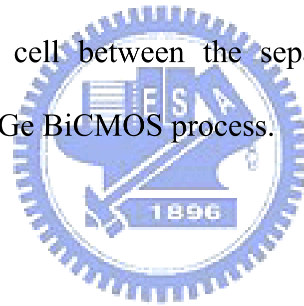
1.2 THESIS ORGANIZATION

The chapter 2 in the thesis discusses the structure and the device characteristics of SiGe HBTs and diodes. Five kinds of diodes including P-well/N-well diode, varactor (for voltage controlled capacitor) diode, and vertical base-collector (VBC) diode with different implantation types such as local-collector, high-speed, or without implantation are investigated. Three kinds of SiGe HBT devices are studied in this thesis, which are the low-voltage (LV) SiGe NPN HBT (BVceo = 3.8V, ft = 47GHz at Vbc = 1V), the high-voltage (HV) SiGe NPN HBT (BVceo = 6V, ft = 30GHz at Vbc = 1V), and the high-speed (HS) SiGe NPN HBT (BVceo = 2.5V, ft = 70GHz at Vbc = 1V).

In chapter 3, a new design to minimize the leakage current of the diode string is proposed. Compared with the traditional P+/N-well diode string, this structure has a deep N-well to isolate P-well and the common P-substrate. An extra bias is applied to the deep N-well to minimize the substrate leakage current. The connection of deep N-well to the extra bias makes the parasitic n-p-n of the triple-well diode being slightly turned on. This current will flow into the next diode of the diode string, but not to the common P-substrate. So, the substrate leakage current can be effectively

decreased. A resistance is further connected between the bias voltage and the deep N-well to control the leakage current level through the diode string. As the substrate leakage current could be reduced, another leakage current path appears. Because of the parasitic n-p-n bipolar transistors of the triple well diode, the leakage current will be a mount of current flow through the junction between P-well and N+ under the high-temperature condition.

In chapter 4, the leakage current and ESD robustness of Low-Leakage-Current Diode String (LLCDS) as the power clamp circuit in SiGe BiCMOS process have been investigated. By calculating the relation between bias resistance and the leakage current of LLCDS, the leakage current of LLCDS can be minimized with specified value of bias resistance. Such LLCDS can be used as the power-rail ESD clamp circuit and ESD connection cell between the separated power rails, to provide effective ESD protection in SiGe BiCMOS process.



CHAPTER 2

Characteristics of ESD Devices in 0.35-μm SiGe BiCMOS Process

2.1 INTRODUCTION

SiGe HBT has become a key technology for RF applications in giga-bit communication systems. ESD protection in SiGe technology plays an important role in telecommunication system reliability [1]-[5]. In a SiGe BiCMOS process, with the consideration of Giga-HZ input signals, the SiGe HBT is also used as the on-chip ESD protection device to protect itself.

In the 1990s a further revolution in bipolar transistor design occurred with the emergence of SiGe HBTs. Previously heterojunction bipolar transistors had only been available in compound semiconductor technologies, such as AlGaAs/GaAs. However, material research showed that a good heterojunction could be obtained if the SiGe layer was thin and the Ge content relatively low.

As the results, the relation between ESD robustness and layout parameters of SiGe HBT should be characterized to achieve a good enough ESD protection design in such high-speed communication integrated circuits. Another successful ESD protection design for RF IC applications had been reported by using the double diodes with the turn-on-efficient power-rail ESD clamp circuit [6], [7].

The relation between ESD robustness and layout parameters of diodes with different junctions in SiGe BiCMOS process should be characterized for ESD protection design. With the detailed experimental results, the on-chip ESD protection

design for Giga-Hz RF circuits can be optimized with both considerations on RF performance and ESD robustness.

In this chapter, the test structures of SiGe HBT devices and diodes with different junctions or layout parameters have been fabricated in a 0.35-µm SiGe BiCMOS process to investigate their ESD robustness.

2.2 TEST STRUCTURE FOR DIODES AND HBTS

2.2.1 Diodes

Five kinds of diodes including P-well/N-well diode, varactor (for voltage controlled capacitor) diode, and vertical base-collector (VBC) diode with different implantation types such as local-collector, high-speed, or without implantation are investigated. Fig. 2.1 shows the top view and cross-sectional view of the P-well/N-well diode, which is used as a reference for comparing with the other diodes of different structures.

Varactor means voltage controlled capacitor; is used as a diode in this research because of the junction between P+ and N-(NEPI). Fig. 2.2 shows the top view and cross-sectional view of varactor (VR) diode, where the attention will focus to the junction between P+ and N- (NEPI).

Fig. 2.3 shows the top view and cross-sectional view of VBC diode with local collector (LC) implantation. The diode junction is formed between base poly (BP) and local collector region with NEPI. In this work, next kind of diode is formed by the part of HBT for SiGe process. The emitter poly is removed and put the contact right on the base poly. As the result, the current flow through the base and collector will be

vertical. The local collector (LC) implantation under the base poly region is further changed as high-speed implantation, or even no implantation in the diode structures to compare their ESD robustness.

In the test structures for investigation, the width (W) of diode junction is drawn in the range from 3 to 12 μm, and the length (L) of diode junction is drawn from 20 to 80 μm in this work.

2.2.2 HBT Devices

The structure of the SiGe HBT device is different from the CMOS bipolar transistor. The SiGe HBT is formed by emitter poly, base poly, and N+ buried layer. Emitter poly is right on the base poly, and the base poly is right on the local collector region. The local collector region is connected with N+ buried layer and through N+ sinker to contact.

Three kinds of SiGe HBT devices are studied in this work, which are the low-voltage (LV) SiGe NPN HBT (BVceo = 3.8V, ft = 47GHz at Vbc = 1V), the high-voltage (HV) SiGe NPN HBT (BVceo = 6V, ft = 30GHz at Vbc = 1V), and the high-speed (HS) SiGe NPN HBT (BVceo = 2.5V, ft = 70GHz at Vbc = 1V). To investigate the ESD robustness of SiGe HBTs, the experimental chips had been fabricated in a 0.35-μm 3.3V/5V RF BiCMOS process.

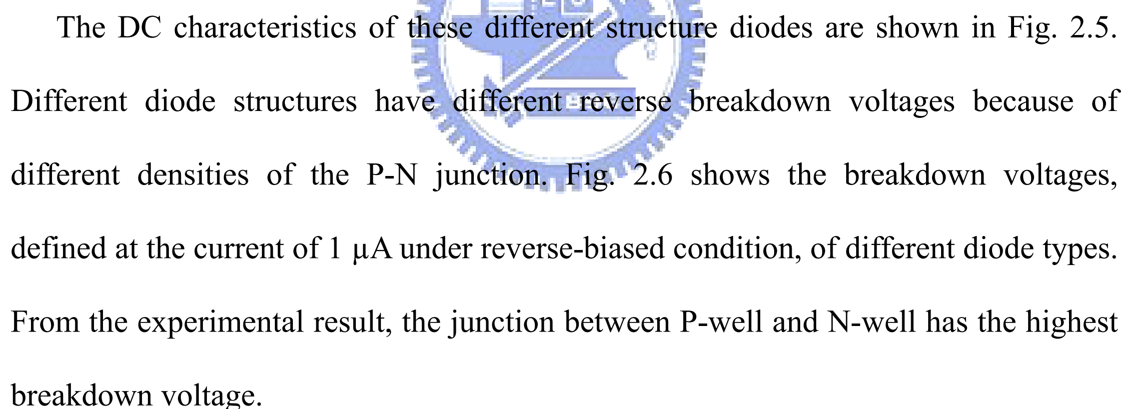
The dependences of emitter length, emitter width, and base resistance on the ESD robustness are investigated for all LV, HV, and HS SiGe HBTs. Moreover, the pattern of high-speed implantation is also drawn with different style to investigate its impact on ESD robustness.

Fig. 2.4 shows the cross-sectional view of a low-voltage SiGe NPN HBT. An

N-type local collector (LC) implantation region is formed under the emitter poly and connecting to the N-type sinker through the bottom N+ buried layer. The N-type sinker is formed as the collector terminal. In the high-voltage SiGe NPN HBT for 5-V operating voltage, the LC implantation is not performed for increasing the breakdown voltage of base/collector junction. On the other hand, the LC implantation is replaced by a high-speed (HS) implantation with high concentration collector region to speed up the operating speed of the HBT device.

2.3 EXPERIMENTAL RESULTS

2.3.1 Diodes



The DC characteristics of these different structure diodes are shown in Fig. 2.5. Different diode structures have different reverse breakdown voltages because of different densities of the P-N junction. Fig. 2.6 shows the breakdown voltages, defined at the current of 1 μA under reverse-biased condition, of different diode types. From the experimental result, the junction between P-well and N-well has the highest breakdown voltage.

In the varactor (VR) diode with a junction between P+ and NEPI (Ñ), this VR diode can work with good characteristics under forward and reverse biased conditions. In the VBC diode with a junction between base poly and the local collector, it also has good characteristics under forward and reverse biased conditions. All of diodes whose leakage is less than 1nA under the normal power bias (Vdd = 3.3 V).

To observe the high current characteristics of ESD devices in SiGe BiCMOS process, transmission line pulsing (TLP) system with a pulse width of 100 ns is used

to measure the second breakdown current, It2 [8], [9]. Three diodes, the P-well/N-well diode, VR diode, and VBC+LC diode, are zapped by the TLP to find their It2. Besides TLP test, the ESD simulator is also used to measure the ESD level of devices. The ESD stress is performed with a commercial KeyTek ZapMaster ESD simulator. The start voltage of human-body-model (HBM) ESD stress is 50 V, and the step voltage is 500 V. Each measurement is performed on 2 samples, at least. Using this method, the ESD robustness of these devices can be investigated and discussed in this work.

The second breakdown current (It2) and HBM ESD robustness of the P-well/N-well diode, VR diode, and VBC+LC diode with different widths under forward-biased condition are shown in Fig. 2.7 and 2.8, respectively. The It2 and ESD robustness on the diode is increased when the diode width is increased, but that of the VBC+LC diode is not significantly improved when the diode width is further increased. Under forward-biased condition, P-well/N-well diode has the highest It2 and ESD level, which is a reference during designing the ESD protection circuit. So the P-well/N-well diode is suitable to be the ESD protection device under forward-biased condition.

Fig. 2.9 shows the second breakdown current (It2) of the P-well/N-well diode, VR diode, and VBC+LC diode with different widths under reverse-biased condition. In Fig. 2.9, the P-well/N-well diode, with a fixed length of 6 μm but different widths, has a very low second breakdown current. Although it has good ESD characteristics under forward-biased condition, it should be avoided in ESD protection design to use the P-well/N-well diode to discharge ESD current in the reverse-biased condition. For the VR diode and VBC+LC diode with a fixed length of 6 μm but different widths, their second breakdown currents are almost proportion to their widths.

Fig. 2.10 shows the dependence of HBM ESD robustness on the diode length of the VBC diode with a fixed width of 40 μm under the forward-biased condition. In Fig. 2.10, the ESD robustness of the VBC diode is independent to the diode length. So, the VBC diode can be drawn with the minimum length for saving layout area to get the same ESD level.

2.3.2 HBT with Different Emitter Lengths

Fig. 2.11 shows three types of ESD stress for the SiGe HBT device. There are BC ESD stress, BE ESD stress and CE ESD stress. BC ESD stress is stress the base node of the SiGe HBT; collector node is grounded and emitter node is floating. BE ESD stress is stress the base node of the SiGe HBT; emitter node is grounded and collector node is floating. CE ESD stress is stress the collector node of the SiGe HBT; emitter node is grounded and base node is floating. In order to study the ESD robustness of these SiGe HBT devices completely, every kind of the junction should be tested by ESD stress.

Fig. 2.12 shows the TLP I-V curve of the low-voltage SiGe HBT with different emitter lengths and a fixed emitter width of 0.45 μm under CE stress. Fig. 2.13 shows ESD robustness of the low-voltage SiGe HBTs with a fixed emitter width of 0.45 μm but different emitter lengths. All the low-voltage SiGe HBT devices only pass 50-V HBM ESD stress when emitter width equals to 0.45 μm. Because the HBM ESD level of the CE ESD stress is too small to see the difference under different emitter lengths, the TLP I-V curve can show the more clear value.

The similar results are also seen in the high-voltage SiGe HBTs with different emitter lengths, as that shown in Fig. 2.14 and Fig. 2.15. This may result from the too

small emitter width and higher junction breakdown voltage. Because the junction between base poly and local collector region has the largest area to deliver the heat under ESD stress, the HBM ESD level is highest in all ESD stress type.

Fig. 2.16 shows the TLP I-V curve of the high-speed SiGe HBT with different emitter lengths and a fixed emitter width of 0.45 μm under CE stress. The high-speed SiGe HBTs with the lowest junction breakdown voltage have an increasing ESD robustness with the increase of emitter length, as that shown in Fig. 2.17, where the emitter width also equals to 0.45 μm.

2.3.3 HBT with Different Emitter Widths

Fig. 2.18 shows the TLP I-V curve of the low-voltage SiGe HBT with different emitter width and a fixed emitter length of 30 μm under CE stress. Fig. 2.19 shows the ESD result versus the emitter width for the low-voltage SiGe HBTs under a fixed emitter length. In Fig. 2.19, the low-voltage SiGe HBT sustains higher ESD level when its emitter width is drawn larger than 0.45 μm, and achieves 800-V ESD robustness when its emitter width equals to 1.5 μm with emitter length of 20.3 μm. This equals about 20 V/μm, which is double of the ESD level of the gate-grounded NMOS in the same BiCMOS process.

Fig. 2.20 shows the TLP I-V curve of the high-voltage SiGe HBT with different emitter width and a fixed emitter length of 30 μm under CE stress. Fig. 2.21 shows the ESD result versus the emitter width for the high-voltage SiGe HBTs under a fixed emitter length. In Fig. 2.21, the high-voltage SiGe HBT shows a relatively low ESD level. Only 200-V ESD level can be sustained, when its emitter width equals to 1.5 μm with emitter length of 20.3 μm.

Fig. 2.22 shows the TLP I-V curve of the high-speed SiGe HBT with different emitter width and a fixed emitter length of 30 μm under CE stress. Fig. 2.23 shows the ESD result versus the emitter width for the high-voltage SiGe HBTs under a fixed emitter length. Similarly, the ESD level increases, when the emitter width of high-speed SiGe HBT increases, as shown in Fig. 2.23. If the emitter width of SiGe HBT is fixed at 0.45 μm, the order of ESD robustness is: LV SiGe HBT = HV SiGe HBT < HS SiGe HBT.

However, when the emitter width of SiGe HBT is fixed at 1.5 μm, the order of ESD robustness is: LV SiGe HBT > HS SiGe HBT > HV SiGe HBT. This is a very interesting phenomenon, and more analysis and experimental measurement will be performed in our following future work to get a clear insight.

2.3.4 HBT with Different Base Resistances

Fig. 2.24 shows the cross-sectional view of a multi-finger SiGe HBT with 4 emitter fingers. The emitter window is 20.3 μm × 0.9 μm. The base resistance can be the minimum value, when all base terminals (B1, B2, B3, B4, and B5) are connected together through the contact layer on its top.

Table I shows the ESD robustness of the low-voltage SiGe HBT when all emitter nodes are grounded, where the ESD zapping are applied to the collector node with some base nodes are grounded, such as only node1 grounded, others floating, or node 1, 3 and 5 grounded, others floating. When all base terminals are connected together to ground, only 100-V HBM ESD stress is passed. The same result also appears when the base terminals B1, B3, B5 are connected to ground.

However, when only B1 and B3 are connected to ground, the ESD robustness will

increase to 1800 V. The floating on the base finger B5 significantly increases the ESD robustness of SiGe HBT. Table II shows the case of only one emitter and one base terminals connecting to ground. SiGe HBT with B1E2 grounded can sustain 700-V ESD stress. But, only 100-V ESD stress can be passed when B1E3 grounded. The above measured results show an interesting phenomenon, and more analysis and experimental measurement will be performed in our following work to get a clear explanation.

2.3.5 HBT with Different Layout Patterns

Fig. 2.25 shows the designed patterns in the high-speed SiGe HBT devices with different high-speed implantation regions. K1 is the standard layout of the high-speed SiGe HBT with unit-square shape. K2, K3, K4, and K5 are designed in different shapes for investigation. Because the SiGe HBT device is a vertical bipolar structure, the current flow may be affected by the different layout patterns of the N+ buried layer. The current flow is vertical from emitter to base, but is horizontal from N+ buried layer to N+ sinker. If the layout pattern of the N+ buried layer is discontinuously, the collector current will be harder flowing to the N+ sinker and the current distribution will not be uniform. As a result, the effect of delivering heat may be worse than other layout pattern.

Because the K4 pattern is parallel to the collector current, the current distributes uniformly, and the heat delivering may be better. As a result, The BC HBM ESD level of K4 layout pattern is the best. As for BE and CE HBM ESD level have less effect by changing N+ buried layer. The emitter window equals to 20.3 μm × 1.5 μm. The ESD robustness degrades with the designed patterns, as shown in Fig. 2.26. The standard

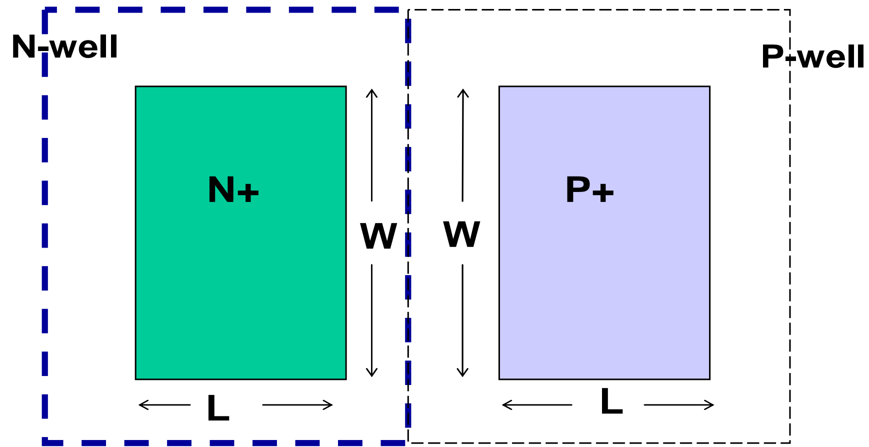
layout has ESD robustness about 22 V/µm, but the other patterns (K2, K3, K4, and K5) degrade to about only 50%.

2.4 CONCLUSION

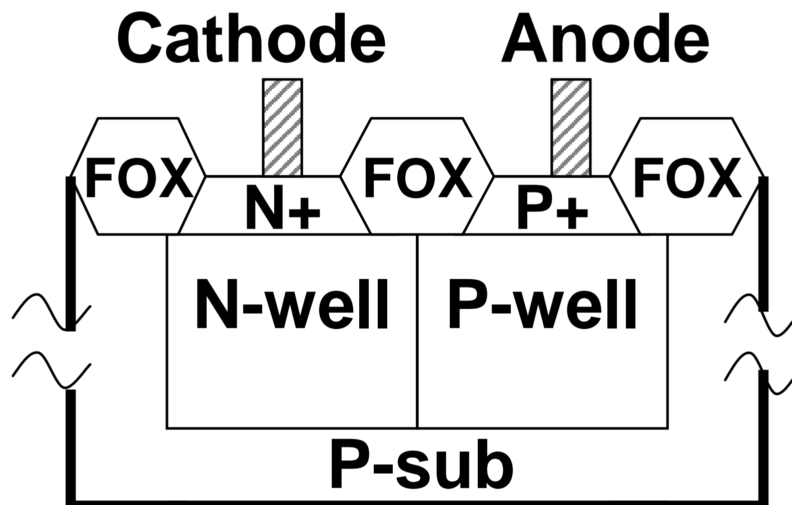
Different electrostatic discharge (ESD) devices in a 0.35-µm Silicon germanium (SiGe) RF BiCMOS process are characterized in high current regime by transmission line pulse (TLP) generator and ESD simulator for on-chip ESD protection design. The test structures of diodes with different p-n junctions and the silicon-germanium heterojunction bipolar transistors (HBTs) with different layout parameters have been drawn for investigating their ESD robustness. The human-body-model (HBM) ESD robustness of SiGe HBTs with low-voltage (LV), high-voltage (HV), and high-speed (HS) implantations has been measured and compared in details.

The characteristics of diodes with different structures in the SiGe BiCMOS process have been investigated for using in ESD protection design. The diodes can work with good ESD robustness under forward-biased condition. The ESD robustness of SiGe hetrojunction bipolar transistor in the SiGe BiCMOS process has been also characterized.

If the emitter width of SiGe HBT is fixed at 0.45 µm, the order of ESD robustness is: LV SiGe HBT = HV SiGe HBT < HS SiGe HBT. However, when the emitter width of SiGe HBT is fixed at 1.5 µm, the order of ESD robustness is: LV SiGe HBT > HS SiGe HBT > HV SiGe HBT. With the proper layout parameters, SiGe HBT can perform double ESD robustness than that of NMOS device in the SiGe BiCMOS process.

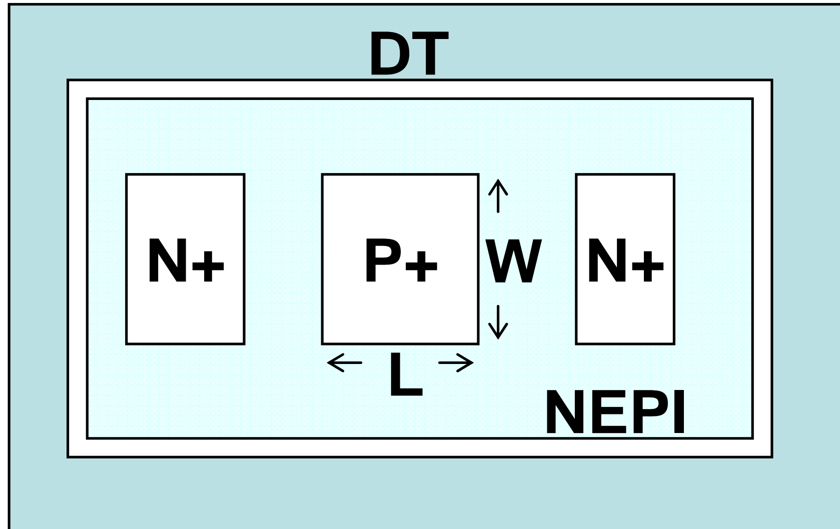


(a)

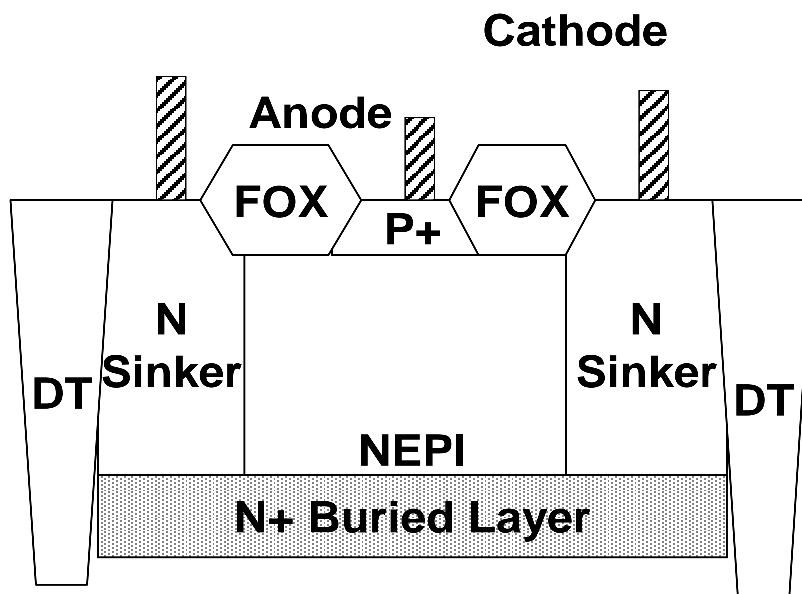


(b)

Fig. 2.1 (a) Top view and (b) cross-sectional view of P-well/N-well diode in a SiGe BiCMOS process.

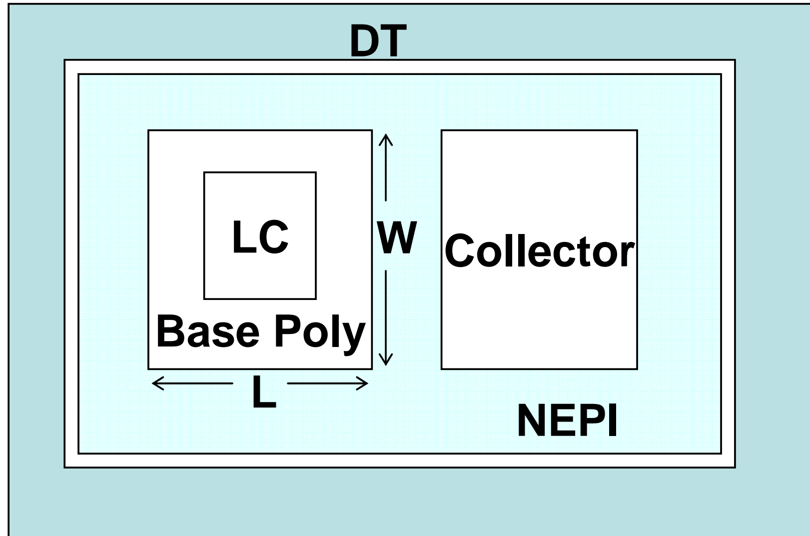


(a)

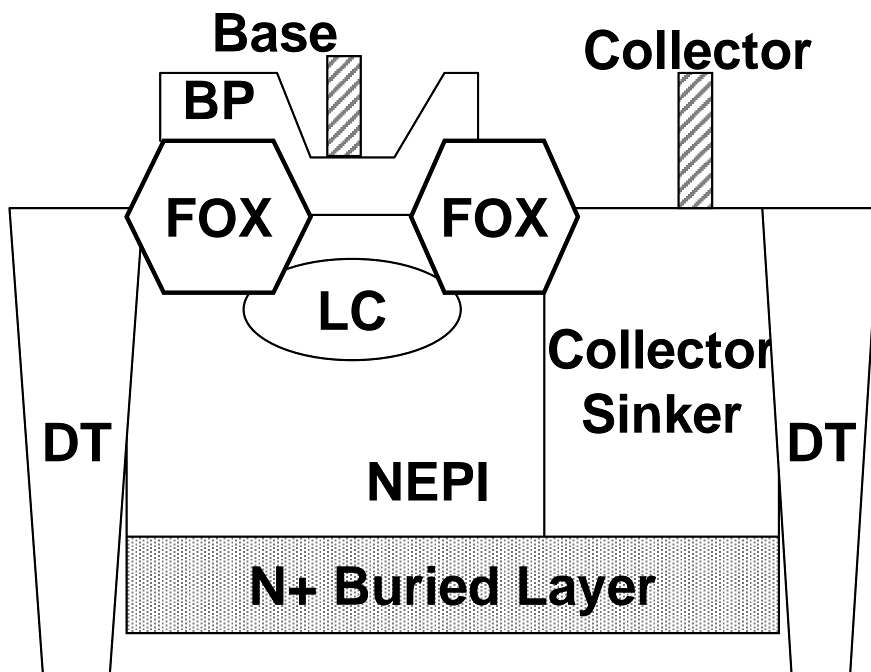


(b)

Fig. 2.2 (a) Top view and (b) cross-sectional view of varactor (VR) diode in a SiGe BiCMOS process.



(a)



(b)

Fig. 2.3 (a) Top view and (b) cross-sectional view of vertical base-collector (VBC) diode in a SiGe BiCMOS process.

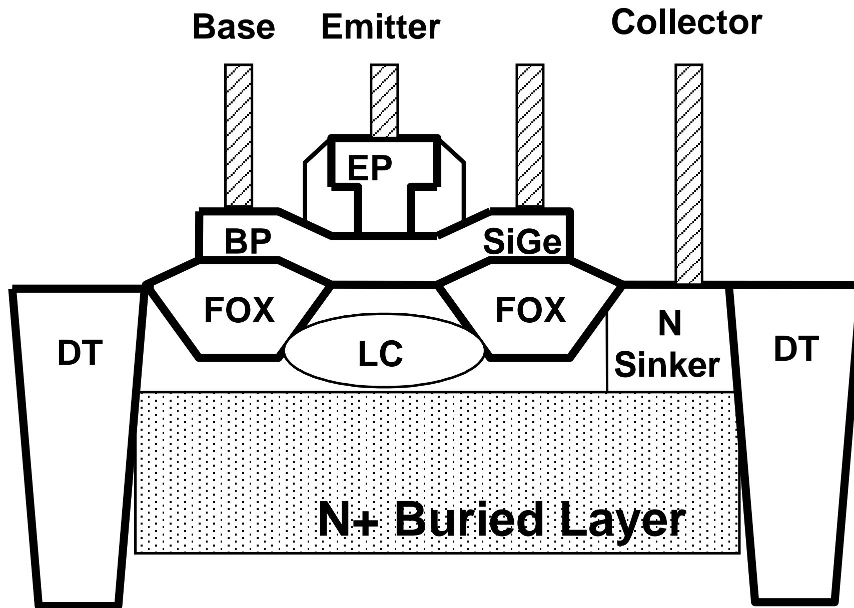


Fig. 2.4 The device cross-sectional view of low-voltage SiGe NPN HBT with local collector (LC) implantation.

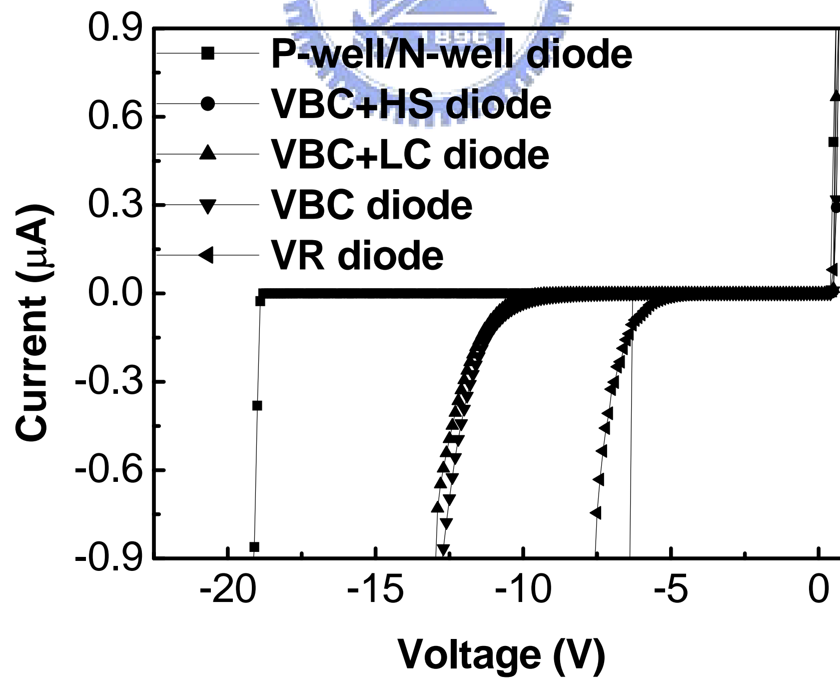


Fig. 2.5 The DC characteristics of these different structure diodes.

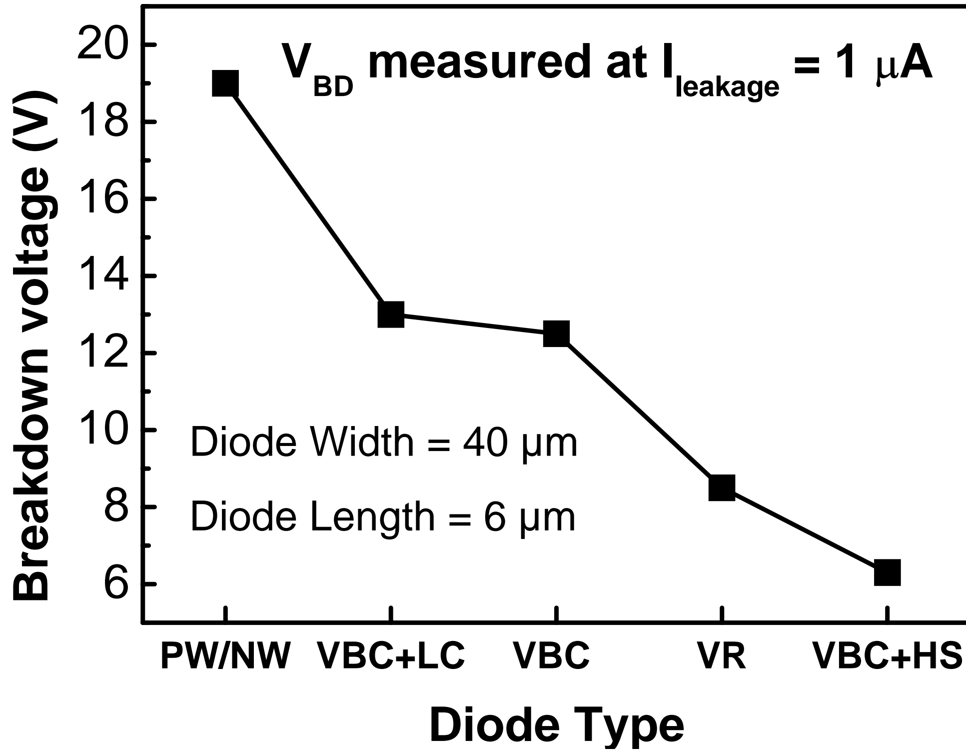


Fig. 2.6 Breakdown voltage versus diode type when leakage current equals to 1 μA.

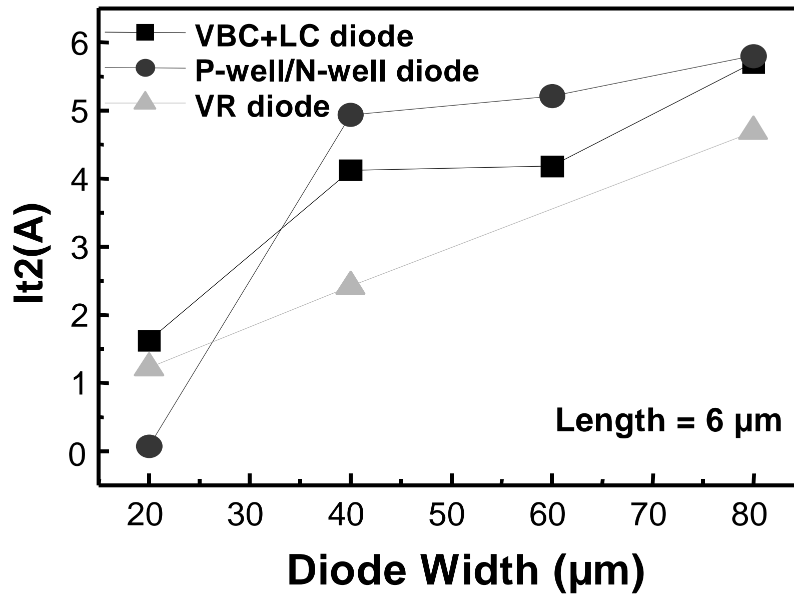


Fig. 2.7 Comparisons of second breakdown current among the P-well/N-well diode, the VR diode, and the VBC+LC diode with different widths under forward-biased condition.

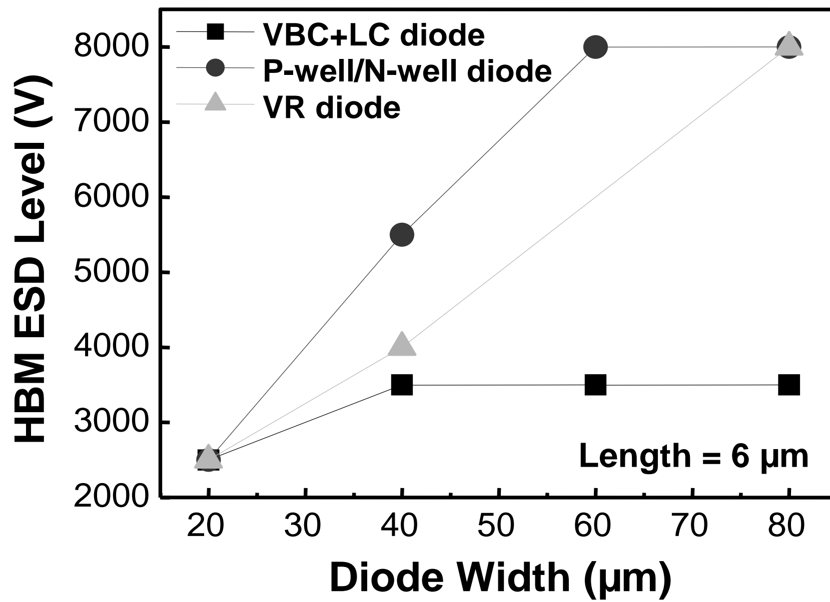


Fig. 2.8 Comparisons of HBM ESD robustness among the P-well/N-well diode, the VR diode, and the VBC+LC diode with different widths under forward-biased condition.

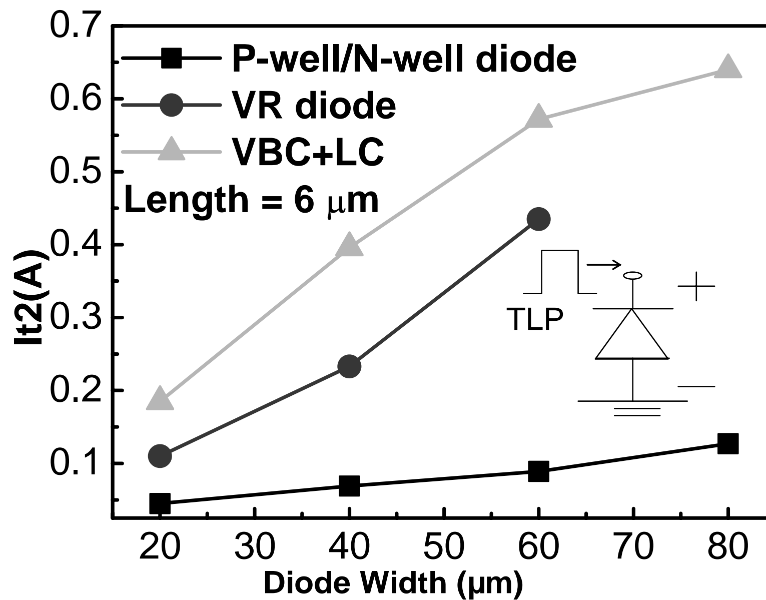


Fig. 2.9 Comparison of second breakdown current among the P-well/N-well diode, VR diode, and VBC+LC diode with different widths under reverse-biased condition.

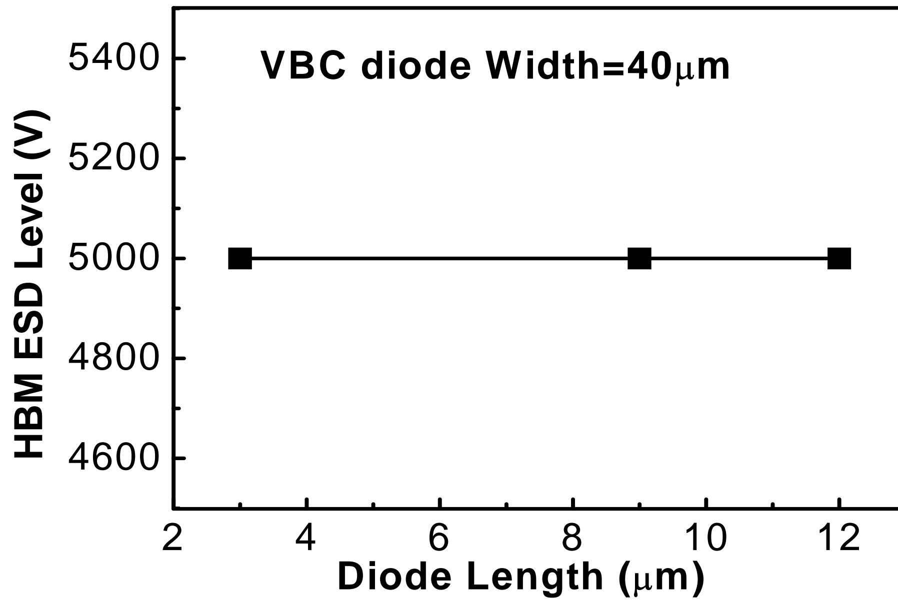


Fig. 2.10 HBM ESD robustness versus diode length of the VBC diode with the diode width of 40 μm under forward-biased condition.

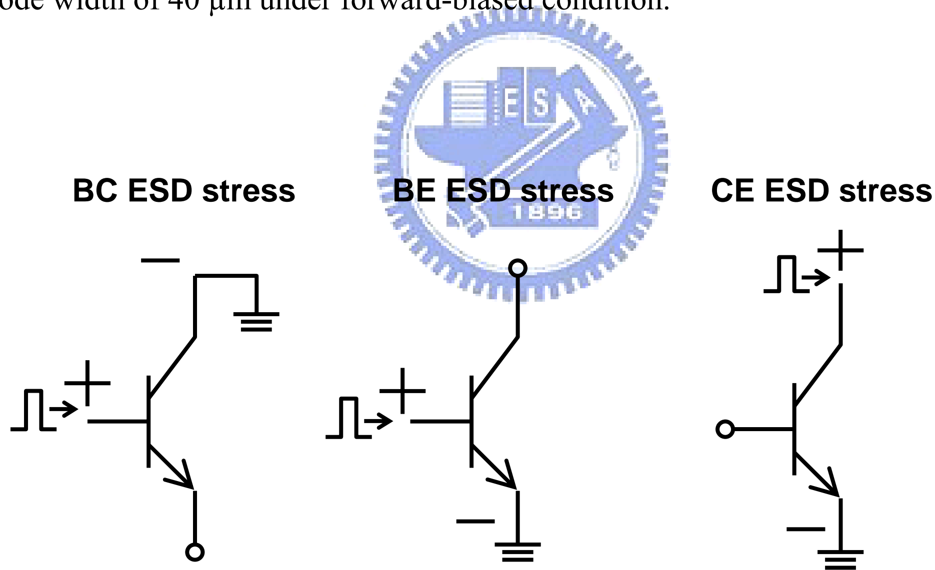


Fig. 2.11 Three types of ESD stress for the SiGe HBT device.

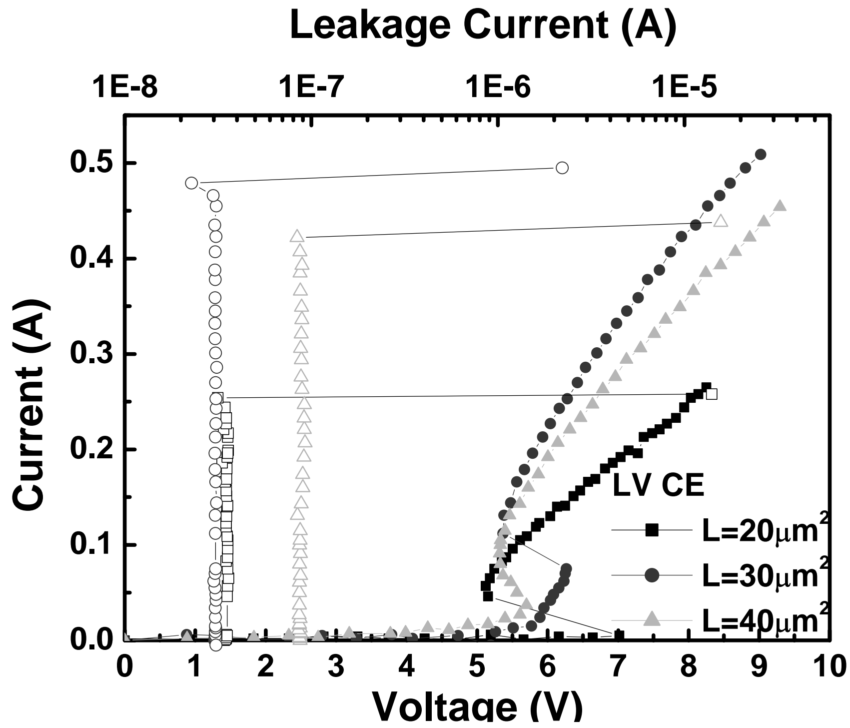


Fig. 2.12 The TLP I-V curve of the low-voltage SiGe HBT with different emitter lengths and fixed emitter width of 0.45 μm under CE stress.

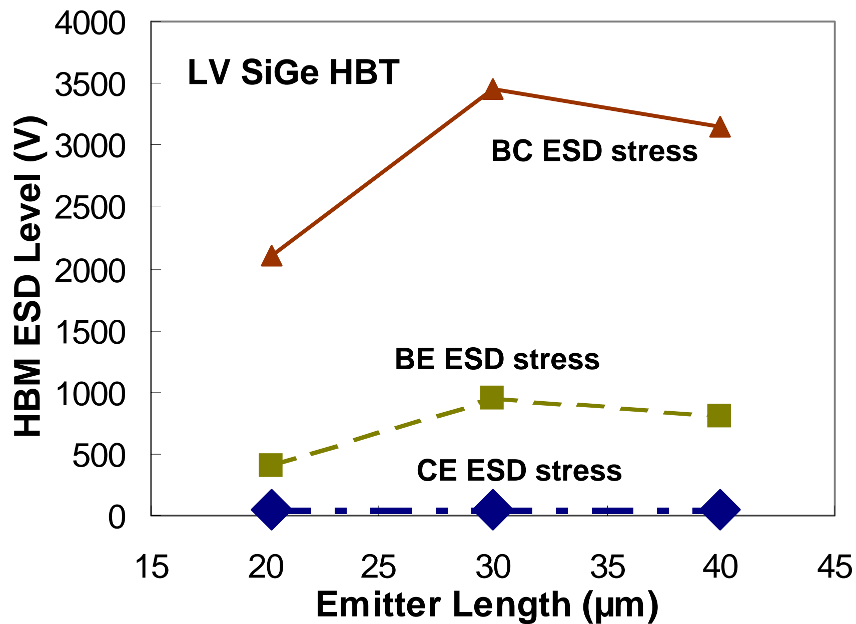


Fig. 2.13 HBM ESD robustness versus emitter length of the low-voltage SiGe HBT with emitter width of 0.45 μm.

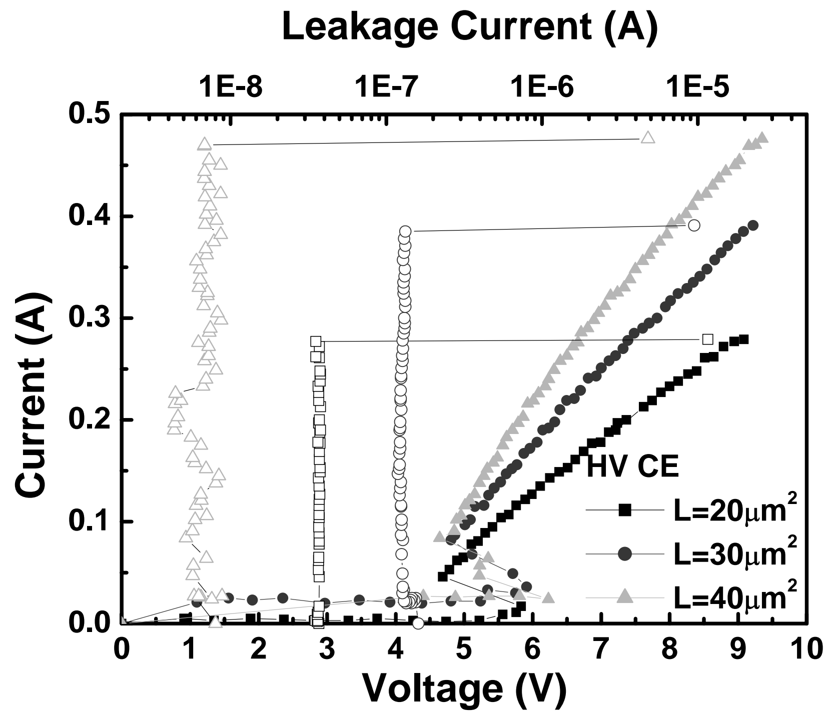


Fig. 2.14 The TLP I-V curve of the high-voltage SiGe HBT with different emitter lengths and fixed emitter width of 0.45 μm under CE stress.

ESA

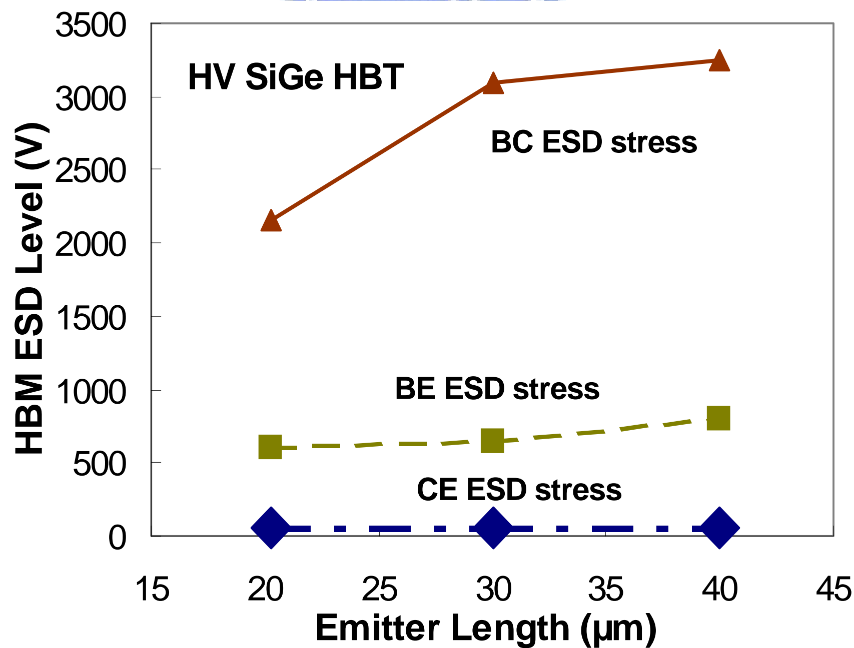


Fig. 2.15 HBM ESD robustness versus emitter length of the high-voltage SiGe HBT with emitter width of 0.45 μm.

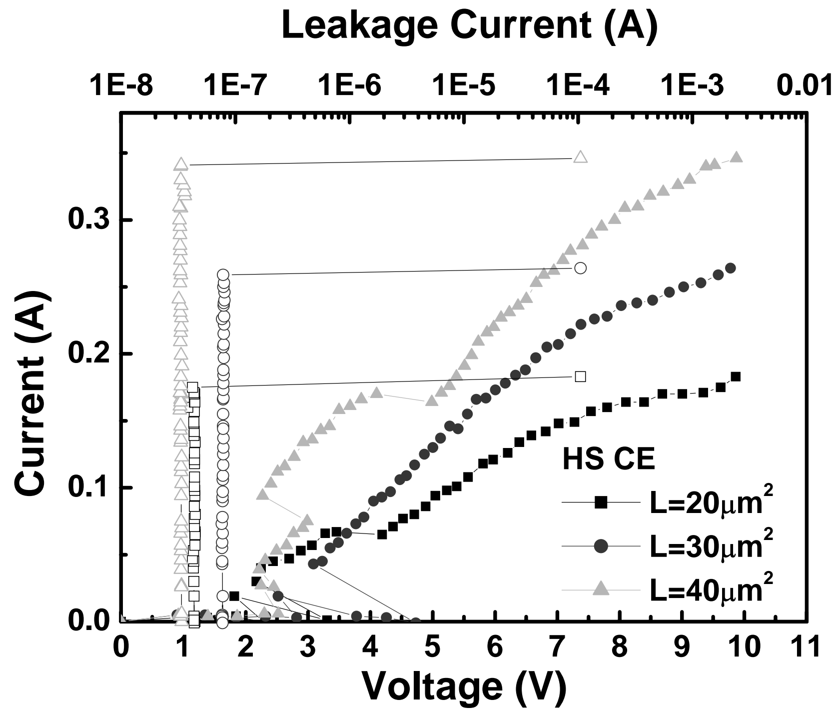


Fig. 2.16 The TLP I-V curve of the high-speed SiGe HBT with different emitter lengths and fixed emitter width of 0.45 μm under CE stress.

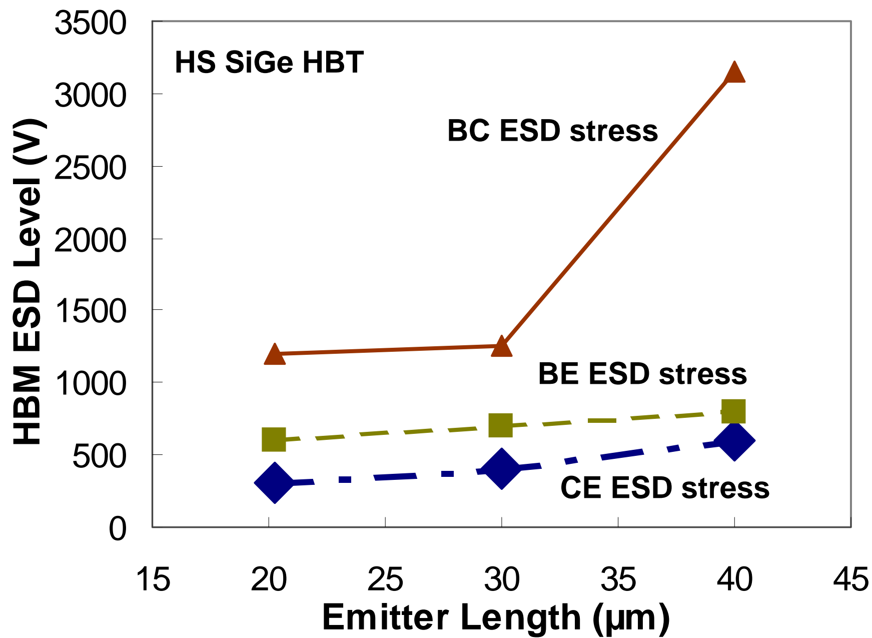


Fig. 2.17. HBM ESD robustness versus emitter length of the high-speed SiGe HBT with emitter width of 0.45 μm.

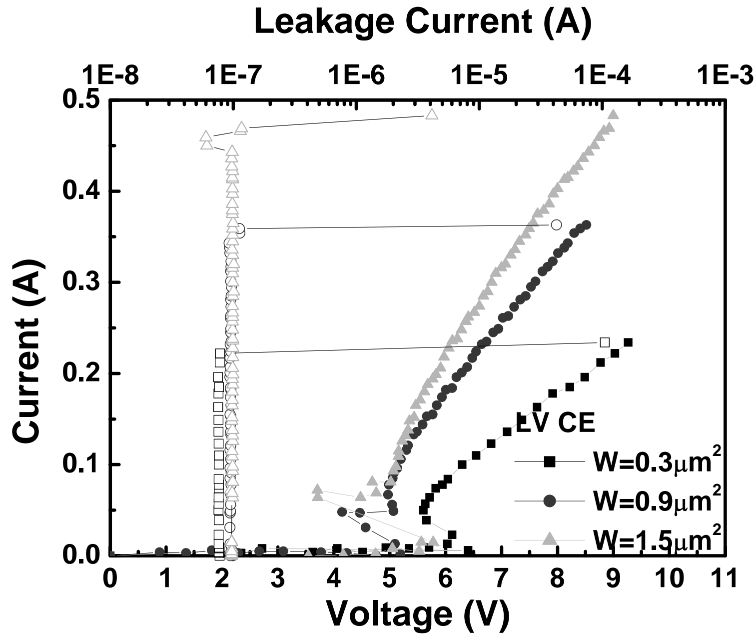


Fig. 2.18 The TLP I-V curve of the low-voltage SiGe HBT with different emitter widths and fixed emitter length of 30 μm under CE stress.

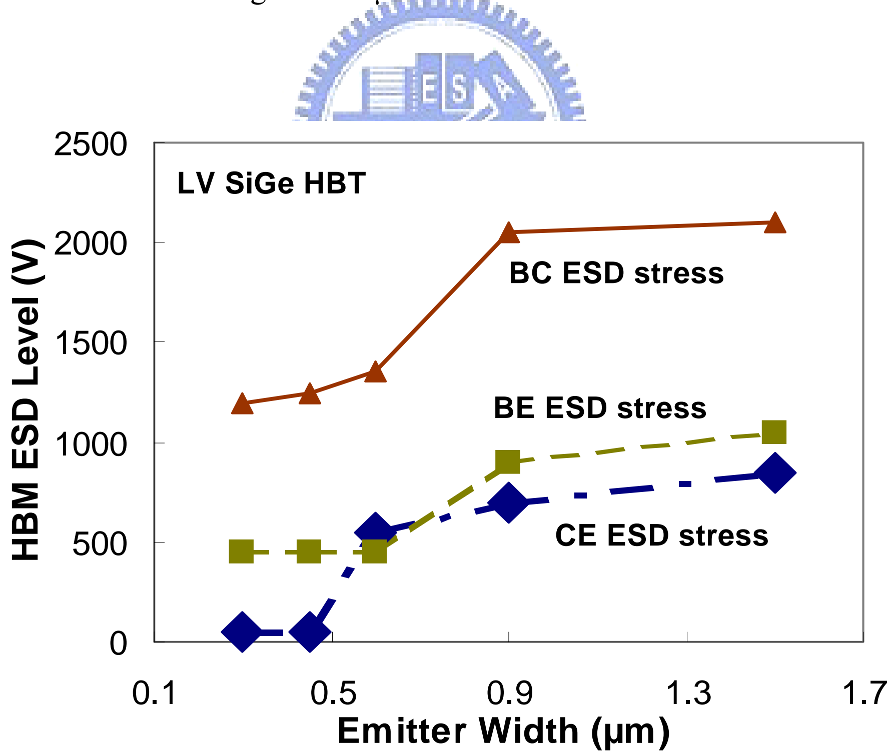


Fig. 2.19 HBM ESD robustness versus emitter width of the low-voltage SiGe HBT with emitter length of 20.3 μm.

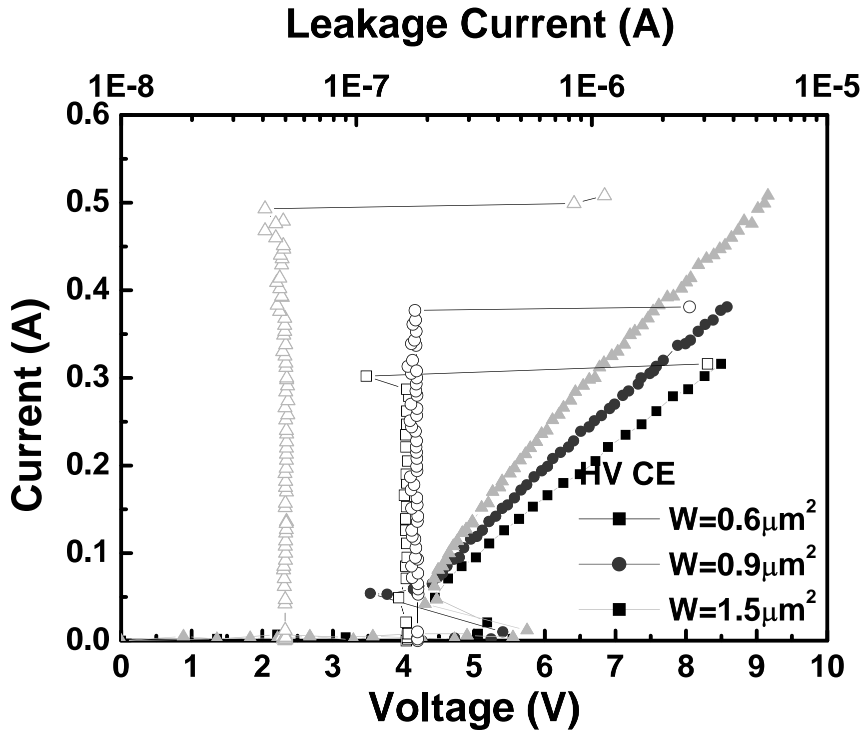


Fig. 2.20 The TLP I-V curve of the high-voltage SiGe HBT with different emitter widths and fixed emitter length of 30 μm under CE stress.

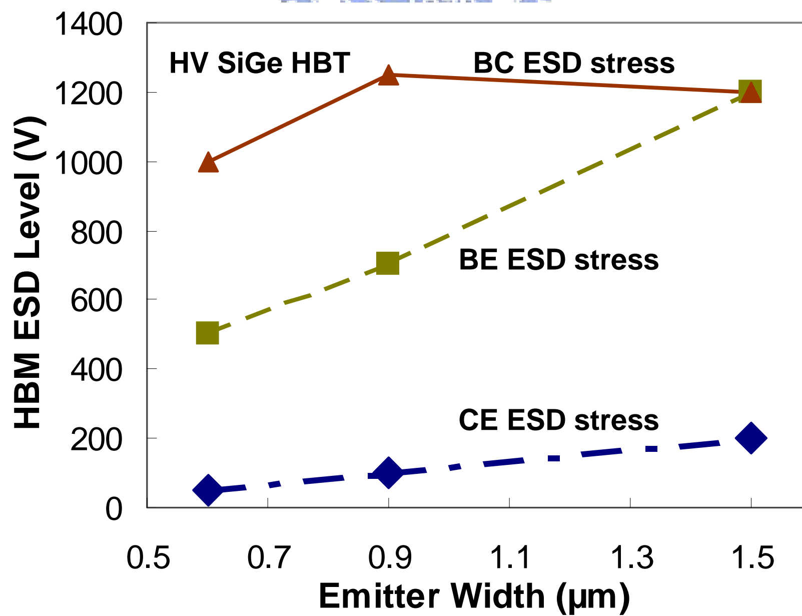


Fig. 2.21 HBM ESD robustness versus emitter width of the high-voltage SiGe HBT with emitter length of 20.3 μm.

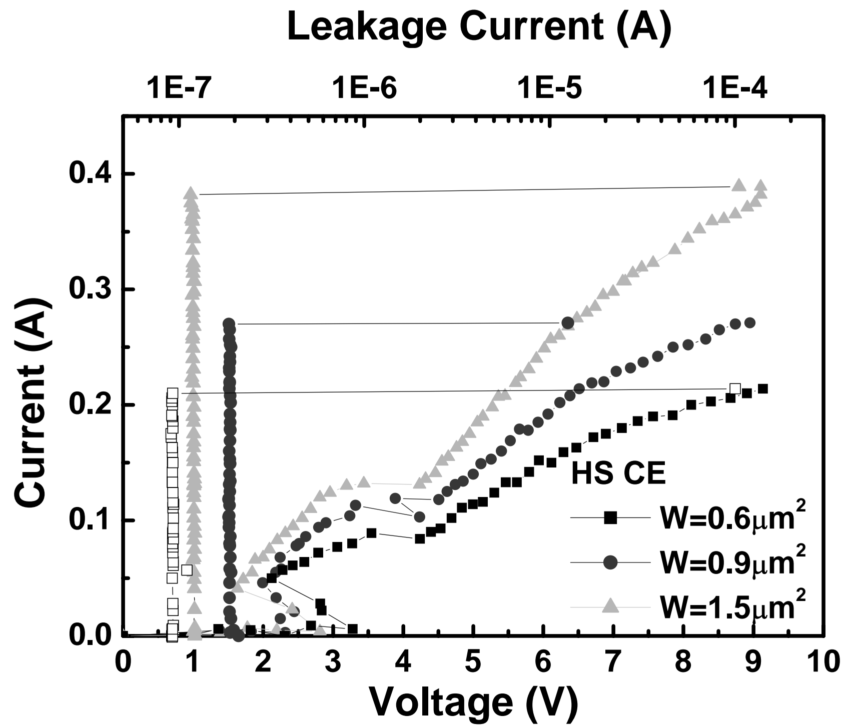


Fig. 2.22 The TLP I-V curve of the high-speed SiGe HBT with different emitter widths and fixed emitter length of 30 μm under CE stress.

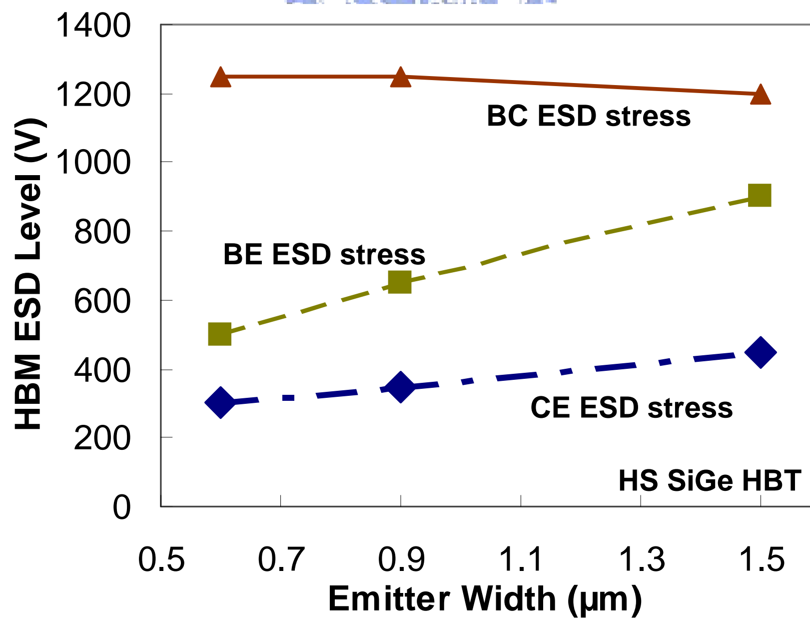


Fig. 2.23 HBM ESD robustness versus emitter width of the high-speed SiGe HBT with emitter length of 20.3 μm.

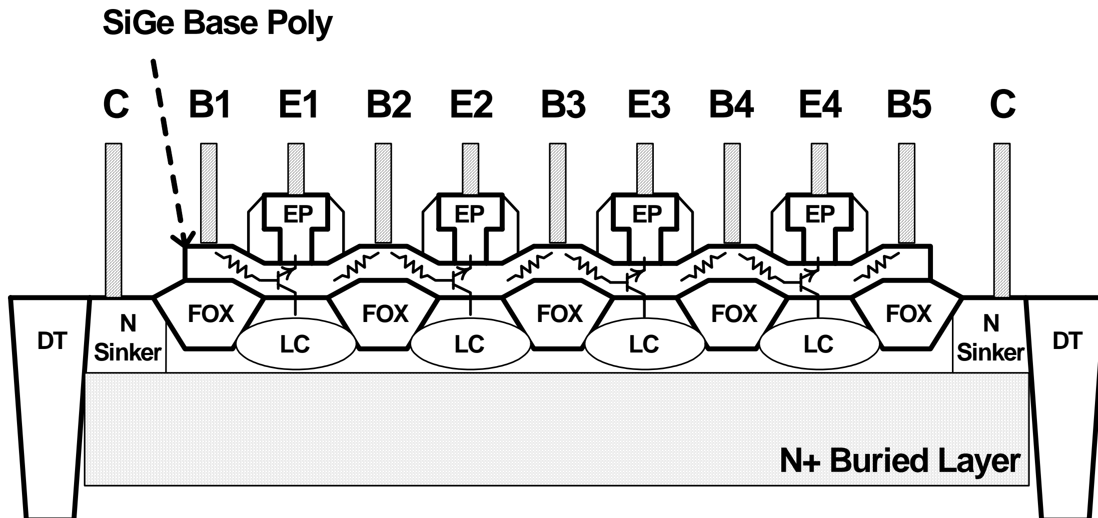


Fig. 2.24 The SiGe HBT with multi-finger device structure. Base resistance will increase if the base terminal is not all connected together through the contact on its top.

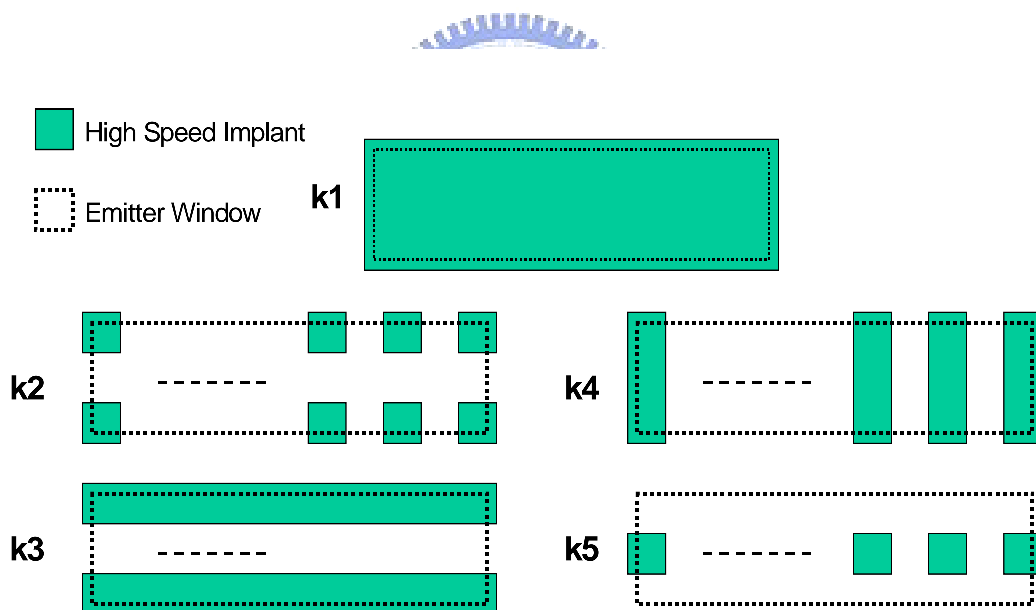


Fig. 2.25 The designed high-speed implantation patterns for HBT device. K1 is the standard layout with uni-square shape. K2, K3, K4, and K5 are designed to different shapes for investigation.

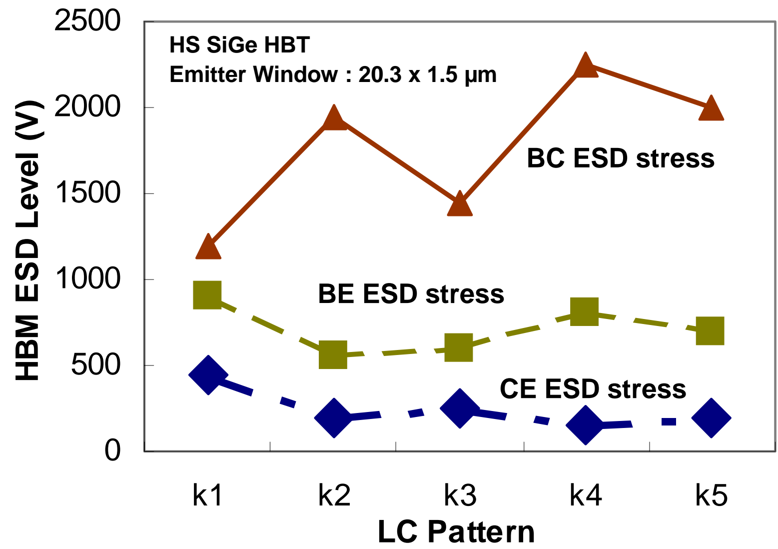


Fig. 2.26 HBM ESD robustness versus high-speed SiGe HBT with different high-speed implantation patterns.

TABLE 2.1

ESD robustness of low-voltage SiGe HBT with different base nodes grounded

Gnd	B12345	B135	B13	B1
HBM ESD	100	100	1800	N/A

TABLE 2.2

ESD robustness of low-voltage SiGe HBT with some emitter and base node grounded

Gnd	B1E1	B1E2	B1E3
HBM ESD	N/A	700	100

Chapter 3

Low-Leakage-Current Diode String in 0.18-μm SiGe BiCMOS Process and Its Application on Power-Rail ESD Clamp Circuits

3.1 INTRODUCTION

Diode under forward-biased condition can sustain very high ESD stress within a smaller silicon area. Therefore, the diode string has been widely used in integrated circuits for ESD protection [13]-[16]. However, a parasitic vertical p-n-p bipolar transistor exists in the conventional P+/N-well diode with the common P-type substrate. This parasitic vertical p-n-p bipolar transistor often causes high leakage current in the diode string [13]-[16], especially in the high-temperature condition. Previous designs on the diode string to reduce leakage current had been reported by T. Maloney [14]-[15], which had been called as Cladded diode string, Boosted diode string, and Cantilever diode string, respectively.

But, those designs still have high leakage current at the high temperature of 125°C [17]. To significantly reduce the leakage current of the diode string in CMOS process, an NMOS-controlled lateral SCR (NCLSCR) device had been added into the diode string to result in a very low leakage level [17], even in the high-temperature condition. However, an ESD detection circuit must be designed in chip to quickly trigger the NCLSCR on.

Recently, in 0.18-μm CMOS process, the triple-well structure has been used in the diode string [18], which is expected to solve the substrate leakage current issue. The

base and emitter of the parasitic p-n-p bipolar transistor is tied together to suppress the substrate leakage current. In SiGe BiCMOS process, the deep trench (DT) was used to reduce the substrate leakage current of the diode string [19]. With the DT and n+ buried layer, the parasitic vertical p-n-p bipolar transistor in the diode string has open-base configuration, which results in a lower substrate leakage current then that of the conventional P+/N-well diode at high temperature.

Fig. 3.1 shows the typical application of the diode string in the power-rail ESD clamp circuit. Since the ESD stress may have positive or negative voltages on an input (or output) pad with respect to the grounded VDD or VSS pins. For a comprehensive ESD verification, the pin-to-pin ESD stress and the VDD-to-VSS ESD stress, had been also specified to verify the whole-chip ESD robustness. With the power-rail ESD clamp circuit, the positive-to-VSS ESD stress on the I/O pin can be discharged through the diode under forward-biased condition to VDD, and then through the power-rail ESD clamp circuit to grounded VSS [10].

So, the ESD clamp circuit between power rails is very helpful to protect I/O pin and the internal circuits of integrated circuits against ESD damage. The diode string in Fig. 3.1 is operated in forward-biased condition to discharge ESD current. Thus, it can sustain very high ESD level in a smaller silicon area. However, the main drawback for using the diode string as power-rail ESD clamp circuit is the leakage issue, especially in the high-temperature condition.

In this work, an extra bias is applied to the deep N-well of the diode string with triple-well structure to further minimize the leakage current of the diode string. The test chip has been designed, fabricated, and verified in a 0.18-µm SiGe BiCMOS process. Such diode string with minimized leakage current has been used in the power-rail ESD clamp circuit, or the ESD connection cell between the separated

power rails, to achieve whole-chip ESD protection.

3.2 REVIEW ON THE DIODE STRING

3.2.1 The Pure Diode String

The cross-sectional view of the pure diode string is shown in Fig. 3.2 [17]. Because of the parasitic vertical p-n-p transistor, the diode string causes more leakage current flowing into the substrate. If the gain of the parasitic vertical p-n-p transistor is above one or even larger, the addition of stacked diodes in the diode string doesn't increase the blocking voltage across the diode string linearly.

This means that more diodes would be needed to support the same blocking voltage. To reduce the leakage current of the pure diode string, three modified designs had been reported in [17]-[18]. In order to reduce the serious substrate leakage current, there are a modified design and a new proposed design in the following section.

3.2.2 The Modified Diode String to Reduce Leakage Current

A modified design to reduce the leakage current by using triple-well technologies had been reported in [18]. Fig. 3.3 shows the cross-sectional view of the n-stage triple-well diode string with its parasitic base-emitter tied p-n-p bipolar transistors. Operating in the forward-biased condition, diode current will flow through the P-well regions, and most holes are not injected into the base region of the parasitic vertical p-n-p bipolar transistors because of the base-emitter tied configuration.

It suppresses the substrate leakage current. The substrate leakage current could be

kept very small all the time before the triple-well diode string turn on. It results from the existence of the parasitic base-emitter tied p-n-p bipolar transistor.

3.3 LLCDS

In this work, low-leakage-current diode string (LLCDS) to minimize the leakage current of the diode string is proposed. The top view and cross-sectional view of the diode with deep N-well in a 0.18-μm SiGe BiCMOS process is shown in Fig. 3.4 and Fig. 3.5. Compared with the traditional P+/N-well diode string, this structure has a deep N-well to isolate P-well and the common P-substrate. An extra bias is applied to the deep N-well to minimize the substrate leakage current.

As shown in Fig. 3.6, the connection of LLCDS has a voltage applied to the deep N-well. The connection of deep N-well to the extra bias makes the parasitic n-p-n of the triple-well diode being slightly turned on. This current will flow into the next stage diode of LLCDS, but not to the common P-substrate. So, the substrate leakage current can be effectively decreased.

With the decreased substrate leakage current, total current flowing from the anode will mainly flow through the diode string itself to build up a higher blocking voltage between the power rails. Therefore, the overall leakage current through the diode string can be minimized. A resistance (R_{bias}) is further connected between the bias voltage and the deep N-well to control the leakage current level through the diode string. As the substrate leakage current could be reduced, another leakage current path appears. Because of the parasitic n-p-n bipolar transistors of the triple well diode, the leakage current will be a mount of current flow through the junction between P-well and N+ under the high-temperature condition.

3.4 MEASUREMENT RESULTS

LLCDS, as shown in Fig. 3.6, has been fabricated in a 0.18-µm BiCMOS SiGe process. In this design, the numbers node of deep N-well in the diode string is connected out for bias, named as Vbias. The P+ anode of the diode string is marked as Vp in Fig. 3.6.

During measurement, the cathode of the diode string and the substrate are grounded with two separated channels, so that the cathode current (In) and the substrate leakage current (Isub) can be monitored separately. The total current flowing into the diode string should equal to the total current flowing out the device. The equation can be expressed as:

$$I_A + I_b = I_n + I_{sub} \quad (1)$$

The measured I-V curves along the diode string with three diodes in series (N=3) under the bias conditions of deep N-well floating, or biased at 1.8V, are shown in Fig. 3.7. The diode string with Vb of 1.8V has a higher blocking voltage and a lower leakage current, as comparing to that with Vb of floating.

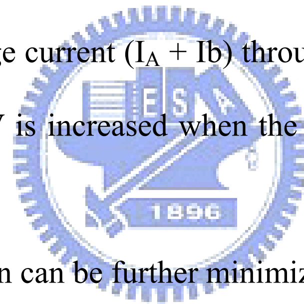
When I_A = 1µA, the value of VDD named the total blocking voltage of the triple-well diode string. Fig. 3.8 shows that the measured I-V curves of the different diode number of the diode string under the bias conditions (Vbias) of deep N-well floating, or biased at 1.8V, at the temperature of 25°C.

The relation between the total blocking voltage (defined at I_A=1µA) and diode number (N) of the diode string is shown in Fig. 3.9, under Vbias=1.8V to the deep N-well. In Fig. 3.9, it is apparent that the extra bias on deep N-well can increase the total blocking voltage of the diode string. The relation between the total blocking voltage (defined at I_A=1µA) and diode number (N) of the diode string is shown in Fig.

3.10, under Vbias floating. Because the leakage current doesn't flow into the substrate due to the extra bias on the deep N-well, the current is all flowing into the next stage diode in LLCDS to result in a higher blocking voltage across the diode string.

According to equation (1), when the current of Isub is far smaller then that of In, most current will flow through the diode string. As a result, applying a bias to the deep N-well will improve the blocking voltage of the triple-well diode string. But, when adding a voltage on the deep N-well, it has a leakage path from Vbias to the ground through the diode string.

So, a bias resistance (R_{bias}) is added to reduce the leakage current from Vb. In Fig. 3.11, the relation between bias resistance (R_{bias}) and the total leakage current (I_A + Ib) through the diode string with four diodes (N=4) is measured under different temperatures. The total leakage current (I_A + Ib) through the diode string (N=4) under voltage bias of Vp= Vb=1.8V is increased when the temperature is 25°C, 75°C, and 125°C.



However, this phenomenon can be further minimized by adding the bias resistance, which limits the current flow through the deep N-well (Ib). Moreover, when Ib decreases with an increasing resistance, the current flow from the anode to cathode will increase. Under this condition, the value of resistance should be optimized. From the measured results, the diode string (N=4) with a bias resistance of 10 kohm has a minimized leakage current. The equations to minimize the leakage current of the diode string with different diode stages or different blocking voltages can be further derived for optimization design.

With a bias resistance of 10 kohm, the ESD robustness of LLCDS with different diode numbers in series are investigated by the transmission-line-pulse generator (TLP) with pulse width of 100ns. As shown in Fig. 3.12, LLCDS with different diode

numbers (N) have different turn-on resistance in high-current region. The diode string with a larger diode number (n) in series has a larger turn-on resistance.

However, the secondary break-down current (It2) of LLCDS with different diode numbers (N) in series did not have obvious variation. The dependence of secondary breakdown current (It2) of LLCDS on the diode number (N) in series is shown in Fig. 3.13, where every diode has the same device dimension of W/L= 40µm/12µm in layout pattern. With an It2 of higher than 4A, LLCDS (under N=4) can sustain the human-body-model ESD stress of 6 kV. In Fig. 3.13, the It2 of the diode string will not obviously decrease when diode number increases. From this result, the number of diode in LLCDS can be reasonably increased to get a higher blocking voltage without degradation on its ESD level.

3.5 CONCLUSION

A new design for the diode string in 0.18-µm SiGe BiCMOS process has been proposed and verified. According to the experimental results, with extra bias to the deep N-well through a bias resistance, the total blocking voltage of the diode string can be effectively increased. Although the additional extra bias will cause some current into the diode string, the overall leakage current of the diode string can be minimized by a bias resistance.

With this new design, the substrate leakage current can be always kept in a very small value with the order of pA, even under the temperature of 125°C. This new proposed diode string is very suitable for applying in the power-rail ESD clamp circuit and the ESD connection cell between the separated power lines. Optimization design to find the best design choice on the bias resistance and its corresponding

circuit implementation will be studied in the future.

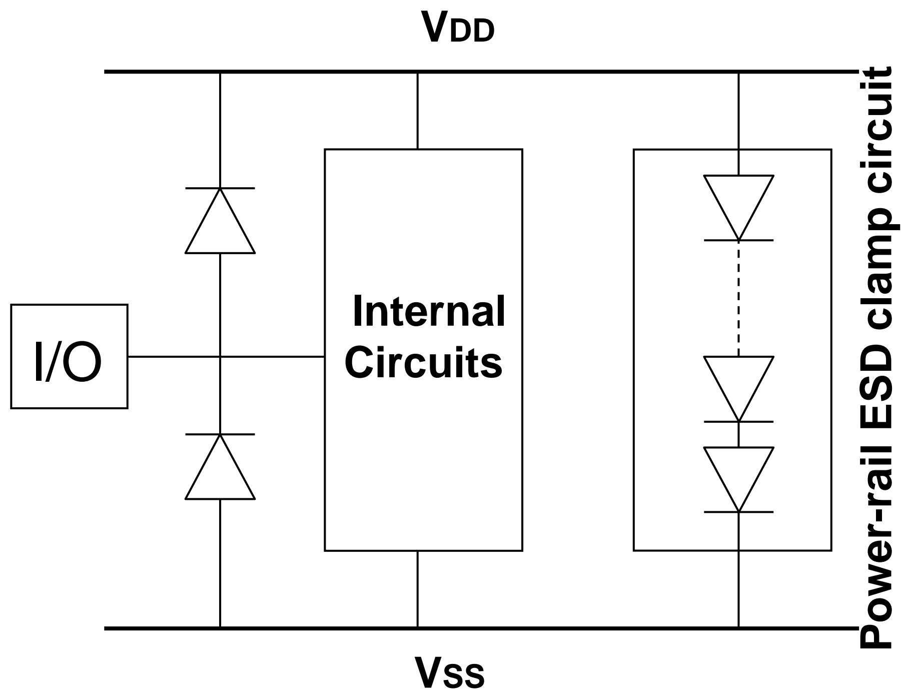


Fig. 3.1 The whole-chip ESD protection design with the diode string applied in the power-rail ESD clamp circuit.

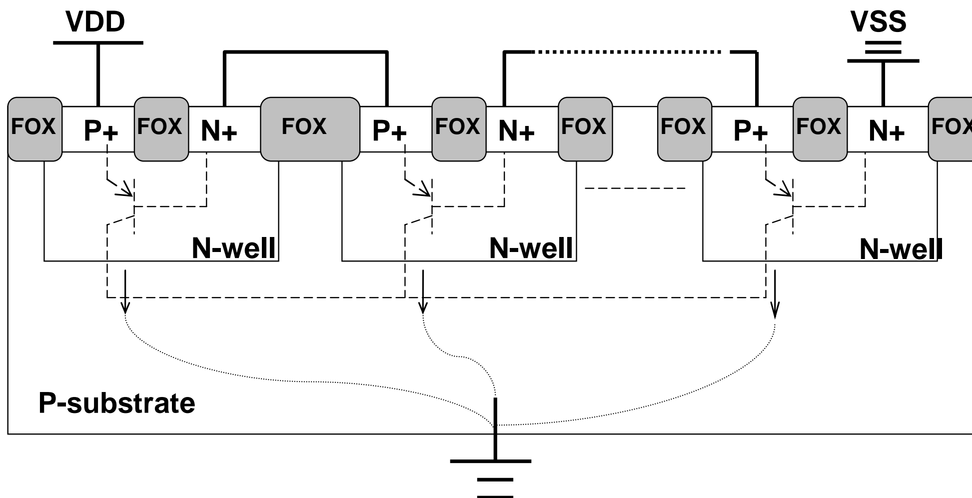


Fig. 3.2 The cross-sectional view of the pure diode string.

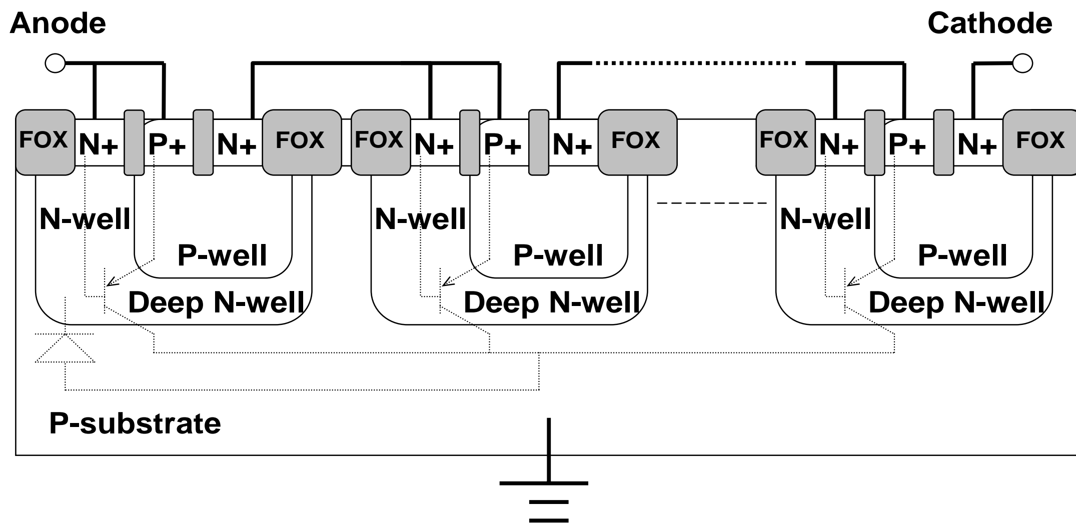


Fig. 3.3 The cross-sectional view of the n-stage triple-well diode string and its parasitic base-emitter tied p-n-p bipolar transistors.

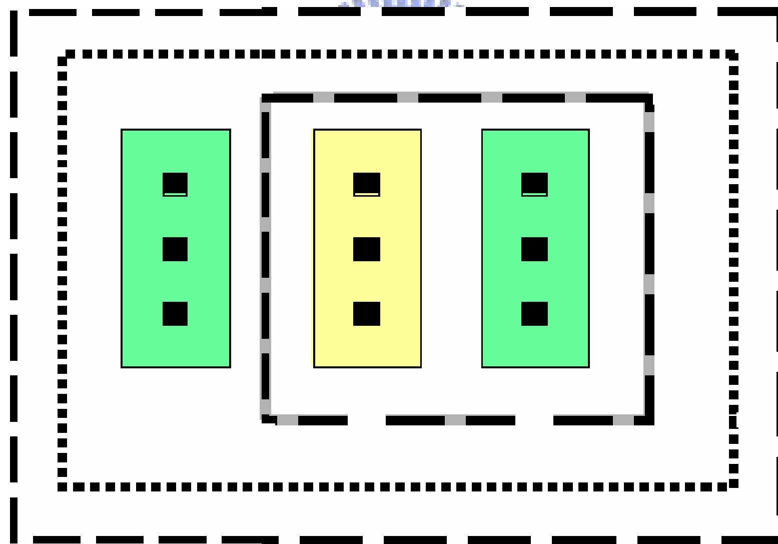


Fig. 3.4 The top view of triple-well diode structure in 0.18-μm BiCMOS SiGe process.

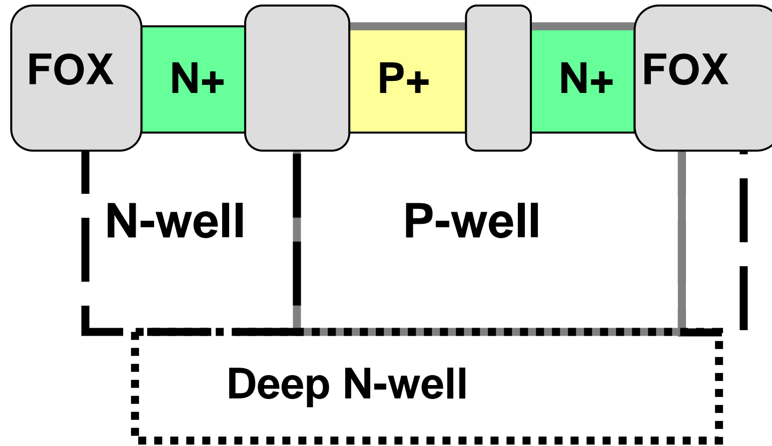


Fig. 3.5 The cross-sectional view of triple-well diode structure in 0.18-μm BiCMOS SiGe process.

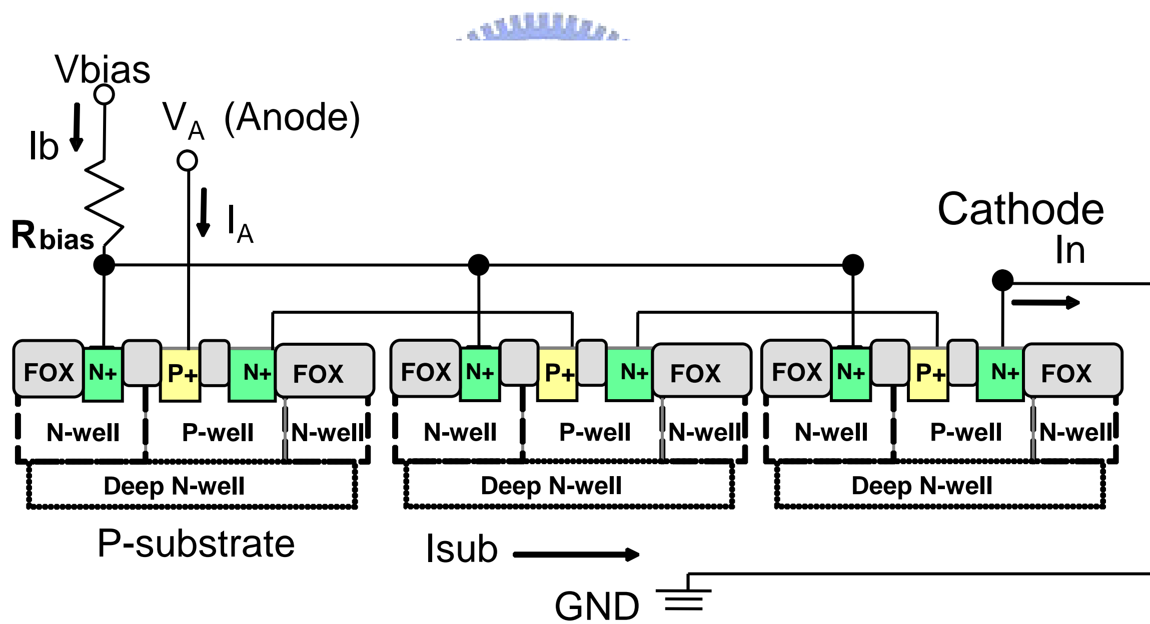


Fig. 3.6 The new proposed diode string with extra bias to the deep N-well to reduce the substrate leakage current.

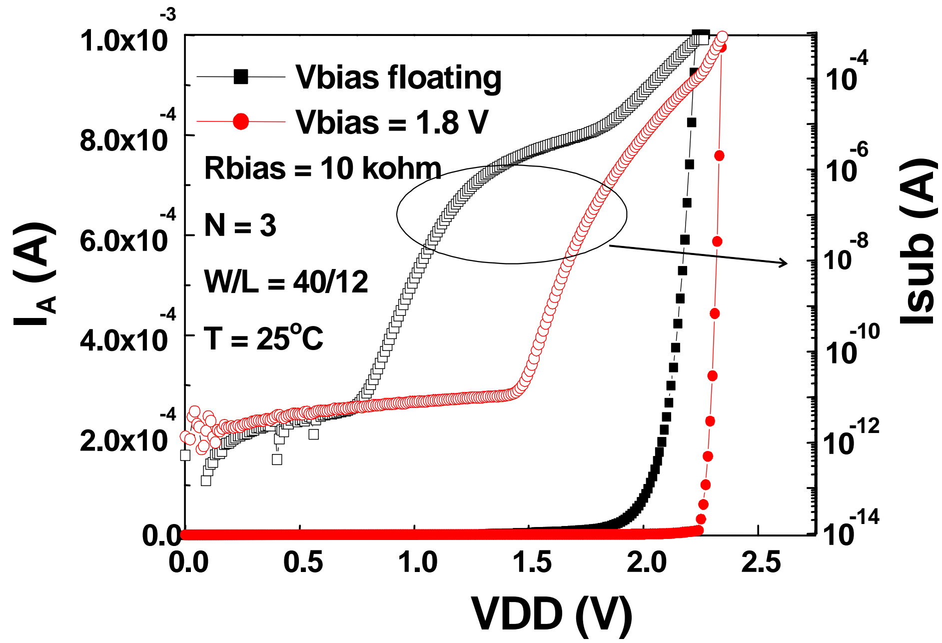


Fig. 3.7 The measured I-V curves along the diode string with three diodes in series (n=3) under the bias conditions (Vbias) of deep N-well floating, or biased at 1.8V.

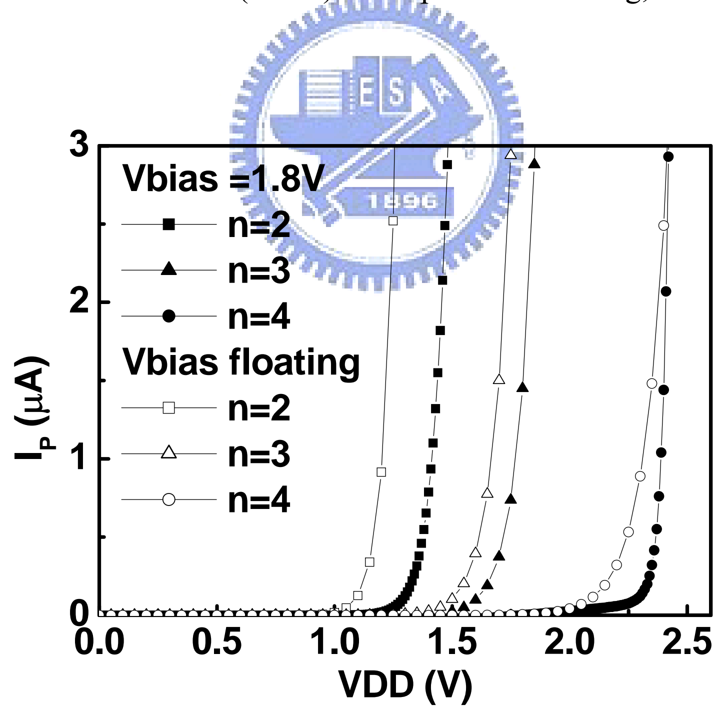


Fig. 3.8 The measured I-V curves of the different diode number of the diode string under the bias conditions (Vbias) of deep N-well floating, or biased at 1.8V, at the temperature of 25°C.

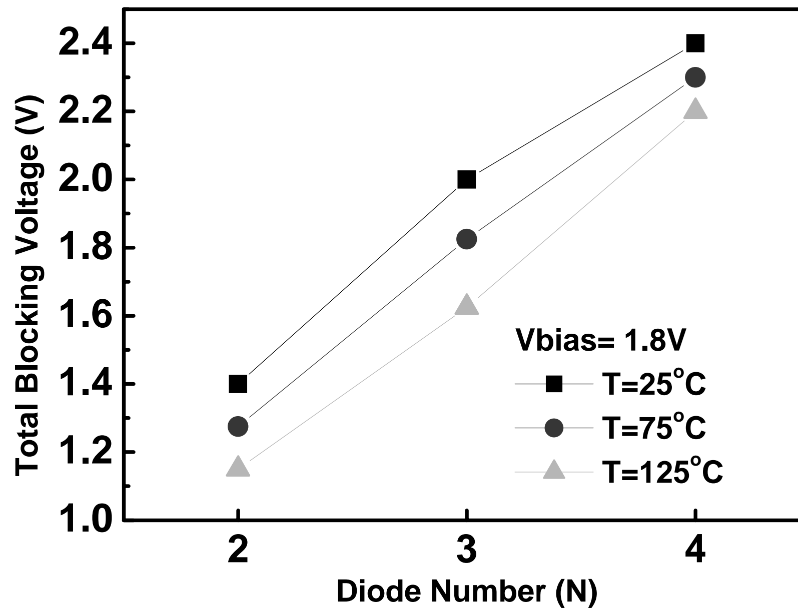


Fig. 3.9 The relation between the total blocking voltage and the diode number (N) of the diode string under Vbias=1.8V at the different temperatures.

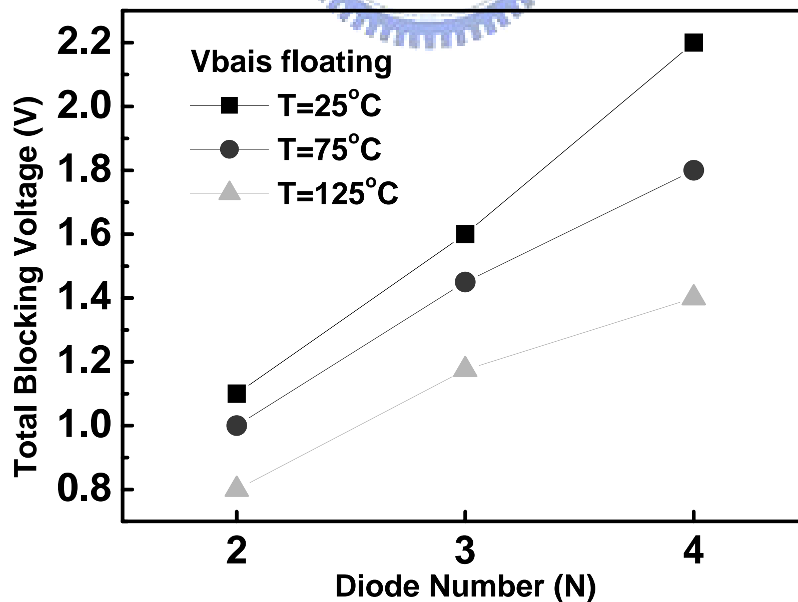


Fig. 3.10 The relation between the total blocking voltage and the diode number (N) of the diode string under Vbias floating at the different temperatures.

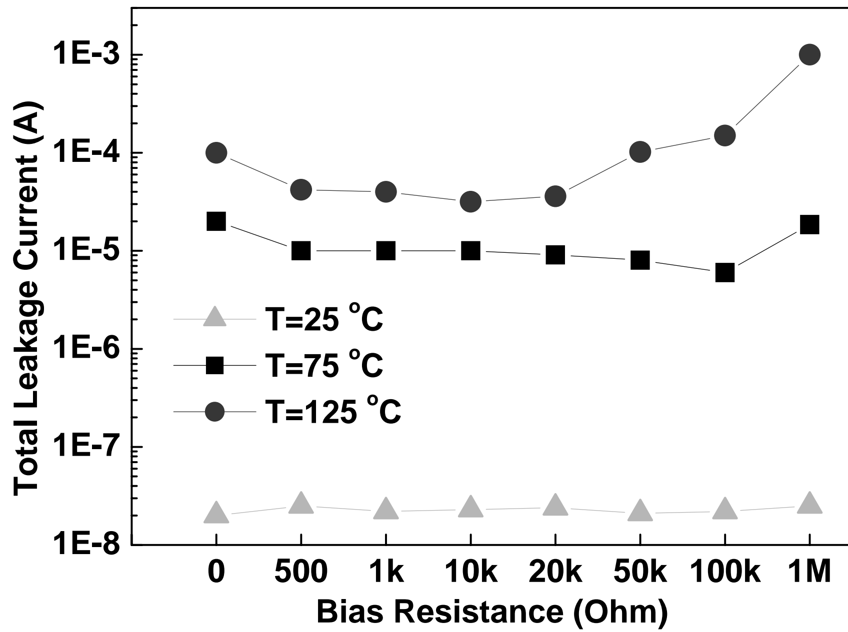


Fig. 3.11 The relation between bias resistance and total leakage current (I_A + Ib) of the diode string with diode number of n=4 and bias condition of Vp=Vb=1.8V, measured at the temperatures of 25°C ,75°C, and 125°C, respectively.

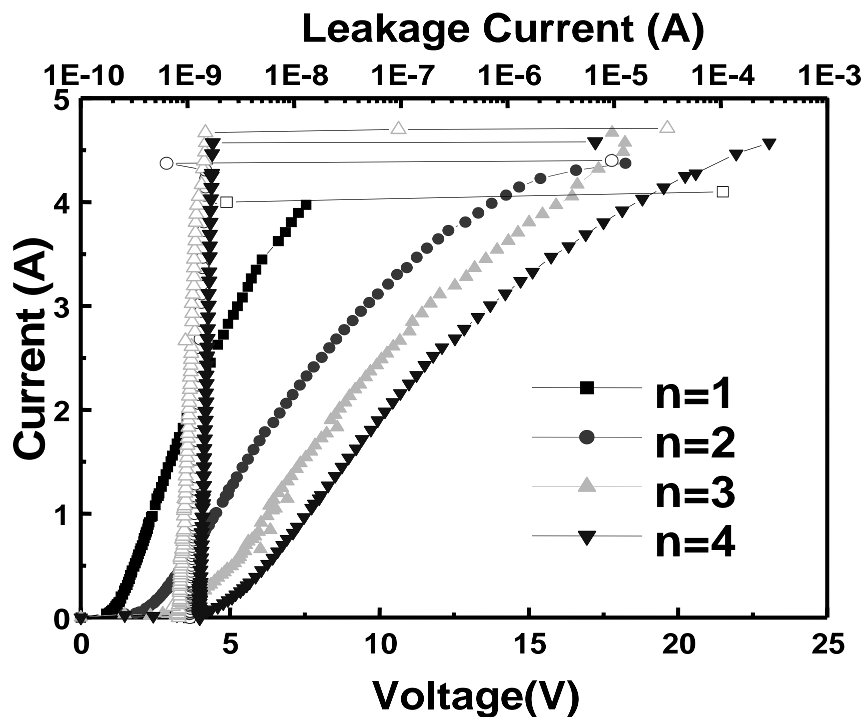


Fig. 3.12 The TLP-measured I-V curves of the diode strings with different diode numbers under the bias resistance of 10 kohm.

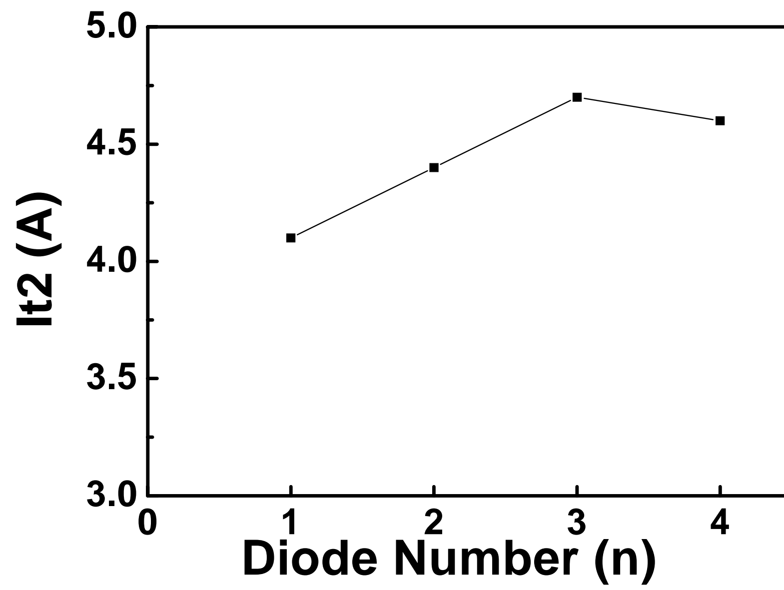


Fig. 3.13 The dependence of secondary breakdown current (It2) of diode string on the diode number (n) in series.

Chapter 4

Minimization of Leakage Current in the Diode String in 0.18-μm SiGe BiCMOS Process

4.1 INTRODUCTION

The SiGe BiCMOS technology has been recognized as one of the best chip solutions for broadband and wireless systems [2]. For ESD protection design in RF circuits, the small input ESD diodes cooperating with the power-rail ESD clamp circuit can meet the circuit requirement and achieve the whole-chip ESD protection scheme[6], [20]. Fig. 4.1 shows the typical ESD protection design in RF circuits, which combines the input ESD diodes and the power-rail ESD clamp circuit. The power-rail ESD clamp circuit is implemented by the diode string [13], [14], as shown in Fig. 4.2.

ESD stress on an input (or output) pad has positive or negative modes, while the VDD or VSS pins are relatively grounded. For a comprehensive ESD verification, the pin-to- pin ESD stress and the VDD-to-VSS ESD stress, have been specified to verify the whole-chip ESD robustness. The ESD clamp circuit between the power rails is very helpful to protect the core circuits against ESD damage for RF circuit application. The ESD current can be discharged by the diode string under forward-bias condition. Therefore, the diode string can sustain a very high ESD level in a small silicon layout area. However, the main drawback for using the diode string as the power-rail ESD clamp circuit is the leakage issue, especially in the high-temperature condition. A

parasitic vertical p-n-p bipolar junction transistor (BJT) exists in the conventional P+/ N-well diode with the common P-type substrate. This parasitic vertical p-n-p BJT often causes high leakage current along the diode string [13], [14], [17], especially in the high-temperature condition.

Some modified designs on the diode string to reduce leakage current have been reported in [14], which called as Cladded diode string, Boosted diode string, and Cantilever diode string, respectively. But, those designs in the bulk CMOS technology still have high leakage current (~mA) at the high temperature of 125°C [17]. In the SiGe process, the deep trench (DT) was used to reduce the substrate leakage current of the diode string [18], [19]. With the DT and n+ buried layer in SiGe prcoess, the parasitic vertical p-n-p BJT in the diode string has a base-open configuration [19], which results in a lower substrate leakage current as compared to that of the conventional P+/N-well diode in CMOS process.

In this work, three kinds of power-rail ESD clamp circuits for RF ESD protection design in BiCMOS SiGe technology are proposed. The first design is the Low-Leakage-Current Diode String (LLCDS), the second design is the Low-Leakage-Current Diode String 2 (LLCDS2), and the third design is the LLCDS-triggered SiGe HBT. In this work, the characteristics of these new proposed power-rail ESD clamp circuits are compared with that of the conventional diode string. In the new proposed LLCDS, an extra bias is applied to the deep N-well of LLCDS to minimize the leakage current of LLCDS.

The cross-sectional view of the conventional diode string is shown in Fig. 4.2. Due to the parasitic vertical p-n-p transistor, the conventional diode string causes more leakage current flowing into the substrate. If the gain of the parasitic vertical p-n-p transistor is more than unity or even larger, the blocking voltage across the

conventional diode string can not increase linearly as the number of stacked diode increases. This means that more stacked diodes would be needed to sustain the required blocking voltage.

4.2 DESIGN ON POWER-RAIL ESD CLAMP CIRCUIT

4.2.1 Low-Leakage current Diode String (LLCDS)

The cross-sectional view of the new proposed of LLCDS in a 0.18-µm BiCMOS SiGe process is shown in Fig. 4.3. The equivalent circuit of LLCDS is shown in Fig. 4.4. Compared with the conventional P+/N-well diode string, the diode structure in LLCDS is formed by the N+/ P-well junction while a deep N-well is used to isolate the P-well from the common P-substrate. In this design, the node of deep N-well in LLCDS is connected to VDD through a resistor R. With the node of deep N-well connecting to VDD, the substrate leakage current due to the parasitic vertical p-n-p transistor (P+/deep N-well/P-sub) is not the concern. However, the leakage current from the parasitic n-p-n transistor in LLCDS will generate, as the equivalent circuit show in Fig. 4.4. The resistor R in LLCDS is applied to further reduce the leakage current from the parasitic n-p-n transistor. The optimized value of resistor R can be derived by the formulas.

The total current flowing into LLCDS should equal to the total current flowing out the device. The total leakage current of LLCDS can be derived as:

$$I_{total\ leakage} = I_{C1} + I_{C2} + I_{C3} + I_{C4} + I_A \quad (1)$$

From the experimental results, the voltage drop across the resistor R is smaller than the voltage drop between the base-emitter of the first parasitic BJT. As a result,

BJT1 will be in the saturation region and BJT2, 3 and 4 will be in the active region. So the collector and emitter current could be easily derived as following.

$$I_E = a_{11}\left(e^{qV_{BE}/kT}-1\right) - a_{12}\left(e^{qV_{BC}/kT}-1\right) \tag{2}$$

$$I_C = a_{21}\left(e^{qV_{BE}/kT}-1\right) - a_{22}\left(e^{qV_{BC}/kT}-1\right) \tag{3}$$

$$V_{BC1} = R \times I_b \tag{4}$$

$$V_{BEn} = \left(kT/q\right)\left[\ln\left(I_{En}+1\right)-\ln\left(I_s\right)\right],\ \text{for } n = 1 \sim 4 \tag{5}$$

$$V_{DD} = \sum_{n=1}^{4}\left(kT/q\right)\left[\ln\left(I_{En}+1\right)-\ln\left(I_s\right)\right] \tag{6}$$

According to equation (4)-(6), the emitter and collector current can be derived.

$$I_{E1} = a_{11}\left(\left(I_{E1}+1\right)/I_s-1\right) - a_{12}\left(e^{qRI_b/kT}-1\right) \tag{7}$$

$$I_{C1} = a_{21}\left(\left(I_{E1}+1\right)/I_s-1\right) - a_{22}\left(e^{qRI_b/kT}-1\right) \tag{8}$$

From the equivalent circuit, the collector current of the BJT2 is the β gain relation with the emitter of the BJT1.

$$I_{C2} = \beta_2 I_{b2} = \beta_2 I_{E1} \tag{9}$$

The value of β of the BJT2 will be determined by its base- emitter voltage.

$$\beta_2 = qN_B/\varepsilon_s\left(V_{bi}-V_{BE2}\right) \tag{10}$$

For the same reason, the collector currents of the others can be derived.

$$I_{C3} = \beta_3 I_{b3} = \beta_2\beta_3 I_{E1} \tag{11}$$

$$\beta_3 = qN_B/\varepsilon_s\left(V_{bi}-V_{BE3}\right) \tag{12}$$

$$I_{C4} = \beta_4 I_{b4} = \beta_2 \beta_3 \beta_4 I_{E1} \tag{13}$$

$$\beta_4 = qN_B / \varepsilon_s \left(V_{bi} - V_{BE4}\right) \tag{14}$$

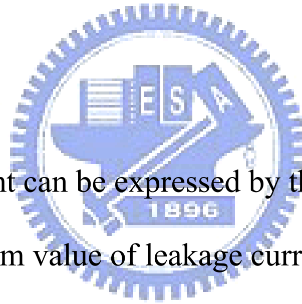
$$I_{C1} + I_{C2} + I_{C3} + I_{C4} = I_{C1} + \left(\beta_2 + \beta_2\beta_3 + \beta_2\beta_3\beta_4 \right) I_{E1} \tag{15}$$

$$I_{E1} = \left[\left(a_{11} / I_s - a_{11}\right) - a_{12}\left(e^{qRI_b / kT} - 1\right) \right] / \left(1 - a_{11} / I_s\right) \tag{16}$$

$$a_{11} = qA\left[D_p n_i^2 / N_B W + D_E n_{EO} / L_E \right] \tag{17}$$

$$a_{12} = qAD_p n_i^2 / N_B W \tag{18}$$

$$I_{B1} = I_{E1} - I_{C1} \tag{19}$$



So, the total leakage current can be expressed by the following equation and it is the function of R. The minimum value of leakage current can be found by letting the differentiation equal to zero, and the optimized value of R could be found.

$$I_{Total\ Leakage} = \left(1 + \beta_2 + \beta_2\beta_3 + \beta_2\beta_3\beta_4 \right) I_{E1} = \left(1 + \beta_2 + \beta_2\beta_3 + \beta_2\beta_3\beta_4 \right) \times \left[\left(a_{11} / I_s - a_{11}\right) - a_{12}\left(e^{qRI_b / kT} - 1\right) \right] / \left(1 - a_{11} / I_s\right) = f(R) \tag{20}$$

The simulation result is shown in Fig. 4.10. There is a minimum value of total leakage current when R is 30kohm. As a result, it can verify the minimum total leakage current exist in LLCDS by choosing a suitable value of R.

4.2.2 Low-Leakage-Current Diode String2 (LLCDS2)

In order to further reduce the total leakage current of LLCDS, there is another method to reduce the total leakage current. The LLCDS2 and its equivalent circuit are shown in Fig. 4.5.

In this method, the β gain of the parasitic bipolar transistor can be lower then the first method, because every resistance connects between the collector of one parasitic bipolar and the collector of the next. When the current flows through the resistance, the voltage drop reduces the collector-emitter voltage of each parasitic bipolar. As a result, the β gain of the parasitic bipolar transistor can be reduced successfully.

The equations are derived as following:

$$I_{Total\ Leakage} = I_b + I_A \tag{21}$$

$$I_A = I_{B1} \tag{22}$$

$$V_1 = VDD - R \times I_b \tag{23}$$

$$R \times I_b < V_{BE1} \tag{24}$$

According to the experimental result, the equation (24) can be proved, so the parasitic BJT1,2, and 4 are in saturation region; the parasitic BJT3 is in active region.

The emitter and collector current are derived.

$$I_E = a_{11}\left(e^{qV_{BE}/kT} - 1\right) - a_{12}\left(e^{qV_{BC}/kT} - 1\right) \tag{25}$$

$$I_C = a_{21}\left(e^{qV_{BE}/kT} - 1\right) - a_{22}\left(e^{qV_{BC}/kT} - 1\right) \tag{26}$$

$$I_b = I_{C1} + I_2 \tag{27}$$

$$I_2 = I_{C2} + I_{C3} \tag{28}$$

According to equation (27),(28),

$$I_b = I_{C1} + I_{C2} + I_{C3} \tag{29}$$

$$V_{BC1} = R \times I_b \tag{30}$$

$$V_{BEn} = (kT/q)\left[\ln(I_{En}+1) - \ln(I_s)\right],\ n = 1 \sim 4 \tag{31}$$

According to equation (29), (30) and (31), the emitter and collector current of the first parasitic bipolar can be derived.

$$I_{E1} = a_{11}\left((I_{E1}+1)/I_s - 1\right) - a_{12}\left(e^{qRI_b/kT} - 1\right) \tag{32}$$

$$I_{C1} = a_{21}\left((I_{E1}+1)/I_s - 1\right) - a_{22}\left(e^{qRI_b/kT} - 1\right) \tag{33}$$

Consider the second parasitic bipolar, its voltage and current can be calculated.

$$V_{BC2} = R \times I_b + R \times I_2 \tag{34}$$

$$V_{BE2} = (kT/q)\left[\ln(I_{E2}+1) - \ln(I_s)\right] \tag{35}$$

$$I_{E2} = a_{11}\left((I_{E2}+1)/I_s - 1\right) - a_{12}\left(e^{qR(I_b+I_2)/kT} - 1\right) \tag{36}$$

$$I_{C2} = a_{21}\left((I_{E2}+1)/I_s - 1\right) - a_{22}\left(e^{qR(I_b+I_2)/kT} - 1\right) \tag{37}$$

Because the third parasitic bipolar is in the active region, its voltage and current can be derived in another formula.

$$\beta_3 = qN_B / \varepsilon_s \left(V_{bi} - V_{BE3}\right) \tag{38}$$

$$\begin{aligned} I_{C3} = \beta_3 I_{b3} = \beta_3 I_{E2} &= qN_B / \varepsilon_s \left(V_{bi} - V_{BE3}\right) \times \{a_{11}\left((I_{E2}+1)/I_s - 1\right) \\ &\quad - a_{12}\left(e^{qR(I_b+I_2)/kT} - 1\right)\} \end{aligned} \tag{39}$$

For the fourth parasitic bipolar, its collector node connects to ground so it works

in the saturation region.

$$V_{BE4} = V_{BC4} \tag{40}$$

$$I_{E4} = (a_{11} - a_{12})\left((I_{E4}+1)/I_s - 1\right) \tag{41}$$

$$I_{C4} = (a_{21} - a_{22})\left((I_{C4}+1)/I_s - 1\right) \tag{42}$$

After calculating all parasitic bipolar, the total leakage current of this diode string can be get.

$$I_{Total\ Leakage} = I_A + I_b = I_A + I_{C1} + I_{C2} + I_{C3} = I_{E1} + I_{C2} + I_{C3} \tag{43}$$

According to equation (33), (37) and (39), the total leakage can be calculation more detail. In this circuit, the β gain of the parasitic bipolar transistor is reduced by applying these resistors. As the result, the total leakage current of LLCDS can be reduced in advance and smaller than the first method.

$$\begin{aligned} I_{Toatal\ Leakage} &= a_{11}\left((I_{E1}+1)/I_s - 1\right) - a_{12}\left(e^{qRI_b/kT} - 1\right) + a_{21}\left((I_{E2}+1)/I_s - 1\right) \\ &\quad - a_{22}\left(e^{qR(I_b+I_2)/kT} - 1\right) + I_{E2} \times qN_B / \varepsilon_s \left(V_{bi} - V_{BE3}\right) \\ &= f(R) \end{aligned} \tag{44}$$

The simulation result is shown in Fig.4.12. There is a minimum value of total leakage current when R is 50kohm. As a result, it can verify the minimum total leakage current exist in LLCDS2 by choosing a suitable value of R. Furthermore, the total leakage current of LLCDS2 is smaller than this of LLCDS. It can reduce total leakage current successfully by adding more stage R in LLCDS2.

4.2.3 HBT Triggered by LLCDS

Using diode trigger HBT has been studied [21] and its circuit design is shown in Fig. 4.6. However, the leakage current of this triggered circuit is studied less. Besides LLCDS alone, the total leakage current can be further reduced with the addition of HBT to LLCDS, as shown in Fig. 4.7. This scheme has a smaller leakage current even under high-temperature condition.

Considering the part of LLCDS in this power-clamp circuit, the parasitic BJT1 will be in the saturation region and the parasitic BJT2, 3 and 4 will be in the active region. So the collector and emitter current could be easily derived as following.

$$I_E = a_{11}\left(e^{qV_{BE}/kT}-1\right) - a_{12}\left(e^{qV_{BC}/kT}-1\right) \tag{45}$$

$$I_C = a_{21}\left(e^{qV_{BE}/kT}-1\right) - a_{22}\left(e^{qV_{BC}/kT}-1\right) \tag{46}$$

Because that:

$$V_{BC1} = R \times I_b \tag{47}$$

$$V_{BEn} = \left(kT/q\right)\left[\ln\left(I_{En}+1\right)-\ln\left(I_s\right)\right], \text{ for } n = 1 \sim 4 \tag{48}$$

$$V_{DD} - \sum_{n=1}^{4}\left(kT/q\right)\left[\ln\left(I_{En}+1\right)-\ln\left(I_s\right)\right] = V_{BE(HBT)} \tag{49}$$

The equation (49) is the key point to differ from pure LLCDS, because the LLCDS does not connect to ground but the base of HBT. Under this condition, all current of LLCDS will flow into the base of HBT and the resistance (Ro).

The equation of the total leakage current could be derived by the similar way. For the SiGe HBT, the base current and the collector current can be expressed as the function of V_{BE}.

The equation of leakage current still can be derived as:

$$I_{total\ leakage} = V_{BE}(R, R_o)/R_o + I_B + I_C \,. \quad (50)$$

Where $$I_B = \frac{qAD_{pe}n_i^2}{W_E N_{de}} e^{qV_{BE}(R,R_o)/kT} \,, \quad (51)$$

and $$I_C = \frac{qAD_{nb}n_i^2}{W_B N_{ab}} e^{qV_{BE}(R,R_o)/kT} \,. \quad (52)$$

The D_{pe} is the diffusion coefficient of emitter, N_{de} is the emitter doping, D_{nb} is the diffusion coefficient of base, and N_{ab} is the base doping.

The resistance (Ro) between the base node of SiGe HBT and ground will affect the total leakage current. Thus, there will be two design parameters, R and Ro, in this circuit. The condition of the total leakage current in this circuit with the SiGe HBT device is different from the one in LLCDS alone because of the SiGe HBT.

1896

These parameters used in SPICE are listed at table 4.1, and those measured from the experiment are listed at table 4.2.

4.3 EXPERIMENTAL RESULTS

The design had been fabricated in a 0.18-μm BiCMOS SiGe process. During measurement, the cathode of LLCDS and the substrate are grounded with two separated channels, so that the cathode current and the substrate leakage current can be monitored separately. The DC characteristics of the conventional diode string, LLCDS, and LLCDS2 are shown in Fig. 4.8, Fig. 4.9, and Fig. 4.10, respectively. According to experimental results, LLCDS and LLCDS2 can have lower substrate leakage current than the conventional diode string.

LLCDS and LLCDS2 have a lower substrate leakage current because there is a

bias applied in the node of deep N-well. In Fig. 4.12, the relationship between bias resistance (R) and the total leakage current through LLCDS with four diodes (N=4) is measured under different temperatures. Because the value of resistance is about kilo ohm order, the N-well resistance is used in these circuits. The total leakage current through the diode string (N=4) is increased when the temperature increases from 25°C to 125°C. Under this condition, the value of bias resistance can be optimized even under high temperature condition.

The relationship between bias resistance (R) and the total leakage current through LLCDS with four diodes (N=4) under different temperatures is shown in Fig.4.14. Compared with Fig. 4.12, the total leakage current indeed reduces in advance. Because adding more stage R, the parasitic bipolar junction transistor can work in saturation region without β gain of base current.

From the measured results, LLCDS (N=4) with a bias resistance of 10 kohm has a minimum leakage current. LLCDS indeed has a lower leakage current if the value of R was chosen properly. The equations to minimize the leakage current of LLCDS with different diode stages or different blocking voltages can be calculated from the aforementioned equations.

The relationship between voltage and the total leakage current of the conventional diode string, LLCDS, and LLCDS2 under 125°C for N=4 are shown in Fig. 4.15. With a bias resistance of 20 kohm, the ESD robustness of LLCDS with different diode numbers in series is investigated by the transmission-line-pulse generator (TLP) with pulse width of 100ns. The dependence of secondary breakdown current (It2) of the conventional diode string, LLCDS, and LLCDS2 on the diode number (N) in series is shown in Fig. 4.16, where every diode has the same device dimension of W/L = 40μm/12μm in layout pattern. However, the secondary break-down current (It2) of the

conventional diode strings and LLCDS with different diode numbers (N) in series did not have obvious variation.

With an It2 of higher than 4A, the diode sting (under N=4) can sustain the human-body-model ESD level of 6 kV. In Fig. 16 the It2 of LLCDS does not decrease when diode number increases. Thus, the number of diodes in the diode string can be reasonably increased to get a higher blocking voltage without degrading the ESD robustness.

The relationship between Ro and total leakage current of the HBT triggered by the conventional diode string, HBT triggered by LLCDS, and HBT triggered by LLCDS2 under 125°C for N=4 are shown in Fig. 4.17. After adding a SiGe HBT, the leakage current was reduced substantially in LLCDS with a HBT while it was not reduced in the conventional diode string with a HBT. The conventional diode string has a smaller blocking voltage because of the serious substrate leakage current, so the V_{BE} of the HBT would be higher than its counterpart in LLCDS with a HBT.

As a result, the leakage current of the conventional diode string with a HBT is much larger than LLCDS with a HBT under high-temperature condition. The TLP I-V curve of the HBT triggered by conventional diode string is shown in Fig. 4.18 for N=4 per unit area of the HBT. The TLP I-V curve of the HBT triggered by LLCDS is shown in Fig. 4.19 for N=4 per unit area of the HBT. The TLP I-V curve of the HBT triggered by LLCDS2 is shown in Fig. 4.20 for N=4 per unit area of the HBT. Because the weakest point is at the collector-emitter junction of the HBT, the ESD robustness of these circuits will be limited by the HBT.

4.4 CONCLUSION

A new design for the diode string in 0.18-μm SiGe BiCMOS process has been proposed and verified. With the additional extra bias to supply little current into the deep N-well of diodes in the LLCDS, the overall leakage current of LLCDS can be minimized. By selecting a suitable bias resistance, the total leakage current of LLCDS can be kept much smaller than that of the conventional diode string. The new proposed LLCDS and the LLCDS-triggered SiGe HBT are very suitable for applying in the power-rail ESD clamp circuits in cooperation with the input ESD diodes to achieve good RF ESD protection design in the SiGe BiCMOS technology.

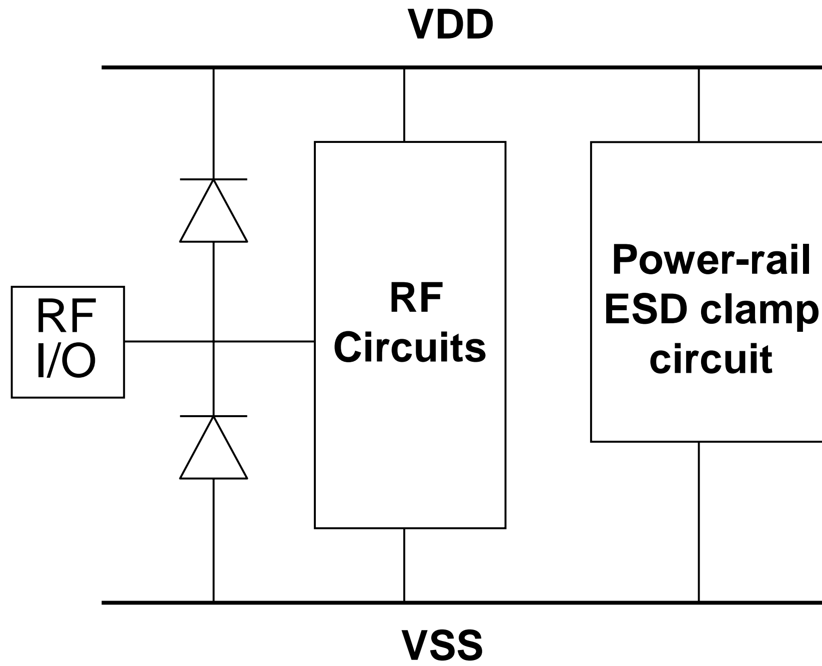


Fig. 4.1 The whole-chip ESD protection design with the diode string applied in the power-rail ESD clamp circuit.

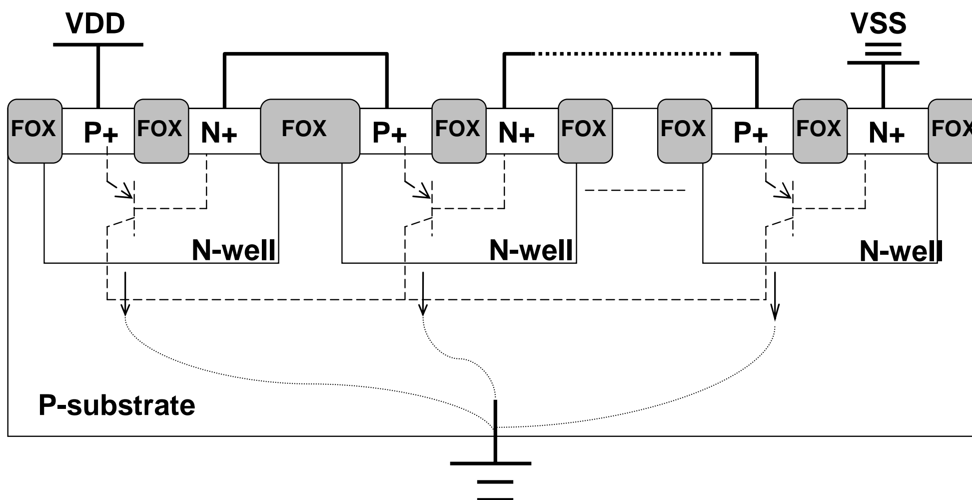


Fig. 4.2 The cross-sectional view of the conventional diode string.

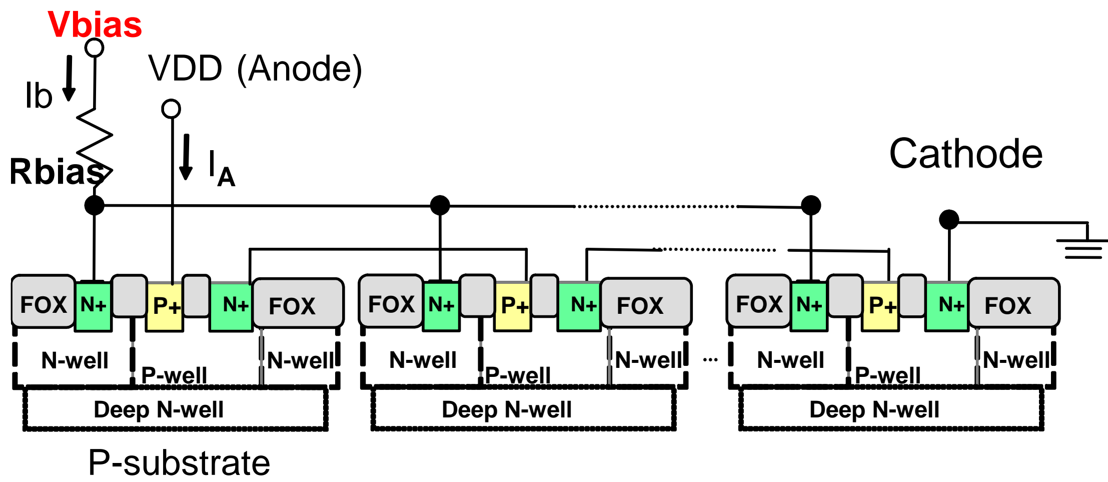


Fig. 4.3 The cross-sectional view of LLCDS in 0.18-μm BiCMOS SiGe.

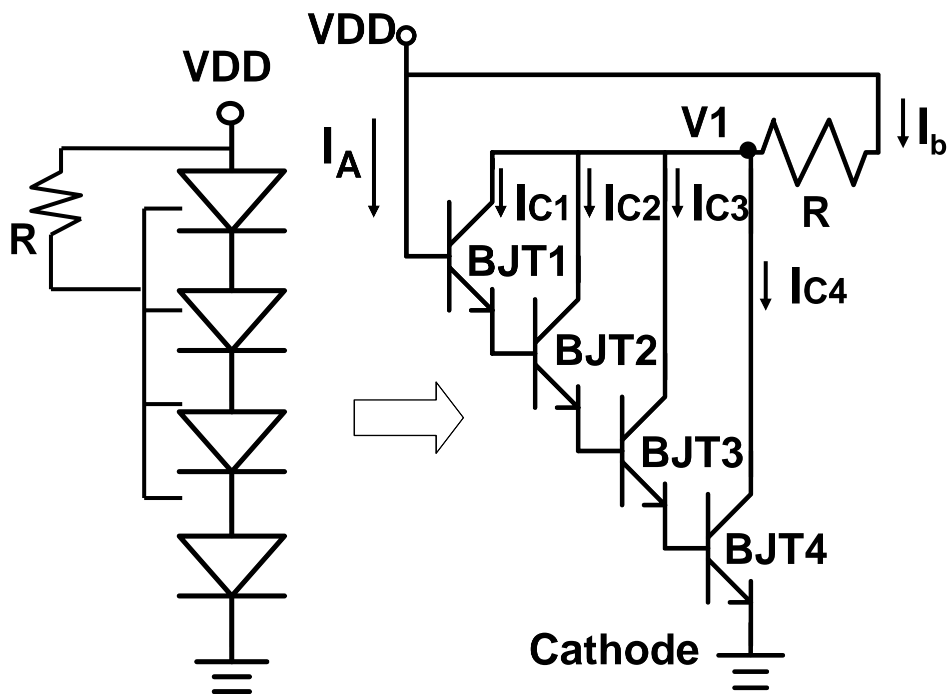


Fig. 4.4 The equivalent circuit of LLCDS in 0.18-μm BiCMOS SiGe.

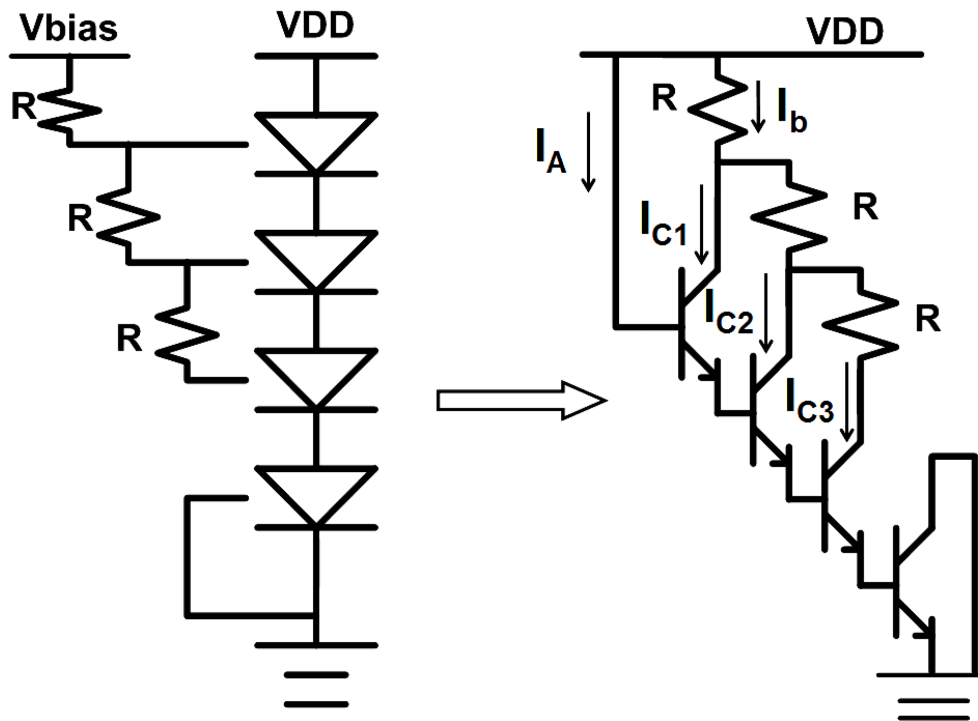


Fig. 4.5 The equivalent circuit of LLCDS2 in 0.18-μm BiCMOS SiGe.

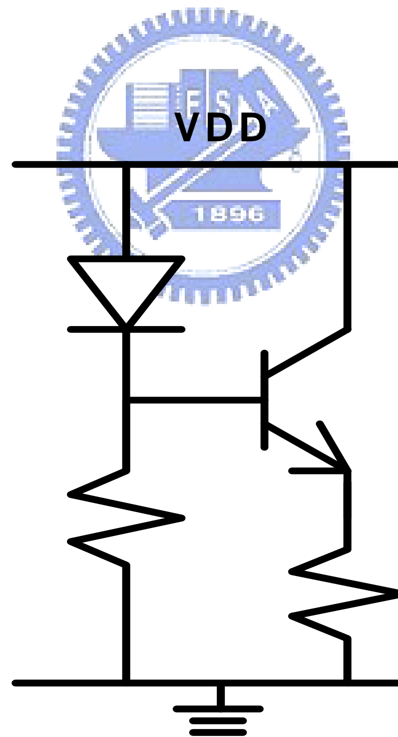


Fig. 4.6 The circuit design on HBT triggered by diode for low-voltage power supply.

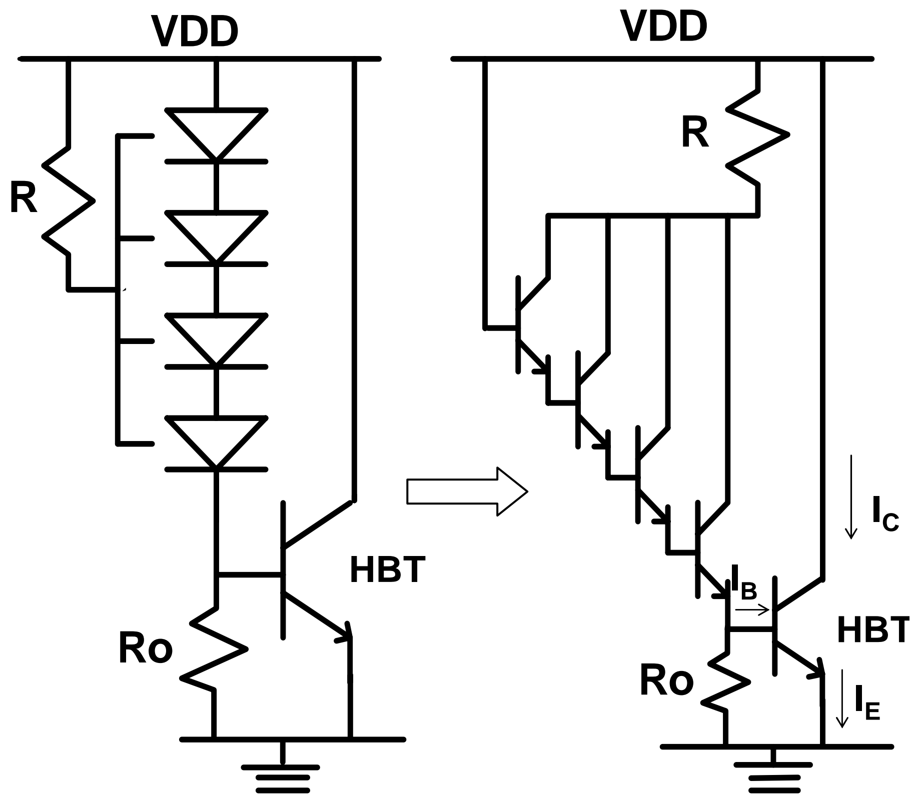


Fig. 4.7 The equivalent circuit of LLCDS applied in another power-rail ESD clamp circuit.

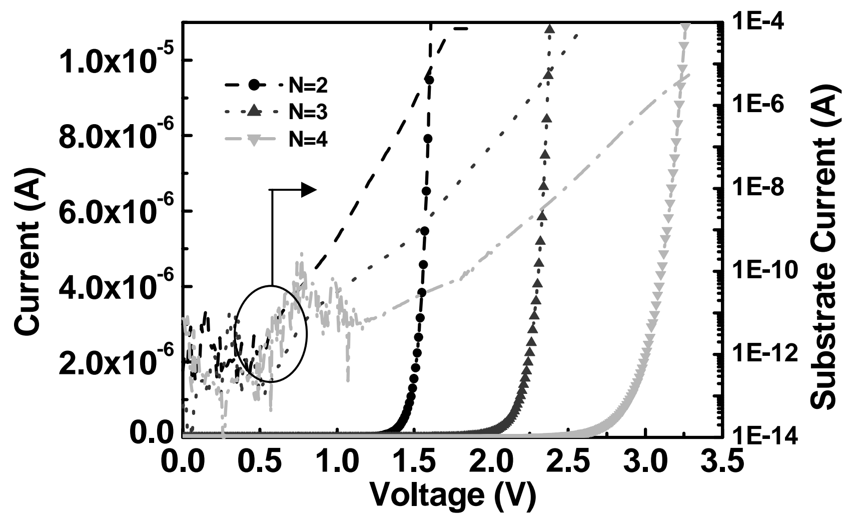


Fig. 4.8 The DC characteristics of the conventional diode string at 25°C.

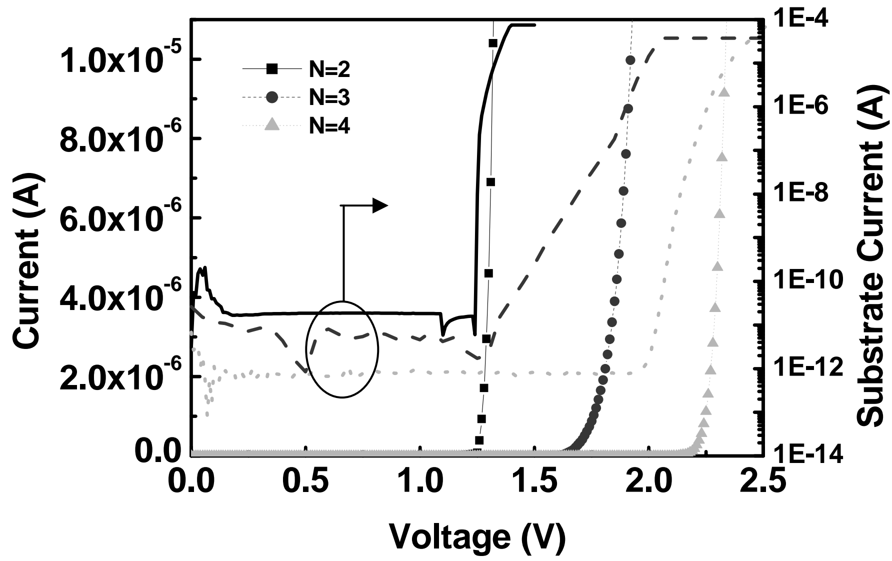


Fig. 4.9 The DC characteristics of LLCDS at 25°C.

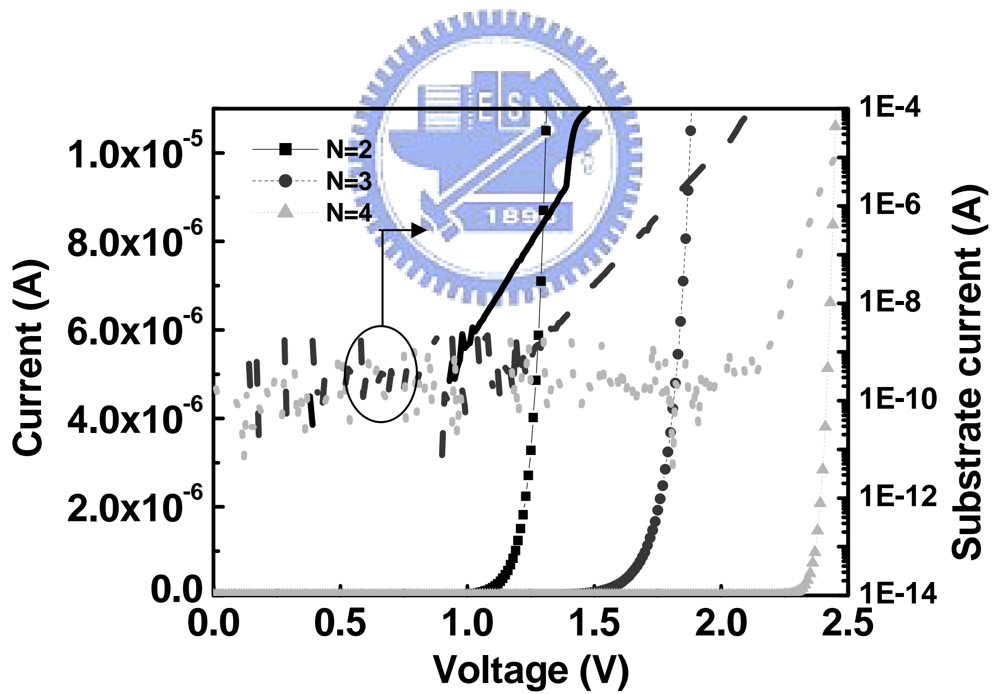


Fig. 4.10 The DC characteristics of LLCDS2 at 25°C.

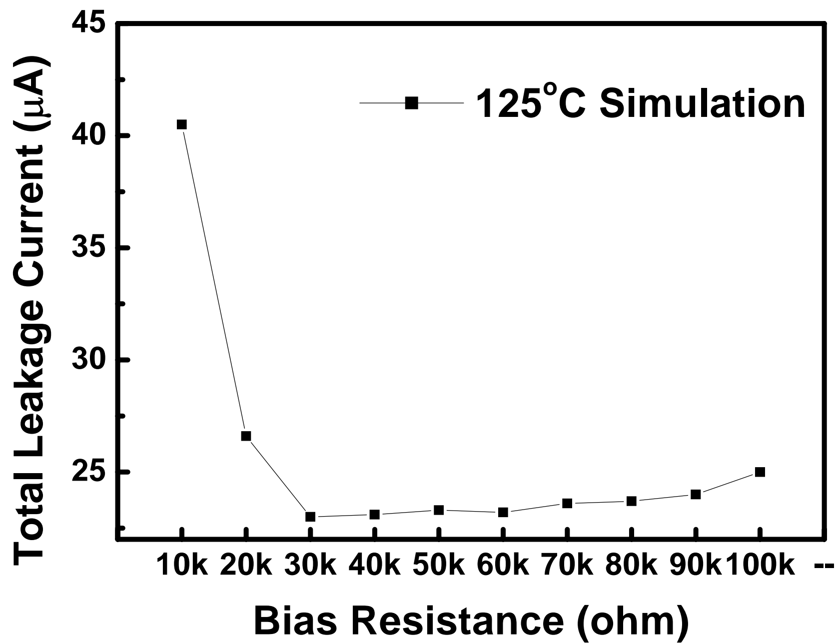


Fig. 4.11 The simulation result of the relationship between bias resistance (R) and total leakage current of LLCDS with diode number of N=4 and bias condition of VDD=1.8V, at the temperatures of 125°C.

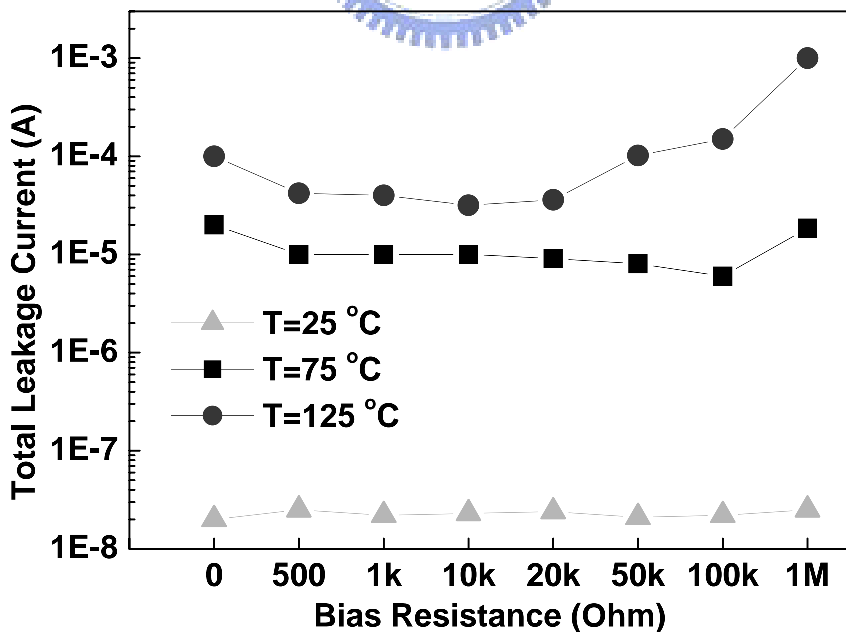


Fig. 4.12 The relationship between bias resistance (R) and total leakage current of LLCDS with diode number of N=4 and bias condition of VDD=1.8V, measured at the temperatures of 25°C, 75°C, and 125°C, respectively.

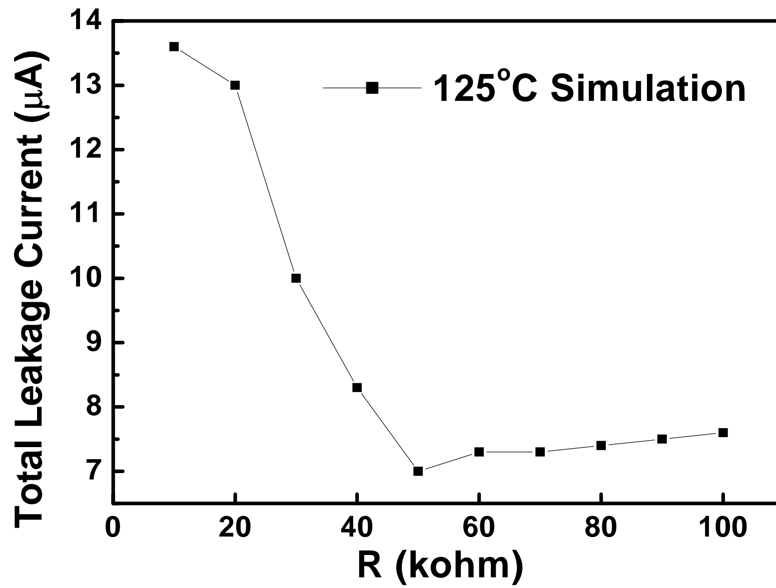


Fig. 4.13 The simulation result of the relationship between bias resistance (R) and total leakage current of LLCDS2 with diode number of N=4 and bias condition of VDD=1.8V, at the temperatures of 125°C.

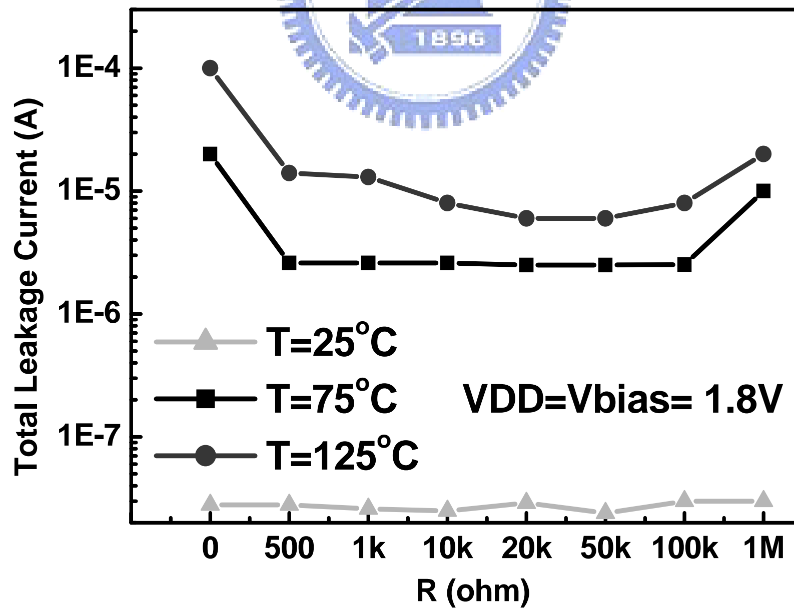


Fig. 4.14 The relationship between bias resistance (R) and total leakage current of LLCDS2 with diode number of N=4 and bias condition of VDD=1.8V, measured at the temperatures of 25°C, 75°C, and 125°C, respectively.

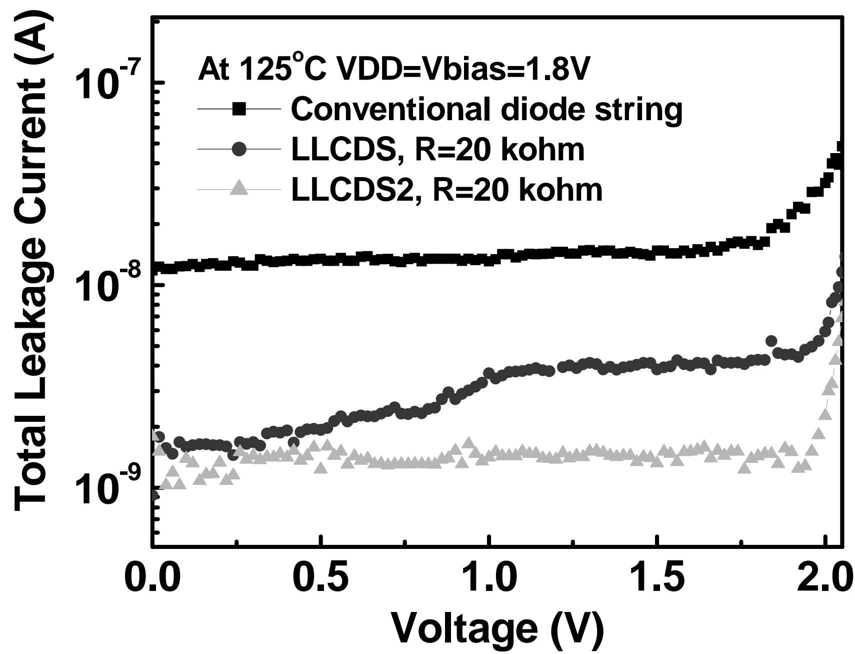


Fig. 4.15 The total leakage current of the conventional diode string, LLCDS, and LLCDS2 under 125°C for N=4 and R=10 kohm.

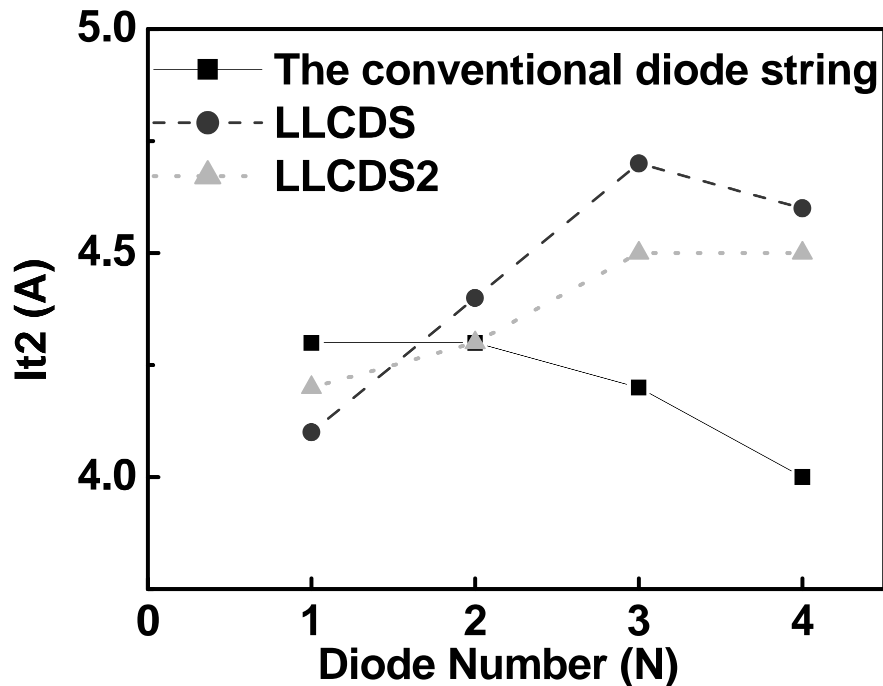


Fig. 4.16 The dependence of secondary breakdown current (It2) of the conventional diode string, LLCDS and LLCDS2 on the diode number (N) in series.

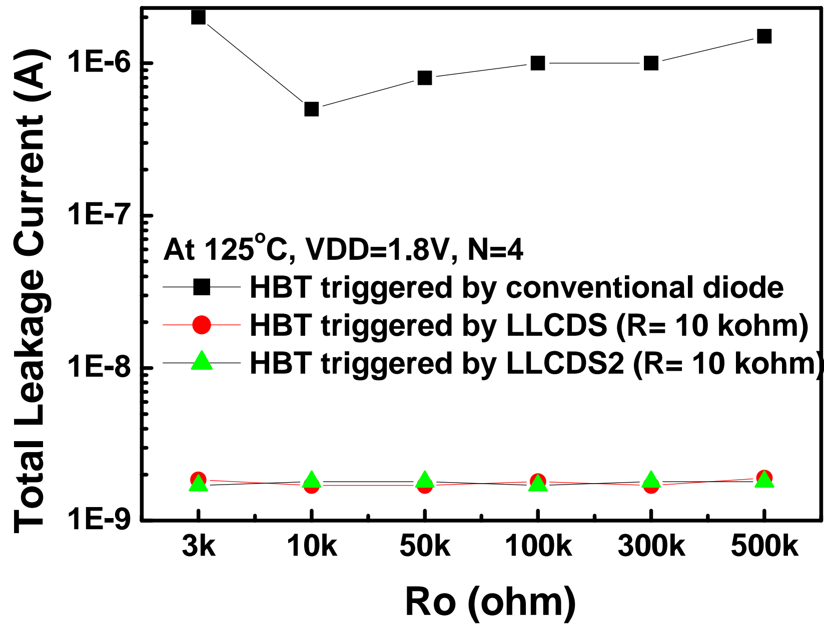


Fig. 4.17 The relationship between Ro and total leakage current of the HBT triggered by conventional diode string , HBT triggered by LLCDS, and HBT triggered by LLCDS2 at bias resistance (R) = 10 kohm under diode number of N=4 and bias condition of VDD=1.8V, measured at the temperatures of 125°C.

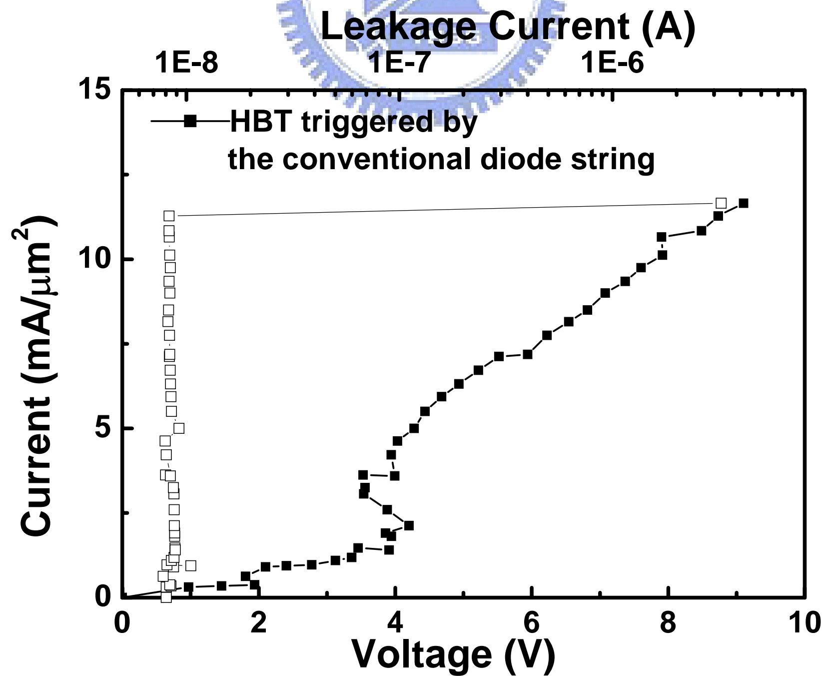


Fig. 4.18 The TLP I-V curve of the HBT triggered by conventional diode string for N=4, VDD=1.8V, and R=Ro=10 kohm.

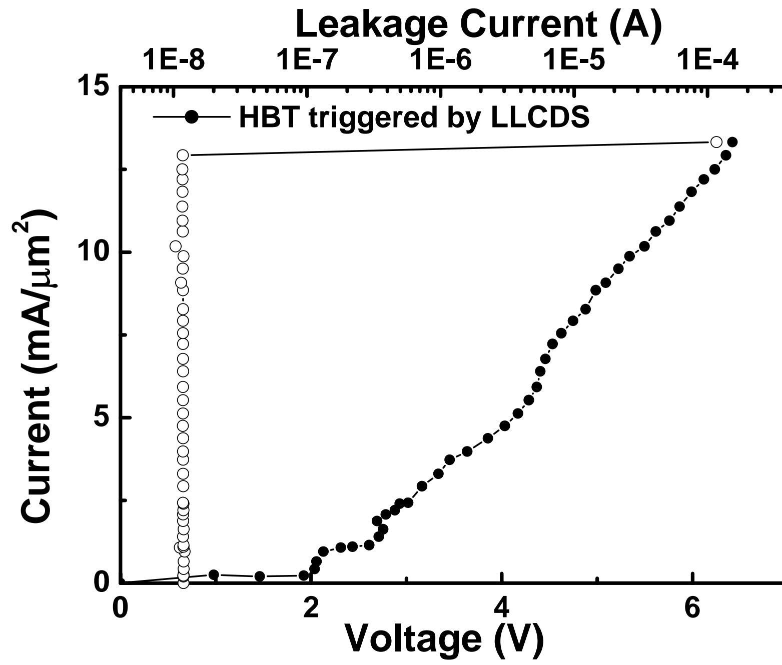


Fig. 4.19 The TLP I-V curve of the HBT triggered by LLCDS for N=4, VDD=1.8V, and R=Ro=10 kohm.

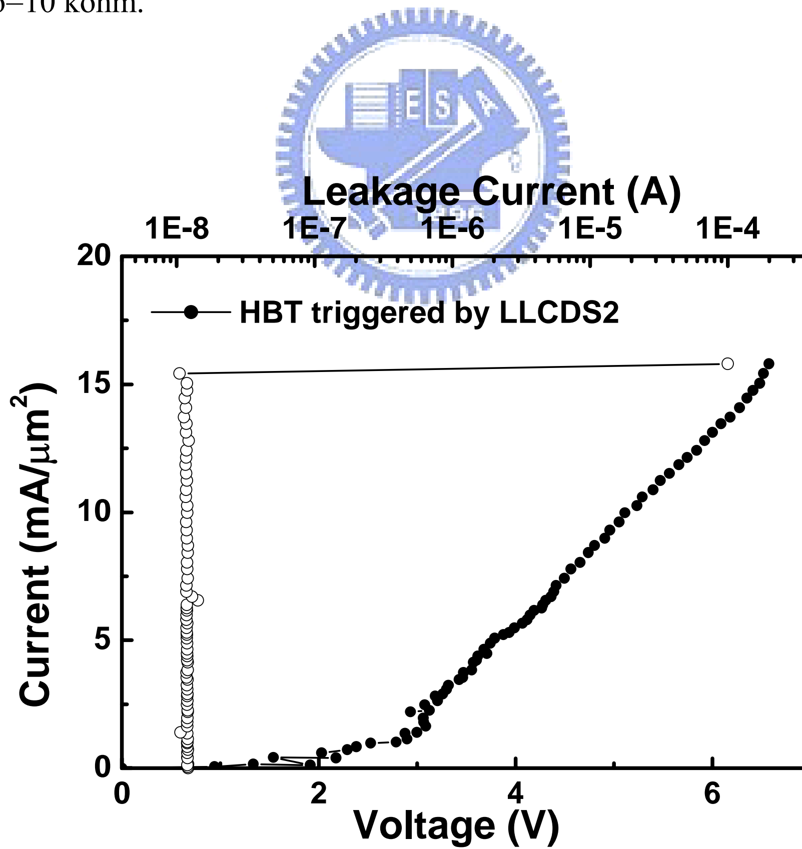


Fig. 4.20 The TLP I-V curve of the HBT triggered by LLCDS2 for N=4, VDD=1.8V, and R=Ro=10 kohm.

TABLE 4.1

Parameters of devices used in the SPICE simulation

	β	Is (Amp)	D_p	D_E	W (nm)	η
Parasitic bipolar	20	8.88e-18	0.989	1.22	30.2	
HBT bipolar	393.3	5.93e-19	0.485	2	7.6	
Diode		1.7e-13				1.04

TABLE 4.2

Parameters of devices measured from the experimental results at 25°C

	β	Is(Amp)	η
Parasitic bipolar	20		
HBT bipolar	360		
Diode		1.1e-12	1.47

Chapter 5

Summary and Future Works

5.1 SUMMARY

In chapter 2, the characteristics of diodes with different structures in the SiGe BiCMOS process have been investigated. A high ESD robustness can be achieved for the diodes under forward-biased condition. The ESD robustness of SiGe hetrojunction bipolar transistor in the SiGe BiCMOS process has been also characterized. If the emitter width of SiGe HBT is fixed at 0.45 μm, the order of ESD robustness is: LV SiGe HBT = HV SiGe HBT < HS SiGe HBT. However, when the emitter width of SiGe HBT is fixed at 1.5 μm, the order of ESD robustness is: LV SiGe HBT > HS SiGe HBT > HV SiGe HBT. With the proper layout parameters, SiGe HBT can perform double ESD robustness than that of NMOS device in the SiGe BiCMOS process.

In chapter 3, a new design on the diode string in 0.18-μm SiGe BiCMOS process has been proposed and verified. From the experimental results, the total blocking voltage of the diode string can be effectively increased by an extra bias to the deep N-well through a bias resistance. Although the additional extra bias will cause some current into the diode string, a bias resistance can minimize the overall leakage current of the diode string**.** Optimization design on the bias resistance and circuit implementation are studied and verified in detail in chapter 4.

In chapter 4, although the additional extra bias may cause leakage current into

LLCDS, the overall leakage current of LLCDS can be minimized by a bias resistance and the total leakage current can be effectively reduced as compared to that of the conventional diode string. This new proposed diode string is very suitable for applying in the power-rail ESD clamp circuit and the ESD connection cell between the separated power lines.

5.2 FUTURE WORKS

In this thesis, the diode strings as the power-rail ESD clamp circuit are developed in SiGe process with low leakage current and high ESD robustness. Because the value of resistance affects the work region of the parasitic BJT, using different values of resistance to optimize the leakage current can be studied in the future. The ESD protection circuit should not interfere with the internal circuits during normal circuit operating condition, while it can provide effective ESD protection to the internal circuit under ESD stress condition.

REFERENCES

[1] S. Voldman, N. Schmidt, R. Johnson, L. Lanzerotti, A. Joseph, C. Brennan, J. Dunn, D. Harame, P. Juliano, E. Rosenbaum, and B. Meyerson, "Electrostatic discharge characterization of epitaxial base silicon germanium heterojunction bipolar transistors," in *Proc. of EOS/ESD Symp*., 2000, pp. 239-251.

[2] S. Voldman, A. Botula, D. T. Hui, and P. A. Juliano, "Silicon germanium heterojunction bipolar transistor ESD power clamps and the Johnson limit," in *Proc. of EOS/ESD Symp*., 2001, pp. 326-336.

[3] S. Voldman, "Variable-trigger voltage ESD power clamps for mixed voltage applications using a 120 GHz/100 GHz (ft/f_{MAX}) silicon germanium heterojunction bipolar transistor with carbon incorporation," in *Proc. of EOS/ESD Symp*., 2002, pp. 52-61.

[4] V. Vashchenko and P. hopper, "Simulation of Si-Ge BiCMOS ESD structures operation including spatial current instability mode," in *Proc. of IEEE Int. Conf. on Microelectronics*, vol. 2, 2002, pp. 745-748.

[5] V. D. Heyn, N. M Iyer, G. Groeseneken, K. Reynders, and P. Moens, "Effect of the n+ sinker in self-triggereing bipolar ESD protection structures," in *Proc. of EOS/ESD Symp*., 2002, pp. 274-280.

[6] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, "ESD protection design for 900-MHz RF receiver with 8-kV HBM ESD robustness," in *Digest of IEEE RFIC Symp.*, 2002, pp. 427-430.

[7] M.-D. Ker and C.-M. Lee, "Interference of ESD protection diodes on RF performance in giga-Hz RF circuits," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, vol. 1, 2003, pp. 297-300.

[8] T.J. Maloney and N.Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. of EOS/ESD Symp*., 1985, pp. 49-54.

[9] J. Barth, J. Richner, K. Verhaege, and L. G. Henry, "TLP calibration, correlation, standards, and new techniques," in *Proc. of EOS/ESD Symp.* , 2000, pp. 85-96.

[10] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuit for submicron CMOS VLSI," *IEEE Trans. on Electron Devices*, vol. 46, pp. 173-183, 1999.

[11] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. on VLSI Systems*, vol. 4, no. 3, pp. 307-321, 1996.

[12] M.-D. Ker, T.-Y. Chen, and C.-Y. Wu, "ESD protection design in a 0.18-µm salicide CMOS technology by using substrate-triggered technique," in *Proc. of IEEE Int. Symp. on Circuits and Systems*, vol. 4, 2001, pp. 754-757.

[13] S. Dabral, R. Aslett, and T. Maloney, “Designing on-chip power supply coupling diodes for ESD protection and noise immunity,” in *Proc. of EOS/ESD Symp*., 1993, pp. 239-249.

[14] T. Maloney and S. Dabral, “Novel clamp circuits for IC power supply protection,” in *Proc. of EOS/ESD Symp*., 1995, pp. 1-12.

[15] T. Maloney, “Electrostatic discharge protection circuits using biased and terminated PNP transistor chains,” U.S. patent 5,530,612, June 1996.

[16] S. Voldman and G. Gerosa, “Mixed-voltage interface ESD protection circuits for advanced microprocessors in shallow trench and LOCOS isolation CMOS technologies,” in *IEDM Tech. Dig*., 1994, pp. 277-280.

[17] M.-D. Ker and W.-Y. Lo, “Design on the low-leakage diode string for using in the power-rail ESD clamp circuits in 0.35-µm silicided CMOS process,” *IEEE J. of Solid-State Circuits*, vol. 35, pp. 601-611, April 2000.

[18] S.-S. Chen, T.-Y. Chen, T.-H. Tang, J.-L. Su, T.-M. Shen, and J.-K. Chen, “Low-leakage diode string designs using triple-well technologies for RF-ESD applications,” *IEEE Electron Device Letters,* vol. 24, pp. 595-597, Sept. 2003.

[19] S.-S. Chen, T.-Y. Chen, T.-H. Tang, J.-K. Chen, and C.-H. Chou, “Characteristics of low-leakage deep-trench diode for ESD protection design in 0.18-µm SiGe BiCMOS process,” *IEEE Trans. Electron Devices*, vol. 50, pp. 1683-1689, July 2003.

[20] M.-D. Ker, T.-Y. Chen, and C.-Y. Chang, “ESD protection for CMOS RF integrated circuits,” in *Proc. of EOS/ESD Symp*., 2001, pp.346-354.

[21] S. Voldman and E. Gebreselasie, “Low-Voltage Diode-Configured SiGe:C HBT Triggered ESD Power Clamps Using a Raised Extrinsic Base 200/285 GHz (fT/fMAX) SiGe:C HBT Device ESD protection for CMOS RF integrated circuits,” in *Proc. of EOS/ESD Symp*., 2004, pp.57-66.

簡歷

姓　　名：吳偉琳

學　　歷：

新竹市實驗高級中學	(85 年 9 月~87 年 6 月)
國立交通大學電子物理學系	(88 年 9 月~92 年 6 月)
國立交通大學電子研究所碩士班	(92 年 9 月~94 年 4 月)

PUBLICATION LIST

[1] Ming-Dou Ker, Woei-Lin Wu, and Chyh-Yih Chang, "Characterization on ESD devices with test structures in Silicon Germanium BiCMOS process," *International Conference on Microelectronic Test Structures (ICMTS)*, 2003, pp. 7-12.

[2] Woei-Lin Wu, Chyh-Yih Chang, and Ming-Dou Ker, "High-Current characteristics of ESD devices in 0.35-mm Silicon Germanium RF BiCMOS process," in *Proc. of Taiwan ESD conference*, 2003, pp.157-162.

[3] Woei-Lin Wu and Ming-Dou Ker, "Design on Diode String to Minimize Leakage Current for ESD Protection in 0.18-μm BiCMOS SiGe Process," in *Proc. of Taiwan ESD conference*, 2004, pp.72-76.

[4] Ming-Dou Ker and Woei-Lin Wu, "ESD Protection Design with the Low-Leakage-Current Diode String for RF Circuits in BiCMOS SiGe Process," accepted by *EOS/ESD Symp.*, 2005.