國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

氟摻雜對二氧化鉿堆疊式閘極 P 型金氧半場效電晶體其可靠性的影響

Effects of Fluorine Incorporation on the Reliability Issues of pMOSFETs with HfO_2/SiON Gate Stack

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摘要

本論文中，我們於源極/汲極摻雜前，先加入氟摻雜，使氟原子在後續的高溫摻雜活化過程中，擴散至通道和閘極介電層，以形成氟併入。藉此，我們深入探討氟對二氧化鉿/氮氧化矽閘極之P型金氧半場效電晶體可靠性的影響。我們發現，導入氟對元件之基本特性，並無明顯改變；但於固定電壓應力(CVS)和負偏壓-溫度應力(NBTS)量測時，有氟併入的元件具有較低的界面狀態產生、和較少的電荷捕捉，而明顯改善元件的穩定性和可靠性。

其次，我們探討電漿效應對二氧化鉿/氮氧化矽閘極之P型金氧半場效

電晶體與負偏壓溫度不穩定效應的關連性、和氟併入對其影響。經由電荷泵浦電流量測，可發現不論在負偏壓-溫度應力(NBTS)前後，界面狀態密度均隨天線面積比而增加。因 NBTS 所導致的臨界電壓漂移，也因受到電漿充電損傷，而更形惡化，並造成嚴重的電洞缺陷。更重要的，電漿充電效應會使大天線面積比元件在二氧化鉿內的的電洞捕捉現象更為惡化，遠較界面產生的缺陷更嚴重。這和傳統以二氧化矽為閘極之 P 型金氧半場效電晶體，其惡化主因為電子捕捉，迥異其趣。利用氟併入，可有效增加對電漿充電損傷的免疫，因而降低具有大天線面積比元件在 NBTS 時的嚴重電洞捕捉現象。

Effects of Fluorine Incorporation on the Reliability Issues of pMOSFETs with HfO_2/SiON Gate Stack

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Abstract

In this work, F was incorporated before the source/drain implant step, which was subsequently diffused into the gate stack during later dopant activation. Effects of fluorine (F) on the reliabilities of pMOSFETs with HfO_2/SiON gate stack have been thoroughly studied. We found that F introduction only negligibly impacts the fundamental electrical properties of the fabricated transistors. In addition, under constant voltage stress (CVS) and negative bias temperature stress (NBTS), lower generation rates of interface states and charge trapping are observed for devices with F incorporation, thus enhances high-k devices' stability and reliability.

Next, effects of plasma charging and fluorine incorporation on the NBTI of p-channel MOSFETs with HfO_2/SiON gate stack were explored in this work. From charge pumping measurements, we confirm that the interface-state density is increased for devices with large antenna ratio, both before and after the BTS. It is clearly shown that the threshold voltage shift during negative bias-temperature stressing (NBTS) is deteriorated by plasma charging damage, causing severe hole traps. More importantly, we also found that hole trappings are aggravated in HfO_2 film as compared to interface trap generation by plasma charging, even on virgin devices with large antenna area ratios prior to negative BTS. This result is different from that observed in traditional pMOSFETs with SiO_2 gate dielectric where electron trapping is dominant. Fluorine incorporation would effectively improve plasma charging immunity, thus reducing the severe hole trapping under NBTS for devices with large antenna area ratios.

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Contents

Table Captions

Figure Captions

Chapter 1
Introduction

1-1 Backgrounds and Motivation

Aggressive gate insulator scaling in CMOS devices leads to excessive gate leakage and device reliability problems. Consequently, alternative gate insulators with higher permittivity than SiO_2 are currently widely investigated for the future generation of MOS transistors. The use of dielectric layers with higher electrical permittivity should allow us to use physically thicker films with the same electrical capacitance than ultra-thin SiO_2, and one would thus expect to reduce the leakage current and improve the reliability of the gate dielectric layer.

The aggressive down scaling of the CMOS technology will require high-k gate dielectrics to meet the specifications in ITRS (see Table 1-1) [1] in terms of sufficiently low gate leakage coupled with thin enough (<1nm) equivalent oxide thickness. Among the high-k dielectrics being studied, HfO_2 appears to be the most promising one due to its relatively high dielectric constant (～25) as compared to Si_3N_4 and Al_2O_3, its relatively high free energy of reaction with Si (47.6 Kcal/mol at 727 ^oC) as compared to TiO_2 and Ta_2O_5, wide band gap (～5.8 eV), and suitable tunneling barrier heights for both electron and holes (＞1 eV). Notwithstanding, there are still a number of pending issues, including channel mobility degradation, large number of fixed charges and charge traps, and threshold voltage instability

that need to be tackled before its induction to mass production. For example, people are working diligently to effectively eliminate the threshold voltage instability by reducing the relatively high trap density presented in the bulk of high-k dielectric and high interface trap density at the interface of high-k/interfacial layer/Si stack structure.

Numerous literatures have been published regarding methods to incorporate nitrogen [2-3] or Si [4-5] into Hf-based films/stack in order to improve the film quality. However, to the best of our knowledge, there are no related reports on the influence of fluorine incorporation on HfO_2 gate dielectric. In this work, fluorine is incorporated into HfO_2 gate stack by fluorine implantation into the source/drain regions, and its impacts on the pMOSFETs reliabilities are studied. It was clearly seen that the degradation is improved in the F-incorporated samples. Moreover, since few studies [6] have been done on the area of plasma effects on HfO_2 gate stack, we have performed a systematic study, and found that higher area antenna ratio will result in more severe degradation. More importantly, we also found that charging damage in devices with HfO_2/SiON can be effectively improved by fluorine implantation. We believe it has the potential to become an industrial standard if MOCVD HfO_2 is the final choice of future dielectric for the ULSI industry.

1-2 Organization of the Thesis

To fully understand the effects of fluorine incorporation on pMOSFETs with HfO_2/SiON gate stack, systematic experiments and measurements were performed in this study. In addition to this chapter that is dedicated to a brief introduction and historical review, this thesis is organized as follows:

In Chapter 2, we describe the process steps for fabricating test devices with HfO_2/SiON gate stack. Some basic electrical properties such as the components in the gate leakage current and their mechanisms, and some reliability issues such as constant voltage stress (CVS), negative bias temperature stress (NBTS) and dynamic AC stress of the devices with and without fluorine are explored and discussed.

In Chapter 3, we present the results on evaluating the plasma charging damage of the devices. We use the NBTI characterization as a sensitive method for characterizing the antenna effects in devices with HfO_2/SiON, which is particularly attractive in light of the fact that conventional indicators are becoming inadequate as oxide is scaled down. The effect of fluorine incorporation on plasma charging damage is also investigated.

Chapter 4 concludes this work by summarizing the major results and important findings we have obtained. Some suggestions for future work on this topic is also given.

Chapter 2

Impacts of Fluorine Incorporation on the Reliability of pMOSFETs with HfO_2/SiON Gate Stack

2-1 Introduction

Recently, negative-bias-temperature instability (NBTI) is recognized as a major reliability issue in scaled pMOSFETs [7]–[8]. During negative bias stress at elevated temperatures, defects can be generated in the device, which in turn cause threshold voltage shifts and drive current reductions. The device parameter degradations can lead to circuit failures, both for analog and digital applications.

Unlike SiO_2 films, high-k films are more susceptible to charge trapping. Charge trapping causes the threshold voltage to shift with stressing time, and is therefore an important transistor reliability issue. Two mechanisms: trapping effect and reaction-diffusion model compete in NBTI for pMOSFETs with high-k gate dielectric.

Fluorine is known to worsen boron penetration in PMOS devices employing p^+ polysilicon gate. As such, fluorine incorporation has been generally regarded as undesirable for PMOS device applications. Nevertheless, an appropriate fluorine implant will enhance oxide reliability.

Huard *et al*. has demonstrated that the use of BF_2 implants, in lieu of B implants, for the

S/D and poly gate for the traditional p^+-gated pMOSFETs with SiO_2 dielectric results in lower device degradation. Fluorine was found to improve the gate oxide reliability. This result has been confirmed by deliberate fluorine implantation, in addition to BF_2 doping, which also shows alleviated NBTI degradation [9].

In this thesis, effects of fluorine (F) on the reliabilities of pMOSFETs with HfO_2/SiON gate stack have been studied. Boron atoms, required to achieve p^+-doped gate layers, have raised some concerns about their possible roles in the NBTI degradation. In this work, F was incorporated during the source/drain implant step, which was subsequently diffused into the gate stack during later dopant activation. Charge pumping measurements were extensively used to investigate the rootcause of the BTI degradation. It will be shown that all reliabilities such as CVS, NBTI and AC dynamic stress are improved by fluorine incorporation.

2-2 Experimental Procedure

In this thesis, local oxidation of silicon (LOCOS) process was used for device isolation. MOS transistors was fabricated on 6-inch p-type Si with (1 0 0)-orientation. After removing the 300Å sacrificial oxide, RCA clean was performed with HF-dip last, and immediately followed by a conventional RTA at 700 ^oC in N_2O ambient to form about 0.7nm interfacial oxynitride layer (SiON). Afterwards, HfO_2 film of approximately 3nm was deposited by atomic vapor deposition (AVD^{TM}) in an AIXTRON Tricent® system at a substrate temperature of 500 ^oC,

followed by 700 ^{o}C N_2 RTA for 20 sec in order to improve the film quality. The MOCVD system was designed for 8-inch wafers, so a 6-inch quartz was used as wafer carrier for film deposition. The physical thickness of the SiON and HfO_2 films was measured by optical n&k analyzer. A 200nm undoped polycrystalline silicon (poly-Si) layer was directly deposited by low pressure chemical vapor deposition (LPCVD) on top of the HfO_2 films. After the gate electrode was patterned by lithography and etching processing, some samples received the fluorine (F, 2×10^{15} cm^{-2}) ion implantation into source/drain region without removing the photoresist on the gate electrode. This was deliberately done in order to avoid the complication of enhanced boron penetration by F. All samples were then processed to form source/drain regions by B implantation, with the dopants activated at 950 ^{o}C by rapid thermal annealing (RTA) for 20 sec in an N_2 atmosphere. It should be noted that the activation thermal budget also served to diffuse the F spices into the gate stack and channel region. After passivation, contact holes formation, Al metallization and patterning were performed. Finally, all devices received the forming gas annealing at 400 ^{o}C for 30 minutes.

Current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics were evaluated by an HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate dielectric was obtained from high frequency (100 KHz) capacitance-voltage (*C-V*) curve at strong inversion without considering quantum effect. The key process flow is summarized in Fig. 2-1.

In this thesis, the interface trap density (N_{it}) was analyzed using the charging pumping technique [10]. Square-wave waveforms (f = 1MHz) were applied to the gate, and the base voltage was varied from inversion to accumulation, while keeping the pulse amplitude at 1.2 V. Fig. 2-2 shows the configuration of measurement setup used in our charge pumping experiment. A MOSFET with gate area A_G gives the charge pumping current as:

$$I_{cp} = qA_G f N_{it,} \qquad (2\text{-}1)$$

Interface trap density could be extracted from the above equation.

The total trap density increase, $\triangle N_{tot}$, which includes the increase of interface trap density and bulk trap density, was calculated from $\triangle V_{th}$ by assuming that the charge was trapped at the interface between the dielectric and the substrate.

$$\triangle N_{tot} = C\triangle V_{th}/qA_G \qquad (2\text{-}2)$$

2-3 Results and Discussion

2-3-1 Basic Electrical Properties of Devices

The *C-V* curves in Fig. 2-3 indicate a slight increase of EOT in F-incorporated sample. Fig. 2-4 (a) shows typical drain current and transconductance characteristics as a function of the gate voltage for the devices, both with and without F incorporation. The inset table shows the initial threshold voltage. I_d-V_g and G_m-V_g characteristics are almost identical between two devices. Fig. 2-4 (b) shows the cumulative probability of the threshold voltage (V_{th}) for the

fabricated devices. It can be found that the V_{th} distribution is not affected by the addition of F. Drain current in the saturation region is shown in Fig. 2-5. Fig. 2-6 illustrates the initial interface state density and subthreshold swing (S.S) of two samples. Output characteristics and initial interface state density are almost identical between two devices. Fig. 2-7 compares the gate leakage currents of the pMOSFETs with HfO_2/SiON gate stack under both inversion and accumulation modes. Gate leakage is similar between two devices. In short, it was found that all fundamental electrical properties, including the EOT, V_{th}, drive current, interface state density (N_{it}), swing, and gate leakage current are almost non-distinguishable between the two splits with and without F incorporation.

The carrier type involved in the leakage current through HfO_2/SiON dielectric layers have also been investigated for unstressed pMOSFETs, using the carrier separation method [11]. The contributing carriers of the gate leakage current can be separated into holes and electrons. Fig. 2-8 shows carrier separation results under the inversion region, and Fig. 2-9 shows carrier separation results under the accumulation region for p^+-gated pMOSFETs with HfO_2/SiON gate stack, both with and without F-incorporation. It is found that the source/drain current I_{SD} dominates the leakage current under inversion region, and the substrate current I_B dominates the leakage current under accumulation region. This indicates holes from S/D that tunnel through gate dielectric is the dominant component of conduction mechanism under inversion region, while electrons from gate electrode that tunnel through gate dielectric is the

dominant component of conduction mechanism under accumulation region.

This could be explained by band-diagrams shown in Fig. 2-10 (a) and carrier separation experiment shown in Fig. 2-10 (b). The substrate current I_B corresponds to the electron current form the gate, while the source/drain current I_{SD} corresponds to the hole current from Si substrate under inversion region. Electrons supply from the gate conduction band in pMOSFETs is limited by the generation rate of minority electrons in p^+ gate. On the other hand, the probability of carriers from S/D that tunnel through gate dielectric is strongly affected by tunneling distance and barrier height [12]. Due to the asymmetry of the HfO_2/SiON band structure, it is more difficult for electrons to tunnel through gate dielectric, as compared to holes. Consequently, the current through the gate stack should be smaller for electrons, as compared to holes. In pMOSFETs, hole current from the channel is the predominant injection current under stressing. The leakage component under accumulation region could also be explained by band-diagrams shown in Fig. 2-11 (a), and the current component flow in carrier separation experiment is shown in Fig. 2-11 (b).

In Figs. 2-12 (a) and (b), the gate current I_g as a function of V_g for the HfO_2/SiON layer is measured from room temperature up to 125 ^oC, both under inversion region and accumulation region for two samples. The current is temperature dependent that increases with increasing temperature. This implies that the conduction mechanism of gate current is trap-related, i.e., trap-assisted tunneling (TAT), Frenkel-Poole, etc.

The gate leakage current for devices with HfO_2/SiON gate stack is composed of two types of carriers, i.e., hole current and electron current. To determine the conduction process in the HfO_2/SiON dielectric, Frenkel-Poole (F-P) plots are fitted for hole current and electron current, respectively, for both samples.

The current from Frenkel-Poole emission is of the form:

$$I \propto V \exp\left(\frac{2a\sqrt{V}}{T} - \frac{q\phi_B}{k_B T}\right) \qquad (2\text{-}3)$$

$$J = B * E_{ox} \exp\left(\frac{-q(\phi_B - \sqrt{qE_{ox}/\pi\varepsilon_{ins}\varepsilon_0})}{k_B T}\right) \qquad (2\text{-}4)$$

$$\ln\left(\frac{J}{E_{ox}}\right) = \frac{q\sqrt{q/\pi\varepsilon_{ins}\varepsilon_0}}{k_B T}\sqrt{E_{ox}} - \frac{q\phi_B}{k_B T} \qquad (2\text{-}5)$$

$\Rightarrow$ Intercept gives the Barrier height $\left(-\frac{q\phi_B}{k_B T}\right)$

where B is a constant in terms of the trapping density in the HfO_2 film, φ_B is the barrier height, E_{ox} is the electric field in HfO_2 film, ε_0 is the free space permittivity, ε_{ins} is HfO_2 dielectric constant, k_B is Boltzmann constant, and T is the temperature measured in Kelvin.

As shown in Fig. 2-13 and Fig. 2-14, under inversion region, excellent linearity for each current characteristic has been observed for both samples. This tendency indicates that both samples exhibit the Frenkel-Poole conduction mechanism for the gate leakage current. Both the electron and hole conduction mechanisms are the same, and the result agrees well with the F-P conduction mechanism. Barrier height φ_B and dielectric constant ε_{HfO2} of HfO_2/SiON can be calculated. The ε_{HfO2} value is found to be $\sim$14.84 and $\sim$14.7 for the control and F-incorporated samples, respectively.

The φ_B for the hole traps in the control sample and F-incorporated sample is about 0.98 eV and 1 eV, respectively. On the other hand, for electron traps, the φ_B of the control sample and F-incorporated sample are about 1.16 eV and 1.17 eV, respectively. The φ_B to be discussed in this chapter is the "effective" value that is representative of the HfO_2/SiON gate stack [13]. We consider the case when the injected carriers flow across HfO_2/SiON by hopping via the trap sites with energy barrier φ_B, whose value depends on the fabrication process [14]. These experimental results indicate that the energy level for traps in the control sample is similar to that of the F-incorporated sample, and the energy barrier φ_B for holes is clearly lower than that for electrons by about 0.2 eV in both samples.

For material analysis, transmission electron microscopy (TEM) was used to determine the exact thickness and identify the interface situation between HfO_2 and Si substrate as well as interface between HfO_2 and gate electrode. Fig. 2-15 shows HRTEM images of the device with HfO_2/SiON gate stack. We can see that owing to RTA treatment, interfacial layer thickness becomes thicker by about 11.4Å, and must be carefully controlled to maintain a thin EOT. From the HRTEM, we can also found that the estimated value of dielectric constant for HfO_2 is about 11.4.

2-3-2 Appropriate Measurement for Evaluating High-K Gate Dielectric

Fig. 2-16 and Fig. 2-17 illustrate I_d-V_g characteristics for the control and F-incorporated

samples, respectively. First, we measured Forward-1 (i.e., 0 V ~ −2 V) as the Step 1, then measured Reverse-1 (i.e., −2 V ~ 0 V) as the Step 2 of the first cycle, and repeated this sweeping cycle again. It can be seen that V_{th} shifts toward negative voltage after the first cycle, which indicates that net positive charges are trapped in the gate dielectric layer during measurements, and also V_{th} recovers during the second cycle without applying a small stress. V_{th} does not fully recover to its initial value, and some positive charges still remain in the gate dielectric. These behaviors indicate that both fast trapping and de-trapping charges are occurring in the HfO_2 during measurements.

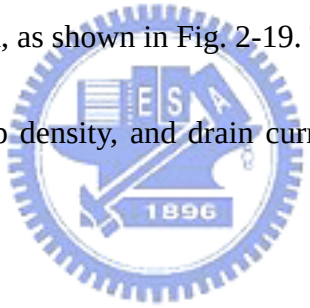
There are two noticeable features for both samples when applying the additional small stress. First, the fact that Forwad-2 I_d-V_g in Cycle 2 matches Forwad-1 I_d-V_g in Cycle 1 reveals that the unstable fast charges are successfully eliminated by using a small stress. This allows us to accurately estimate the result of the measurement. Secondly, the fact that V_{th} of Forward I_d-V_g for both cycles maintains the same value implies that using a small stress does not cause any extra damage to the gate stacks, nor does it affect device parameters. Fig. 2-18 shows a schematic illustration for the possible case of fast charging effects (FCE).

In order to reduce the unstable fast charge trapping and detrapping effects [15]-[19], a small positive voltage (e.g., 0.5 V) for several seconds was applied to detrap them before I_d-V_g and charge pumping measurements without causing any extra damage to the gate stacks. The purpose of this step is to more accurately estimate the density of slow traps without being

affected by the variation of interval between the stress and measurement. In order words, we will just focus on the slow traps in the gate stacks in this work.

2-3-3 NBTI of Control and Fluorine-Incorporated Devices

Negative bias temperature instability (NBTI) is an important reliability issue as it causes the threshold voltage to shift with electrical stressing. To evaluate device degradations due to the bias temperature (BT) stress, the gate electrode of the device was subjected to stress condition with negative bias (−3.5 V) varying from 25 ^{o}C to 125 ^{o}C, while the drain/source and substrate were all grounded, as shown in Fig. 2-19. The dependences of threshold voltage, interface trap density, bulk trap density, and drain current on stress time are investigated at various temperatures.



For both control and fluorine-incorporated devices, negligible change in S.S is observed under constant voltage stress at room temperature, as shown in Figs. 2-20 (a) and (b). This indicates that interface state generation plays no significant role, rather, charge trapping in the bulk dielectric is the primary mechanism leading to CVS issues in high-k dielectrics. V_{th} shift of the control sample is found to be slightly larger.

The threshold voltage shift ($\triangle V_{th}$) is measured with respect to the I_d-V_g curves shown in Fig. 2-21 (a) in linear scale and (b) in logarithm scale. The threshold voltage shifts toward negative gate voltage ($\triangle V_{th} < 0$), thus implying that net positive charges are trapped in the

gate dielectric layer as the device is stressed. It is clear that the F-incorporated sample always shows smaller $\triangle V_{th}$ than the control sample under different stress voltages. Fig. 2-21 (b) shows that V_{th} degradation obeys the power law [20]-[21],

$$\triangle V_{th}(t) = At^b \qquad (2\text{-}6)$$

and the exponential values of both samples at $V_g = -4$V (~0.12) are much larger than those of the devices at $V_g = -3.5$ V (about 0.03~0.04). This indicates that V_{th} degradation is more severe for the devices under larger constant voltage stressing. The exponential value is voltage dependent relative to bulk trap generation.

To further gain insights into the degradation mechanism during voltage stressing, the interface state generation, $\triangle N_{it}$,, and the increase of effective total trap density, $\triangle N_{tot}$, are plotted as a function of the stress time in Fig. 2-22 (a) and (b), respectively. Apparently, $\triangle N_{tot}$ (= $\triangle N_{it}$ +$\triangle N_{ot}$) is significantly larger than $\triangle N_{it}$, suggesting that the degradation under CVS is dominated by the charge trapping in the bulk of HfO_2 film, rather than the generation of interface states, irrespective of whether F is added or not. The instability of HfO_2/SiON gate stack is mainly determined by the bulk charge traps, contrast to that in the SiON gate stacks. In addition, the improvement in charge trapping is larger than that in interface generation for F-incorporated samples.

The degradation in drain current after CVS for the devices are shown and compared in Fig. 2-23. Due to larger V_{th} shift and interface state generation ($\triangle N_{it}$) of the control sample,

more severe drain current degradation is observed.

Fig. 2-24 shows that the F-implanted sample depicts lower degradation of (a) threshold voltage shift ($\triangle V_{th}$) and (b) interface trap density shift ($\triangle N_{it}$), as compared to the control sample, with scaling channel length. This reduction is mainly due to the fact that more fluorine is incorporated into the gate dielectric during dopant activation as the channel length becomes smaller, leading to a reduction of bulk traps density and interface traps density. Therefore, it is interesting to find that the impact for $\triangle V_{th}$ and $\triangle N_{it}$ increases as the channel length decreases. Since the diffusion distance of F atoms is constant, the ratio of diffusion distance divided by the channel length would be higher as the channel length decreases, and more F could become trapped. This indicates that the method of using fluorine implant into S/D is feasible for future CMOS technology. The improvement may be due to fluorine atoms, similar to nitrogen atoms, form complexes at the interface and dielectric, which reduce the total number of available Si-H bonds, and passivate the bulk trap, leading to less CVS degradation.

It can be seen that I_d-V_g curves shift toward more negative voltage with increasing stress time at 125 ^{o}C for both the control and fluorine incorporated devices, as shown in Figs. 2-25 (a) and (b), respectively. Further, V_{th} shift of the control sample is slightly larger. There is observable change in S.S at high temperature, compared to that at room temperature, indicating that $\triangle N_{it}$ increases with increasing temperature. This phenomenon is consistent

with our results as shown in Fig. 2-26 (a) and (b) for both samples. It can be seen that fluorine-incorporated devices always show smaller $\triangle N_{it}$ than the control devices at all temperatures.

Fig. 2-27 (a) compares the NBT-stress-time dependence of threshold voltage shift for the HfO_2/SiON gate stack with and without F incorporation. A significantly smaller V_{th} shift is observed for the F-incorporated sample under the BT stress, $V_g = -3.5$ V at 25 °C and 125 °C. Such phenomena can be attributed to fluorine incorporation into the gate dielectric. Fig. 2-27 (b) shows that the exponential values of both samples at 125 °C (about 0.13~0.14) are much larger than those of the devices at 25 °C (about 0.03~0.04). This indicates that the V_{th} degradation could be more severe for the devices under BT stress at high temperature [22]. The exponential value is temperature dependent relative to bulk trap generation.

Figs. 2-28 (a) and (b) show $\triangle N_{it}$ and $\triangle N_{tot}$ as a function of time during NBTI for both devices measured at different temperatures. It is found that for both devices, V_{th} degradation during NBTI stressing is primarily caused by the charge trapping in bulk HfO_2, rather than the interfacial degradation. Drain current degradation for F-incorporated device is shown in Fig. 2-29. All results are consistent with the effectiveness of fluorine incorporation in alleviating the BT instability. The major degradation of NBTI is caused by the positive charge trapping in the films rather than the interface generation, suggesting that the positive charge trapping is not completely caused by the H^+ capturing. Hence, it can be concluded that, except for

positive charge caused by H species, a large amount of extra trapping centers is also present in the HfO_2/SiON gate stack. F atoms seem to effectively decorate these trapping centers, leading to less degradation.

Note that the activation energies of NBT degradation for fluorine incorporated HfO_2/SiON gate stack are identical with those without fluorine incorporation, as shown in Figs. 2-30 (a) and (b). Specifically, the activation energies of $\triangle V_{th}$ and $\triangle N_{it}$ are 0.08 eV and 0.14 eV, respectively, for both devices. Note that the activation energy of $\triangle V_{th}$ is lower than that of $\triangle N_{it}$, indicating that V_{th} instability is not simply contributed by interface trap generation, but mainly comes from the more significant charge trapping in the bulk of high-k dielectric. Furthermore, it should be noted that both $\triangle V_{th}$ and $\triangle N_{it}$ are improved by fluorine incorporation, while maintaining almost identical activation energies.

2-3-4 AC Stressing

Most gate dielectric reliability stressing tests rely on DC stressing because of its simplicity. However, in actual CMOS circuit operation, AC gate bias with specific frequency and duty cycle is usually used. AC stress is thus more realistic, and can provide additional insights into the trapping dynamics. It has been reported that AC stressing of SiO_2 usually results in longer lifetime than DC stressing [23]-[24]. Fig. 2-31 illustrates the schematics of the measurement setup for threshold voltage instability testing under dynamic stress. During

the stress, AC square wave pulses from a pulse generator are applied to the gate through the switch; while the other three terminals are grounded. The sum of 'on-time' during the stress is defined as the total stress time in unipolar AC stress.

For different bias frequencies, cumulative 'on-time' under AC unipolar stress is defined as the 'stress time'. The duty cycle is fixed at 50% for all samples. While for different duty cycles, frequency is fixed at 10KHz for all the samples. Negligible variation in $\triangle N_{it}$ is observed with increasing frequency and decreasing duty cycle under AC stress for both samples, as shown in Fig. 2-32 and Fig. 2-33. As shown in Fig. 2-34 and Fig. 2-35, $\triangle V_{th}$ turns around and shifts toward positive gate voltage in AC stress for both samples. Figs. 2-36 (a) and (b) show that $\triangle N_{it}$ of the F-incorporated sample is smaller than that of the control sample under AC stress for any frequency or duty cycle. This is in agreement with the result in $\triangle N_{it}$ presented in DC stress. It is observed from Figs. 2-37 (a) and (b) that V_{th} degradation is strongly dependent on the frequency and duty cycle of the dynamic stress. V_{th} for both cases shift toward more positive gate voltage as frequency increases. Similar trend is observed as duty cycle decreases. $\triangle V_{th}$ for F-incorporated sample is lower than the control sample, irrespective of frequency and duty cycle. The film quality of fluorine incorporation is more robust under AC stress.

Since V_{th} degradation of PMOS is primarily caused by charge trapping in the HfO_2 film and shifts toward negative gate voltage under DC stress. The bulk traps of HfO_2 appears to be

the dominant factor in the threshold voltage instability of pMOSFETs with the HfO_2/SiON dielectric by trapping or detrapping charges during AC stress. This finding suggests that both hole trapping and electron trapping occur during DC stress, and hole trapping is dominant due to the fact that the hole current is larger than the electron current under inversion region from carrier separation experiments. Although holes do not have enough time to get trapped, electrons trapped during on-period result in a significant V_{th} shift toward positive gate voltage, and electron trapping is dominant under AC stress. Electrons are more likely to be trapped, compared to holes, because holes must first go through SiON before getting trapped in HfO_2 film. This observation could be explained by band diagram shown in Fig. 2-10 (a). Higher frequencies and lower duty cycles result in larger V_{th} shift toward positive gate voltage, and are considered to be due to the fact that holes can not follow the step of high frequency variation, and few hole charges get trapped during on-period in HfO_2 gate dielectric.

2-4 Summary

In this work, we find the exponential value of $\triangle N_{it}$ is about 0.23~0.25 for both samples either under CVS or NBTI. This value of $\triangle N_{it}$ is similar to that of traditional SiO_2 dielectric under stressing, while the exponential value of $\triangle V_{th}$ is voltage dependent and temperature dependent. As a result, we can confirm again that charge traps in the bulk of HfO_2/SiON gate stack are responsible for the instability. We can expect a continuous distribution of charge

trapping cross sections, instead of a discrete-value capture cross section, in HfO_2 high-k film [15]. A better interface is expected to help reduce V_{th} instability, therefore bulk traps need to be reduced.

The experimental results show that hole trapping is dominant in DC stress and electron trapping is dominant in AC stress. Bias frequency and duty cycle dependence under AC dynamic stress lead us to conclude that the bulk trap of HfO_2 is primarily responsible for changing $\triangle V_{th}$ polarity in HfO_2/SiON pMOSFETs.

Chapter 3

Improved Immunity against Plasma Charging Damage of pMOSFETs with HfO_2/SiON Gate Stack by Fluorine Incorporation

3-1 Introduction

Plasma processes have been known to cause gate oxide and MOSFET degradations. Many plasma processing steps, such as poly-silicon etching for transistor gate length definition [25]-[26], metal etching [27], and photo-resist ashing [28] are indispensable for wafer fabrication. With the scaling of the transistor gate length and gate oxide thickness, the gate edge damage and gate oxide damage could both become more serious by the poly-silicon etching. Meanwhile, it has been shown that metal etching and its subsequent resist ashing could induce serious plasma charging damages. With the fabrication of multi-level metal interconnect in ULSI circuits, repetitive exposures to plasma processes are unavoidable. Consequently, better understanding of plasma damage is essential to achieve highly reliable ULSI circuits.

To detect plasma process-induced damage (P^2ID), the typical test structure is a small area capacitor or transistor connected to a large conductive antenna receiver. Metal antenna structures attached to the gate electrode with various antenna area ratios (AAR) were used to

monitor the plasma charging damage. In conventional pMOSFETs with SiO_2 gate, severe charging damage could occur at the center, due to the non-uniform plasma generation caused by the gas injection mode of the asher.

In this chapter, HfO_2/SiON pMOSFETs with antenna structures are employed as the test devices. We also study the effects of fluorine incorporation on plasma charging damage. The HfO_2/SiON gate stack degradation due to the charging damage can be evaluated using constant voltage stress (CVS) and bias-temperature stress (BTS). Furthermore, more detailed information, such as the effects of antenna size, charging polarity and the device location on the wafer, is carefully examined. We for the first time demonstrate that F incorporation into HfO_2/SiON gate stack could strengthen the immunity against plasma charging damage [29].

3-2 Plasma Charging Damage in Control and Fluorine-Incorporated Samples

PMOS transistors with p^+ poly-Si gate were fabricated on 6-inch wafers. Metal antennas with various antenna ratios (AAR) were attached to the gate. The AAR is defined as the area ratio between the metal pad and the active device region. Schematic of a transistor with area antenna is shown in Fig. 3-1.

In our processing, after metal patterning, the remaining photo-resist layer was stripped off with O_2 plasma in a down-stream plasma asher, whose configuration and plasma potential

can be found in [30]. Previously, CHARM-2 wafer sensor was used to establish the potential distribution in the chamber. Highly negative and positive potential values were identified at the wafer center and edge, respectively, as shown in Fig. 3-2 (a) and Fig. 3-2 (b).

Fig. 3-3 (a) and Fig. 3-3 (b) compare the interface state density as function of device location on the wafer before and after H_2 sintering. The interface-state density of the antenna devices was also analyzed using the charge pumping technique. Fig. 3-4 (a) and Fig. 3-4 (b) show the results as function of device location on the wafer before and after H_2 sintering. It is interesting to find that the $|V_{th}|$ values for the control devices with AAR of 60K are larger than the other devices, irrespective of sintering. In Fig. 3-3 (b), it is seen that N_{it} is higher for the control devices with AAR of 60K. This indicates unambiguously that hole trapping is solely responsible for the observed high $|V_{th}|$ on fresh devices with large antenna, as shown in Fig. 3-4 (b). Both V_{th} and N_{it} of two devices are lower after sintering. Forming gas anneal effectively improves MOSFET characteristics. These can be attributed to improved interface quality and reduced bulk trap in HfO_2 film by H atoms.

Fig. 3-5 (a) and Fig. 3-5(b) display the cumulative probability of the threshold voltage (V_{th}) and interface trap density (N_{it}) for the fabricated devices located near the wafer center. Remarkably, the control devices with AAR of 60K depict larger $|V_{th}|$ and N_{it} values than their counterparts with F incorporation. Plasma charging damage would cause more charge trapping in HfO_2 film and more interface state density, resulting in larger $|V_{th}|$.

Output characteristics for the fresh devices with AAR of 1K and 60K, both with and without F incorporation are shown in Fig. 3-6. It is interesting to find that the drain current in the fresh devices is actually smaller for the control device with AAR of 60K. This is ascribed to a high $|V_{th}|$ for the fresh devices with a large antenna, implying that more hole trapping events occur after plasma processing. This result is different from the traditional PMOS transistor with SiO_2 gate and a larger antenna has a low $|V_{th}|$, implying that more electron trapping events occur during plasma processing. Moreover, all these results testify that the plasma antenna charging effect creates more hole traps in the HfO_2/SiON gate stack, and F incorporation can significantly reduce the impact of plasma charging effect.

3-3 Effects of Plasma Charging Damage on NBTI

Figs. 3-7 (a) and (b) show the time evolution of threshold voltage shift at 25 ^{o}C for devices with area antenna ratios (AAR) of either 1K or 60K, both with and without F incorporation, in linear scale and logarithm scale, respectively. All mesured devices were selected from the same die location on the wafer center. It should be noted that in Fig. 3-7 (a) V_{th} shift is larger for the control device with AAR of 60K, indicating that negative (i.e., wafer center) plasma charging could degrade the CVS. Fig. 3-7 (b) shows that V_{th} degradation obeys the power law and the exponential values of all devices at $V_g = -4$ V (about 0.1~0.13) are similar. Fig. 3-8 (a) and Fig. 3-8 (b) compare $\triangle N_{tot}$ and $\triangle N_{it}$ as function of time. It should be

noted that $\triangle N_{tot}$ was calculated from $\triangle V_{th}$ assuming that the charge was trapped at the interface between the dielectric and the substrate. $\triangle N_{tot}$ is about 1.5～2 order larger than $\triangle N_{it}$ for all devices, indicating that charge trapping in the bulk trap dominates threshold voltage shift. Apparently, the F incorporation is shown to be effective in suppressing $\triangle N_{tot}$ and $\triangle N_{it}$ on the devices with large antenna. The reductions in drain current after CVS for the devices are shown and compared in Fig. 3-9. Due to larger V_{th} shift caused by plasma charging effect, enhanced drain current degradation is observed for control devices with AAR of 60K.

When the antenna size increases, NBTI worsens, as shown in Fig. 3-10 (a). The V_{th} shift is higher for devices with large AAR (e.g., 60K). This indicates that the generation rates of interface states and the positive charges during the NBTI stressing are degraded due to the plasma charging damages. Fig. 3-10 (b) shows that the exponential values of the devices with AAR of 60K at $V_g = -3.5$ V (~0.18) are much larger than that of the devices with AAR of 1K at $V_g = -3.5$ V (~0.1), both with and without F incorporation. This implies that the degradation could be more serious for the devices with AAR of 60K under NBTI stressing. Such V_{th} shift observed in p-channel MOSFETs can be attributed to the enhanced positive charge build-up in the HfO_2 dielectric and an increase in interface state density, as shown in Fig. 3.11 (a) and Fig. 3-11 (b). More hole charges trapped in the HfO_2 dielectric cause more severe threshold voltage shift. In Fig 3-12, PMOS with high-k dielectrics also demonstrate

higher sensitivity to the BTS of the I_d degradation parameter on the plasma charging damage with larger antenna.

V_{th} shift in Fig. 3-13 and N_{tot} and N_{it} shift in Fig. 3-14 as function of stress time are for the devices with a large antenna (e.g., AAR = 60K) under NBTI stressing at 25 ^{o}C and 125 ^{o}C. A large degradation in all parameters is observed when stress temperature increases [31]-[34]. These results show that when temperature increases, the increase of the bulk trap generation is higher than the interface state generation, resulting in larger V_{th} shift. Bulk trap generation is the main degradation in HfO_2 high-k film, and becomes even more severe at high temperature. More importantly, F-incorporated films do exhibit better NBTI improvement.

The above results confirm that the NBTI of PMOS devices is degraded by plasma charging effect. The possible mechanism is that the enhanced hole trapping events caused by the plasma charging increases the generation of interface states and bulk traps. The hole trapping in the bulk, rather than the interface generation, is the dominant mechanism responsible for the degradation; while it can be significantly improved by the F incorporation.

3-4 Summary

In this study, the effects of metal etching and subsequent resist ashing on the gate oxide integrity and device characteristics were studied. Our results show that the main factor that affects gate oxide integrity is the severe plasma charging damages. As a result, the devices

with large antenna depict degraded V_{th}, N_{it} and I_d. The enhanced degradations occurred during photo-resist stripping step. Increase of positive trapped charges in the gate dielectrics is a plausible cause for aggravated NBTI.

Finally, we also proposed that the CVS and NBTI characterization could be cleverly employed as a sensitive method for characterizing the antenna effects in the devices with HfO_2/SiON gate stack. Both CVS and NBTI on HfO_2/SiON pMOSFETs with antenna structures are also found to be primarily due to charge trap generation in the bulk of HfO_2 ($\triangle N_{ot}$), instead of at the interface ($\triangle N_{it}$). We demonstrated for the first time that plasma charging effect induces hole trapping in the HfO_2/SiON gate stack; while it can be effectively suppressed with F incorporation. In other words, F incorporation can reduce hole traps in HfO_2 high-k film.

Chapter 4
Conclusions and Future Work

4-1 Conclusions

In this thesis, the effects of fluorine incorporation into HfO_2/SiON gate stack were investigated. Several important phenomena were observed and summarized as follows:

First, we have investigated its basic electrical properties. The initial electrical properties of the devices are negligibly affected by fluorine incorporation. The gate leakage current is analyzed by the carrier separation measurement, and can be explained by the band structure of the gate stack. The source/drain current I_{SD} that corresponds to the hole current dominates the leakage current under inversion region, while the substrate current I_B that indicates the electron current dominates the leakage current under accumulation region. All leakage currents can be categorized by fitting to be of Frenkel-Poole type.

Secondly, we have studied the NBTI mechanism and AC dynamic stressing of the polysilicon gate HfO_2 MOSFETs, with and without F incorporation. $\triangle V_{th}$ is primarily caused by the charge traps in the HfO_2 dielectric, not by the interfacial degradation. F incorporation is effective in suppressing $\triangle N_{it}$ as well as $\triangle N_{ot}$, thus improving threshold voltage instability.

For traditional SiO_2 gate dielectric, both $\triangle V_{th}$ and $\triangle N_{it}$ are improved by fluorine incorporation, maintaining almost the same activation energies of about 0.2 eV. Similar trends

are observed in our devices. The activation energy of $\triangle V_{th}$ is 0.08 eV and that of $\triangle N_{it}$ is 0.14 eV for both devices. Fluorine is found to be able to electrically passivate traps without changing the NBTI mechanism.

AC dynamic stressing provides more realistic and precise prediction in estimating device reliability and charging dynamics in high-k HfO_2. The experimental results show that threshold voltage shifts toward more negative voltage in DC stress, but shifts toward more positive voltage under AC unipolar stress. This is believed to be due to less hole charge trapping during on-ptime. The interface trap generation depends weakly on both frequency and duty cycle. Instead of interface trap, the bulk trap of HfO_2 eventually plays a preponderant role during AC stress.

Finally, we have clearly shown that plasma charging damage introduces more hole traps in the HfO_2/SiON gate stack, thus aggravating the NBTI. F incorporation can significantly reduce the impact of plasma charging effect.

Suppressing the traps in bulk is important for pMOSFETs with HfO_2/SiON gate stack. Fluorine incorporation is found to be an excellent technique to improve BTI immunity and strengthen the immunity against plasma charging damage, thus enhances high-k devices' stability and reliability.

4-2 Future Work

It is generally conceived that the introduction of high-k gate dielectrics is inevitable for the technology nodes of 50 nm and beyond, in order to satisfy the stand-by power requirement without sacrificing metal oxide semiconductor field effect transistor (MOSFET) performance. HfO_2 is considered as one of the most promising high-k dielectrics. However, threshold voltage instability and inadequate mobility of HfO_2 MOSFETs are major issues that remain to be solved.

For the threshold voltage instability issue, we found that the exponential value of $\triangle V_{th}$ for pMOSFETs with HfO_2 gate dielectric is voltage and temperature dependent due to charge trapping in bulk HfO_2. More efforts on the model of time evolution of V_{th} instability, so that we could extrapolate ten years lifetime for devices by this model, are necessary.

Introduction of the strained silicon could enhance channel mobility while locally strained pMOSFETs with HfO_2 gate dielectric have not yet been reported. More research efforts are needed to understand channel mobility and reliability of this structure, and their impacts on future ULSI technology.

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ITRS 2004

Year of Production	2004	2005	2006	2007	2008
EOT (physical) for high-performance (nm)	1.2	1.1	1.0	0.9	0.8
Electrical thickness adjustment for gate depletion and inversion layer effects (nm)	0.8	0.7	0.7	0.4	0.4
Nominal gate leakage current density limit (at 25°C) (A/cm^2)	450	520	600	930	1100

Manufacturable solutions are known

Manufacturable solutions are NOT known

Table 1-1 2004 International Technology Roadmap for Semiconductors.
The color shade means the solution known and unknown for physical limit.

- **Standard LOCOS process**
- **RCA clean and HF-last dip**
- **RTA 700 ^{o}C in N_2O ambient ~ SiON 0.7nm**
- **MOCVD of 3nm HfO_2 (500 ^{o}C)**
- **PDA 700 ^{o}C 20 sec in N_2 ambient**
- **Poly-Si deposition 200nm and patterning (no PR removal)**
- **Split (F implant, Dose:2E15cm^{-2}, E:10Kev, Tilt:0 degree)**
- **S/D implant, followed by PR removal**
- **Dopant activation: 950 ^{o}C, 20 sec**
- **Passivation then metallization**
- **Sintering in FG: 400 ^{o}C, 30 min**

Fig. 2-1 Process flow.

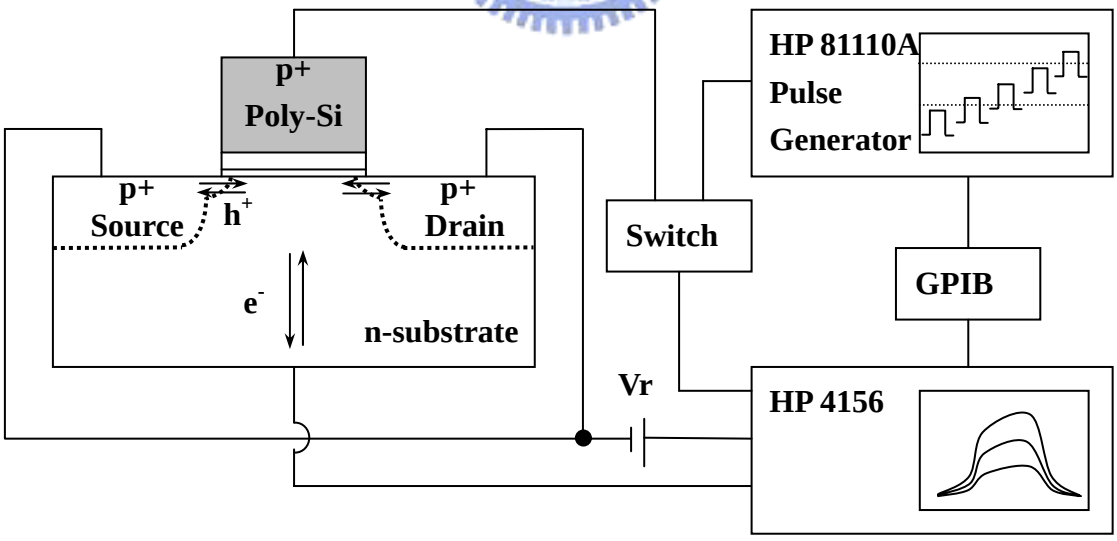


Fig. 2-2 Basic experimental setup of charge pumping measurement.

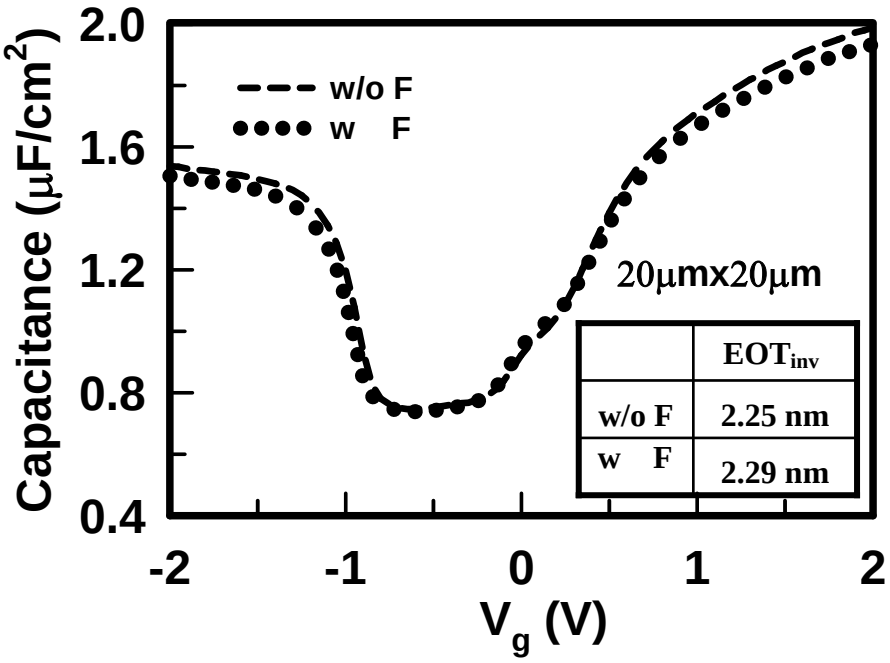
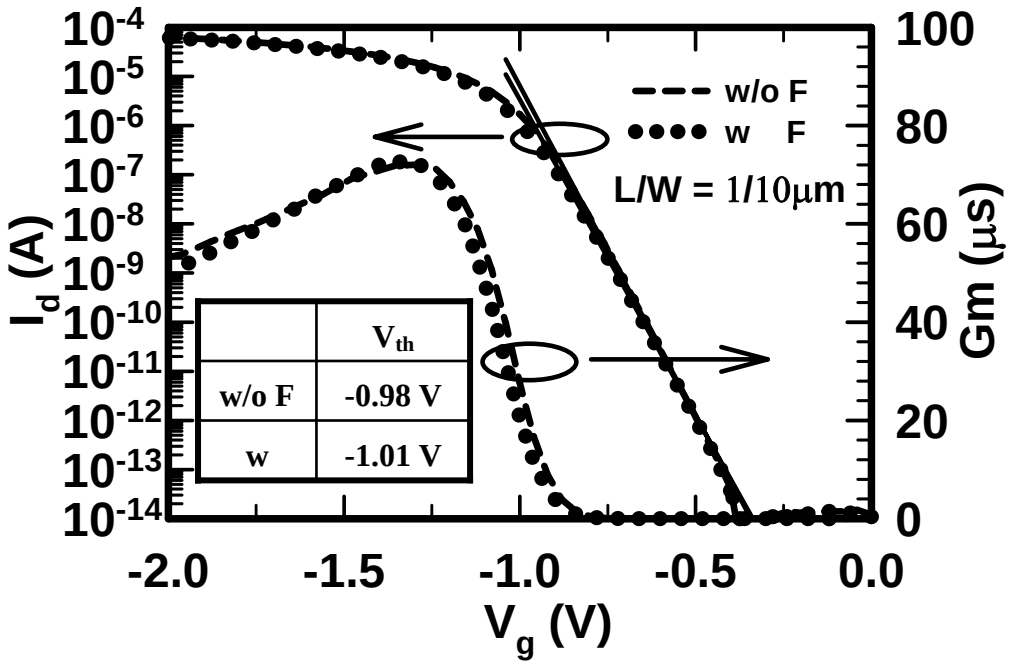
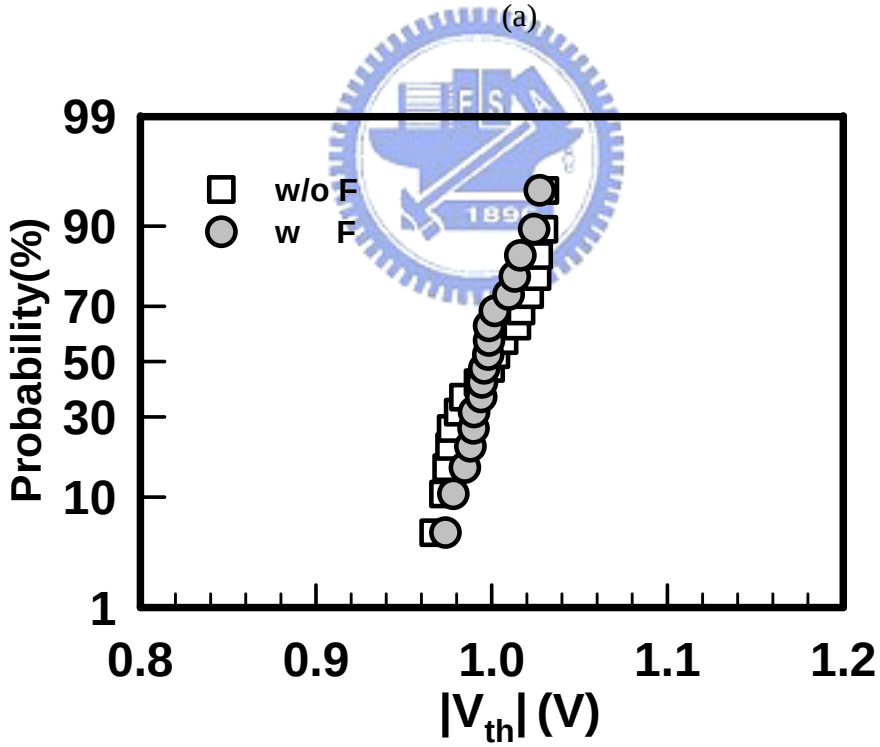


Fig. 2-3 *C-V* curves for pMOSFETs.



(a)



(b)

Fig. 2-4 (a) Pre-stress I_d-V_g and G_m-V_g characteristics for fresh p-channel devices, (b) Cumulative probability of the threshold voltage (V_{th}).

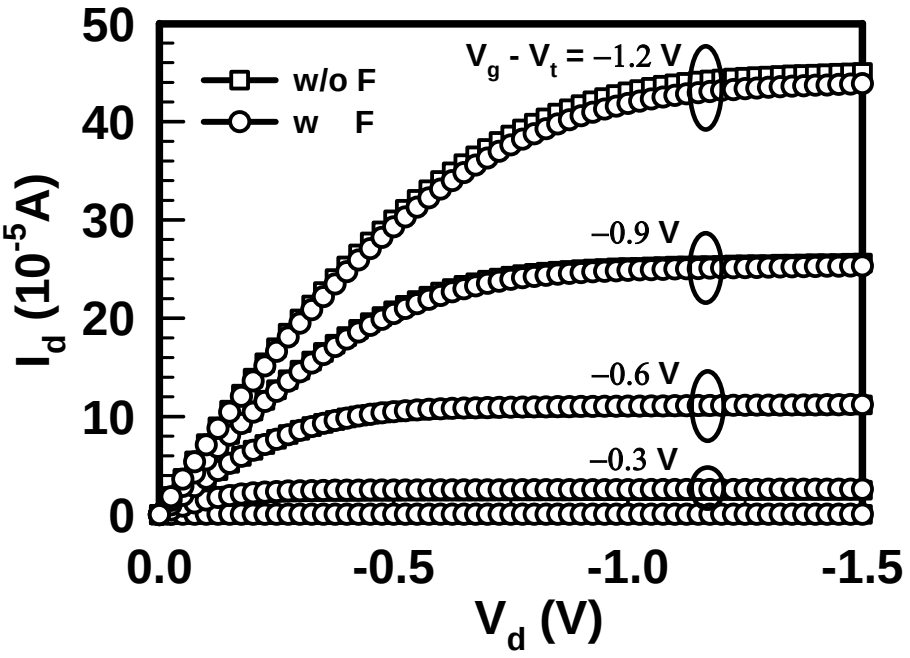


Fig. 2-5 Pre-stress I_d-V_d characteristics for fresh p-channel devices.

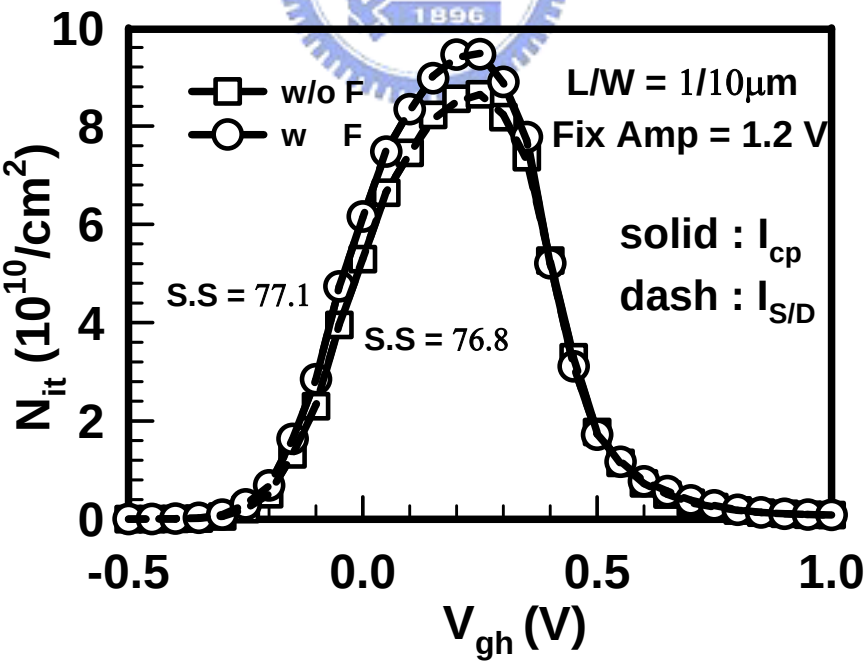


Fig. 2-6 Pre-stress interface trap density (N_{it}) characteristics for fresh p-channel devices.

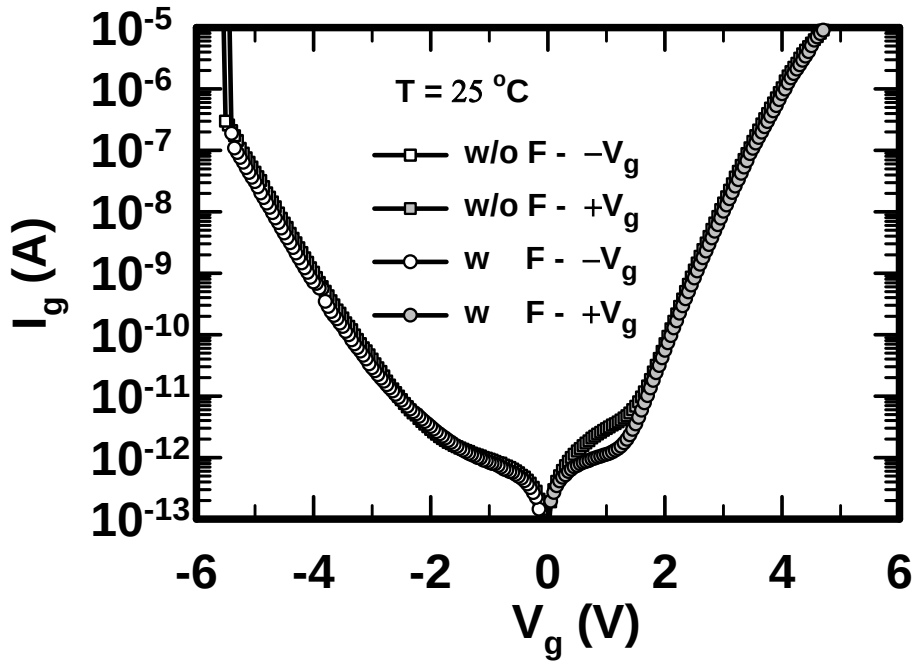
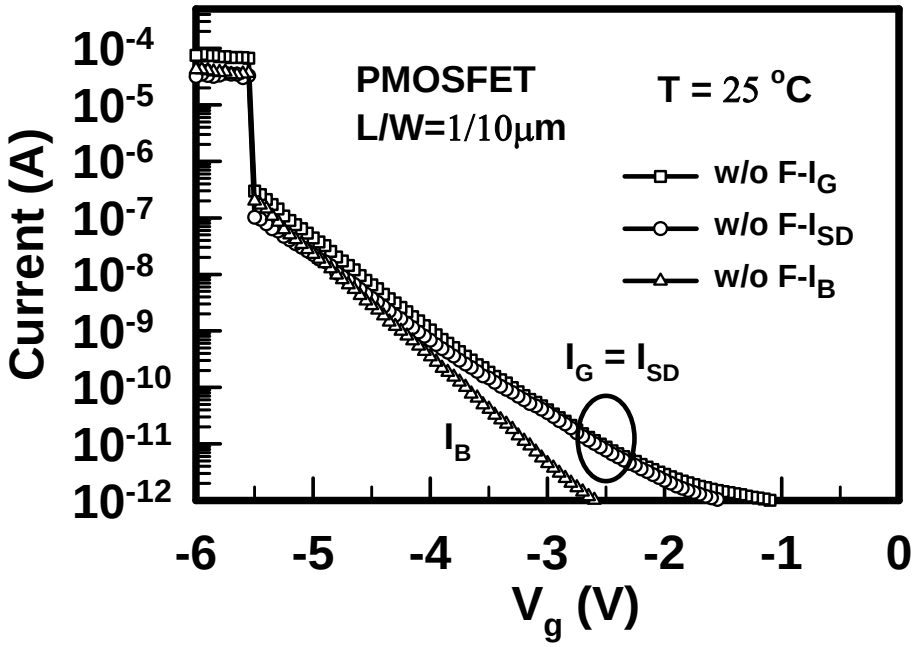
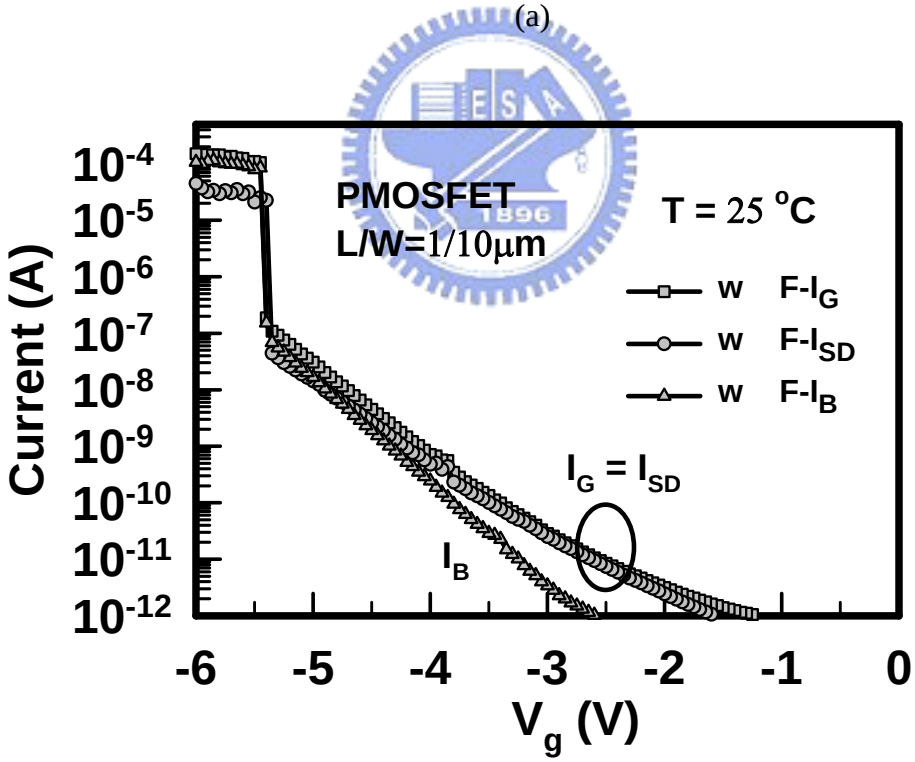


Fig. 2-7 Gate leakage current versus gate bias for fresh p-channel devices at room temperature.

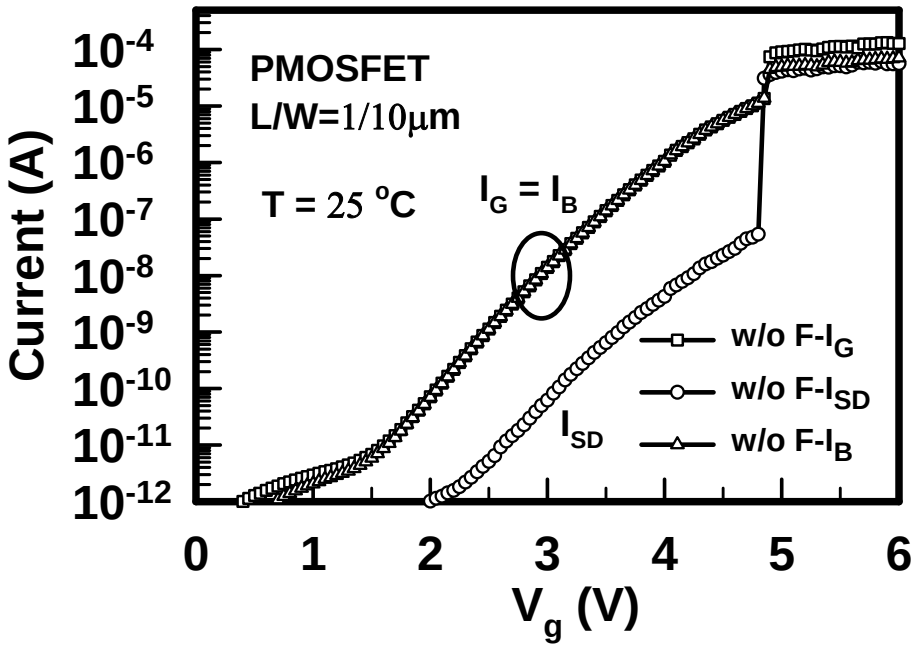


(a)

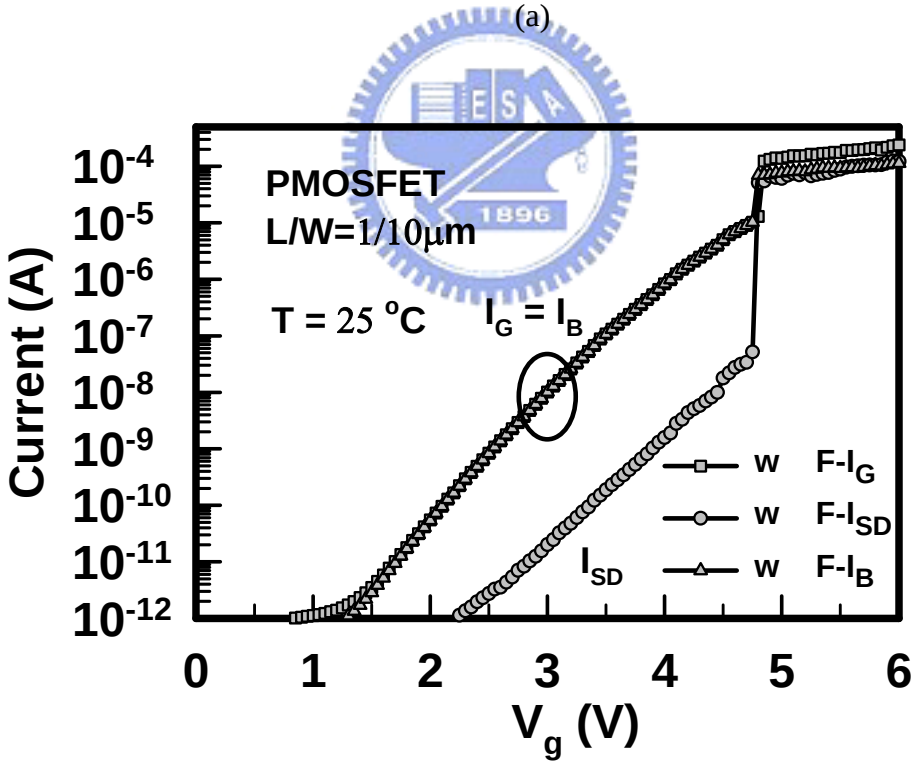


(b)

Fig. 2-8 Carrier separation under inversion region (a) w/o F sample, and (b) with F sample.



(a)



(b)

Fig. 2-9 Carrier separation under accumulation region (a) w/o F sample, and (b) with F sample.

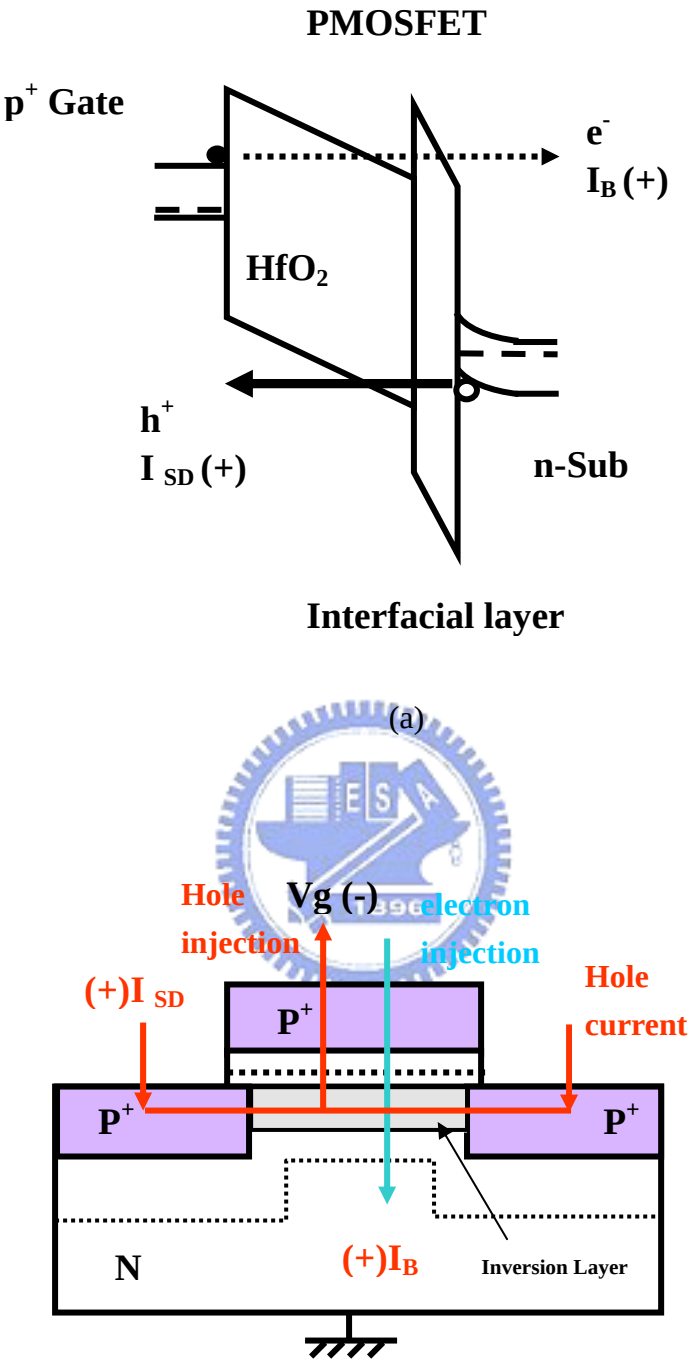


Fig. 2-10 p^+-gated pMOSFET with HfO_2/SiON gate stack under inversion region (a) Band diagrams, and (b) Schematic illustration of carrier separation experiment.

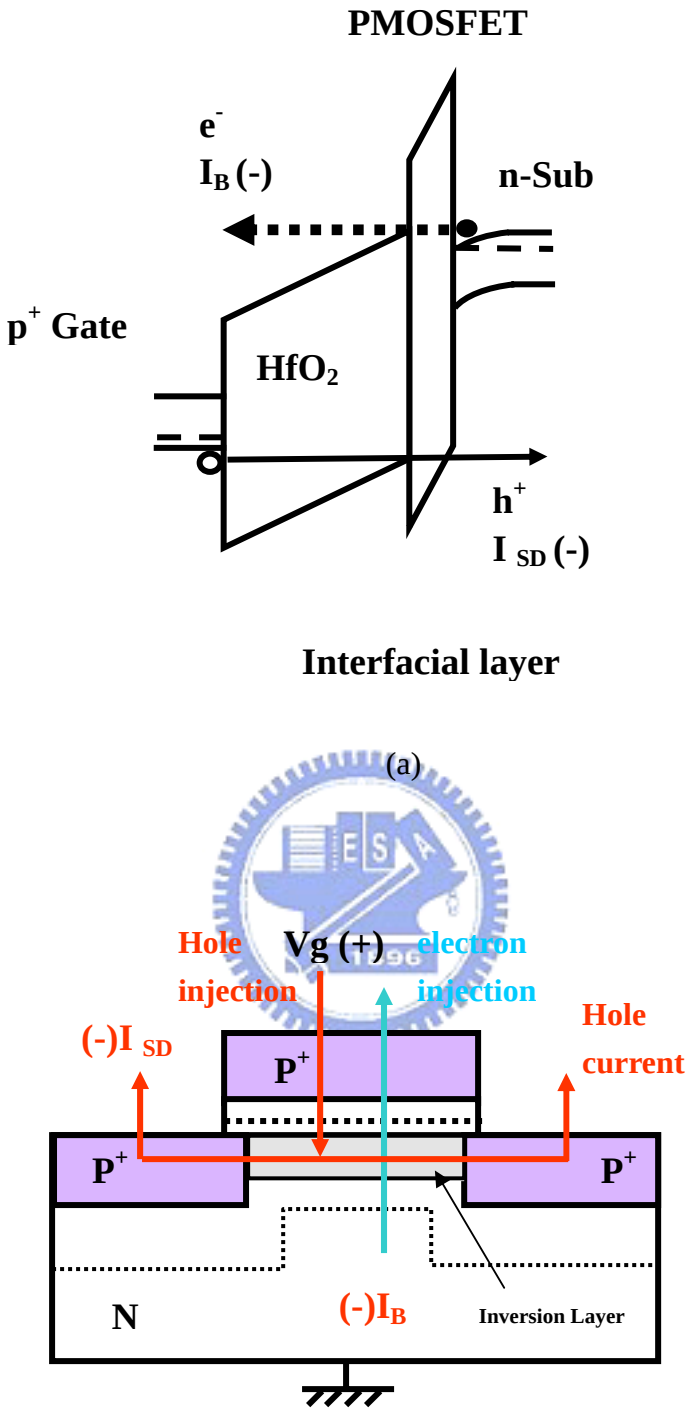
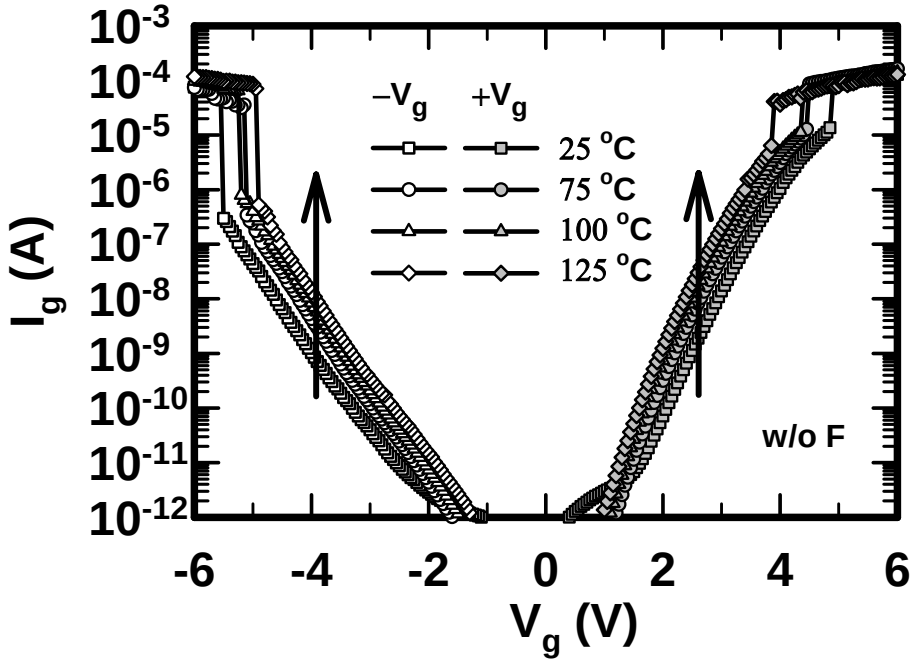
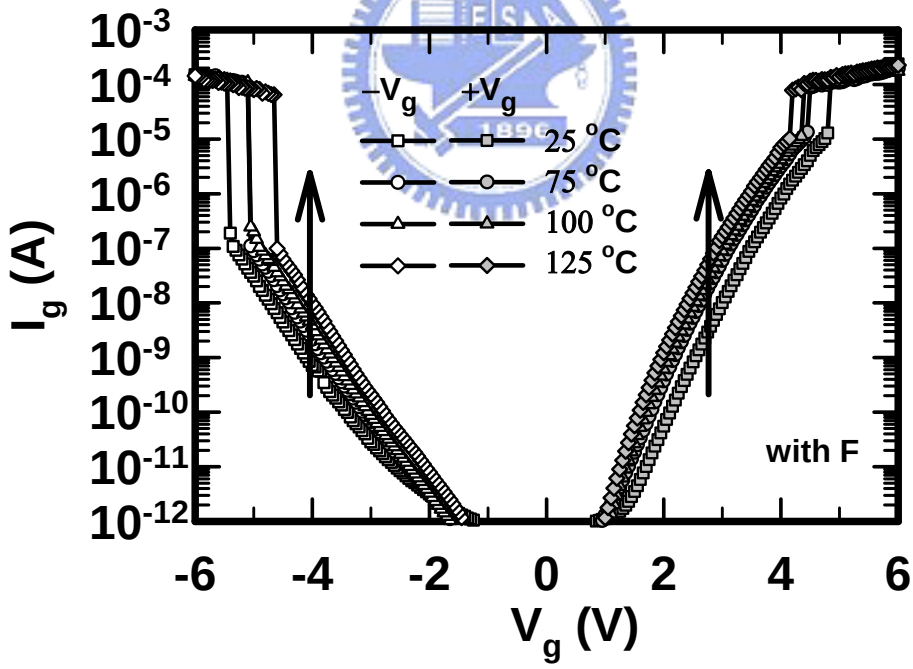


Fig. 2-11 p^+-gated pMOSFET with HfO_2/SiON gate stack under accumulation region (a) Band diagrams, and (b) Schematic illustration of carrier separation experiment.

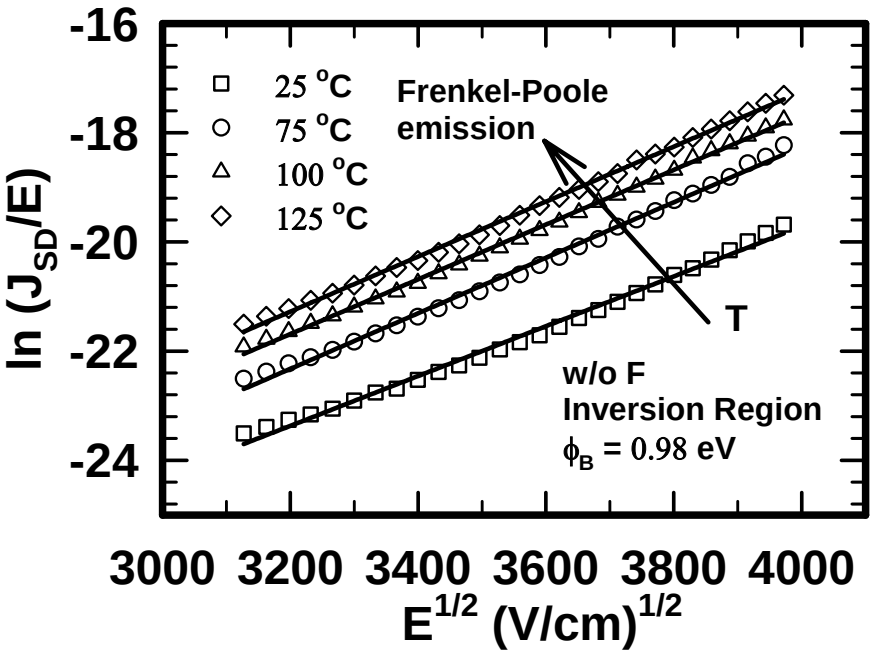


(a)

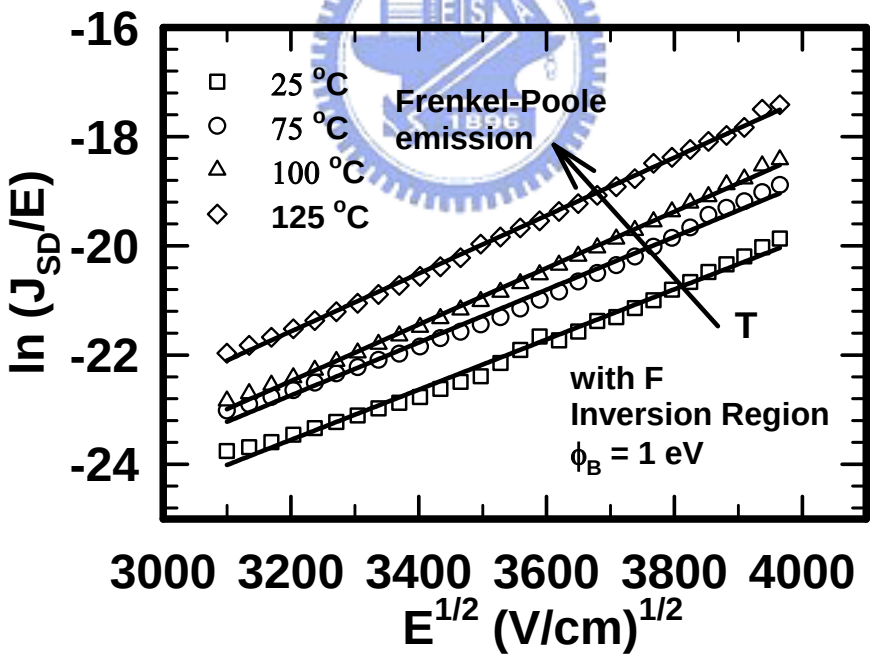


(b)

Fig. 2-12 Gate leakage current versus gate bias for fresh p-channel devices at various temperatures (a) w/o F sample, and (b) with F sample.

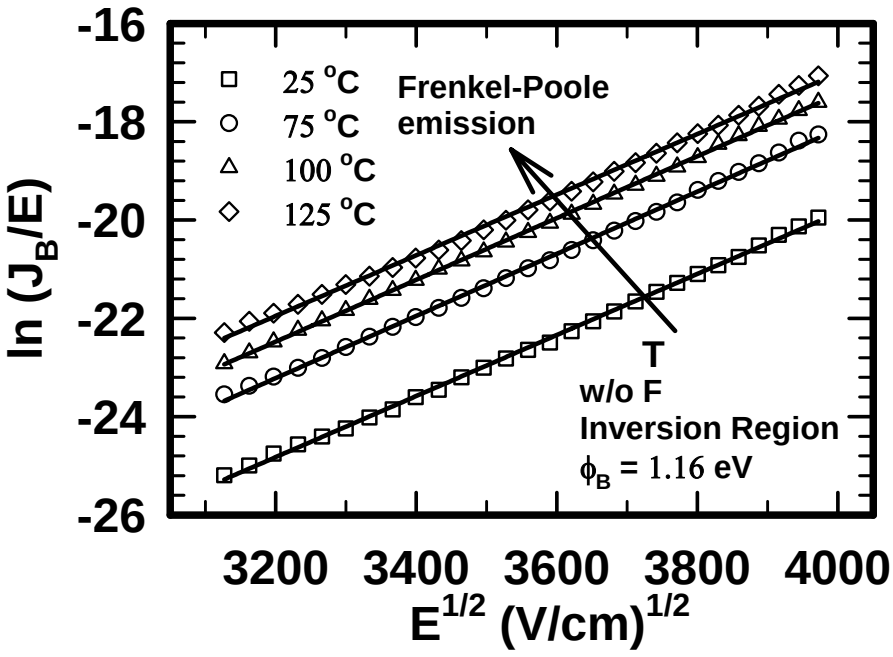


(a)

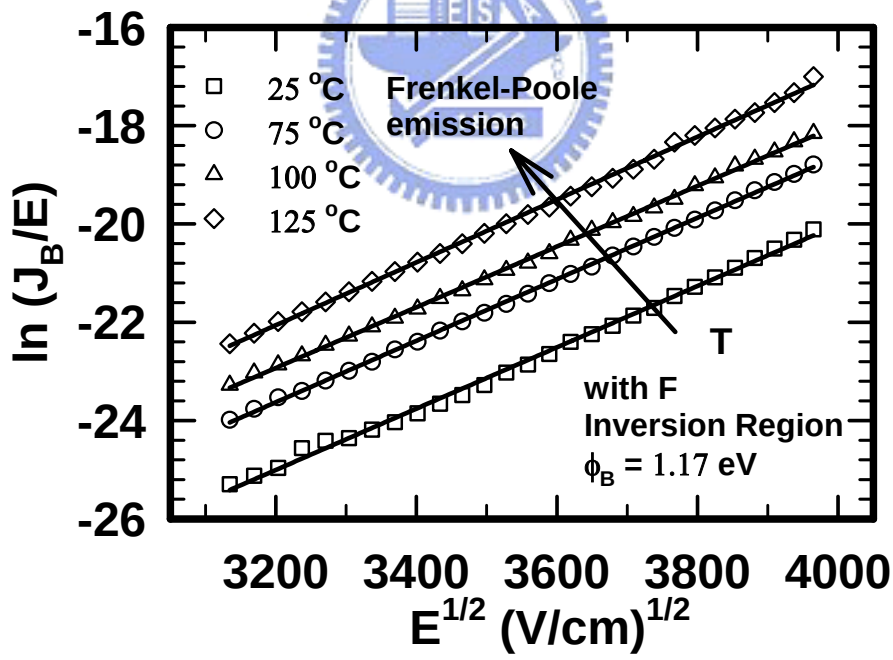


(b)

Fig. 2-13 Conduction mechanism for source/drain current fitting under inversion region (a) w/o F sample, and (b) with F sample.



(a)



(b)

Fig. 2-14 Conduction mechanism for substrate current fitting under inversion region (a) w/o F sample, and (b) with F sample.

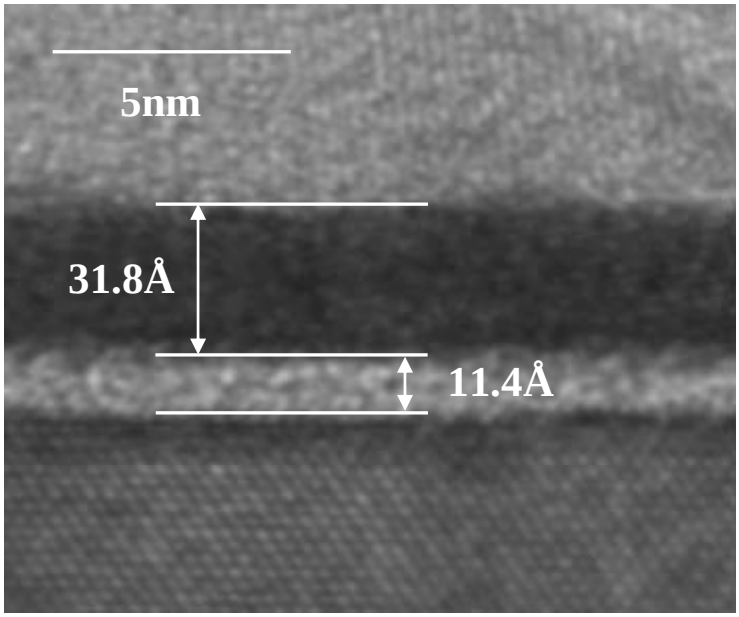
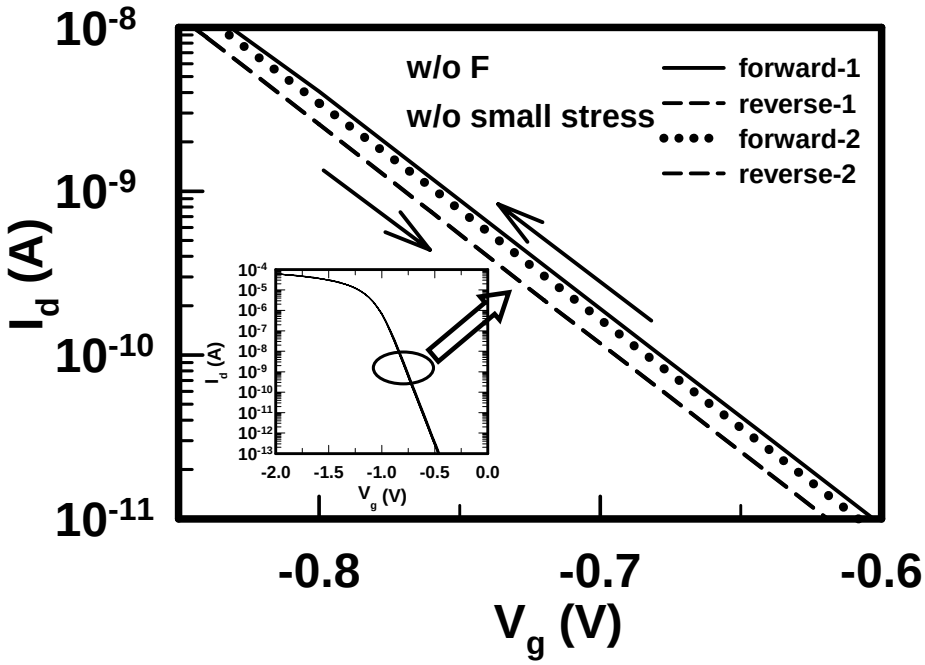
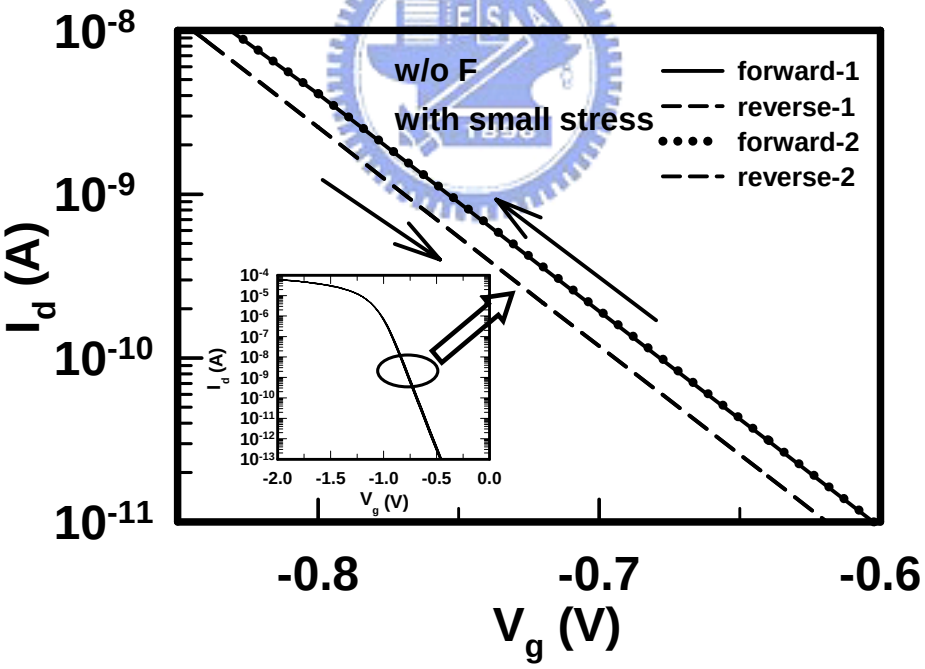


Fig. 2-15 HRTEM image of a device with HfO_2/SiON gate stack.

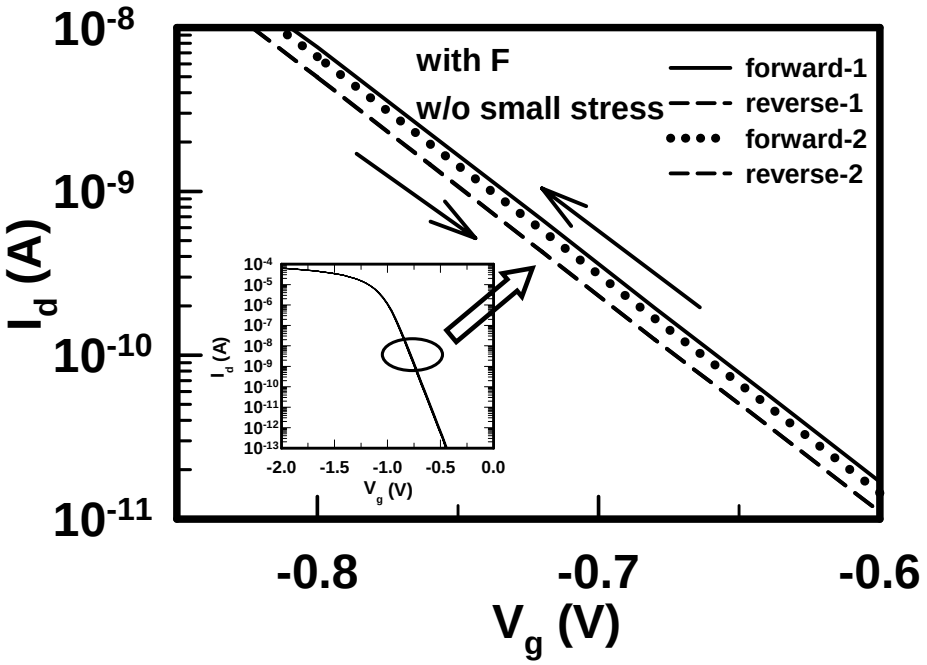


(a)

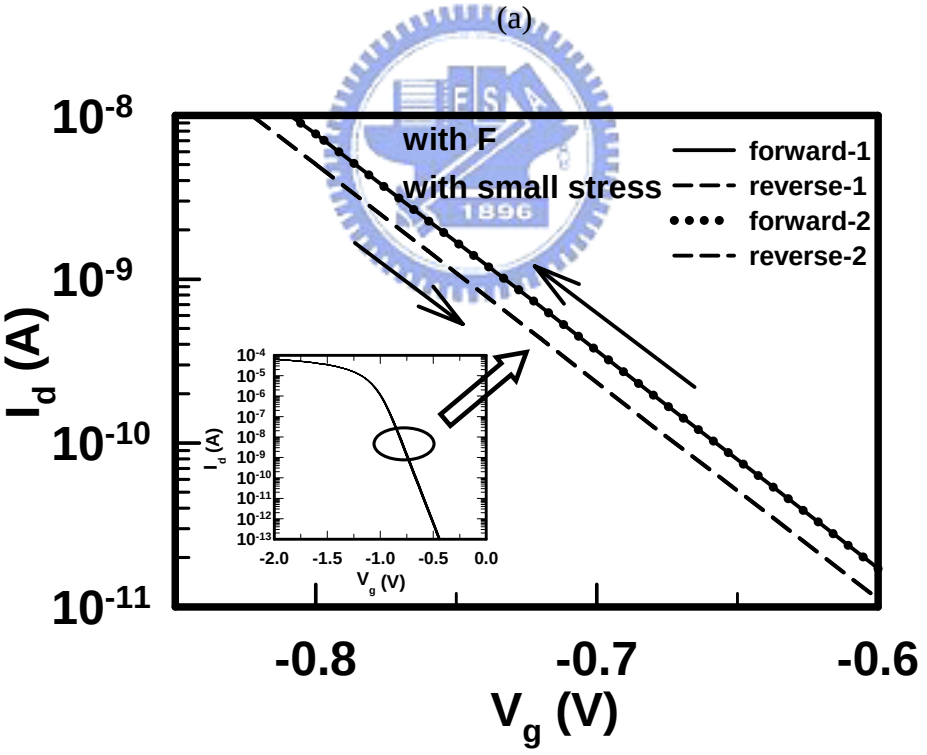


(b)

Fig. 2-16 I_d-V_g characteristics for p^+-gate pMOSFET without F incorporation (a) w/o small stress, and (b) with small stress.



(a)



(b)

Fig. 2-17 I_d-V_g characteristics for p^+-gate pMOSFET with F incorporation (a) w/o small stress, and (b) with small stress.

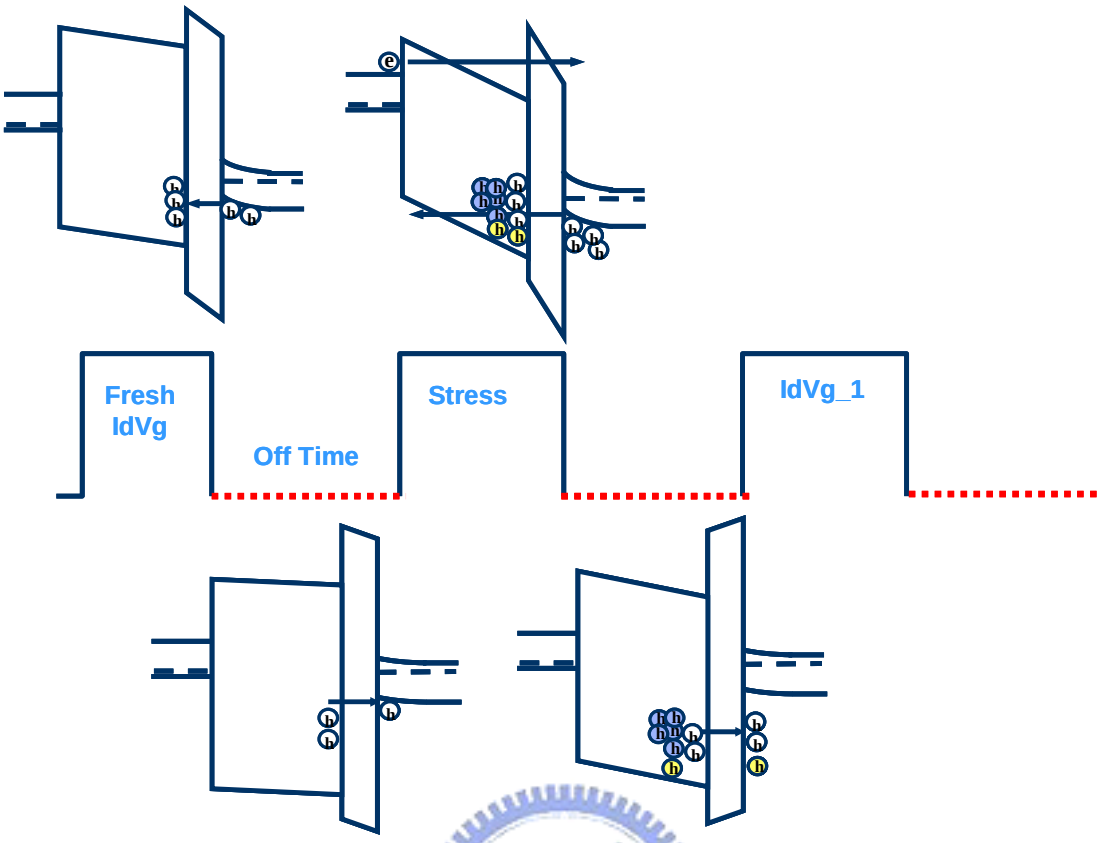


Fig. 2-18 Schematic illustrations for possible fast charging effects (FCE).

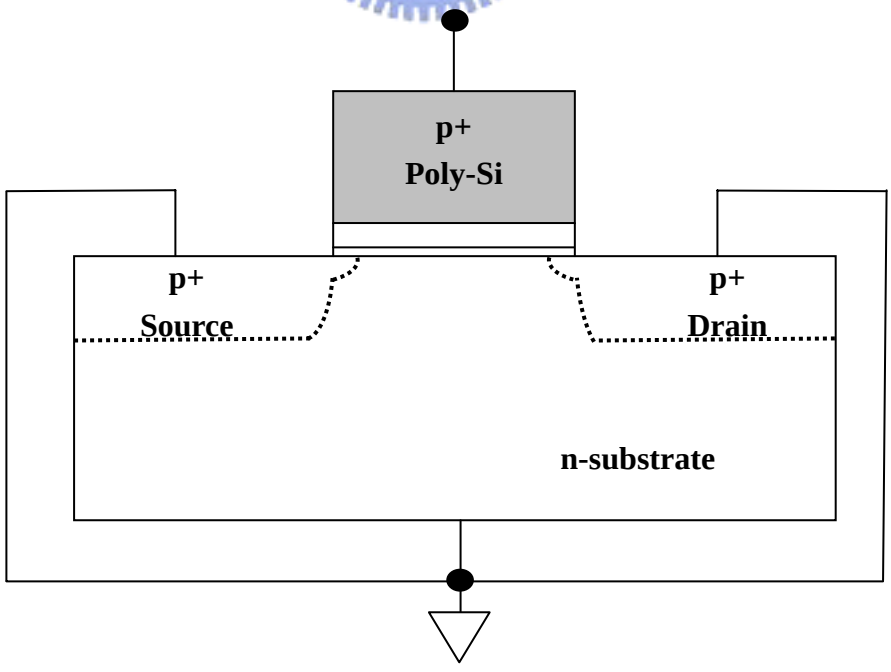
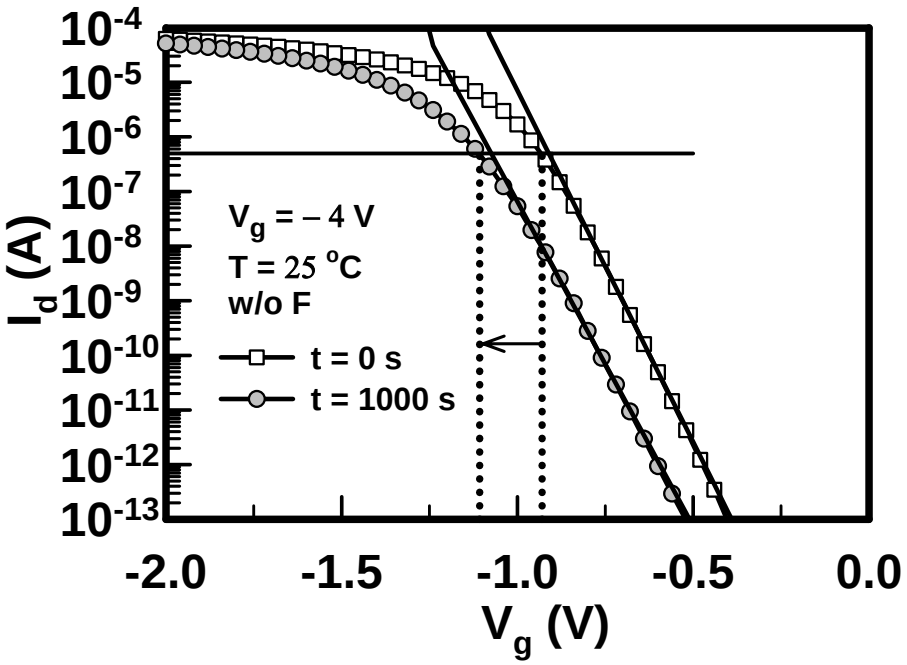
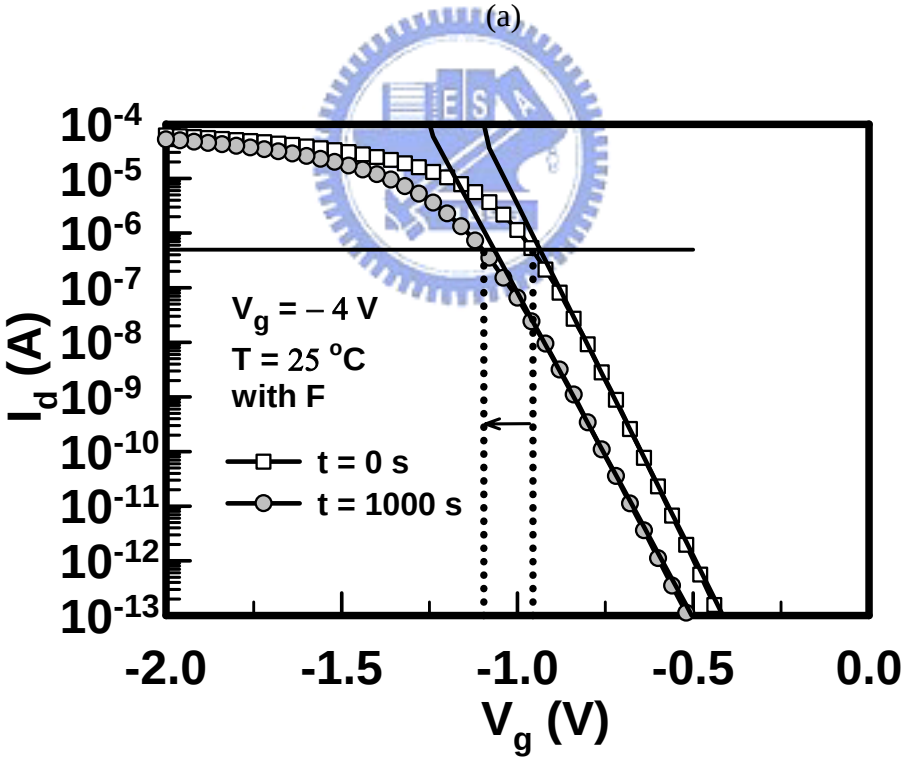


Fig. 2-19 Configuration for NBTI stressing.

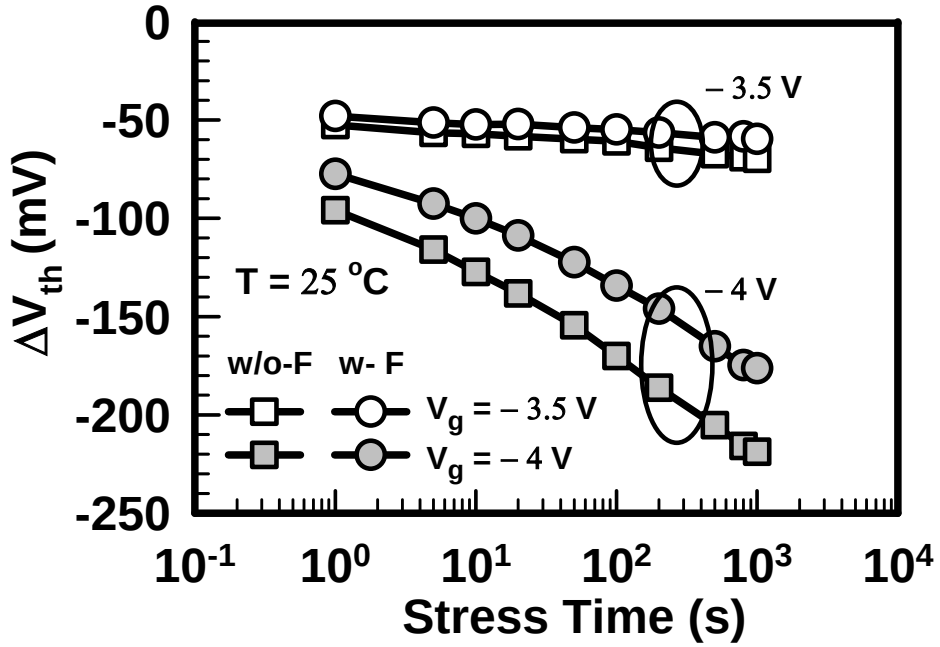


(a)

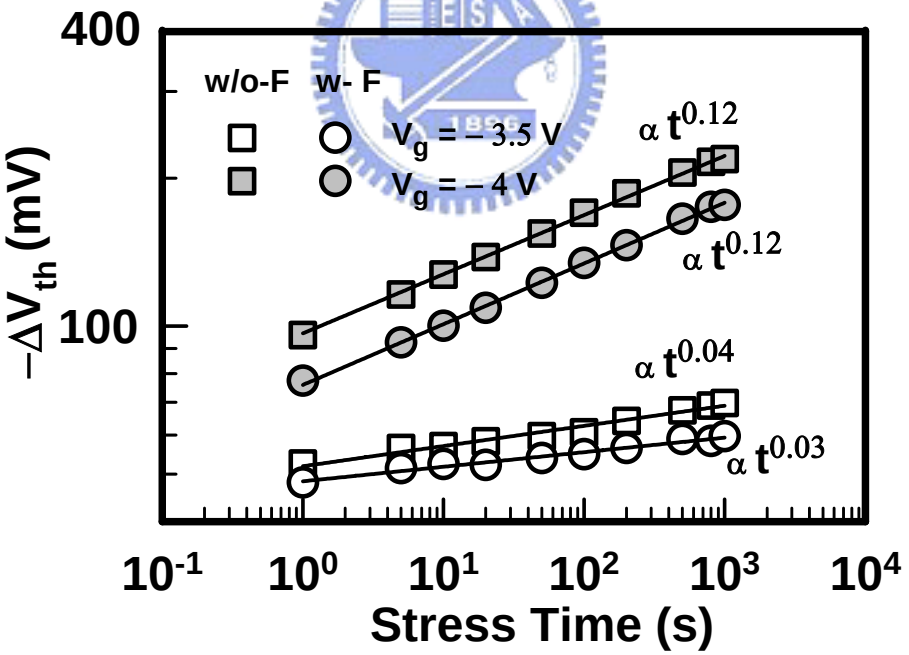


(b)

Fig. 2-20 I_d-V_g characteristics for p^+-gate pMOSFETs before stress and after stress 1000 s at 25 °C (a) w/o F sample, and (b) with F sample.

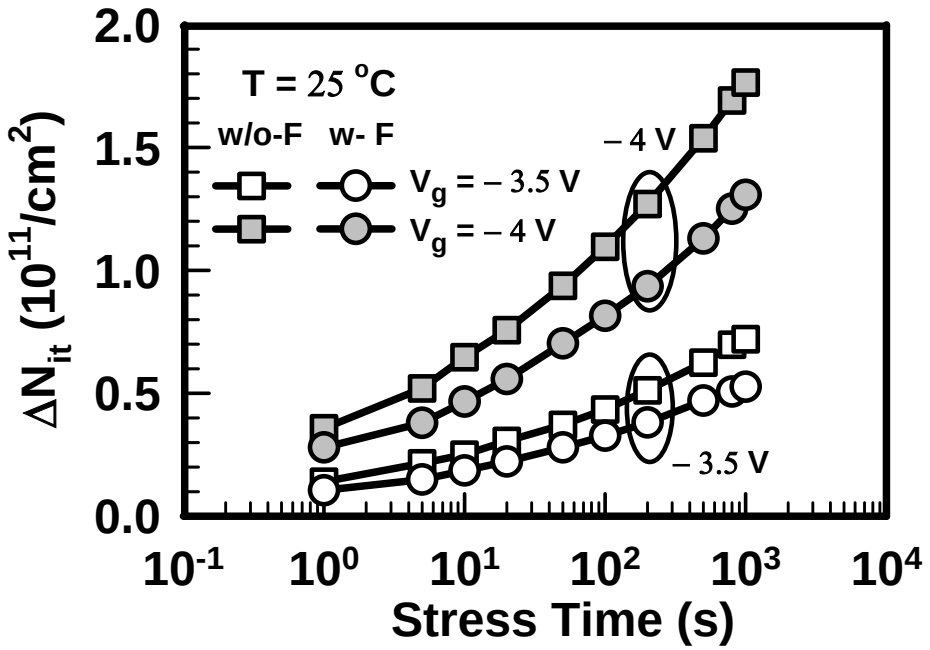


(a)

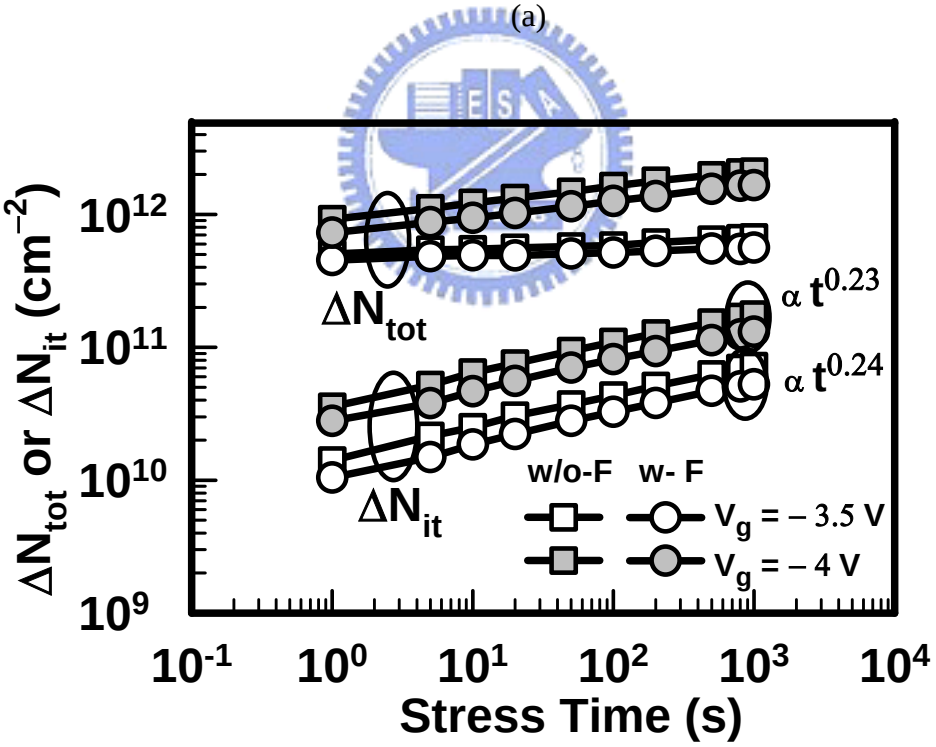


(b)

Fig. 2-21 Threshold voltage shift as a function of stress time, stressed at 25 °C, V_g = – 3.5 V & – 4 V with (a) linear scale, and (b) logarithm scale.



(a)



(b)

Fig. 2-22 (a) Interface trap density shift, and (b) total trap density increase as a function of stress time. Devices were stressed at 25 °C, V_g = — 3.5 V & — 4 V.

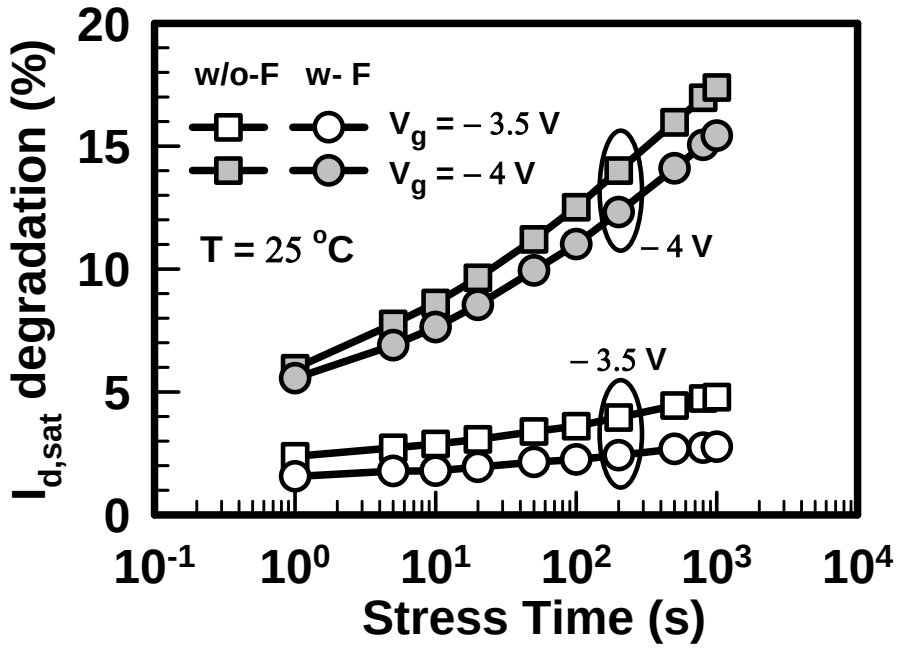
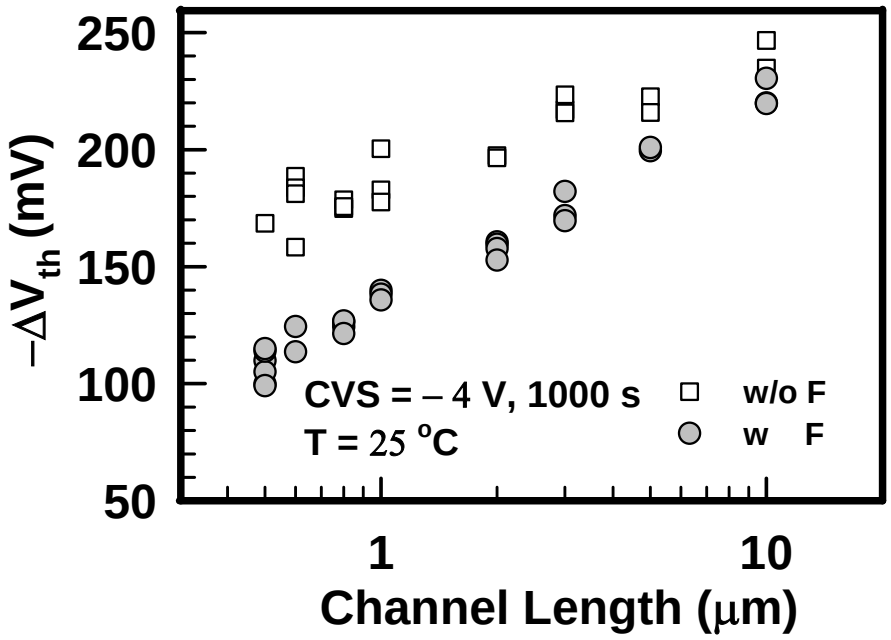
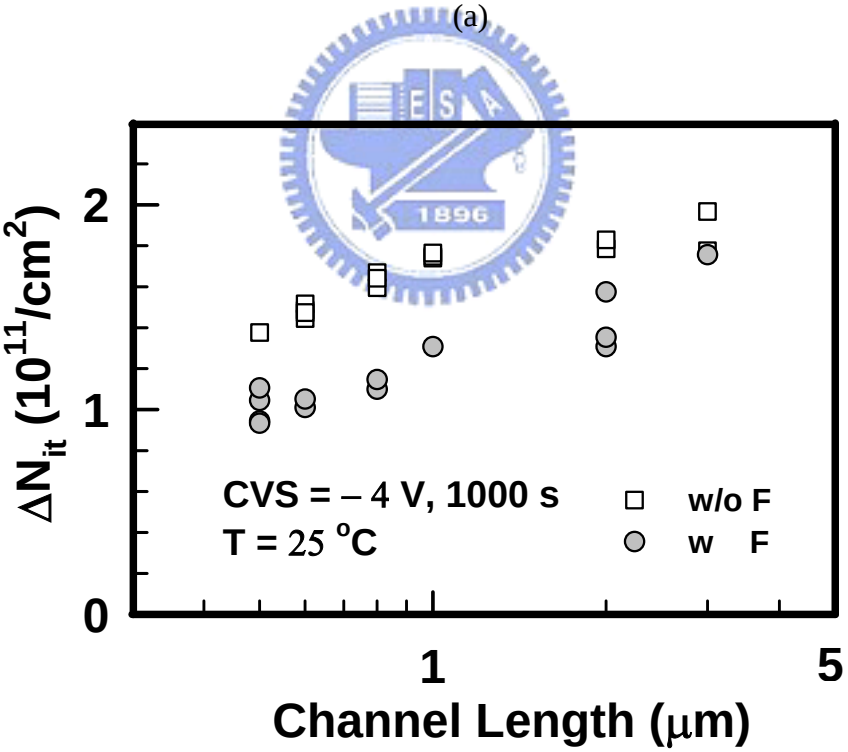


Fig. 2-23 Drain current degradation under saturation regime over stress time. Devices were stressed at 25 °C, V_g = −3.5 V & −4 V.

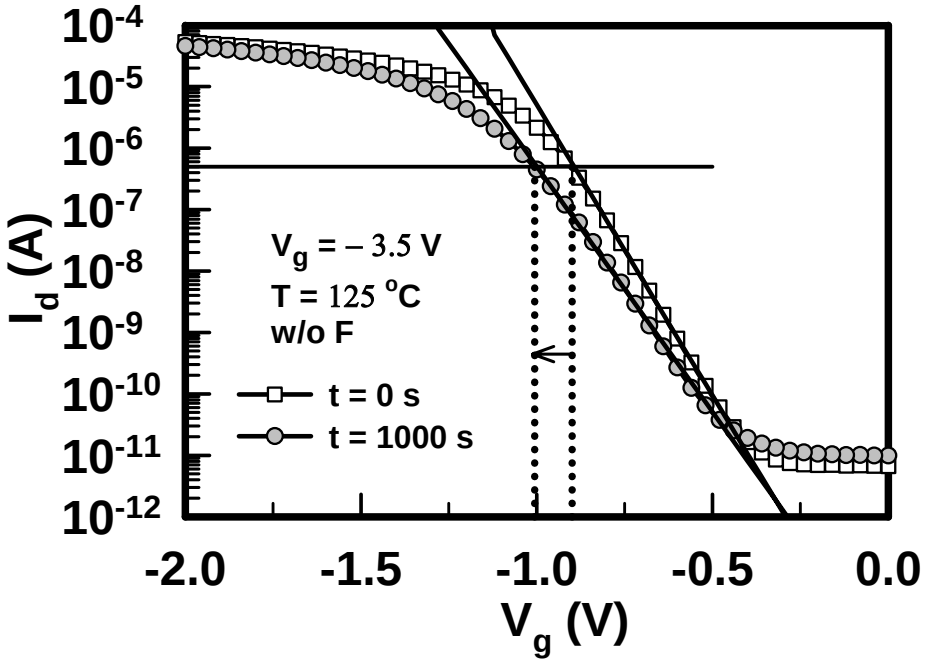


(a)

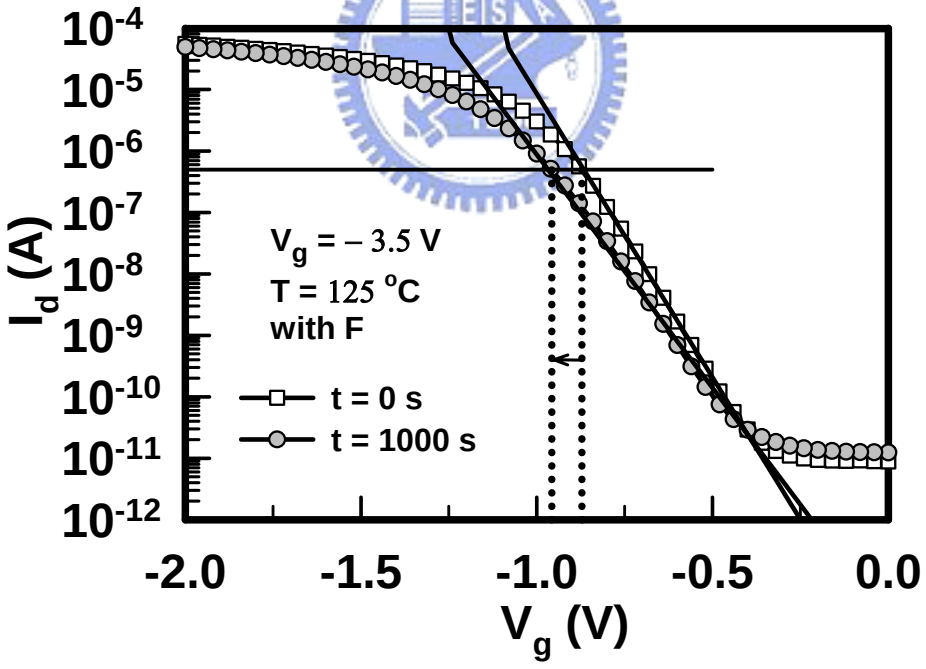


(b)

Fig. 2-24 (a) Threshold voltage shift, and (b) interface trap density shift as a function of channel length. Devices were stressed at 25 °C, $V_g = -4$ V.

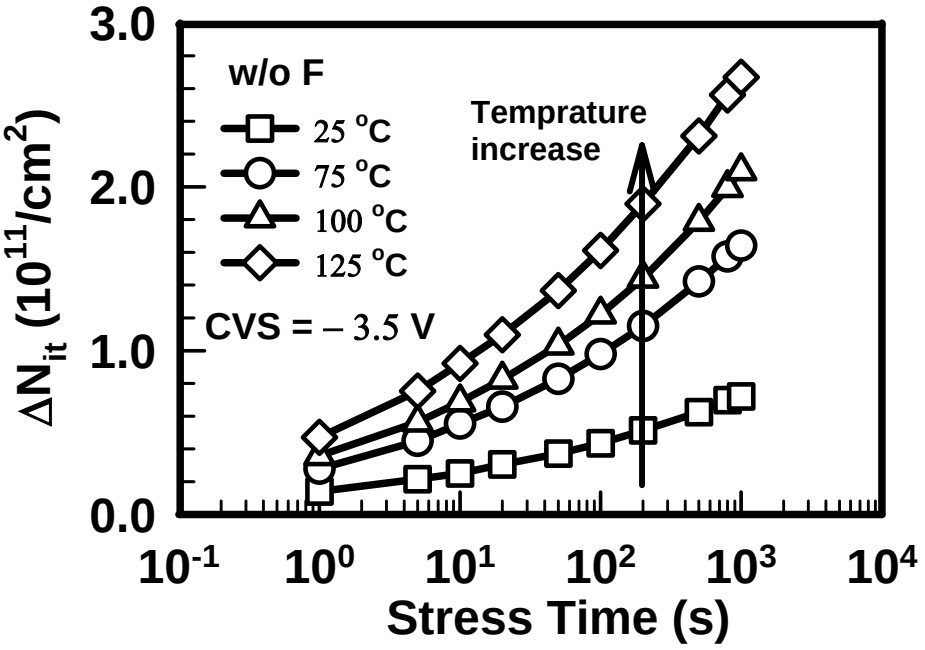


(a)

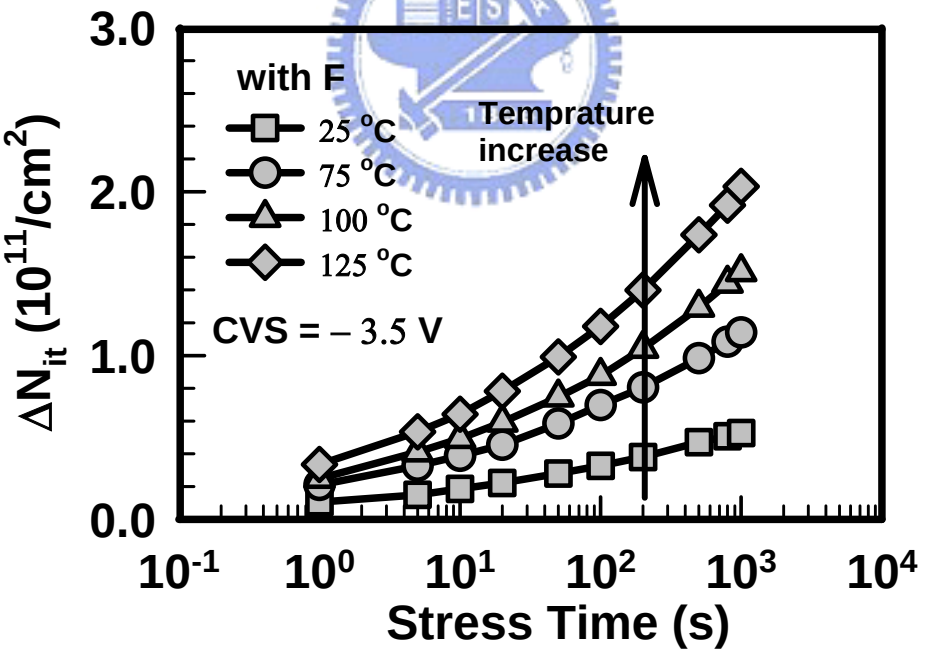


(b)

Fig. 2-25 I_d-V_g characteristics for p^+-gate pMOSFETs before stress and after stress 1000 s at 125 °C (a) w/o F sample, and (b) with F sample.

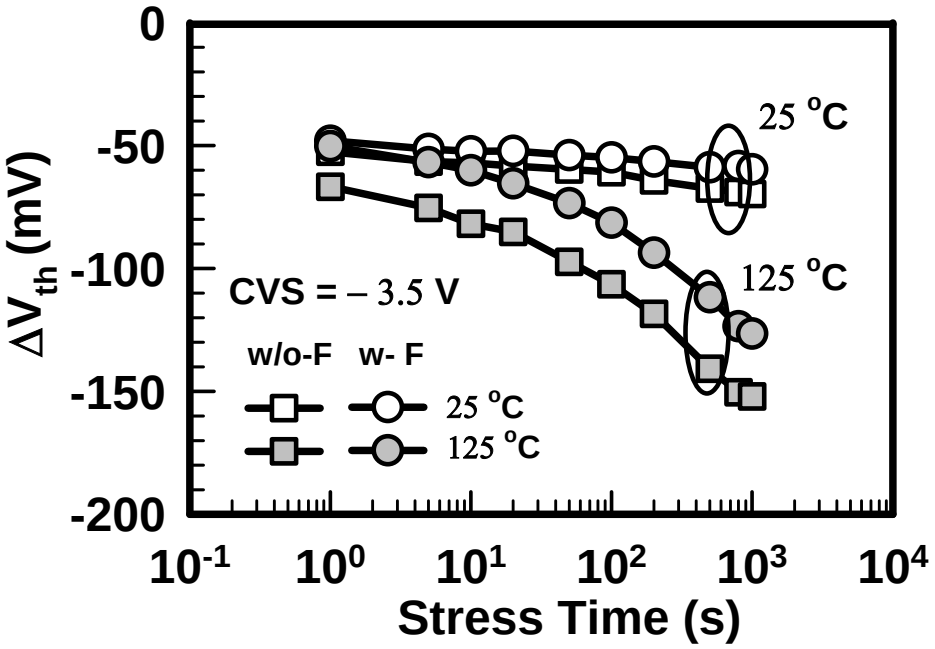


(a)

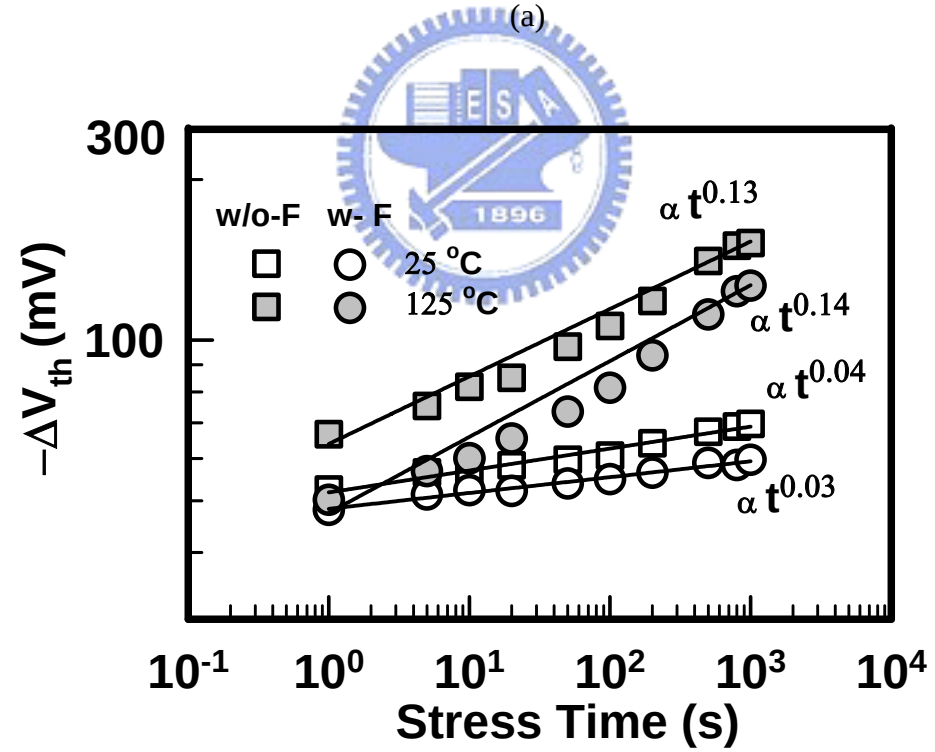


(b)

Fig. 2-26 Interface trap density shift as a function of stress time under BTS at different stress temperature, $V_g = -3.5$ V (a) w/o F sample, and (b)with F sample.

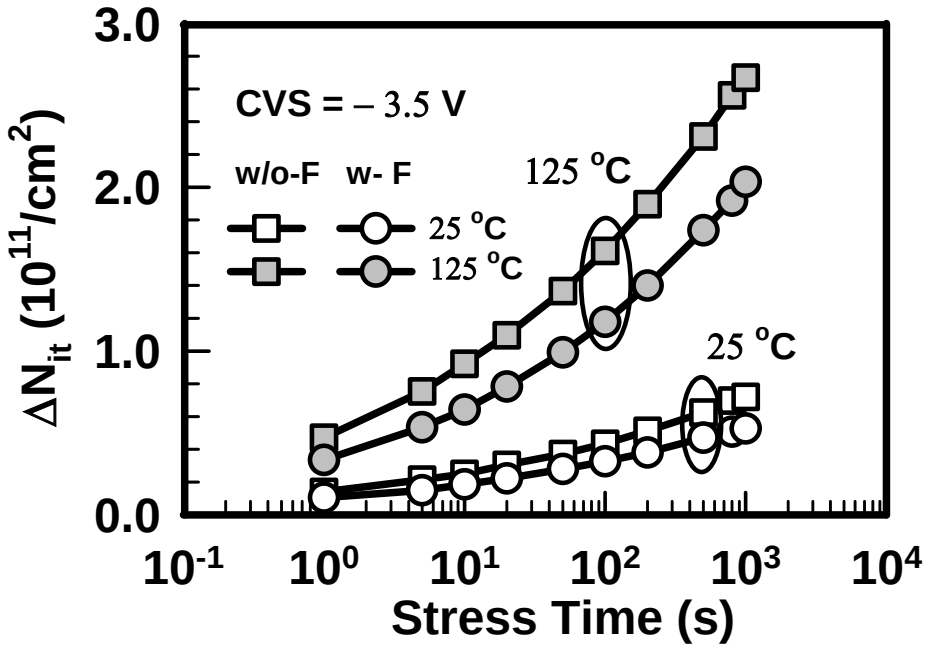


(a)

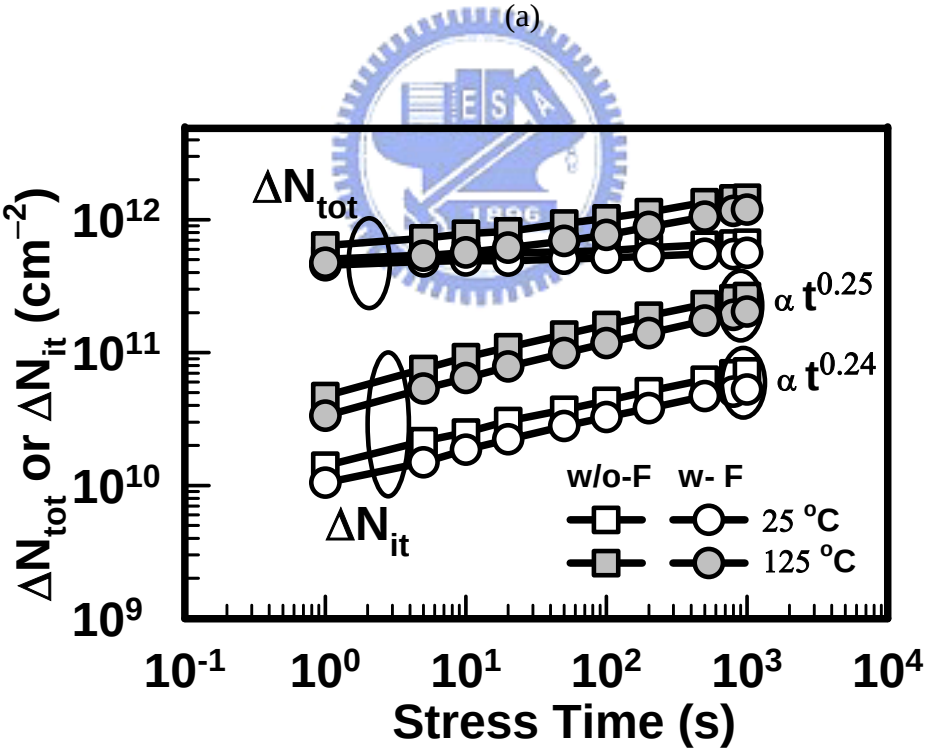


(b)

Fig. 2-27 Threshold voltage shift as a function of stress time under BTS at different stress temperatures, $V_g = -3.5$ V, (a) linear scale, and (b) logarithm scale.



(a)



(b)

Fig. 2-28 (a) Interface trap density shift, and (b) total trap density increase as a function of stress time under BTS at different stress temperatures, $V_g = -3.5$ V.

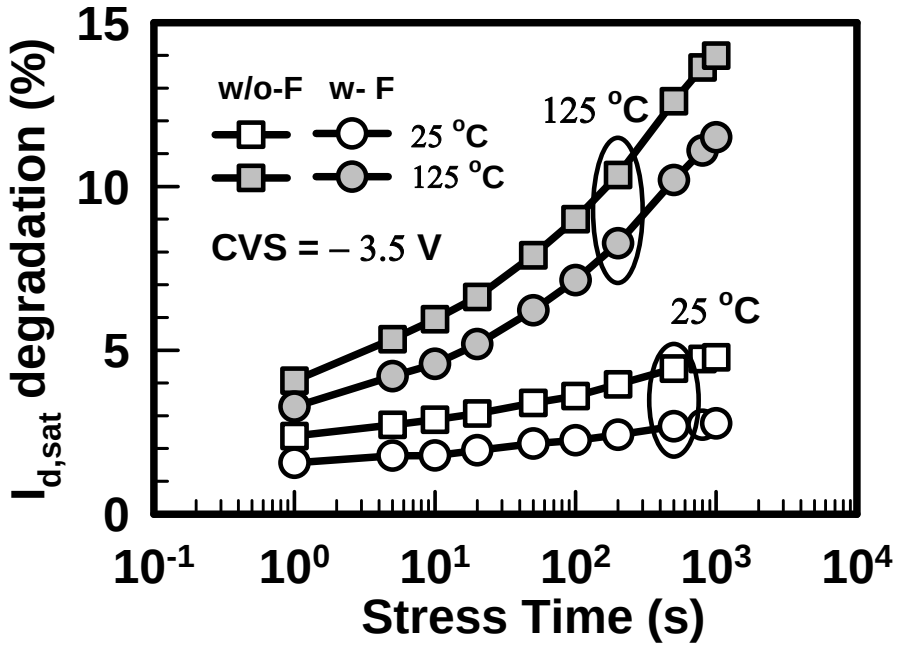
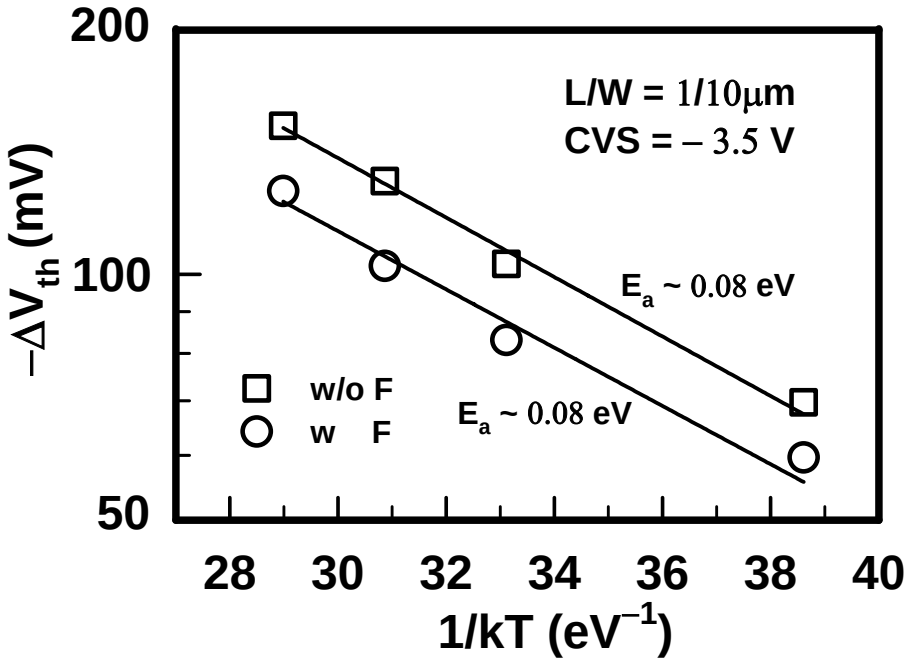
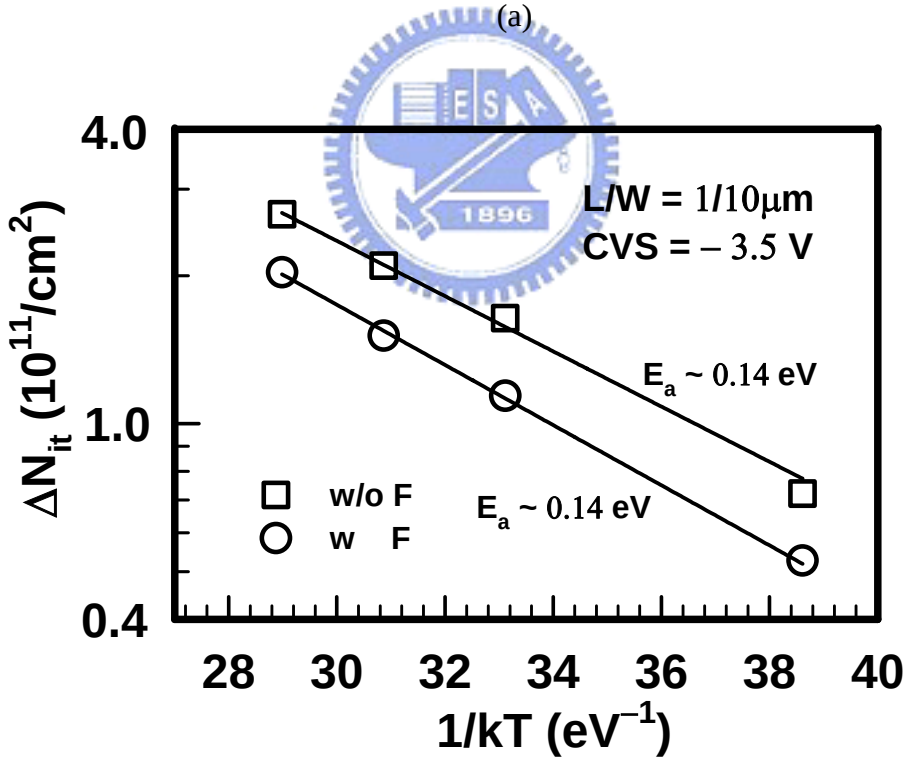


Fig. 2-29 Drain current degradation under saturation over stress time. Devices were stressed at different stress temperatures, V_g = – 3.5 V.



(a)



(b)

Fig. 2-30 Temperature dependence of (a) $\triangle V_{th}$ (b) $\triangle N_{it}$. NBT stress was applied under V_g = −3.5 V.

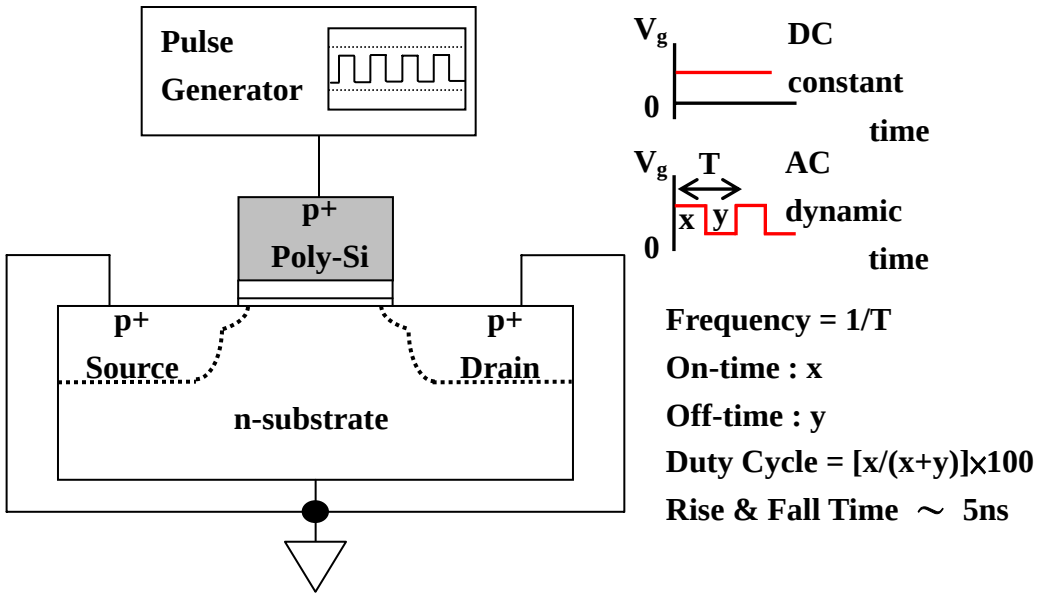
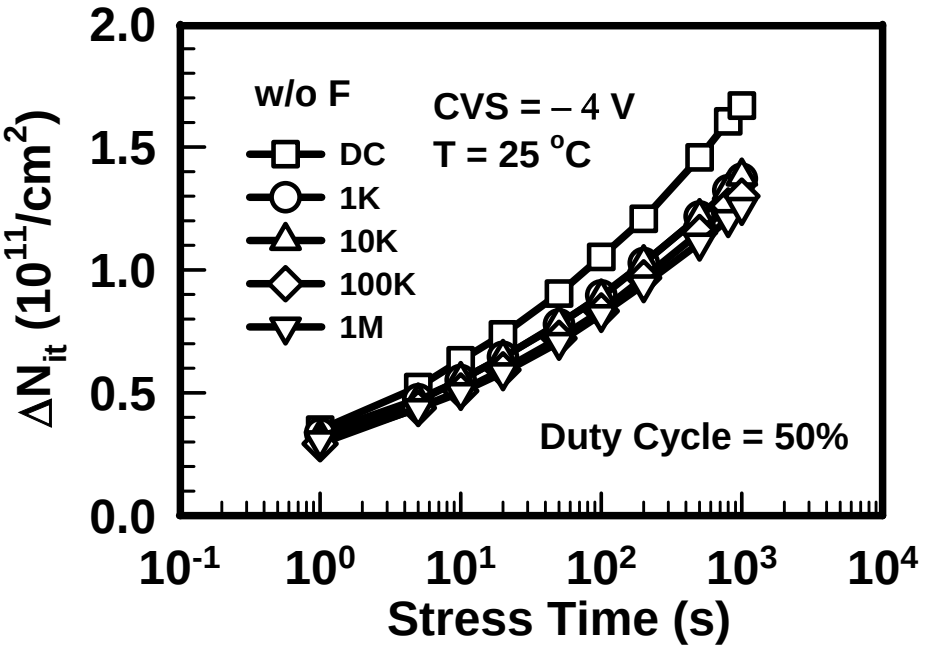
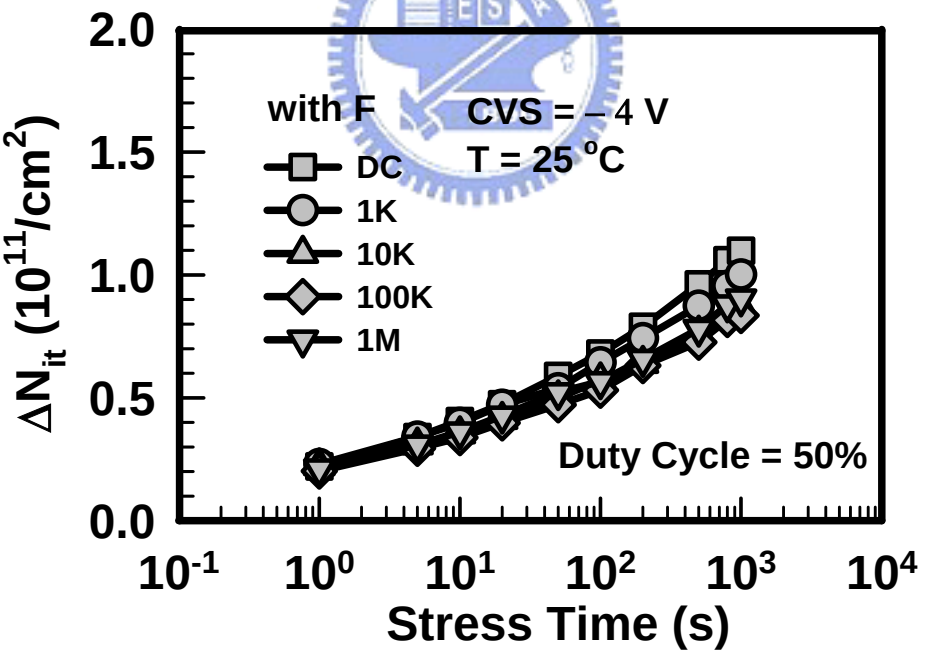


Fig. 2-31 Schematic setup and several parameters for measuring threshold voltage instability under AC dynamic stress.

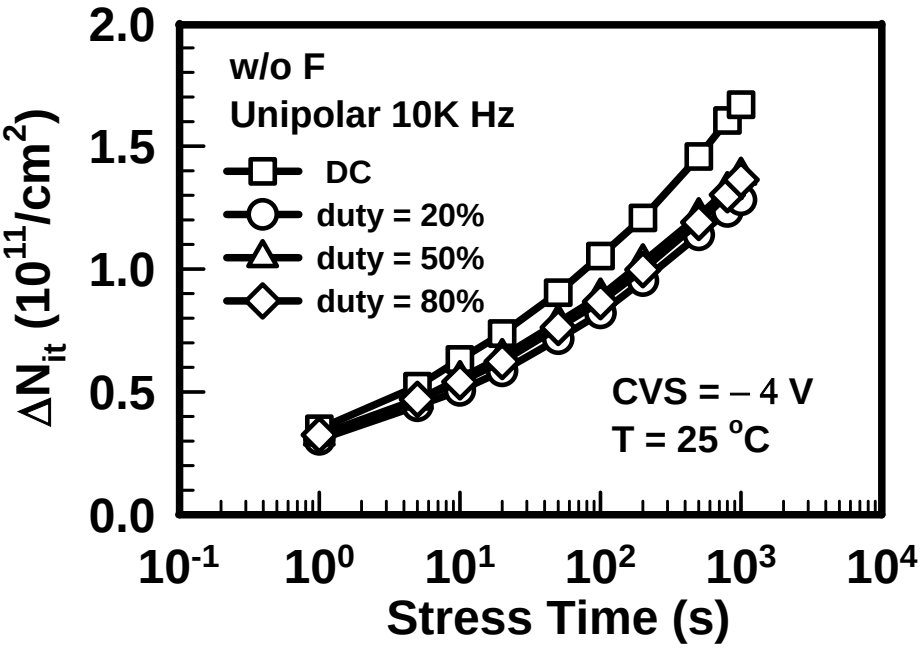


(a)

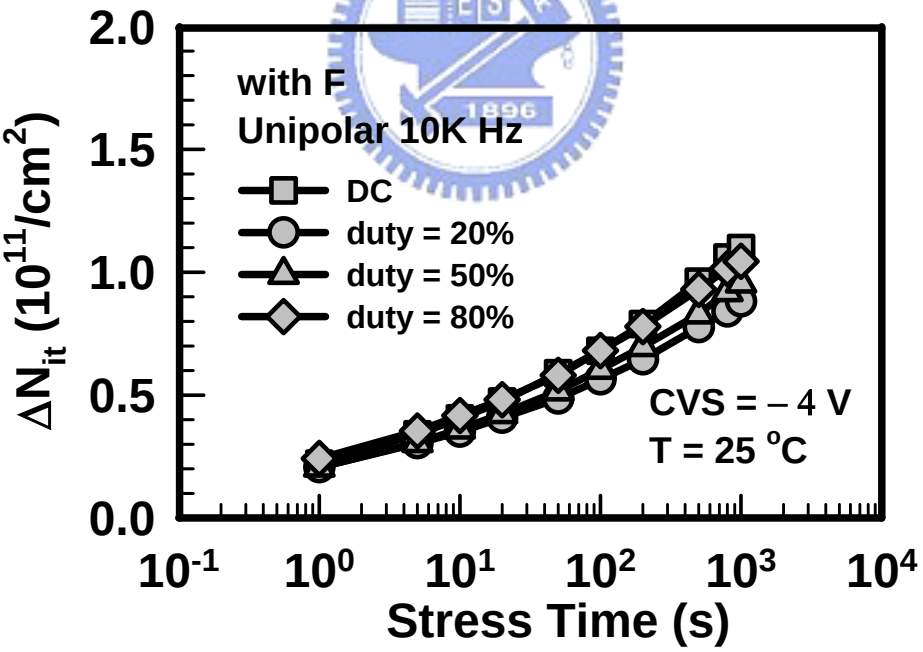


(b)

Fig. 2-32 N_{it} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different frequencies (a) w/o F sample, and (b) with F sample.

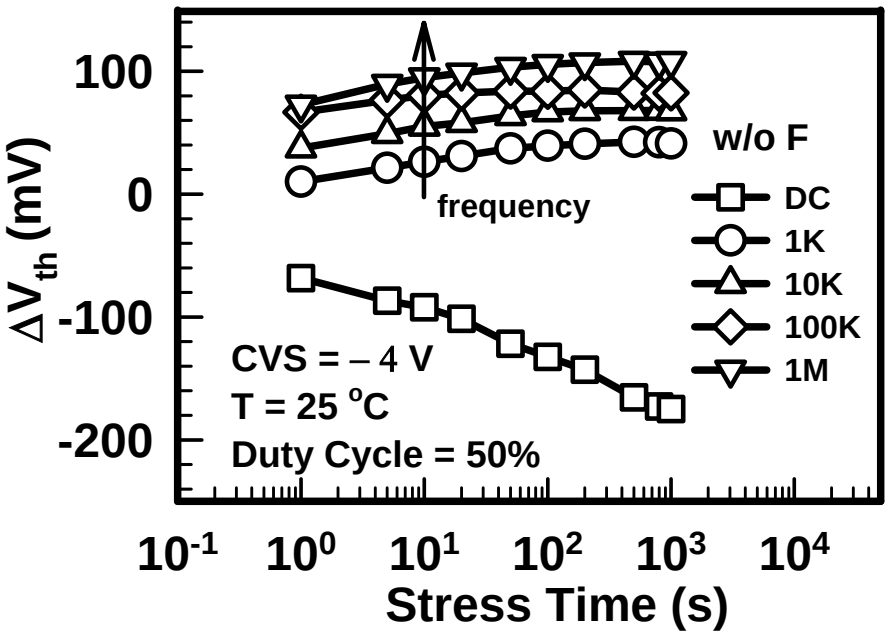


(a)

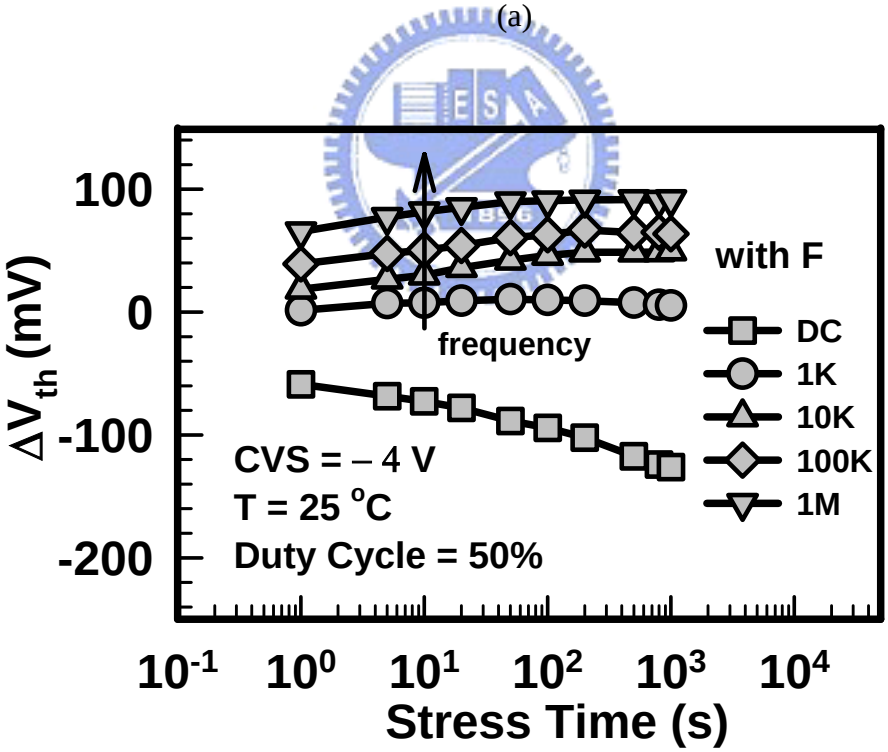


(b)

Fig. 2-33 N_{it} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different duty cycles (a) w/o F sample, and (b) with F sample.

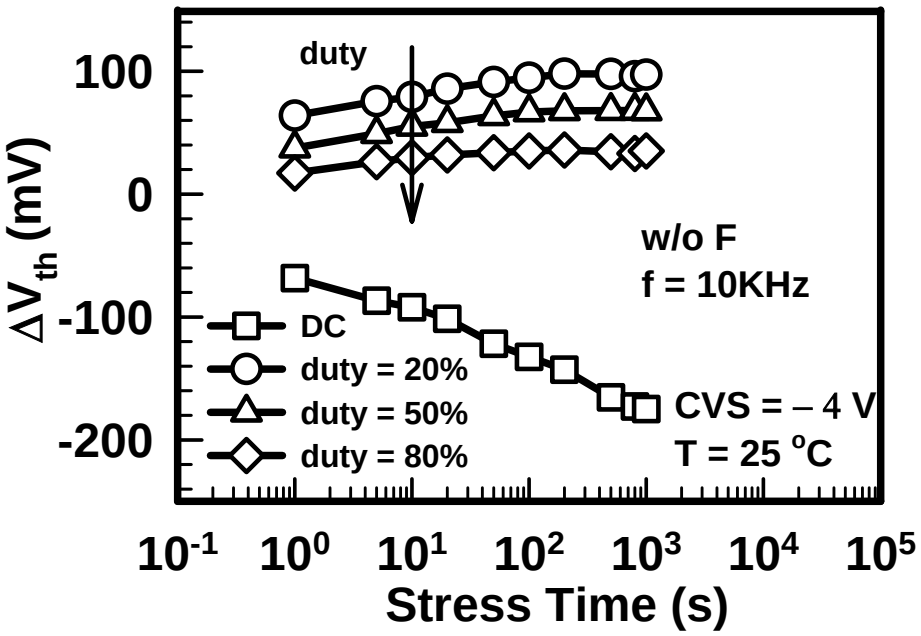


(a)

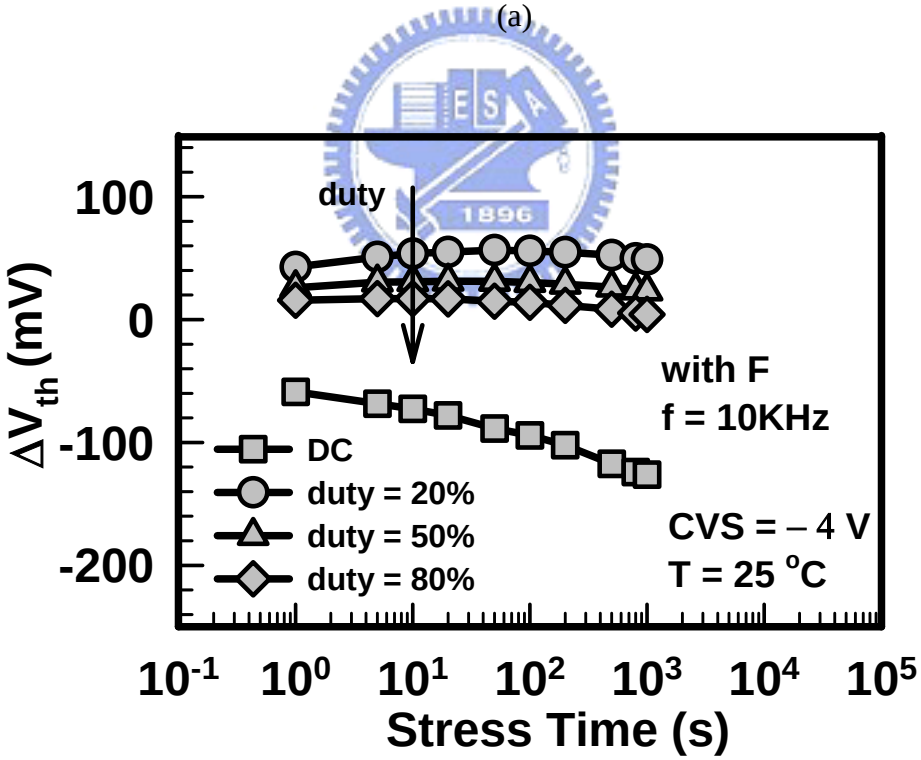


(b)

Fig. 2-34 V_{th} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different frequencies (a) w/o F sample, and (b) with F sample.

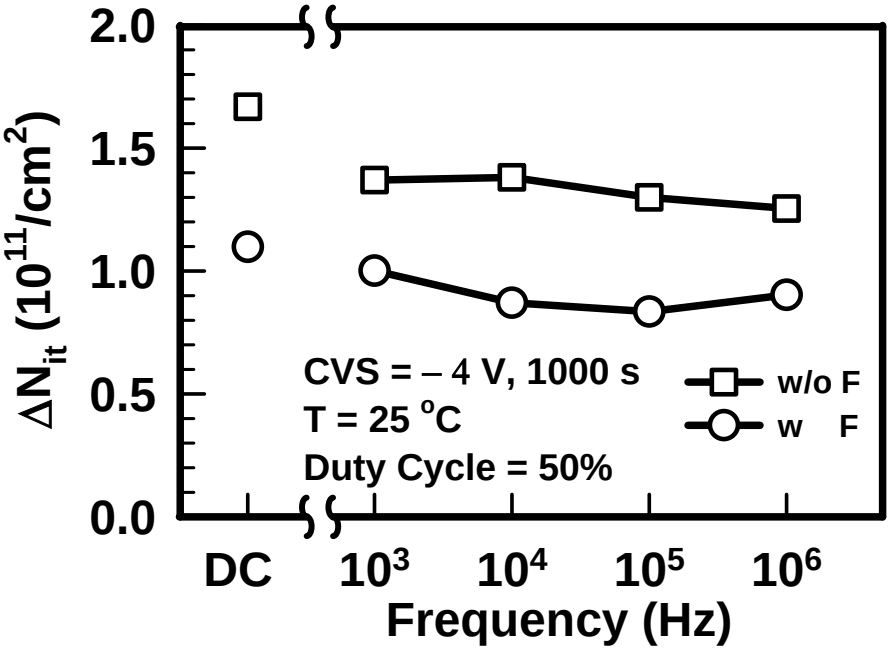


(a)

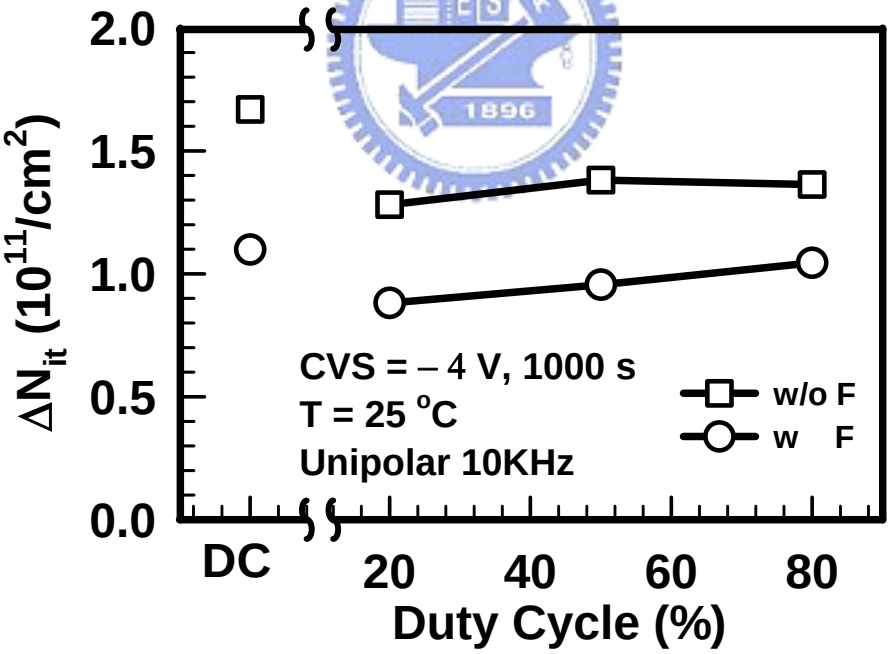


(b)

Fig. 2-35 V_{th} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different duty cycles (a) w/o F sample, and (b) with F sample.

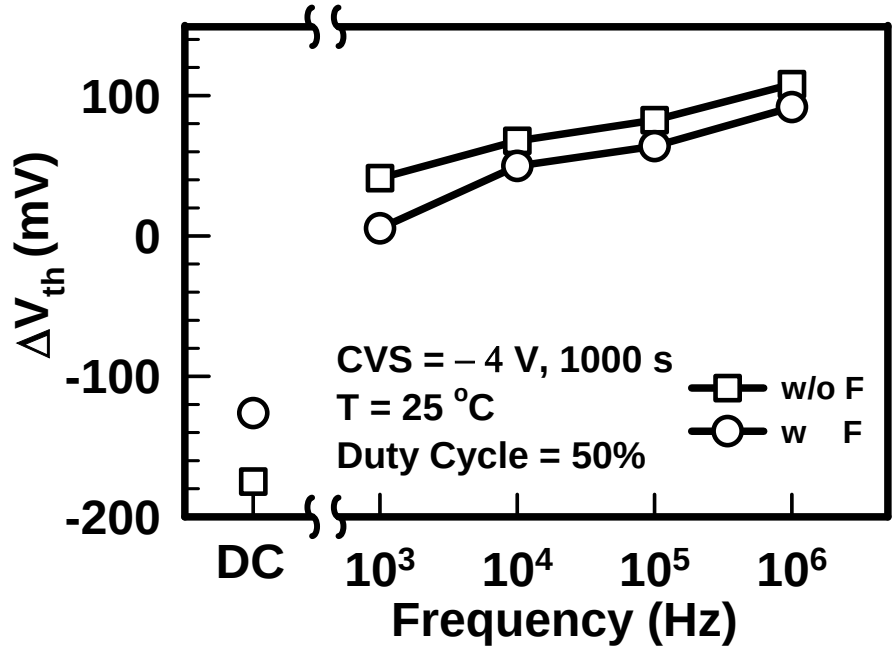


(a)

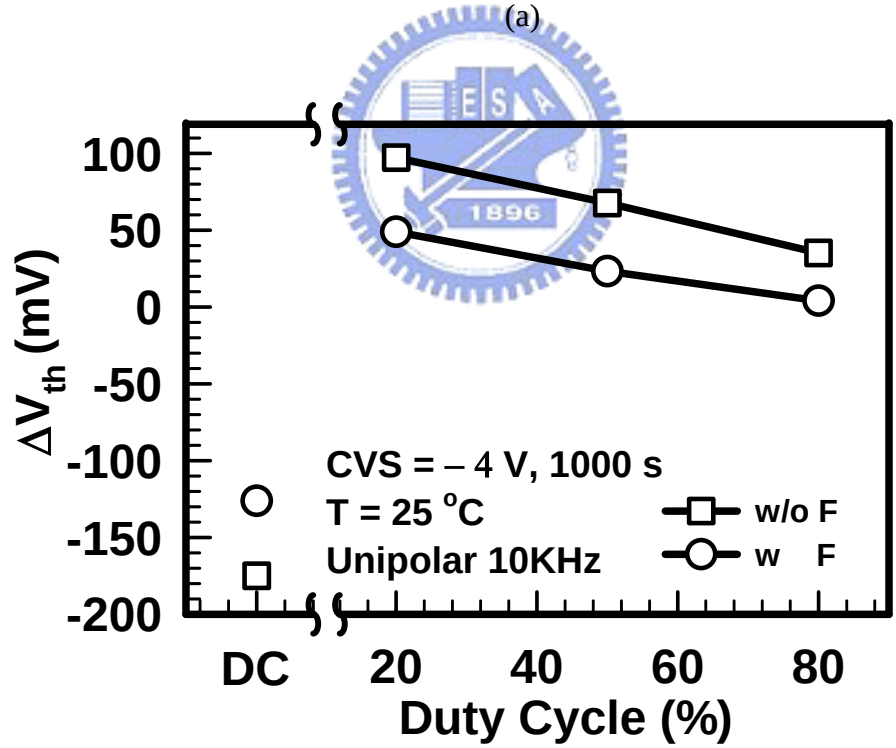


(b)

Fig. 2-36 (a) Frequency dependence of $\triangle N_{it}$, stressed at 25 °C, $V_g = -4$ V, duty cycle = 50% (b) Duty Cycle dependence of $\triangle N_{it}$, stressed at 25 °C, $V_g = -4$ V under unipolar 10KHz.



(a)



(b)

Fig. 2-37 Frequency dependence of $\triangle V_{th}$, stressed at 25 °C, $V_g = -4$ V, duty cycle = 50% (b) Duty Cycle dependence of $\triangle V_{th}$, stressed at 25 °C, $V_g = -4$ V under unipolar 10KHz.

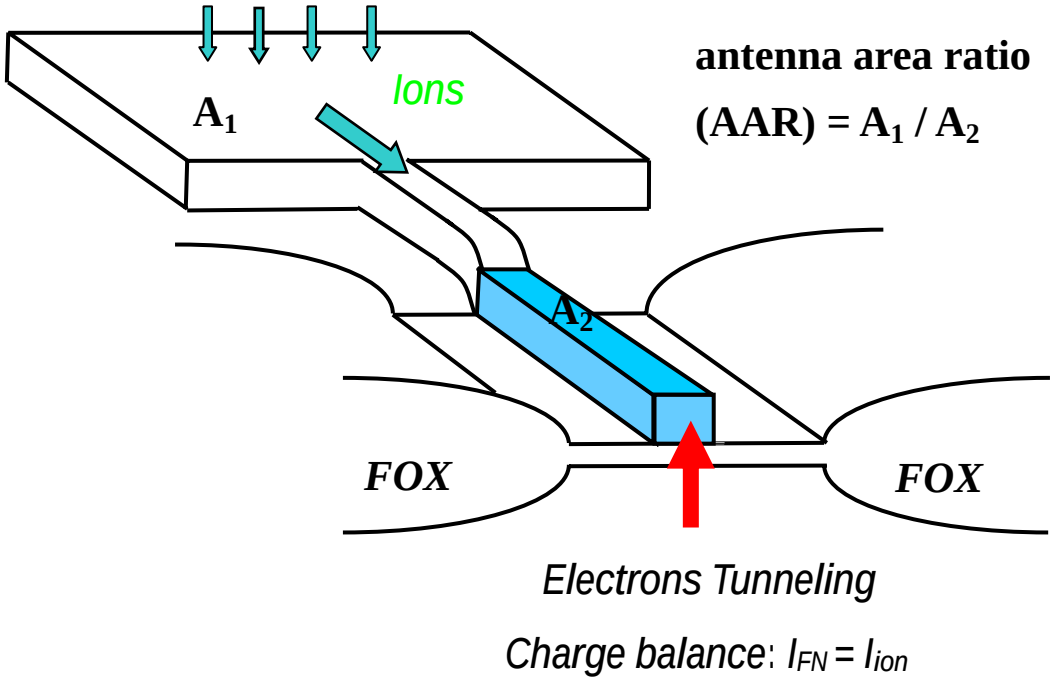
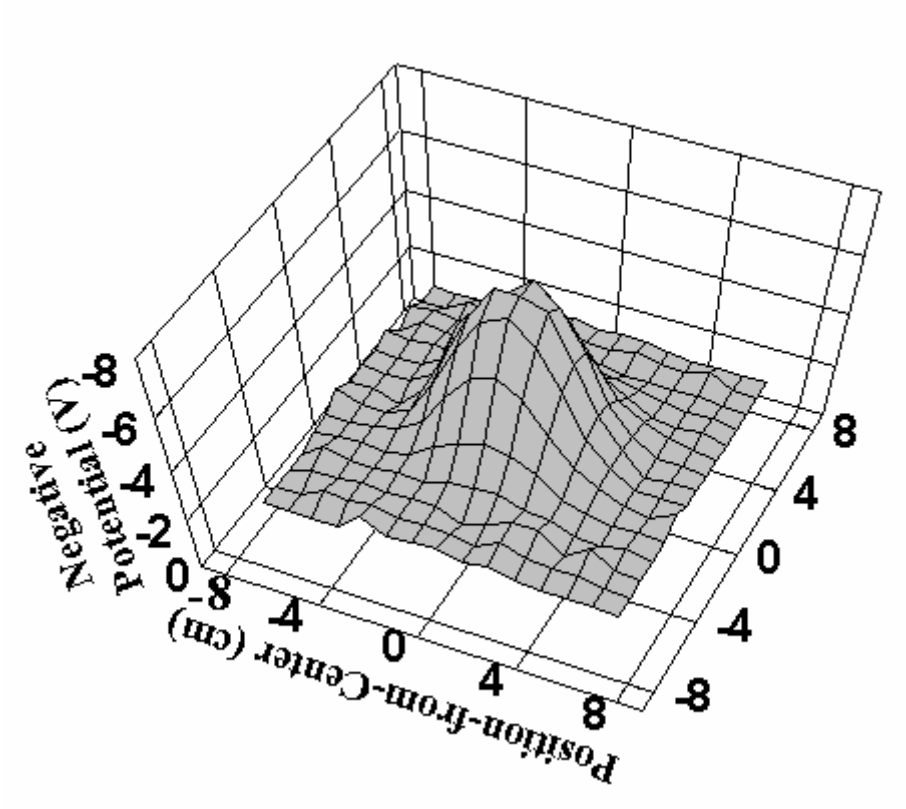
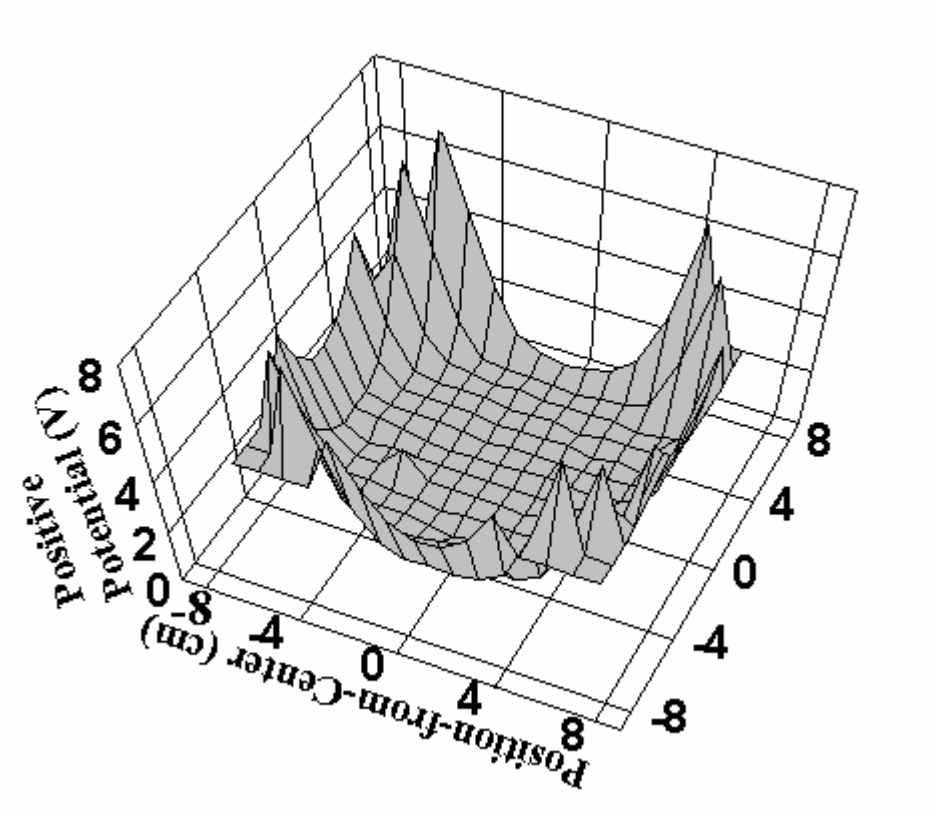


Fig. 3-1 Schematic of a transistor with area antenna.

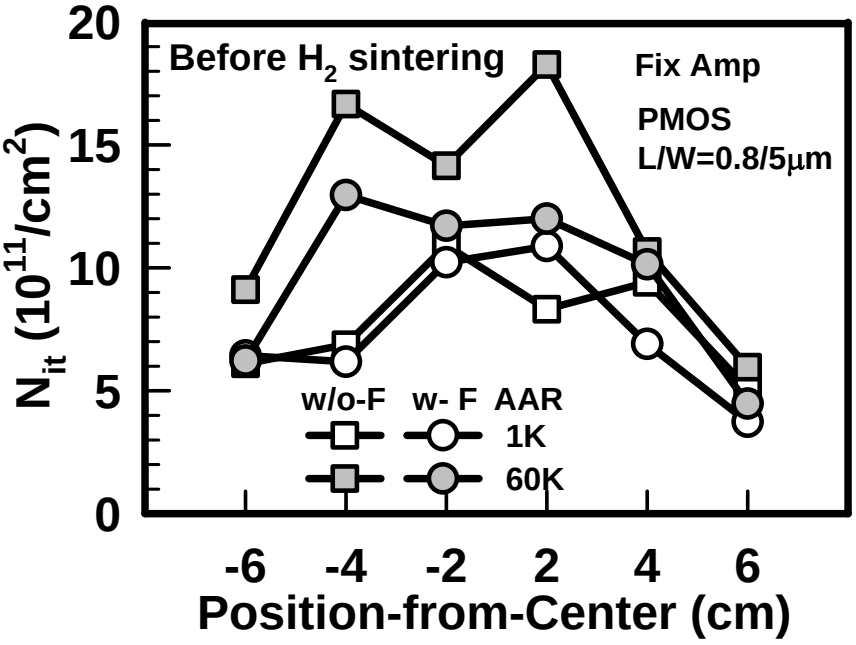


(a)

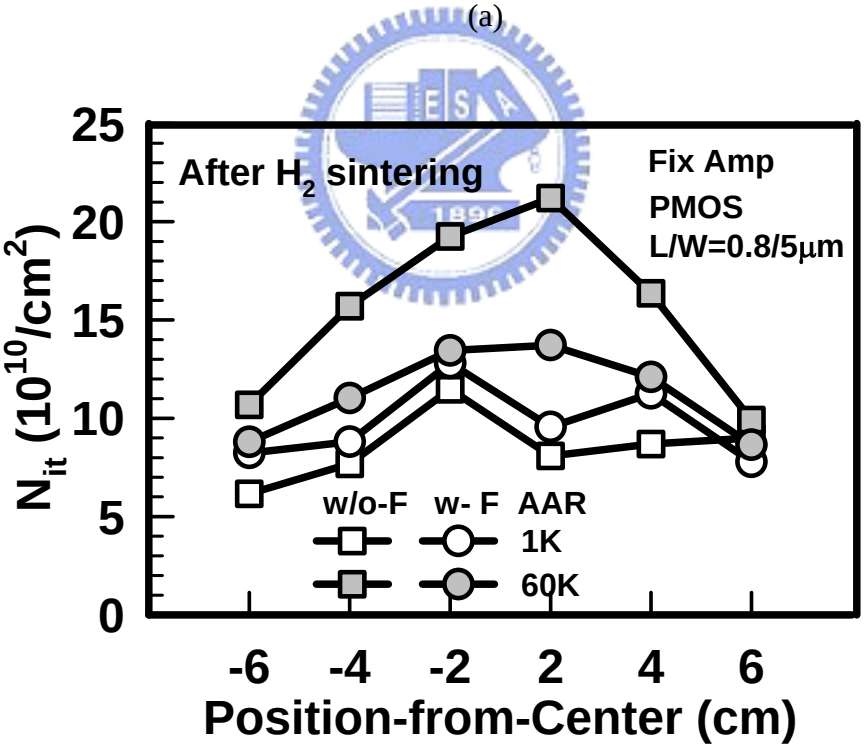


(b)

Fig. 3-2 Wafer mappings of (a) negative and (b) positive potential values recorded by CHARM-2 sensors.

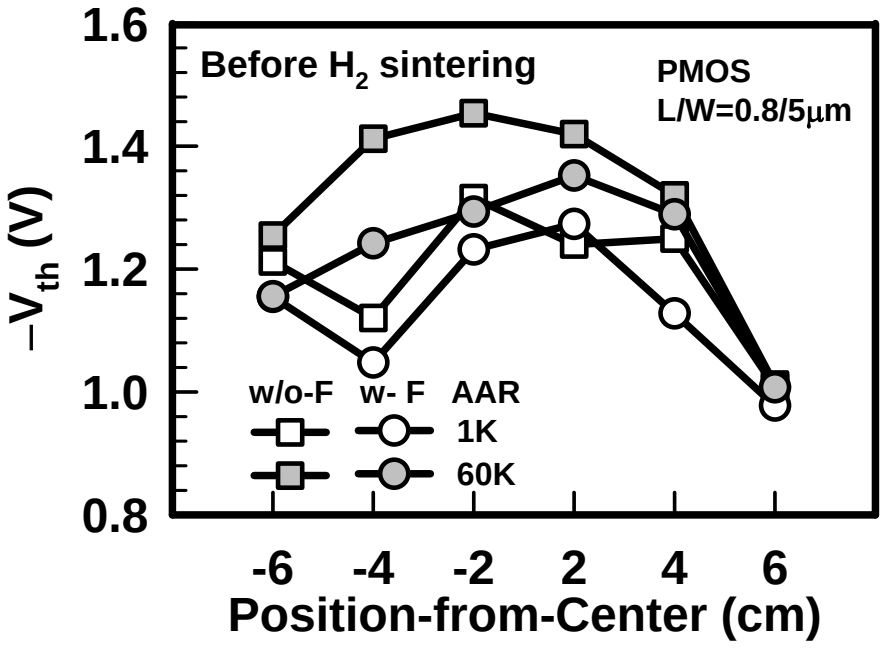


(a)

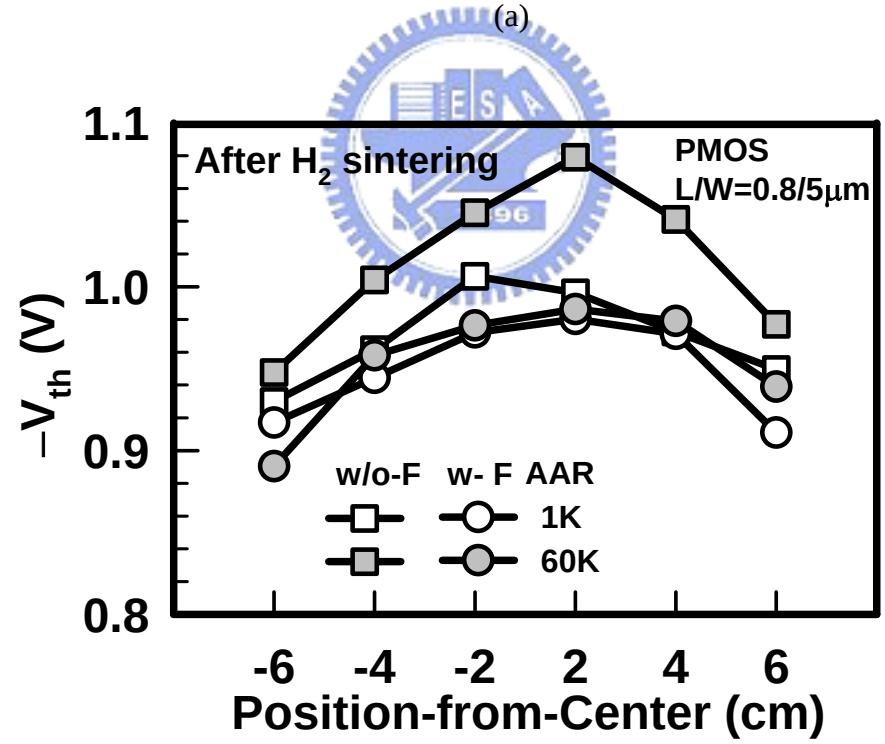


(b)

Fig. 3-3 N_{it} of PMOS devices (a) before sintering, and (b) after sintering, both as a function of device location on the wafer.

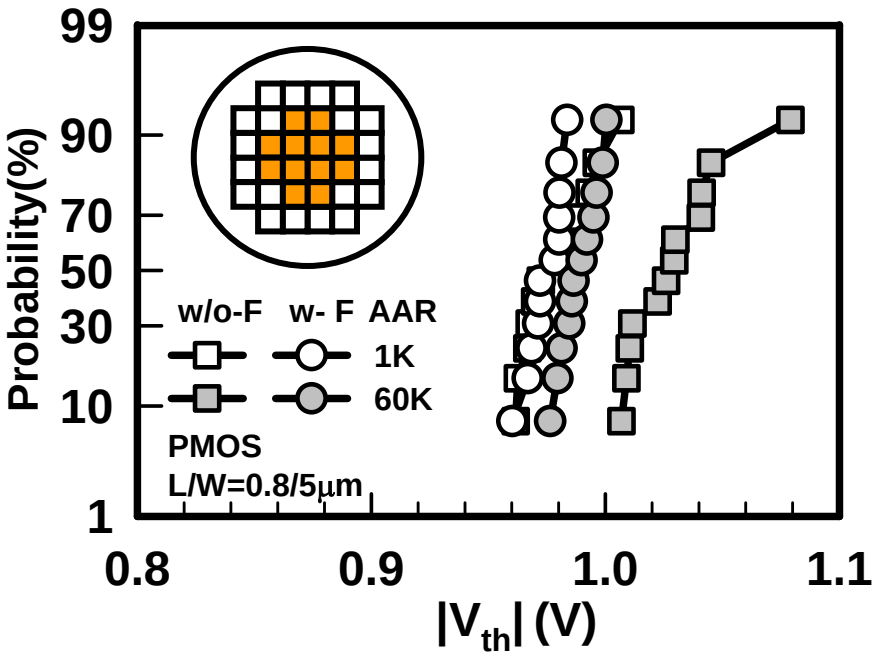


(a)

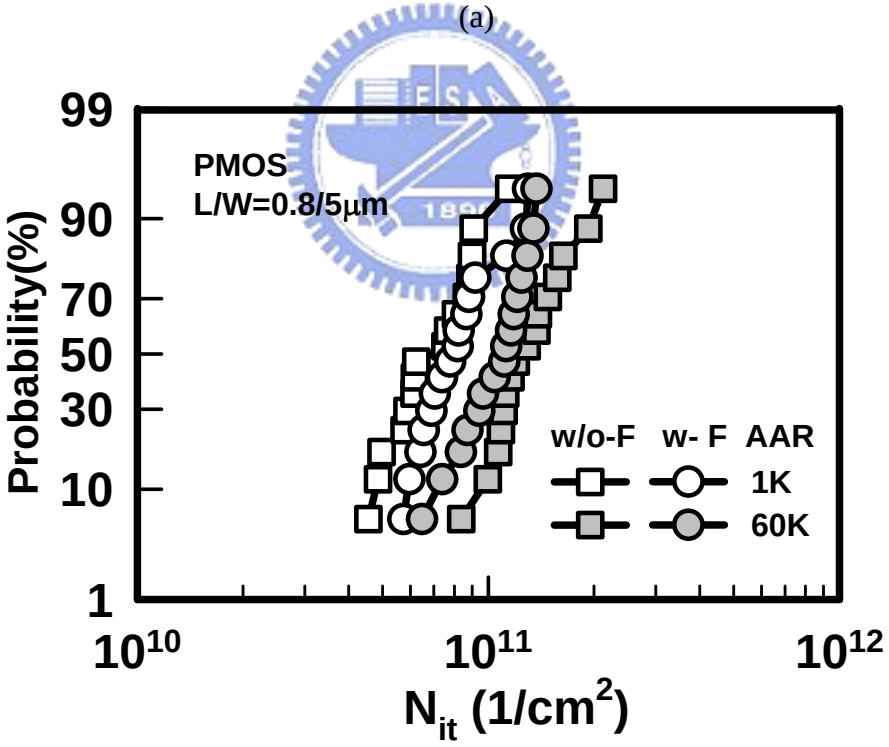


(b)

Fig. 3-4 V_{th} of PMOS devices (a) before sintering, and (b) after sintering, both as a function of device location on the wafer.



(a)



(b)

Fig. 3-5 Cumulative probability of the (a) threshold voltage (V_{th}), and (b) interface trap density (N_{it}).

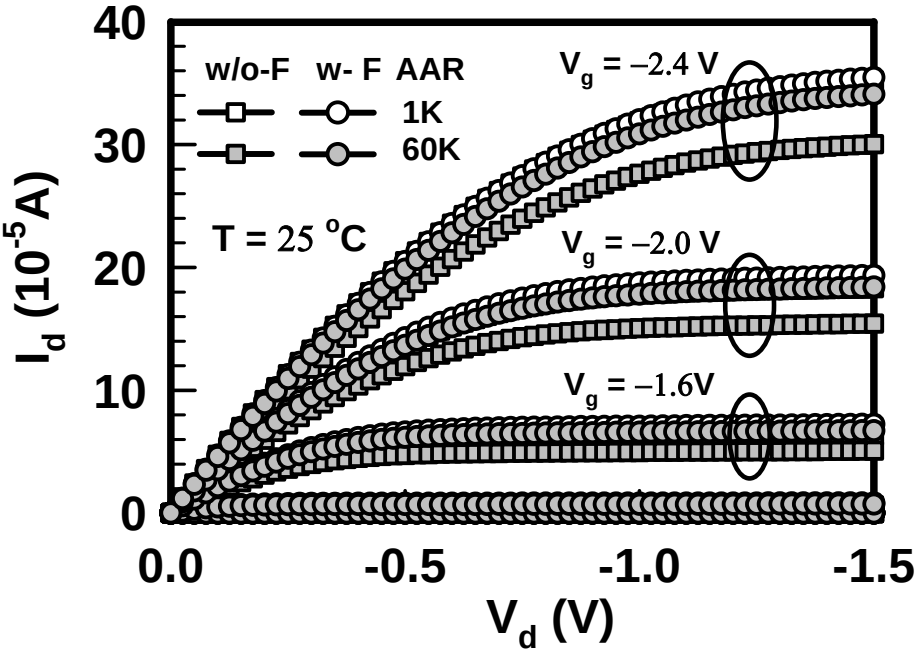
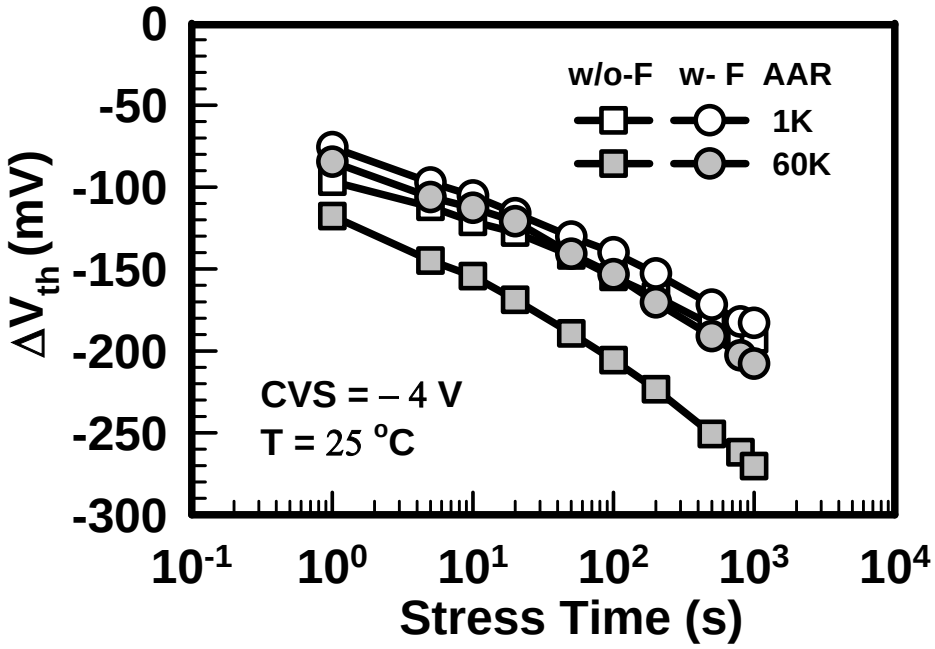
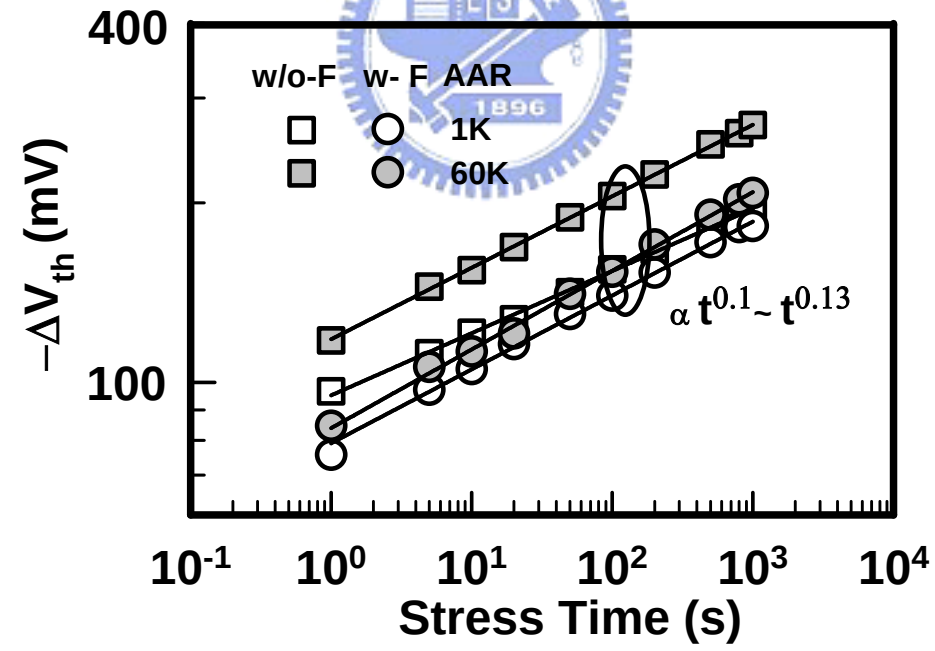


Fig. 3-6 Output characteristics for fresh devices with AARs of 1K and 60K.

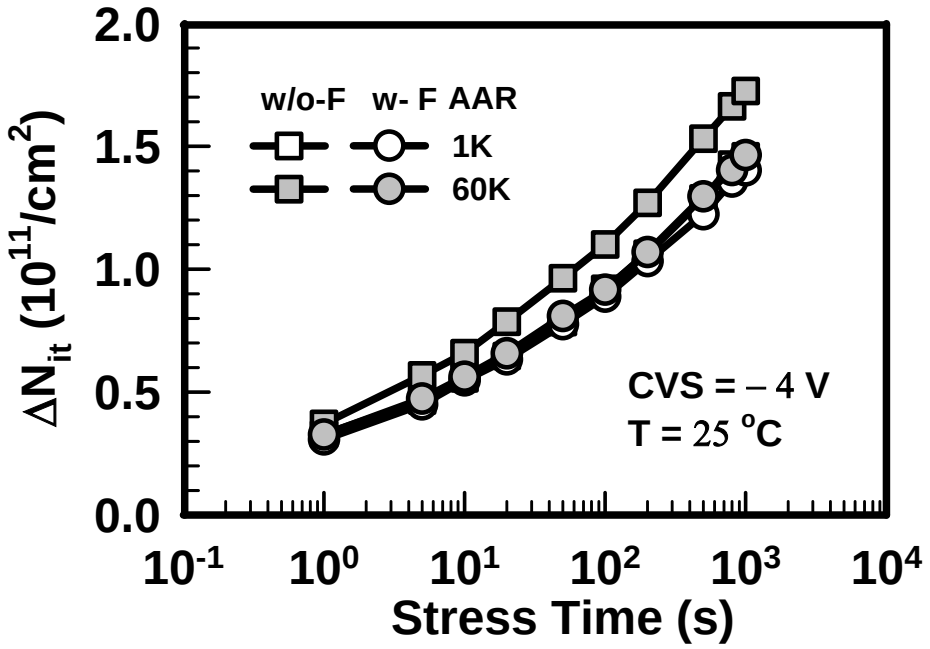


(a)

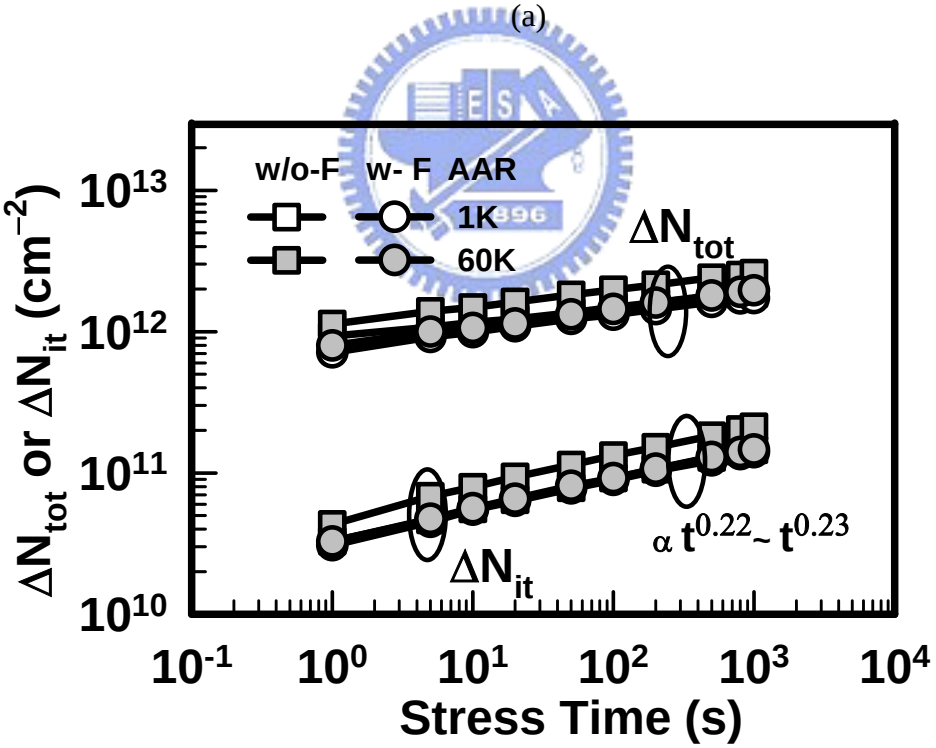


(b)

Fig. 3-7 Threshold voltage shift as a function of stress time, stressed at 25 °C, $V_g = -4$ V, plotted in (a) linear scale, and (b) logarithm scale.



(a)



(b)

Fig. 3-8 (a) Interface trap density shift, and (b) total trap density increase, as a function of stress time. Devices were stressed at 25 °C, V_g = — 4 V.

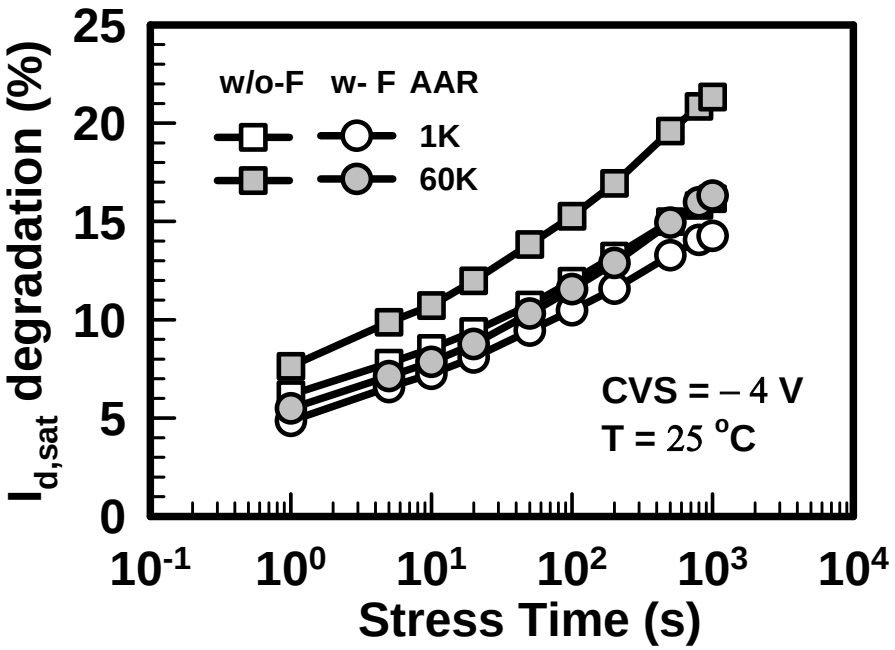
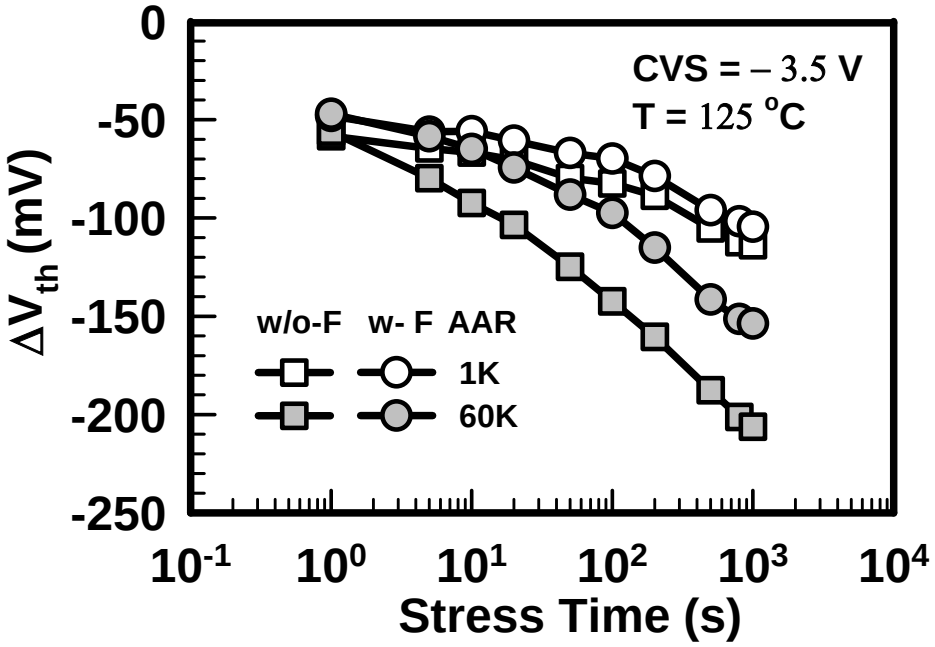
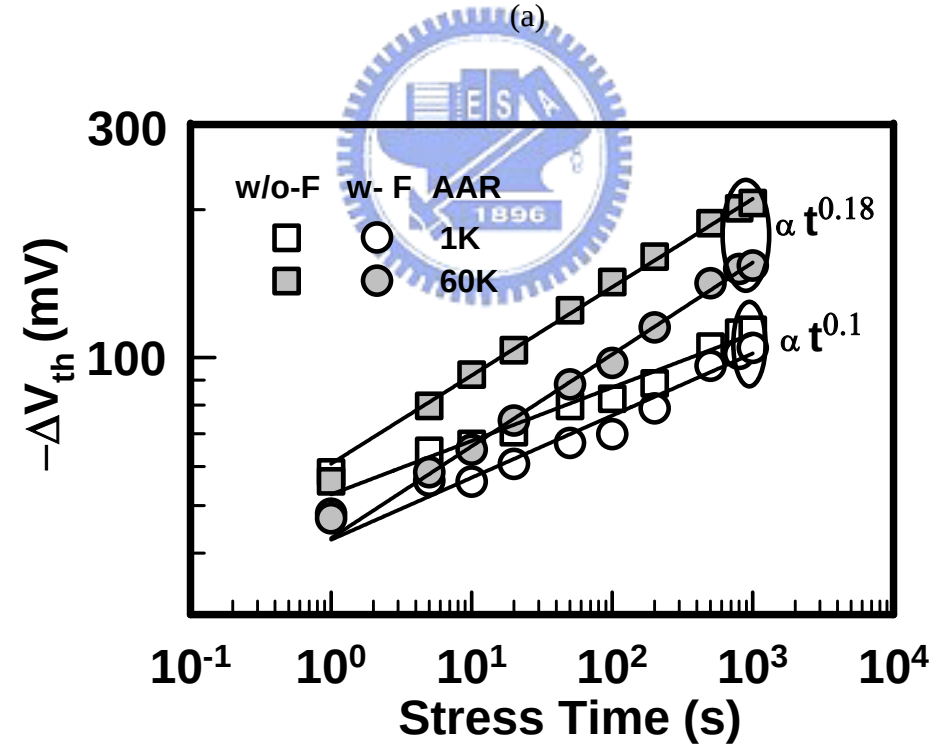


Fig. 3-9 Drain current degradation under saturation regime over stress time. Devices were stressed at 25 °C, V_g = – 4 V.

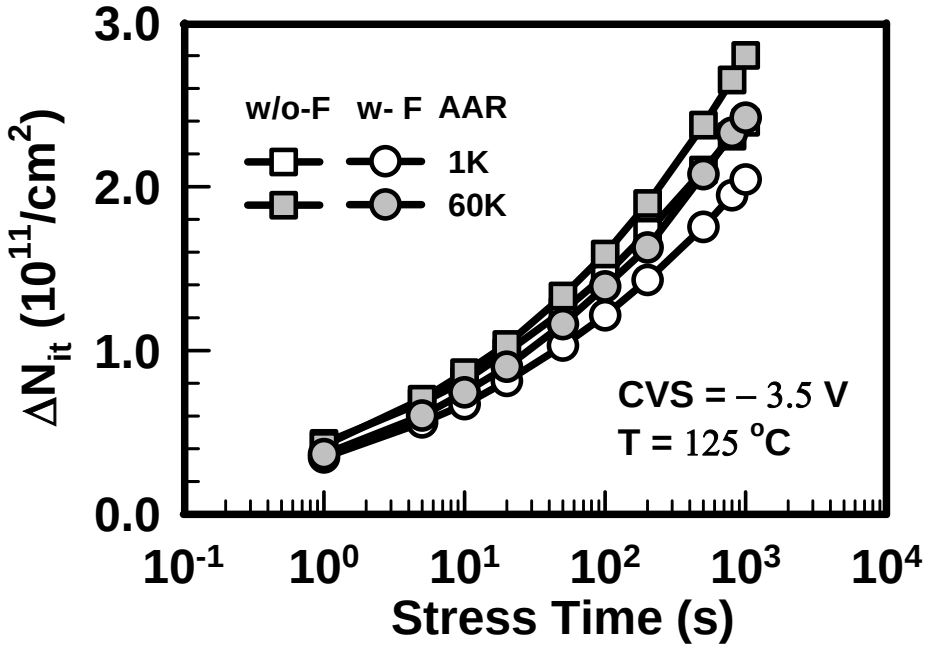


(a)

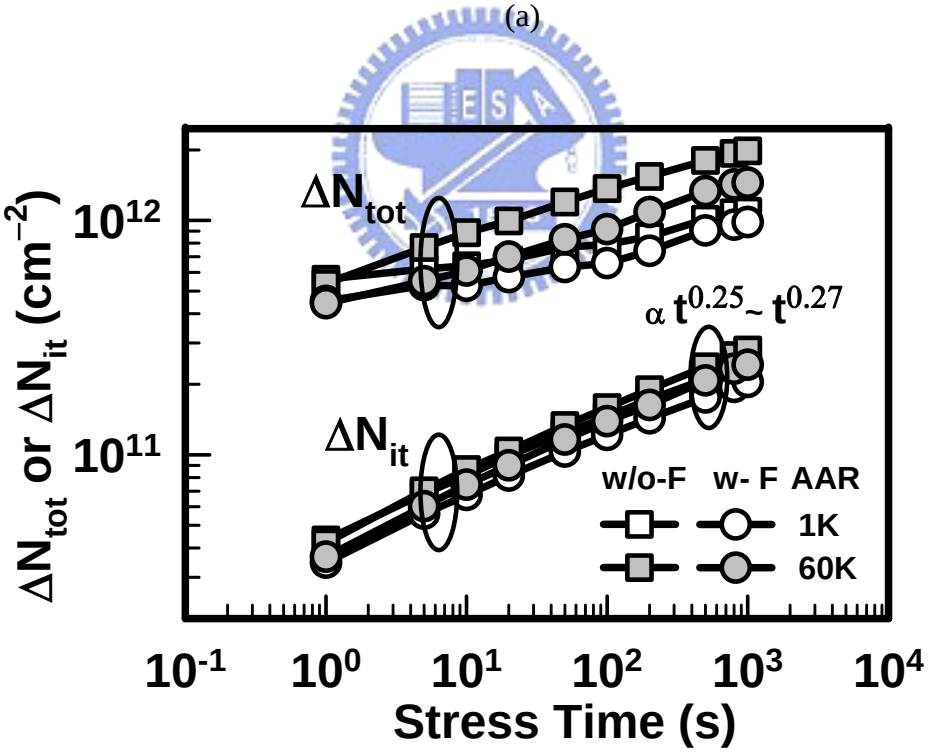


(b)

Fig. 3-10 Threshold voltage shift as a function of stress time, stressed at 125 °C, V_g = — 3.5 V, plotted in (a) linear scale, and (b) logarithm scale.



(a)



(b)

Fig. 3-11 (a) Interface trap density shift, and (b) total trap density shift as a function of stress time. Devices were stressed at 125 °C, V_g = — 3.5 V.

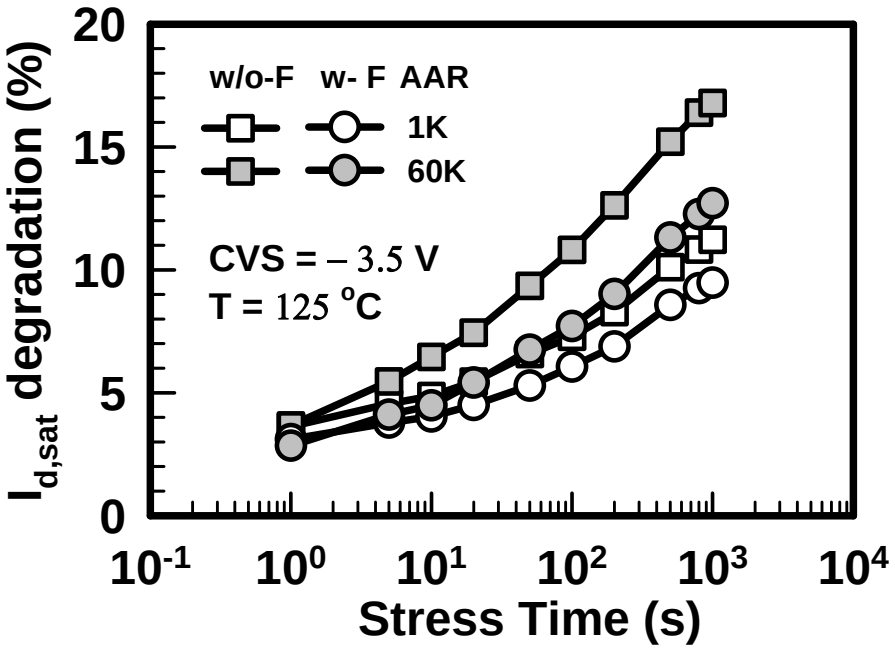
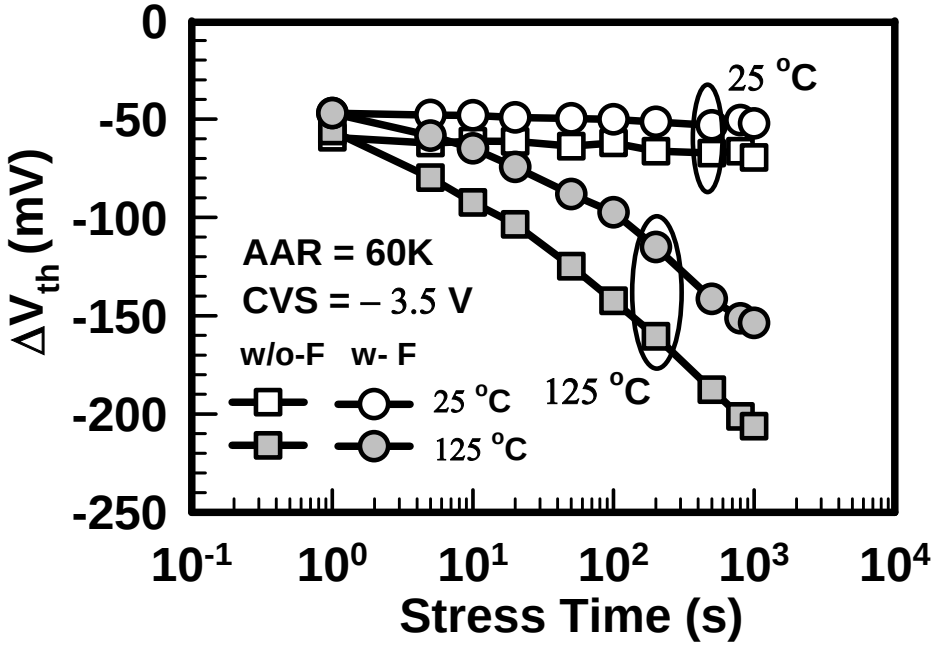
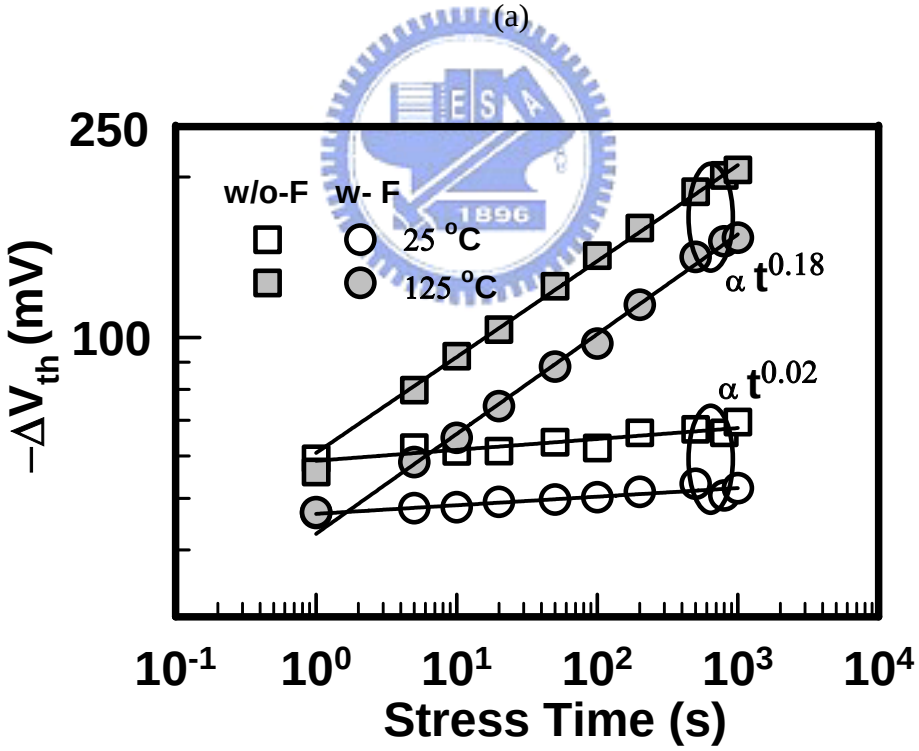


Fig. 3-12 Drain current degradation under saturation regime over stress time. Devices were stressed at 125 °C, V_g = – 3.5 V.

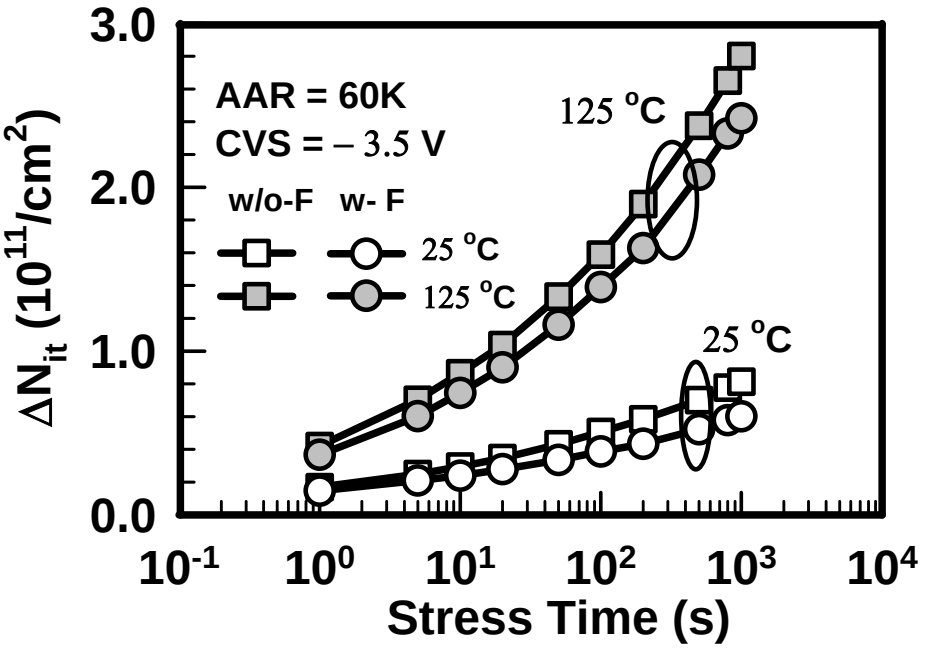


(a)

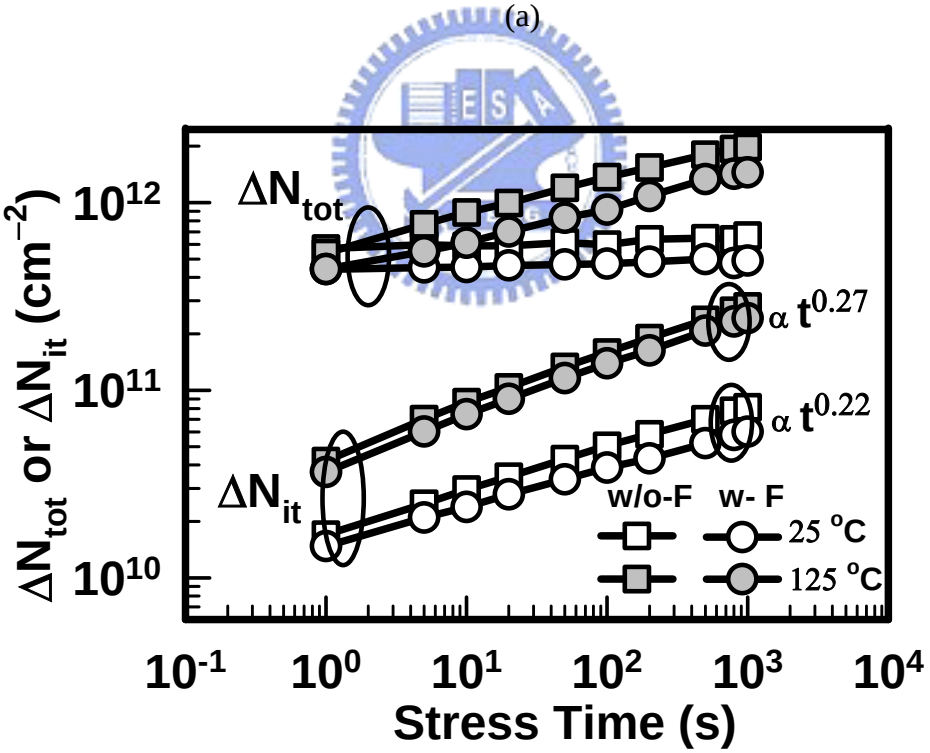


(b)

Fig. 3-13 Threshold voltage shift as a function of stress time under BTS at different stress temperatures, V_g = — 3.5 V and AAR of 60K, plotted in (a) linear scale, and (b) logarithm scale.



(a)



(b)

Fig. 3-14 (a) Interface trap density shift, and (b) total trap density shift as a function of stress time under BTS at different stress temperatures, $V_g = -3.5$ V. AAR is 60K.

簡歷

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碩士論文題目： 氟摻雜對二氧化鉿堆疊式閘極 P 型金氧半場效電晶體其可靠性的影響

Effects of Fluorine Incorporation on the Reliability Issues of pMOSFETs with HfO_2/SiON Gate Stack