國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

低溫複晶矽薄膜電晶體負偏壓溫度不穩定與天線效應之研究

Study on Negative Bias Temperature Instability and Antenna Effect of Low-Temperature Polycrystalline Silicon Thin-Film Transistors

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博士論文

A Dissertation
Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
In Partial Fulfillment of the Requirements
For the Degree of
Doctor of Philosophy
in
Electronics Engineering
September 2007
Hsinchu, Taiwan, Republic of China

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摘　要

此論文探討了低溫複晶矽薄膜電晶體(LTPS TFTs)的可靠度，包含了負偏壓溫度不穩定(NBTI)與天線效應(antenna effect)。此外，我們也針對天線效應對低溫複晶矽薄膜電晶體負偏壓溫度不穩定的影響進行探討。最後，我們提出一個新模型來解釋負偏壓溫度不穩定與熱載子效應(hot-carrier effect)相結合下對元件特性的影響。

首先，我們證實負偏壓溫度不穩定對 p 型通道低溫複晶矽薄膜電晶體可靠度而言是重要的可靠度問題，在負偏壓溫度不穩定應力(NBTI stress)測試下，我們發現臨界電壓漂移(threshold-voltage shift)與晶界缺陷態位(grain-boundary trap states)和界面缺陷態位(interface trap states)的產生息息相關，實驗結果也顯示，低溫複晶矽薄膜電晶體之負偏壓溫度不穩定劣化機制可由 diffusion-controlled electrochemical reactions 來解釋。此外，我們也分析臨界電壓回復(threshold-voltage recovery)，並且推論此回復是由 diffusion-controlled electrochemical reactions 的逆反應所造成。我們藉由修改傳統金氧半

場效電晶體(MOSFET)的負偏壓溫度不穩定模型，提出了一個新模型來解釋低溫複晶矽薄膜電晶體負偏壓溫度不穩定的劣化機制。我們也利用電荷幫浦(charge pumping)的技術來探討此劣化機制，分析出基底(bulk)缺陷態位的特性(包含晶界缺陷態位與界面缺陷態位)，並萃取出固定氧化層電荷(fixed oxide charge)的密度。因此，低溫複晶矽薄膜電晶體之負偏壓溫度不穩定劣化機制更確信是由界面缺陷態位、晶界缺陷態位與固定氧化層電荷的產生所造成。

接著，我們針對低溫複晶矽薄膜電晶體設計不同的天線結構，來探討天線效應對元件特性和可靠度的影響。實驗結果發現，當元件具有較大的天線面積時，元件特性會發生不穩定的現象，特別是造成臨界電壓的不均勻分佈，另外在閘極偏壓應力(gate-bias stress)與熱載子應力下也有較差的可靠度。此外，我們也研究天線效應對負偏壓溫度不穩定的影響，並發現天線效應會加速負偏壓溫度不穩定的程度，導致元件有較差的臨界電壓、次臨界擺幅(subthreshold swing)、場效載子遷移率(field-effect mobility)和驅動電流(drive current)。

最後，我們研究 p 型通道低溫複晶矽薄膜電晶體在負偏壓溫度不穩定與熱載子應力測試下的劣化機制。在固定的閘極電壓應力下，我們探討在不同的汲極電壓應力對元件劣化的影響。實驗結果顯示，在低的汲極電壓應力下，元件的劣化主要是負偏壓溫度不穩定所主導；在高的汲極電壓應力下，負偏壓溫度不穩定會被抑制，元件劣化機制轉由熱載子應力所主導。為了定量分析負偏壓溫度不穩定與熱載子應力兩者對元件所造成的劣化，我們針對負偏壓溫度不穩定與熱載子應力的模型加以修改，並提出了一個與實驗結果相吻合的新模型。

Study on Negative Bias Temperature Instability and Antenna Effect of Low-Temperature Polycrystalline Silicon Thin-Film Transistors

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ABSTRACT

In this thesis, the reliability of low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) was studied, including negative bias temperature instability (NBTI) and antenna effect. In addition, the impacts of antenna effect on the NBTI behaviors of LTPS TFTs were explored. Finally, a new model was proposed to explain the combined NBTI and hot-carrier effects on the device characteristics.

First, NBTI is demonstrated to be an important reliability issue in *p*-channel LTPS TFTs. The threshold-voltage shift of LTPS TFTs under NBTI stress is highly correlated to the generation of both the grain-boundary and interface trap states. Experimental results show that the NBTI-degradation mechanism can be explained by diffusion-controlled electrochemical reactions. Besides, the recovery of the threshold-voltage shift was also

analyzed and found to be the reverse process of diffusion-controlled electrochemical reactions. By expanding the model proposed for metal-oxide-semiconductor field-effect transistors (MOSFETs), a new model is introduced to explain the NBTI-degradation mechanism of LTPS TFTs. The mechanism is also analyzed by a charge-pumping technique to directly characterize the bulk trap properties (including grain-boundary and interface trap-state density) in LTPS TFTs. The fixed-oxide-charge density is also extracted and the NBTI degradation can therefore be confirmed to be caused by the generation of interface trap states, grain-boundary trap states and fixed oxide charges.

Second, LTPS TFTs having different antenna structures were used to study the influence of antenna effect on the performance and reliability of the devices. Experimental results show that performance instability of the devices occurs for those samples having relatively large-area antennas, especially causing non-uniform distribution of the threshold voltages. Devices having larger antenna areas also show a more degraded reliability under gate-bias stress and hot-carrier stress (HCS) than those of the samples having smaller antenna areas. In addition, the impact of the antenna effect on the NBTI behavior of LTPS TFTs is investigated. The antenna effect accelerates NBTI, and results in an enhanced degradation of threshold voltage, subthreshold swing, field-effect mobility and drive current.

Finally, degradation mechanisms of *p*-channel LTPS TFTs upon NBTI and HCS were investigated. Under a fixed stress gate voltage, the dependence of the device degradation on the stress drain voltage was analyzed. At a low stress drain voltage, the device degradation is dominated by the NBTI; at a high stress drain voltage, NBTI is retarded, and HCS dominates the degradation. To quantify the combined effects of NBTI and HCS, a modified model, based on the empirical NBTI and HCS models, is proposed, which is demonstrated to be consistent with the experimental results.

誌 謝

此論文的完成，要感謝的人實在太多了！沒有眾人的支持與鼓勵，就無法成就這一切。首先，感謝我的指導教授－雷添福博士，對我的指導與教誨，讓我學習到研究的態度及方法，更重要的是教導我待人處世之道，令我獲益良多。

感謝王獻德學長的提攜，帶我進入薄膜電晶體的領域，並提供新穎的研究方向；感謝統寶光電林孝義學長、葉冠麟學長及陳維成學長，在百忙之中提供實驗上的協助；感謝李介文學長，在我研究遇到瓶頸時提供寶貴的意見；還要感謝伯浩和統億，在實驗量測上的協助及實驗數據上的分析，此論文是我們一起努力的成果。

感謝在研究中曾給我幫助的前輩們，特別是元件計測實驗室的彭作煌先生、電子教學實驗室的彭兆光先生，與奈米中心的徐秀鑾小姐、黃月美小姐、林素珠小姐、楊月嬌小姐、范秀蘭小姐、陳悅婷小姐、何惟梅小姐、劉曉玲小姐，以及國家奈米元件實驗室的工程師們，因為有你們的大力幫忙，讓我在研究及學習上事半功倍，在此獻上我最深的敬意。

感謝薄膜與量測實驗室的所有人員：李名鎮學長、余正明學長、李宗霖學長、王哲麒學長、謝明山學長、陳建豪學長、楊紹明學長、游信強學長、林育賢學長、郭柏儀學長、謝德慶學長、李美錡學姐、賴久盟學長、謝松齡學長、羅韋翔學長、林余俊學長和江國誠學長，感謝你們帶我進入半導體領域，並給予指導與勉勵。感謝同窗好友家文及任逸，在課業上的砥礪及生活上的協助。感謝小馬、俊嘉、宗元、源竣、梓翔、錦石、仕傑、文呈、久騰、明爵、哲綸、子恆、張婷、冠良、文彥、小春、伊容，實驗室因為有你們而充滿歡樂，並陪我度過漫長的研究歲月。

由衷感謝我敬愛的父母，陳忠明先生與呂綿女士，感謝你們提供一個溫暖的家，以及二十多年來的養育之恩，由於你們的付出，我才能無後顧之憂地完成學業；感謝大哥炫文、大嫂詩茹、二哥峰志、二嫂春蘭，在學業上的支持與生活上的照顧；感謝女友青燕，在精神及生活上給我莫大的關心與扶持，讓我非常感動。

謹以此論文，獻給我的家人，及所有關心我的朋友

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Chapter 1

Introduction

1.1 Overview of Thin-Film Transistors

Although the concept of a thin-film field-effect transistor was presented as early as 1935 [1.1], the first functional thin-film transistor (TFT) was reported by P. K. Weimer in 1961 [1.2]. Fig. 1.1 shows the cross-sectional and top views of the first TFT in literature, which is composed of a microcrystalline cadmium sulfide (CdS) semiconductor layer, a gate dielectric layer, with gold (Au) source, drain, and gate electrode [1.3]. After that, TFTs have been intensively researched for possible electronic and display applications. The first active-matrix liquid-crystal display (AMLCD) was composed of CdSe TFTs and nematic liquid crystal [1.4]. Although there are many successful demonstrations of CdSe TFT LCDs, the industry did not fly until the report on the feasibility of doping amorphous Si (α-Si) by the glow discharge technique in 1975 was introduced [1.5].

Since then, α-Si TFT LCDs have become the standard for mass-produced AMLCDs for several reasons. First, the characteristics of α-Si TFTs are remarkably well matched to the requirements of liquid-crystal driving, since they have a low OFF current with good ON/OFF ratios. Second, both the gate insulator and the α-Si layers can be deposited in the same plasma-enhanced chemical vapor deposition (PECVD) system, so that contamination of the critical interface can be avoided. Finally, α-Si TFTs can be made at low temperatures (250－350 ^{o}C), thus allowing the use of inexpensive glass substrates [1.6].

However, there are some drawbacks of the α-Si TFTs. The most serious drawback is the low carrier mobility of the α-Si TFT, which is in the range of 0.5－1.0 cm^2/Vs. This makes

α-Si TFTs sufficient only for switching devices for each pixel in a display, and cannot meet the desired specifications for high-resolution panels. In addition, the α-Si TFT is not compatible with the CMOS process.

1.1.1 Advantages of Poly-Si TFTs

The problem of the low carrier mobility for the α-Si TFTs can be overcome by introducing polycrystalline silicon (poly-Si) instead of α-Si as a semiconductor layer of TFTs. In addition to a high carrier mobility, there are several advantages of poly-Si TFT LCD. First, the driver circuitry can be integrated on the display's substrate to realize the system on panel (SOP). Therefore, the size of the total panel and cost, including drivers and related processes, is reduced compared to the α-Si TFT LCDs. Second, the driver contact number of the poly-Si TFT LCD is more than one order of magnitude smaller than that of the α-Si:H TFT LCD. Third, the poly-Si TFT plate has a smaller pixel size and larger aperture ratio in each pixel than that of the α-Si:H TFT plate. Higher mobility means that the pixel charging can be achieved by a smaller-sized TFT, so that it contributes more pixel area for light transmission. Finally, a TFT LCD with self-alignment and CMOS process compatibility can be achieved [1.7], [1.8].

According to the process temperature, there are high-temperature and low-temperature poly-Si TFTs. The process temperatures of low-temperature poly-Si TFTs are as high as 900 ^{o}C, thus, expensive quartz substrates are required. Due to the limited profitability of quartz substrate size, most typical applications for high-temperature poly-Si TFT-LCDs are panels for projection displays, because the panel size is limited to small sizes. For low-temperature poly-Si TFTs (LTPS TFTs), since the maximum fabrication temperature is below 600 ^{o}C, low-cost glass substrates could be used which could lead to the production of large-area displays such as monitors and televisions [1.9]. Therefore, LTPS TFTs have attracted more and more attention due to their increasing application in high-resolution flat displays such as

active-matrix liquid-crystal displays (AMLCDs) [1.10]－[1.14], and active-matrix organic light-emitting diode (AMOLED) displays [1.15]－[1.18].

1.1.2 Crystallization of α-Si Thin Films

Among the many barriers to the low-temperature process of LTPS TFTs, the formation of poly-Si films is the most important one. There are several ways to fabricate a low-temperature poly-Si film, described as follows:

(a) **Solid-Phase Crystallization (SPC)**

Solid-phase crystallization (SPC), focusing on low-temperature annealing, is usually performed at 600 ^{o}C [1.19]. The SPC occurs through the processes of nucleation and grain growth, and both processes are characterized by specific activation energies. For the SPC of α-Si by homogenous nucleation, the activation energy of grain growth is less than that of nucleation [1.20]. Therefore, the amount of the nucleation relative to grain growth decreases with decreasing temperature. To enlarge the grain size, it is desirable to minimize the nucleation/grain growth ratio. Therefore, SPC is typically done at a low temperature [1.21]. However, it is time-consuming (several hours) for the crystallization of the α-Si film to a poly-Si film by SPC. Besides, such poly-Si films have a high density of intra-grain defects which result in a decrease in the field-effect mobility and an increase in the threshold voltage of the TFT [1.22].

(b) **Metal-Induced Lateral Crystallization (MILC)**

With some metals added to the α-Si films, the crystallization temperature can be lowered to below 600 ^{o}C, and this phenomenon is known as *metal-induced crystallization* (MIC) [1.23]. Metals such as Au, Al, Sb, and In, which form eutectics with Si, or metals such as Pd, Ti, and Ni, which form silicides with Si, have been added to α-Si to enhance the

nucleation rate. During the MIC process, metal atoms dissolved in α-Si may weaken Si bonds, and enhance the nucleation of crystalline Si [1.24]. Some results were reported to be successful in lowering the crystallization temperature down to 500 °C. However, an undesirable metal contamination at the channel region results in the poor electrical properties of the devices. A new method which can reduce metal contamination, the so called *metal-induced lateral crystallization* (MILC), has been reported for Pd, where large grains over several tens of microns are obtained [1.25]. Besides, many groups have demonstrated TFTs to be successful in terms of device characteristics and mass productivity with MILC poly-Si, using pure Ni [1.26], [1.27], Ge [1.28] and Ni－Co alloys [1.29].

(c) Excimer Laser Annealing (ELA)

Excimer laser annealing (ELA) is thought to be the most preferable method for the fabrication of LTPS TFTs [1.30]－[1.32]. The ELA method is performed by melting α-Si with high-power pulsed laser irradiation. The irradiated α-Si film is then cooled and solidified as a crystal. During the melt-growth period, however, the solidification velocity is too high for the film to form nuclei and to grow sufficiently. The grain size of the poly-Si film is therefore not large enough. Besides, non-uniformity of grain size and narrow process window make it difficult to achieve uniform TFT performance.

To realize this, some techniques such as the bridge method [1.33], low-temperature substrate heating during laser irradiation [1.34], and two-step laser crystallization [1.35] have been proposed to reduce the solidification velocity. Additionally, for obtaining higher mobility, lateral crystallization is one of the techniques used. The laser beam intensity is spatially modified over the α-Si to control the solid/liquid interface, resulting in lateral crystallization of the film. With this technique, the field-effect mobility of TFTs more than 300 $cm^2/V \cdot sec$ can be achieved [1.36].

1.2 Reliability Issues in LTPS TFTs

Research has shown that the instability of LTPS TFTs is more serious after electrical stress than that of single crystalline silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) [1.37]－[1.39]. The poor stability of LTPS TFTs is due to the high density of grain-boundary defects and the poor properties of the poly-Si/SiO_2 interface and the gate insulator. A considerable amount of research has focused on the stability of LTPS TFTs. The instabilities are basically associated with hot-carrier degradation, negative gate bias instability, and gate-induced carrier injection [1.40]. In the following, some reliability issues in LTPS TFTs will be roughly reviewed, including negative bias temperature instability, plasma-induced damage, and hot-carrier effects.

1.2.1 Negative Bias Temperature Instability

Negative bias temperature instability (NBTI), which has been known since the 1970s, has been recognized as a serious reliability concern for *p*-channel MOSFETs, because it can result in the failure of the integrated circuit (IC) [1.37]－[1.43]. Either negative gate voltages or an elevated temperature can produce NBTI, but a stronger and faster effect is produced by their combined action. It occurs primarily in *p*-channel MOSFETs with negative gate bias stress, but appears to be negligible for positive gate bias stress [1.44]. The NBTI stress is generally performed at an elevated temperature with oxide electric fields typically below 6 MV/cm, and this leads to the degradation of the transistor parameters (drive current, transconductance, and threshold voltage). The low electric fields suppress the carrier injection by Fowler－Nordheim (FN) electron tunneling through a gate oxide, and subsequently there was no direct observable current flow through the oxide [1.45].

In recent years, many fundamental studies have been devoted to NBTI, and it is found that the defects responsible for NBTI are either interface trap states or fixed oxide charges

[1.45]—[1.53]. It is believed that the interface defects responsible for NBTI are P_b centers, which are depassivated when the negative bias is applied. Fixed oxide charges are created in the SiO_2 as by-product trivalent silicon defects [1.45], [1.50]. The amount of generated interface trap states and fixed oxide charges are strongly dependent on fabrication processes such as oxidation and/or annealing. However, this charge-buildup phenomenon is reported to be universal, irrespective of the gate materials, such as Al or polycrystalline silicon, for all wet or dry oxide layers of the $Si-SiO_2$ system [1.45].

Interface traps at the SiO_2/Si interface are electrically active defects with an energy distribution throughout the Si band gap. They are acceptor-like in the upper half and donor-like in the lower half of the band gap [1.54]. Interface traps act as generation/recombination centers and contribute to leakage current and low-frequency noise; in addition, they reduce carrier mobility, drain current, and transconductance. Since electrons or holes occupy interface states, they also contribute to threshold-voltage shifts.

However, interfaces traps affect threshold-voltage shifts in *n*-channel and *p*-channel devices differently. Fig. 1.2 shows the energy band diagrams of an (a) *p* substrate and an (b) *n* substrate at flatband and inversion conditions. At flatband conditions, the *n* channel has *positive* and the *p* channel has *negative* interface trap charges (Q_{it}). At inversion conditions, the *n* channel has *negative* and the *p* channel has *positive* interface trap charges. Since the fixed oxide charges (Q_f) are positive, we have at inversion: $Q_f - Q_{it}$ for the *n* channel and $Q_f + Q_{it}$ for the *p* channel. Therefore, *p*-channel MOSFETs are more severely affected by NBTI [1.55].

NBTI has a fractional power-law dependence on time. The value of the exponent is most likely 1/4. From this $t^{1/4}$-like evolution, Jeppson and Svensson first proposed a diffusion-controlled electrochemical reaction model for the NBTI of MOSFETs [1.56]. The model can be expressed as:

$Si_3 \equiv Si - H$ (interface) + $\equiv Si - O - Si \equiv$ (gate oxide) $\longleftrightarrow$

$Si_3 \equiv Si \bullet$ (interface trap state) + $O_3 \equiv Si^+$ (fixed oxide charge) + $O_3 \equiv Si - OH$ + e^-,

(*Eq.* 1.1)

where $Si_3 \equiv Si - H$ indicates a hydrogenated trivalent silicon, and $O_3 \equiv Si^+$ is a trivalent silicon defect in the oxide. They assume that the silicon interface contains a large number of defects which are electrically inactive, but may become electrically active upon stress. When the defect is activated, the hydrogen, which is weakly bonded to the Si atom, reacts with the SiO_2 and forms an OH group bonded to an oxide silicon atom, leaving one trivalent $O_3 \equiv Si^+$ in the oxide and one trivalent $Si_3 \equiv Si \bullet$ at the silicon surface. The $O_3 \equiv Si^+$ forms the fixed positive charge and the $Si_3 \equiv Si \bullet$ forms the interface trap state. The essence of the diffusion-controlled electrochemical reaction model is that the rate at which the reaction causing the generation of interface trap states takes place is controlled by the diffusion of hydrogen that has been previously released from hydrogen-passivated defect sites. The reaction is schematically represented in Fig. 1.3.

Although the diffusion-controlled electrochemical reaction is generally accepted, there still remains some controversy and debate about the chemical species involved in this dissociation reaction. Some possible diffusing species have been proposed, such as interstitial atomic hydrogen[1.57] – [1.64], molecular hydrogen[1.65] – [1.67], and the hydroxyl (OH) group [1.68], including the hydronium (H_3O^+) and the dydroxide (OH^-) ions. Furthermore, the involvement of ionic hydrogen transport in the reaction has been proposed [1.69]. To generalize the original diffusion-reaction concept to include the charged-diffusing species as well as the neutral-diffusing ones, Ogawa *et al.* proposed a generalized model which ignores details of the dissociation reaction [1.45], [1.46]. The model is constructed based on the trivalent silicon and its hydrogen compounds to explain the interfacial charge formation. They denote the diffusing state of released hydrogen by the symbol *X* (i.e., whether it is atomic or molecular/ionic or neutral). The reaction can be expressed as:

(interface defects) $\longleftrightarrow$ (fixed oxide charge)$^{+}$ + (interface trap state)

+ $X_{\text{interface}}$ + e^{-} (to the silicon), (*Eq.* 1.2)

and

$X_{\text{interface}} \longleftrightarrow X_{\text{bulk}}$. (*Eq.* 1.3)

When the interface defect is electrically activated, the diffusing species leaves a defect site at the Si—SiO_2 interface where an interface trap state and a positive fixed oxide charge are left. This model agrees with observations that equal numbers of interface trap states and fixed oxide charges are produced. The process has been considered as being both field dependent, since a transfer of charge takes place, and diffusion controlled, since the time dependence of such a process was found to be characterized by the fractional power-law temporal variation.

In addition to single crystalline silicon MOSFETs, some studies investigated the effects of bias temperature stress on amorphous silicon (α-Si) TFTs. Charge-trapping models [1.70]—[1.72] and meta-stable state creation models [1.73], [1.74] were proposed for positive and negative bias temperature stress. Charge-trapping models attributed the threshold-voltage shift to charge trapping into trap states in the gate insulator from the α-Si layer. Meta-stable state creation models interpreted the threshold-voltage shift as the increase of Si dangling bonds generated by breaking of weak-bonds in α-Si active layers. Meta-stable state creation models have interpreted the threshold-voltage shift as an increase of Si dangling-bonds generated by the breaking of weak-bonds in α-Si active layers. NBTI was also studied in polycrystalline silicon thin-film transistors (poly-Si TFTs) [1.75]—[1.77]. In both *p*-channel and *n*-channel poly-Si TFTs, it was found that NBTI stress causes an observable threshold-voltage shift, while PBTI causes a negligibly small shift. The threshold-voltage shift caused by NBTI stress has exponential dependence on both the stress gate voltage and the reciprocal of the temperature. Moreover, unlike MOSFETs having single crystalline Si

channels, the grain boundary in the poly-Si channel of TFTs plays an important role in the NBTI-degradation mechanism.

1.2.2 Plasma-Induced Damage

Plasma is a collection of charged and uncharged particles. Positively charged particles are ions; negatively charged particles are either electrons, negative ions or both. Electrons are light and mobile while ions are heavy and comparatively immobile. Plasma is quasi-neutral because it contains equal amount of positive and negative charges. In addition, plasma is not a system at thermal equilibrium; however, it is at a steady state very far from equilibrium.

In the fabrication of VLSI devices and circuitry, plasma processing is widely applied for material etching. Etching can be accomplished by physically displacing atoms or molecules, and this mechanism is called *physical sputtering*. In this process, ion bombardment can cause breakage of chemical bonds and damage to the dielectric and semiconductor materials. Alternatively, a chemical reaction can also be used to form a volatile product of the atoms or molecules to be removed, and this process is called chemical etching. In chemical etching, the plasma creates a reactive etchant species such as radicals or neutrals, and reactant species are produced through dissociation and reaction. Table 1.1 summarizes the various types of damage to the materials involved in semiconductor fabrication [1.78]. During the plasma etching process, plasma-induced damage affects the material properties and device parameters. One of the damages caused by plasma is charging damage, which is becoming a serious reliability problem for device fabrication and has been reported to cause degradation to the hot-carrier lifetime, transistor performance, and gate oxide quality [1.79]－[1.83].

The nature of charging damage in the gate oxide of a transistor is similar to that of FN stress. In the plasma ambient, plasma non-uniformities cause a charge collection by conducting layers such as metal or poly-Si electrodes [1.84]. If the conducting layer is

connected to the gate oxide, the collected charges cause an electrical stress on the gate oxide. When the non-uniformity is large enough and the potential across the gate oxide exceeds the critical value (corresponding to a field of 5－6 MV/cm), an FN tunneling current flows through the gate oxide. During plasma processing, the injection process could be either substrate injection or gate injection depending on potential distribution at the wafer surface [1.85]. Several processes responsible for oxide and transistor degradation take place simultaneously during the FN current flow. First, some of the injected electrons are trapped in existing electron traps. At the same time, holes generated by injected hot electrons are trapped in existing hole traps. Additionally, interface states are generated, resulting in a high density of interface states. Finally, new electron traps are generated, and fill in the oxide bulk. All of these phenomena occur during the charging stress due to plasma exposure of the conducting layers [1.86]. The net result is an accumulation of a net charge in the oxide, and hence it is referred to as the *oxide charging effect*. The charging effect additionally is found to be amplified by the ratio of the area of the conducting surface to the gate area, and this ratio is called the *antenna area ratio* (AR). This phenomenon is referred as the *antenna effect*. It is therefore customary to use a device with different antenna structures to study charging damage. For LTPS TFTs, because they have a high potential to be used in the driving circuit, the antenna structure will be very common in the circuit layout, and the antenna effect becomes an important reliability issue.

1.2.3 Hot-Carrier Effect

For the realization of SOP, the technology of LTPS TFTs is expected to be increasingly applied because of the high carrier mobility, as compared to α-Si TFTs. LTPS TFTs in peripheral circuits are subjected to high pulse voltages compared to that of pixel TFTs. Therefore, the hot-carrier effect becomes one of the most serious issues affecting the reliability of LTPS TFTs [1.87]. The hot-carrier degradation phenomenon originating from a

high drain field has been widely studied in many articles [1.87]—[1.89]. Carriers obtain energy from a high electric field and break weak bonds easily, creating lots of oxide charges and trap states in the channel film and at poly-Si/SiO_2 interface. Hot-carrier stress degrades devices by decreasing the maximum transconductance and causing a variation of the threshold voltage. In addition, the power dissipation increases and the reliability of digital circuit degrades. Therefore, the hot-carrier effect restricts the design of flat-panel displays.

In LTPS TFTFs, unlike the fundamental MOSFETs theory, electrical parameters such as the threshold voltage, maximum transconductance, and subthreshold swing could depend on the properties of grain, grain boundaries, and poly-Si/SiO_2 interface. Farmakis *et al.* have investigated electrical parameters in TFTs, as shown in Table 1.2, to clarify which mechanisms modify device electrical parameters during hot-carrier stress [1.90]. The deep trap states in the grain boundaries or poly-Si/SiO_2 interface mainly affect the threshold voltage. In addition, hot-carrier injection into the gate oxide also causes a threshold-voltage shift. The generations of tail trap states in the grain boundaries or poly-Si/SiO_2 interface degrades the maximum transconductance. Furthermore, the subthreshold swing mainly depends on both intra-grain trap states in the poly-Si film and deep interface trap states.

1.3 Motivation

Since the reliability of LTPS TFTs is important for the application of high-performance displays with integrated circuits, the degradation mechanism of LTPS TFTs must be investigated carefully. For driving circuit operation, LTPS TFTs must be designed using the CMOS inverter configuration and operate with a relatively high duty cycle. Therefore, NBTI becomes a reliability issue for *p*-channel LTPS TFTs since they are subjected to negative bias stress during circuit operation. In LTPS TFTs, because of the poor thermal conductivity of the glass substrate and high operation voltage, NBTI can be further accelerated because it

can be thermally and electrically accelerated. Besides, due to the grain boundaries in the channel regions, the NBTI-degradation mechanism of LTPS TFTs may be different from that of MOSFETs. However, the NBTI degradation has not been thoroughly studied in LTPS TFTs, and the mechanism is not well known. Therefore, in Chapter 2, the NBTI-degradation mechanism of *p*-channel LTPS TFTs will be studied.

It is important to investigate the degradation of the bulk channel region in LTPS TFTs under NBTI stress because the characteristics of LTPS TFTs are generally influenced by the bulk trap states (including grain-boundary and poly-Si/SiO_2 interface trap states). In traditional studies, the bulk trap-state evaluation methods were based on the current-voltage characteristics. However, the channel current is affected only through the potential barrier formed by the trap states and hence is not directly related to the bulk trap properties. To directly characterize the bulk trap properties of LTPS TFTs, a charge-pumping technique will be used in Chapter 3, because carriers are observed as the generation-recombination current, and hence the charge-pumping current directly indicates the trap properties. Besides, in previous NBTI studies of LTPS TFTs, the correlation between the fixed-oxide-charge generation and NBTI degradation has not been clearly identified. Therefore, the role of fixed-oxide-charge generation will also be analyzed in Chapter 3.

In addition to the NBTI degradation, plasma-induced damage is an important reliability issue for LTPS TFTs, because plasma-etching processes are widely adopted during the fabrication procedure to achieve good process repeatability and precise control over the feature sizes in the insulators, semiconductors, and metals. Plasma non-uniformity causes charge collection on the device and develops a stress voltage across the gate dielectric, resulting in the degradation of oxide quality. Besides, the degree of plasma damage is strongly related to the topography of the gate interconnection. It is worthy noting that the antenna effect will be a reliability problem for LTPS TFTs, because antenna structures will be commonly used in circuit layout. However, the effects of the antenna effect on the

performance and reliability of LTPS TFTs have not been explored to an appropriate degree. Therefore, in Chapter 4, *n*-channel LTPS TFTs designed with various antenna structures will be used to investigate the impacts of the antenna effect.

Both the NBTI and the antenna effect are serious reliability issues for LTPS TFTs. An antenna effect mainly occurs during the fabrication process and degrades the oxide quality, while NBTI primarily occurs during circuit operation and degrades the performance. Pagaduan *et al.* have pointed out that devices suffering plasma damage exhibit an aggravated threshold-voltage shift after NBTI stress [1.91]. However, the correlation between the antenna effect and NBTI in LTPS TFTs has not been explored. Therefore, in Chapter 5, effects of NBTI stress will be analyzed on *p*-channel LTPS TFTs designed with various antenna structures to verify the impact of the antenna effect on the NBTI behaviors in LTPS TFTs.

Hot-carrier effects, which originate from the high electric field near the drain junction, have been commonly used for reliability assurance, and widely studied in LTPS TFTs. Because the LTPS TFT driving circuit is designed using the CMOSFET structure, hot-carrier stress (HCS) becomes a transient phenomenon that mixes with the effect of NBTI. However, the mixed effects of NBTI and HCS are rarely explored for LTPS TFTs. Therefore, in Chapter 6, the combined effect of NBTI and HCS will be investigated, in which the LTPS TFTs will be stressed with a fixed gate bias and variable drain bias to identify the drain bias dependence of the threshold voltage shift.

1.4 Thesis Organization

This thesis is organized as follow:

In Chapter 1, the overview of LTPS TFTs and some reliability issues are illustrated. The motivation of this thesis is also described.

In Chapter 2, NBTI of *p*-channel LTPS TFTs is thoroughly studied. In addition to the threshold-voltage shift, the generation of grain-boundary trap states and interface trap states are analyzed. A stressing-passivation-stressing procedure is also used to study the effect of threshold-voltage recovery. From the experimental results, the NBTI-degradation mechanism of LTPS TFTs is identified.

In Chapter 3, a charge-pumping technique is utilized to analyze the NBTI degradation of LTPS TFTs. In addition to the increase of bulk trap states (including interface and grain-boundary trap states), the increase of fixed oxide charges is also extracted. By using this technique, the NBTI-degradation mechanism of LTPS TFTs can be further confirmed

In Chapter 4, *n*-channel LTPS TFTs designed with different antenna area ratios are used to study the impacts of an antenna effect on the device performance and reliability. Electrical characteristics of the devices were measured to identify the influence of the antenna effect. Finally, gate-bias stress and hot-carrier stress were used to analyze the degradation of device reliability.

In Chapter 5, the impacts of the antenna effect on the NBTI behaviors are investigated. NBTI stress was performed on the LTPS TFTs having different antenna area ratios. By extracting the related device parameters, the antenna effect can be demonstrated to enhance the NBTI degradation in LTPS TFTs.

In Chapter 6, a reliability model is proposed which successfully introduces the physical mechanisms of both the NBTI and HCS for *p*-channel LTPS TFTs. The stress drain bias voltage is introduced into the conventional NBTI degradation model to develop a drain-bias-modulated NBTI degradation model. Combined with the HCS model, a new reliability model is proposed which can predict the drain bias dependence of the threshold-voltage shift of LTPS TFTs under NBTI stress.

Finally, conclusions of this dissertation and recommendations for further research are presented in Chapter 7.

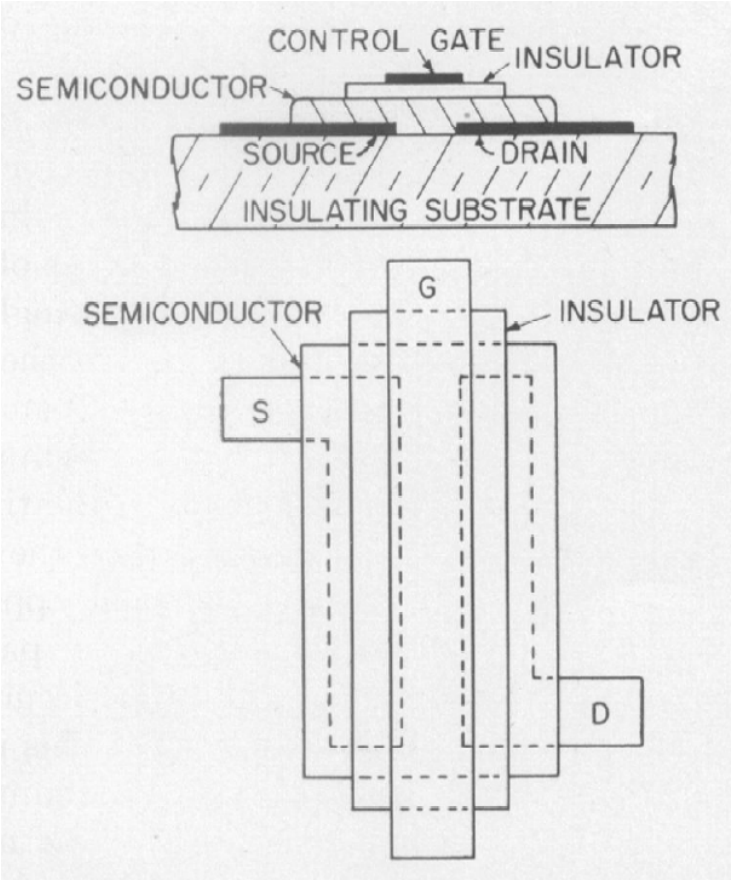


Fig. 1.1 Cross-sectional and top views of the first TFT in literature.

(Ref. Weimer, *IRE-AICE Device Research Conference*, 1961)

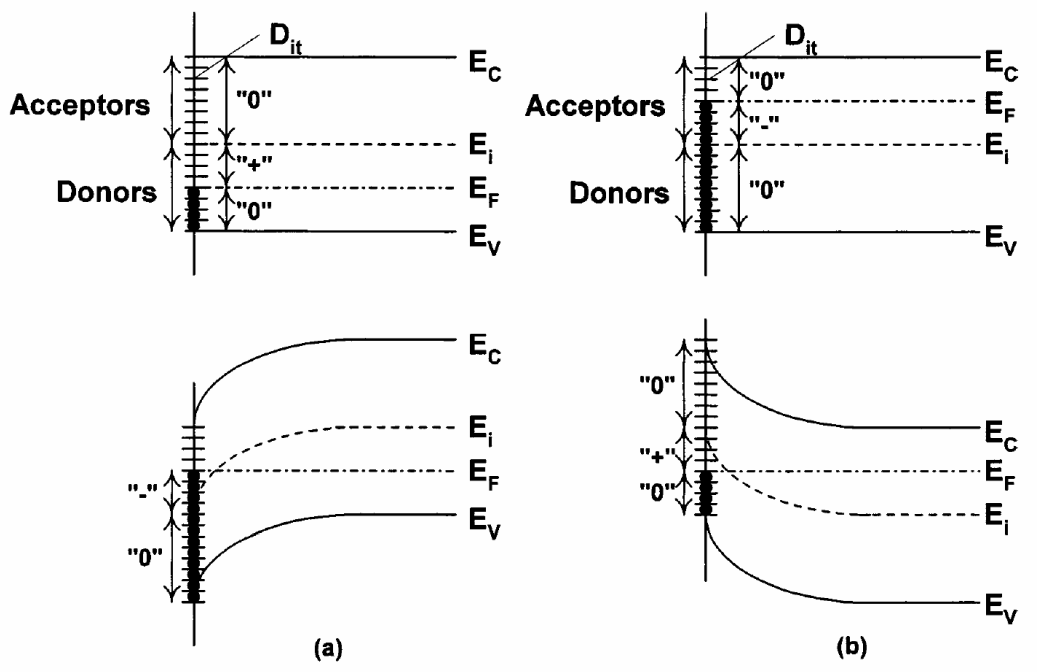


Fig. 1.2 Energy band diagrams of the Si substrate showing the occupancy of interface traps and the various charge polarities: an (a) *p*-type substrate with positive interface trap charges at flatband condition and negative interface trap charges at inversion condition, and an (b) *n*-type substrate with negative interface trap charges at flatband condition and positive interface trap charges at inversion condition.

(Ref. Schroder and Babcock, *J. Appl. Phys.*, 2003)

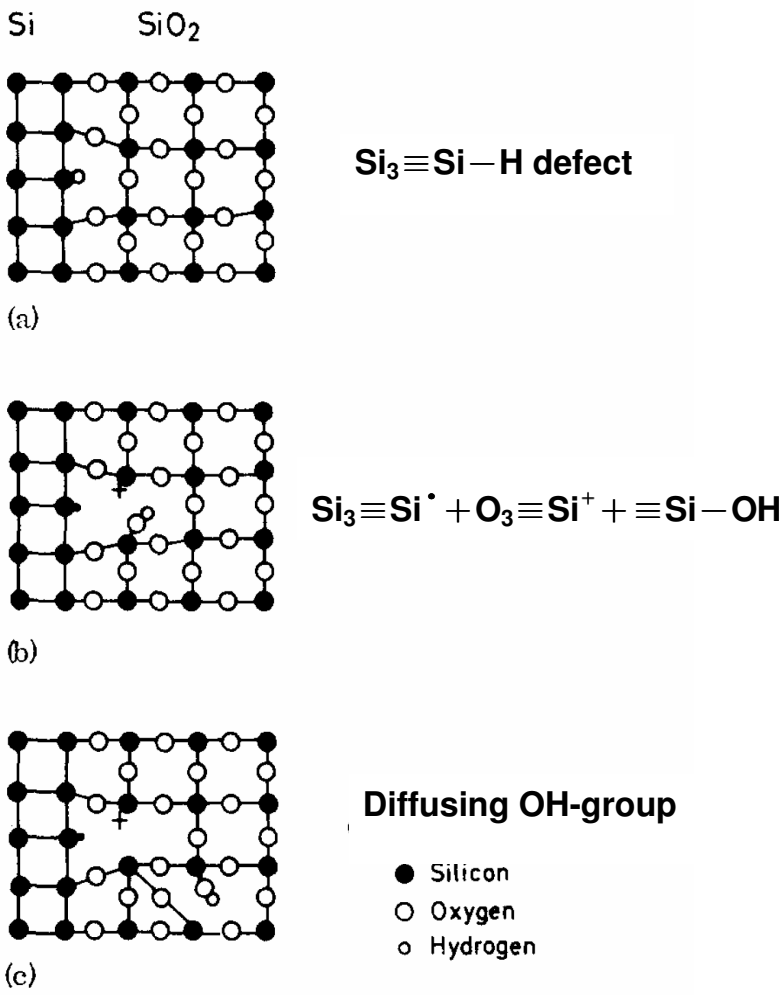


Fig. 1.3 Schematic two-dimensional representation of the $Si-SiO_2$ interface, showing (a) the $Si_3 \equiv Si-H$ defect, and (b) how this defect may be electrically activated during NBTI stress to form a surface trap , an oxide charge, and a hydroxyl group, that (c) may diffuse in the oxide and be the reaction-limiting factor.

(Ref. Jeppson and Svensson, *J. Appl. Phys.*, 1977)

Table 1.1 Various types of material damage involved in the semiconductor fabrication.

(Ref. Rakkhit *et al.*, in *Proc. IEEE Int. Reliab. Phys. Symp.*, 1993.)

Material	*Damage Source*	*Damage*
Semiconductor	**Energetic Particles**	**Creation of Traps and G-R Centers** **Creation of Defects** **Impurity Incorporation** **Dopant Deactivation**
	Chemical Reaction	**Creation of Traps and G-R Centers** **Defect Generation and Propagation** **Addition or Removal of Hydrogen**
Gate Oxide	**Charging Damage** **UV Ionization Damage**	**Creation of Traps** **Charging Up of Traps** **Creation of Fixed Charges**
	Chemical Reaction	**Addition or Removal of Hydrogen** **Creation of Traps**
Oxide-Semiconductor Interface	**Energetic Particles**	**Roughening of the Interface**
	Charging Damage	**Creation and Charging Up of Interface States**
Metal	**Energetic Particles**	**Topology Changes**

Table 1.2 Parameter variations and corresponding possible degradation mechanics.

(Ref. Farmakis *et al.*, *IEEE Electron Device Lett.*, 2001.)

Electrical parameters after stressing	**Mainly depending on**
Δg_{mmax}	▫ interface state generation ▫ state generation in the grain boundaries (tail states)
ΔV_{ON}	▫ charges injected into the gate oxide ▫ interface state generation (deep states) ▫ state generation in the grain boundaries (deep states)
ΔS (subthreshold swing)	▫ intra-grain defect density generation (bulk states) ▫ interface state generation (deep states)

Chapter 2

Negative Bias Temperature Instability in Low-Temperature Polycrystalline Silicon Thin-Film Transistors

2.1 Introduction

LTPS TFTs are attracting much research interest for their various applications, such as driver circuits of active matrix liquid crystal displays (AM-LCDs) and active matrix organic light emitting diode displays (AM-OLED). Moreover, due to the high carrier mobility of LTPS TFTs, they have high potential of realizing system on panel (SOP), in which the peripheral drivers can be integrated on the glass substrates to minimize the panel size, improve the reliability and resolution of the displays, yield a light and thin display having a reduced number of connection pins, and reduce the fabrication cost [2.1], [2.2]. For the driving circuit operation, LTPS TFTs must be designed using the CMOS inverter configuration. Unlike the functionality for pixel switching, the peripheral driving circuits operate with a relatively high duty cycle. Accordingly, the *p*-channel and *n*-channel TFTs are subjected to negative and positive bias stress, respectively. Fig. 2.1 gives a more detailed picture of the correlated information. It presents the bias conditions of a CMOS inverter for driving circuit operation. When the input is at a low voltage level and the output is at a high voltage level, the *p*-channel TFT is under negative bias stress. In contrast, when the input is at a high voltage level and the output is at a low voltage level, the *n*-channel TFT is under positive bias stress [2.3]. Therefore, the characteristic of negative bias temperature instability (NBTI) for the *p*-channel LTPS TFTs is very important.

In *p*-channel MOSFETs, NBTI has been found to be an important reliability problem which has been widely investigated. The NBTI-degradation in MOSFETs is mainly attributed to the generation of interface trap states and fixed oxide charges, and it can be thermally and electrically activated [2.4]－[2.7]. Besides, it is accepted that degradation partially recovers once stress is removed [2.8], [2.9]. The recovery of the NBTI degradation comes from the reduction of interface trap states and fixed oxide charges. In LTPS TFTs, due to the poor thermal conductivity of the glass substrate and high operation voltage, we suppose that NBTI is important to the reliability of LTPS TFTs. Okuyama *et al.* have pointed out that the NBTI stress causes a performance degradation in poly-Si TFTs as well as in MOSFETs [2.10], [2.11]. However, the NBTI degradation and the recovery effect have not been thoroughly studied in LTPS TFTs, and the mechanisms are not well known. In addition, we speculate that the NBTI-degradation mechanism in LTPS TFTs, due to grain boundaries in the channel regions, may be different from those in MOSFETs. Some studies have indicated that the NBTI stress on poly-Si TFTs may generate trap states in the grain boundaries [2.11]; however, the correlation between the grain-boundary trap-state generation and the device degradation during NBTI stress in LTPS TFTs has not been well explored.

In this chapter, the instability and mechanism of *p*-channel LTPS TFTs under NBTI stress have been studied. Positive bias temperature instability (PBTI) is also measured to be compared with the NBTI effect. By measuring and analyzing the transfer and output characteristics before and after NBTI stress under different stress gate voltages and stress temperatures, the NBTI degradation and recovery mechanisms of LTPS TFTs were studied and a new model is proposed to explain the experimental results.

2.2 Experiments

LTPS TFTs were fabricated on the glass substrates with top-gate structures. The process

flow of the *p*-channel LTPS TFT is shown in Figs. 2.2(a) – 2.2(g). First, a 400-Å amorphous-Si layer was deposited by a plasma-enhanced chemical-vapor deposition (PECVD) system on a buffer layer and crystallized into a poly-Si film through excimer laser annealing. After defining the active region, the gate dielectric of the 1000-Å SiO_2 layer was deposited at 300 ^oC. Mo was then deposited at a thickness of 3000 Å and patterned as the gate electrode. Self-aligned source and drain were formed through plasma doping. Following that, hydrogenation was performed with an NH_3 plasma treatment at 300 ^oC to passivate the dangling bonds at the poly-Si/SiO_2 interface and in the grain boundaries. A 5000-Å inter-layer dielectric of SiO_2 was then deposited and densified through rapid thermal annealing (RTA) at 700 ^oC for 30 s. The dopants were activated during the densification of the inter-layer dielectric. Finally, after a contact-hole opening, 5000-Å Al was deposited and patterned as the interconnection metal. The channel length (L) and width (W) of the device used in this study were 10 μm and 20 μm, respectively.

During stress, the glass substrate was heated to stress temperatures ranging from 25 ^oC to 150 ^oC. Stress gate biases were +15 V as PBTI stress, and ranging from −15 to −30 V as NBTI stress. Source and drain were electrically grounded. The stress was periodically stopped to measure the basic device characteristics, including transfer and output characteristics, to characterize the NBTI effect. All the measurements were taken at stress temperatures.

2.3 Results and Discussion

Figs. 2.3(a) and 2.3(b) show the transfer characteristics in the linear scale of the LTPS TFTS before and after 1000 s NBTI and PBTI stress, respectively, with a stress voltage of ± 15 V at 100 ^oC. It is obvious that the *p*-channel LTPS TFT shows a parallel shift in the on-current after NBTI stress, while it shows a small on-current shift under PBTI stress. This

indicates that PBTI is an important issue for *p*-channel LTPS TFTs. Besides, during inverter operation, *p*-channel LTPS TFTs will be subjected to NBTI stress instead of PBTI stress. Therefore, only NBTI degradation will be discussed below.

2.3.1 Device Degradation Due to NBTI

Figs. 2.4(a) and 2.4(b) show the transfer characteristics and output characteristics of the LTPS TFT under NBTI stress, respectively. The stress was performed at 100 ^{o}C with a stress gate voltage of −30 V for 1000 s. In Fig. 2.4(a), it is observed that the threshold voltage shifts to the negative direction after the NBTI stress. In addition, the NBTI stress also leads to the performance degradation in the subthreshold swing, field-effect mobility, and drive current. The degradation of the subthreshold swing and field-effect mobility is attributed to the interface-trap-state generation. The drive current of LTPS TFTs can be given in the simple form:

$$I_{ON} = \frac{\mu_{FE} C_{ox} W}{L}(V_{GS} - V_{th})V_{DS}. \qquad (Eq.\ 2.1)$$

The two parameters leading to the degradation of the drive current (I_{ON}) are the threshold-voltage (V_{th}) shift and field-effect mobility (μ_{FE}) decrease. Therefore, the reduction of the drive current after NBTI stress can be attributed to the threshold-voltage shift and field-effect mobility degradation. Furthermore, the leakage current also increases after stress which leads to the increase of standby current.

In MOSFETs, the threshold-voltage shift caused by the NBTI stress is generally attributed to the generation of fixed oxide charges and interface trap states [2.4]−[2.7]. In poly-Si TFTs, however, there are many grain boundaries in the channel regions, and the grain boundaries may be degraded under NBTI stress. Therefore, in addition to the generation of fixed oxide charges and interface trap states, we suggest that the threshold-voltage shift in poly-Si TFTs is also attributed to the grain-boundary trap-state creation. The detailed

analysis of the correlation between the grain-boundary trap-state generation and the threshold-voltage shift under NBTI stress will be discussed in the latter section.

2.3.2 Analysis of the Threshold-Voltage Shift

Figs. 2.5(a)－2.5(c) show the dependence of the threshold-voltage shift on the stress time, stress voltage, and stress temperature, respectively. The gate voltage at a specified threshold drain-current (I_{DS}), (W/L) × 10 nA for V_{DS} = －0.1 V, is taken as the threshold voltage. In Fig. 2.5(a), the threshold-voltage shift increases upon increasing the stress time, and it shows a power law dependence on the stress time. It is observed that the threshold-voltage shift slightly fluctuates as a function of the stress time; this is because the magnitude of the threshold-voltage shift under NBTI stress is very small (< 0.1 V for short stress time). Actually, the correlation coefficients of the four fitting curves in Fig. 2.5(a) are all above 0.98, which means that the measured data and the fitting curves almost fit together. In Figs. 2.5(b) and 2.5(c), it is found that the NBTI degradation is enhanced at a higher stress voltage or stress temperature, indicating that the NBTI can be electrically and thermally activated.

The behavior of the threshold-voltage shift can be empirically modeled as [2.12]

$$\Delta V_{th} \propto t^{n} e^{(-E_a/kT)} e^{C|V_G|}, \qquad (Eq.\ 2.2)$$

where the exponent n approximates from 0.28 to 0.34 in our experimental results, which is similar to the results previously reported for poly-Si TFTs [2.10], [2.11], and bulk MOSFETs [2.11]. The parameter C, extracted from Fig. 2.5(b), is between 0.10 and 0.13, which is dependent on the process and independent of stress voltage. The activation energy (E_a) extracted from Fig. 2.5(c) is about 0.14 eV.

It is important to distinguish whether the devices' degradation under NBTI stress is due to the ionic drift, to the charge trapping in the gate dielectric, or to the state creation. If the

NBTI-degradation mechanism is related to the ionic drift, as shown in Fig. 2.6(a), the threshold voltage should shift to the positive direction, however, this clashed with the experimental results. On the other hand, in some models of charge trapping in gate dielectric [2.14], it is revealed that when the device is under gate bias stress, charges may inject into the gate dielectric and generate extra trap states, leading to the threshold-voltage shift, as shown in Fig. 2.6(b). In our experiments, there are several reasons to explain why the device degradation under NBTI stress was not due to the charge trapping in the gate dielectric. First, if the threshold-voltage shift is caused by the electron injection from the gate into the gate dielectric, the threshold voltage should shift to the positive direction. However, this clashed with the experimental results. Second, if the degradation is caused by the hole injection from the channel to the gate dielectric, the threshold voltage will shift to the positive direction. This seems consistent with the experimental results. However, the electric field across the gate dielectric (below 3 MV/cm) was not high enough to cause hole injection, and the Fowler－Nordheim current was undetectable at these bias conditions, as shown in Fig. 2.7. Therefore, the extra trap-state generation and device instability caused by small currents can be neglected [2.16]. Third, previous studies showed that the threshold-voltage shift caused by the charge-trapping process exhibits exponential dependence on $1/V_G$ and is virtually temperature independent [2.14], [2.15]. If the threshold-voltage shift is caused by charge trapping, it should have the same dependence on the stress gate voltage and stress temperature as in the charge-trapping model. However, the charge-trapping model can't explain the exponential dependence of the threshold-voltage shift on V_G and $1/T$ as shown in Figs. 2.5(b) and 2.5(c), respectively. Finally, the charge-trapping models [2.14] cannot explain the linear fit of the log-log plot of the threshold-voltage shift versus the stress time as shown in Fig. 2.5(a). Therefore, instead of ionic drift or charge trapping in the gate dielectric, we suggest that the threshold-voltage shift caused by NBTI stress is due to the charge defect creation in the gate oxide, and trap-state generation at the poly-Si/SiO_2 interface and in the

grain boundaries. Detailed analysis of the degradation mechanism will be discussed in the later sections.

The lifetimes of the LTPS TFTs are plotted as a function of the stress voltage, with various stress temperatures, as shown in Fig. 2.8. The lifetime is defined as the time taken for the device to reach a threshold-voltage shift of 100 mV under NBTI stress. Obviously, the lifetime degrades upon increasing the stress voltage or temperature because NBTI can be electrically and thermally activated.

2.3.3 Analysis of the Grain-Boundary Trap-State Generation

Due to the grain boundaries in the channel regions, the NBTI-degradation mechanism for LTPS TFTs may be different from MOSFETs. To investigate the effects of grain boundaries in the LTPS TFTs during NBTI stress, the grain-boundary trap-state densities (N_{trap}) before and after stress were estimated by the Levinson and Proano method [2.17], [2.18]. Fig. 2.9 exhibits the plots of $ln\,[I_{DS} / (V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ curves at low V_{DS} and high V_{GS}, where the flat-band voltage (V_{FB}) is defined as the gate voltage that yields the minimum drain-current from the transfer characteristic with V_{DS} = −0.1 V. The grain-boundary trap-state density can be determined from the square root of the slope:

$$N_{trap} = \frac{C_{OX}}{q}\sqrt{|Slope|}\,. \qquad (Eq.\ 2.3)$$

From Fig. 2.9, it is apparent that the grain-boundary trap-state density increases after NBTI stress, indicating that grain-boundary trap-state generation plays an important role in the NBTI degradation for LTPS TFTs. Therefore, in addition to the generation of fixed oxide charges and interface trap states as is well known in the MOSFETs, the grain-boundary trap-state creation must be considered to explain the NBTI-degradation mechanism of LTPS TFTs.

Fig. 2.10(a) shows the dependence of the grain-boundary trap-state generation on the

stress time at 100 °C with various stress voltages. The grain-boundary trap-state density variation, like the threshold-voltage shift, follows a power-law dependence on the stress time with exponents from 0.25 to 0.32, which is similar to the exponent factors extracted from Fig. 2.5(a). In addition, we also examined the dependence of the grain-boundary trap-state density variation on the stress voltage and stress temperature, as shown in Figs. 2.10(b) and 2.10(c). It was found that the grain-boundary trap-state density variation (ΔN_{trap}) has the same function form as the threshold-voltage shift, which can be represented as:

$$\Delta N_{trap} \propto t^{n'} e^{(-E_a'/kT)} e^{C'|V_G|}. \qquad (Eq.\ 2.4)$$

The parameters *n'*, E_a', *C'* under various NBTI stress conditions are shown in Fig. 2.11 and are compared with *n*, E_a, and *C* extracted from the threshold-voltage shift. It is worth noting that *n'*, *Ea'*, and *C'* are similar to *n*, E_a, and *C*, respectively; this implies that the grain-boundary trap-state generation and the threshold-voltage shift show the same dependence on the stress time, stress voltage, and stress temperature.

Fig. 2.12 describes the correlation between the grain-boundary trap-state generation and the threshold-voltage shift. As the grain-boundary trap-state density increases, the threshold-voltage shift becomes larger. Both the two physical quantities are closely related, because they have the same dependence as on the stress time, stress voltage, and stress temperature discussed above. Therefore, we have proven that the grain-boundaries trap-state generation is closely related to the NBTI-degradation mechanism for LTPS TFTs.

2.3.4 Analysis of the Interface-Trap-State Generation

In addition to the grain-boundary trap-state generation as discussed above, we suggest that the interface trap states at the poly-Si/SiO_2 interface are also generated in the LTPS TFTs during NBTI stress. Figs. 2.13(a) and 2.13(b) reveal the correlation between the degradation of the subthreshold swing, the maximum transconductance, and the threshold-voltage shift.

The generation of interface states is reflected in both the degradation of subthreshold swing and maximum transconductance. Furthermore, it has been reported that the subthreshold swing is more closely related to the trap states located near the mid-gap region (deep states), while the mobility is more associated with the trap states located near the band edge (tail states) [2.19]. The deep states and tail states originate from the dangling bonds and strain bonds, respectively. In addition, the degradation of subthreshold swing is found to be severer than maximum transconductance degradation; accordingly, we suggested NBTI causes the generation of interface states, and the interface state creation is mainly attributed to the formation of dangling bonds.

To correlate the generation of grain-boundary trap states with trap states near the poly-Si/SiO_2 interface, the interface-trap-state density must be estimated**.** By neglecting the depletion capacitance in the active layer, an effective interface-trap-state density (N_{it}) near the poly-Si/SiO_2 interface can be evaluated from the subthreshold swing (S) [2.20]:

$$N_{it} = \left[\left(\frac{S}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{OX}}{q}\right). \qquad (Eq.\ 2.5)$$

Fig. 2.14 shows the correlation between the generation of interface-trap-state density (N_{it}) and grain-boundary trap-state density (N_{trap}). It is observed that the generations of the grain-boundary and interface trap states during NBTI stress are in the same order. Therefore, we have demonstrated that the trap-state generation occurs both in the grain boundaries and at the poly-Si/SiO_2 interface for LTPS TFTs under NBTI stress.

2.3.5 Recovery Behavior of NBTI

Fig. 2.15 shows the time dependence of the threshold-voltage shift under static stressing condition and stressing-passivation-stressing processes at 100 ^{o}C. The recovery of the threshold voltage increases with the increase of passivation voltage, indicating that the threshold-voltage recovery can be electrically activated. Fig. 2.16 compares the recovery of

the threshold voltage under various temperatures and passivation voltages. Generally, as the temperature or passivation voltage increases, the recovery of the threshold voltage is enhanced. This confirms that the recovery of the threshold voltage can be thermally and electrically activated. It is worth noting that, as we mentioned earlier, the NBTI degradation can also be thermally and electrically activated. This leads us to speculate that the mechanism of the threshold-voltage recovery is the reverse process of the NBTI degradation, because both of these can be activated thermally and electrically.

Fig. 2.17(a) shows the time dependence of the threshold-voltage shift of the devices during NBTI stress. The shift of the threshold voltage follows a power dependence on the stress time with an exponent from 1/3 to 1/4, and this can be explained by the diffusion-controlled electrochemical reactions. In Fig. 2.17 (b), the threshold-voltage recovery of the devices during the passivation process also follows a power-law dependence on the stress time, with similar exponents as the threshold-voltage shift. Therefore, the mechanism of the passivation process can be interpreted by the reverse of the NBTI-degradation mechanism.

2.3.6 Physical Model of NBTI

In MOSFETs, NBTI degradation has been widely attributed to the generation of fixed oxide charges and interface trap states. In LTPS TFTs, however, our experimental results indicate that grain-boundary trap-state generation must also be considered to clarify the degradation mechanism. The results show that both the threshold-voltage shift and the grain-boundary trap-state generation have almost the same power-law dependence on the stress time. The exponent approximates from 1/3 to 1/4, which is generally explained by the diffusion-controlled electrochemical reactions [2.5], [2.21].

The values of the exponent factor n are slightly larger than those extracted in the NBTI experiments of MOSFETs having SiO_2 gate dielectric (about 0.25). We think there are two

possible reasons to explain this phenomenon. First, the difference may be explained from Table 2.1 proposed by Chakravarthi *et al.*, which shows the effect of different species on fractional time dependence of NBTI evolution for a diffusion-limited system [2.22]. In MOSFETs, the primary degradation mechanism is dominated by the diffusion of a neutral hydrogen species (H^o). Therefore, the exponent is about 0.25 [2.5]. In LTPS TFTs, the larger values of the exponents indicate that the hydrogen species participate in the NBTI reaction may consist of H^o and H^+. Second, in LTPS TFTs, the gate oxide is deposited by the PECVD system. The quality of the PECVD-deposited SiO_2 is not as good as the thermal-grown SiO_2, thus it is easier for the hydrogen species to diffuse in the PECVD-deposited SiO_2 than in the thermal-grown SiO_2. Because NBTI degradation is a diffusion-limited mechanism, therefore, we suggest that the poor quality of PECVD-deposited SiO_2 accelerates the diffusion of the hydrogen species and results in larger value of the exponent.

By expanding the model proposed for bulk-Si MOSFETs [2.21], we propose a new model to explain the NBTI-degradation mechanism for LTPS TFTs as shown in Figs. 2.18(a) −2.18(c). The NBTI-degradation model for LTPS TFTs can be given by the following:

$$\begin{aligned} &Si_3{\equiv}Si-H \text{ (interface and grain boundary)} + {\equiv}Si-O-Si{\equiv} \text{ (gate oxide)} \longleftrightarrow \\ &Si_3{\equiv}Si\bullet \text{ (interface and grain boundary trap states)} + O_3{\equiv}Si^+ \text{(fixed oxide charge)} \\ &+ O_3{\equiv}Si-OH + e^-. \end{aligned}$$

(*Eq.* 2.6)

We assume that the Si dangling bonds at the poly-Si/SiO_2 interface and in the grain boundaries are passivated by the hydrogen atoms initially, forming $Si_3{\equiv}Si-H$ bonds. During NBTI stress, the hydrogen atoms at the poly-Si/SiO_2 interface and in the grain boundaries, being weakly bonded to the Si atoms, react with the holes from the inversion layer and dissociate from the Si atoms. A hydrogen depassivation results in the generation of interface trap states and grain-boundary trap states ($Si_3{\equiv}Si\bullet$); in addition, the generation of

the interface trap states and grain-boundary trap states during NBTI stress are in the same order. The released hydrogen species from the interface and grain boundaries diffuse or drift into the gate oxide and react with it, forming OH groups bounded to oxide Si atoms ($O_3 \equiv Si - OH$) and leaving positive fixed oxide charges ($O_3 \equiv Si^+$) in the gate oxide. Finally, the hydrogen species diffuse in the gate oxide, becoming a reaction-limiting factor. Besides, the reaction is reversible because the threshold-voltage shift and the threshold-voltage recovery show a similar power-law dependence on the stress time.

2.4 Summary

NBTI of *p*-channel LTPS TFTs has been studied in this chapter, and we have proven that NBTI is important on the reliability of LTPS TFTs. We found that the threshold voltage, subthreshold swing, field-effect mobility, and drive current of the LTPS TFTs degrade after NBTI stress. The NBTI degradation increases upon increasing the stress temperature and electric field, indicating that NBTI can be thermally and electrically activated. Due to the grain boundaries in the channel regions of LTPS TFTs, the grain-boundary trap-state generation must be considered to explain the NBTI-degradation mechanism. In this study, we have proven that the threshold-voltage shift is closely related to the grain-boundary trap-state generation, because both of these two physical quantities follow almost the same power-law dependence on the stress time; that is, the same exponential dependence on both the stress voltage and on the reciprocal of the ambient temperature. The exponential value of the power-law dependence on the stress time approximates from 1/3 to 1/4, which is explained by the diffusion-controlled electrochemical reactions. The values of the exponent *n* are slightly larger than those extracted from MOSFETs under NBTI stress. This can be attributed to the different hydrogen species participating in the NBTI degradation or/and poor quality of the PECVD-deposited SiO_2. From the experimental results, we conclude that the NBTI

degradation in LTPS TFTs is caused by the generation of fixed oxide charges, interface trap states, and grain-boundary trap states. Besides, these charges or trap states become passivated as the stress voltage is removed or a positive voltage is applied on the gate, leading to the threshold voltage recovery. The recovery of the NBTI degradation can be explained by the reverse process of the diffusion-controlled electrochemical reactions.

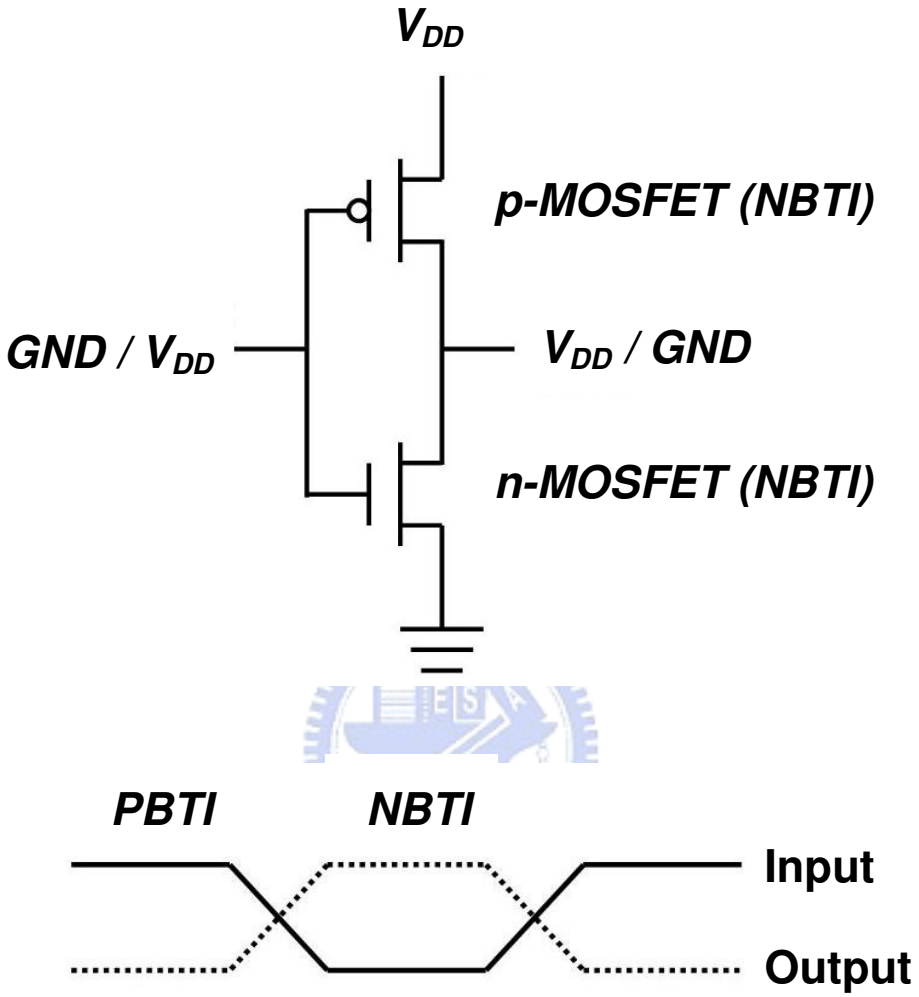
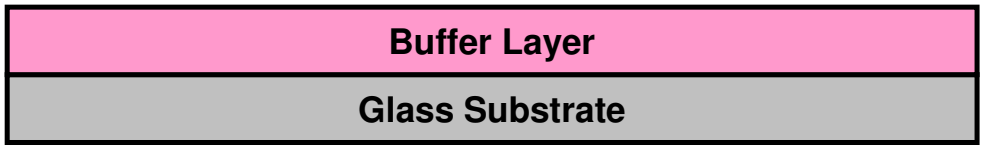
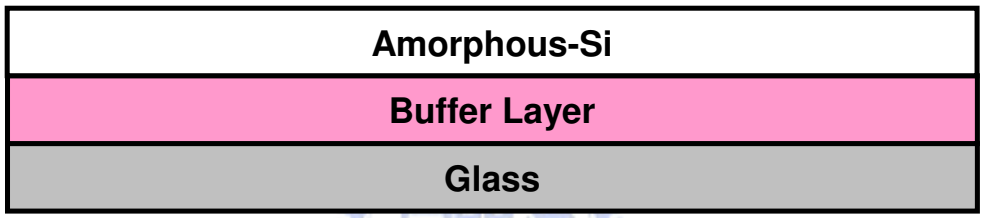


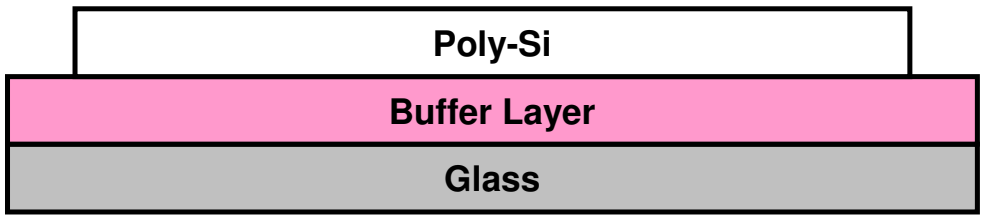
Fig. 2.1 Bias conditions of a CMOS inverter during circuit operations.



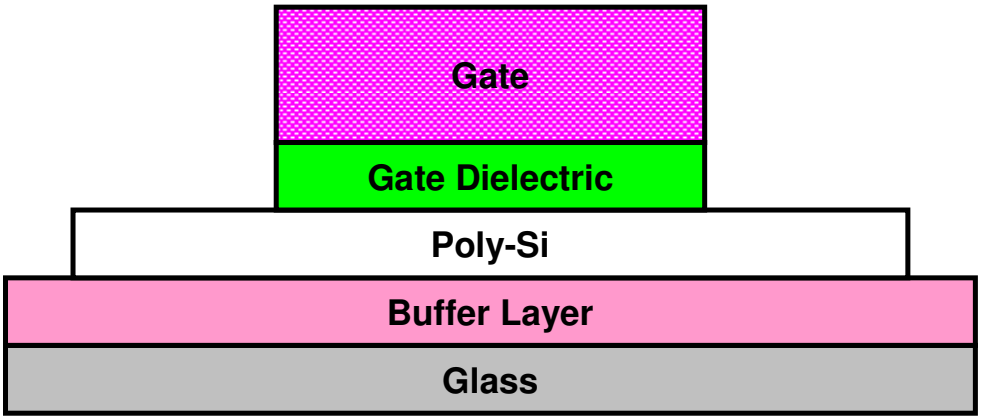
(a) Buffer layer deposition on the glass substrate.



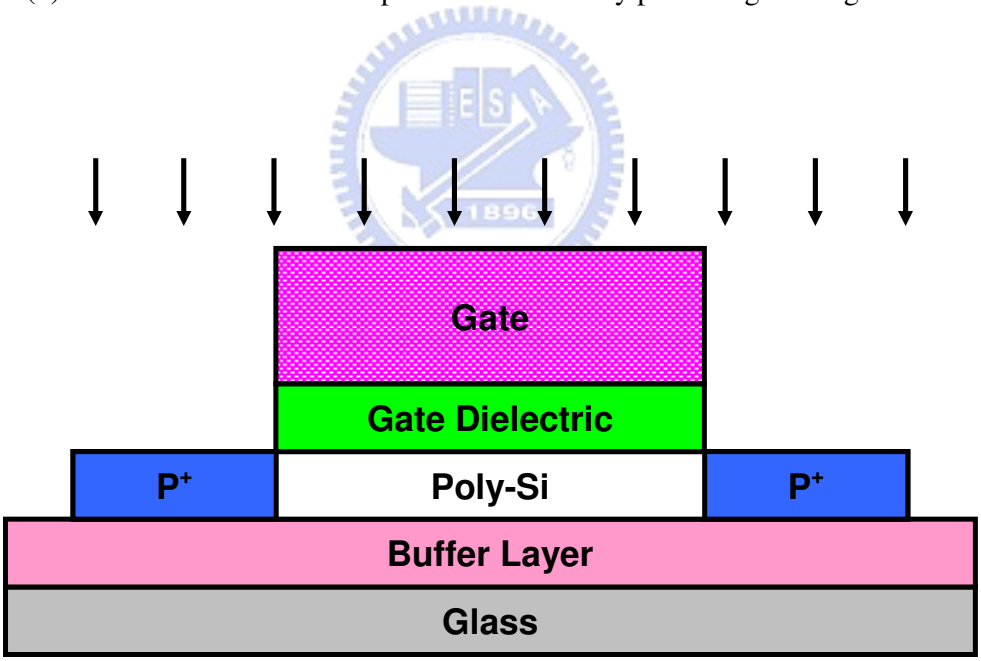
(b) Amorphous-Si layer deposition by PECVD.



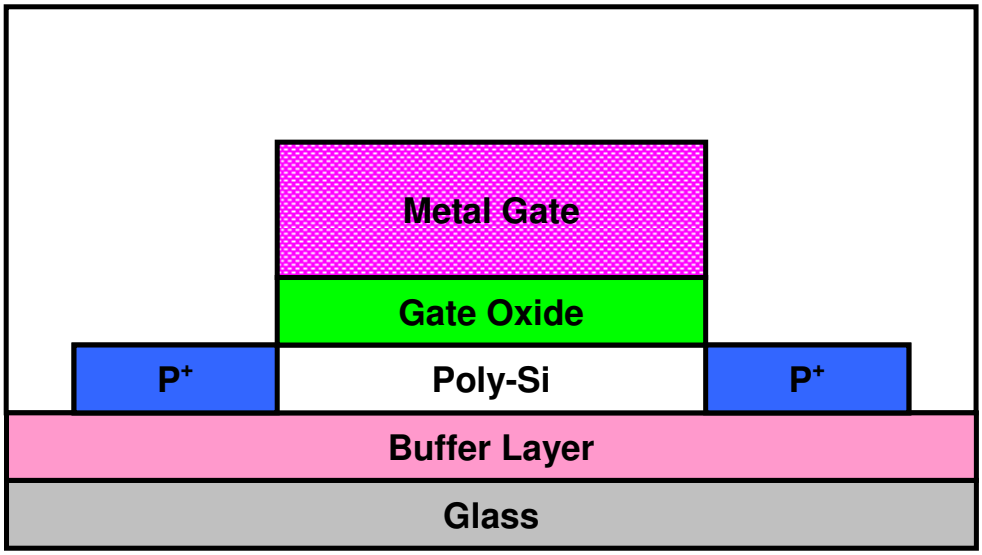
(c) Crystallization of the amorphous-Si film followed by active region definition.



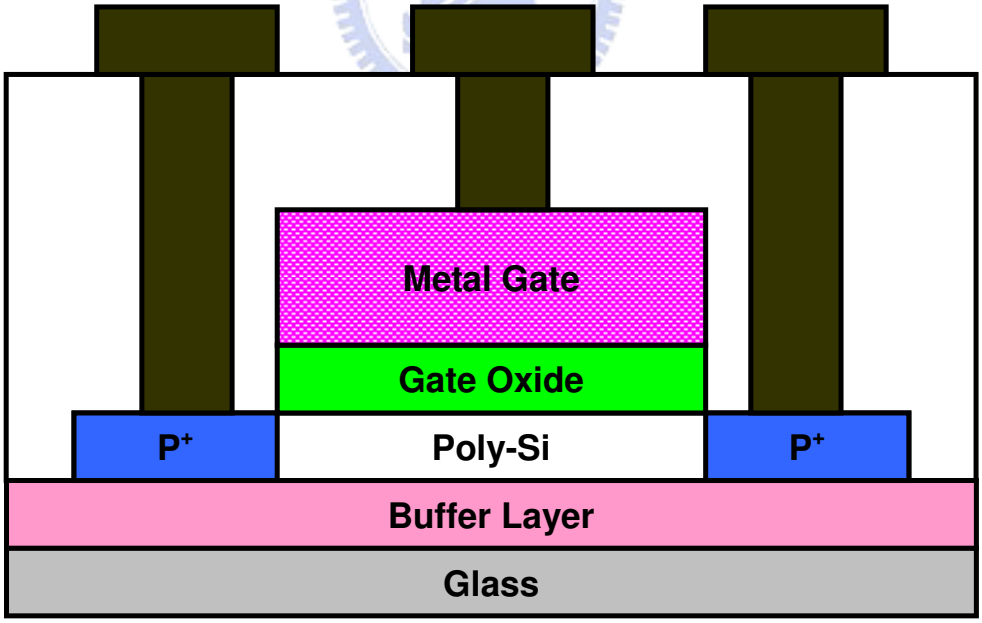
(d) Gate dielectric and Mo deposition followed by patterning as the gate electrode.



(e) Self-aligned source and drain dopping followed by hydrogenation.

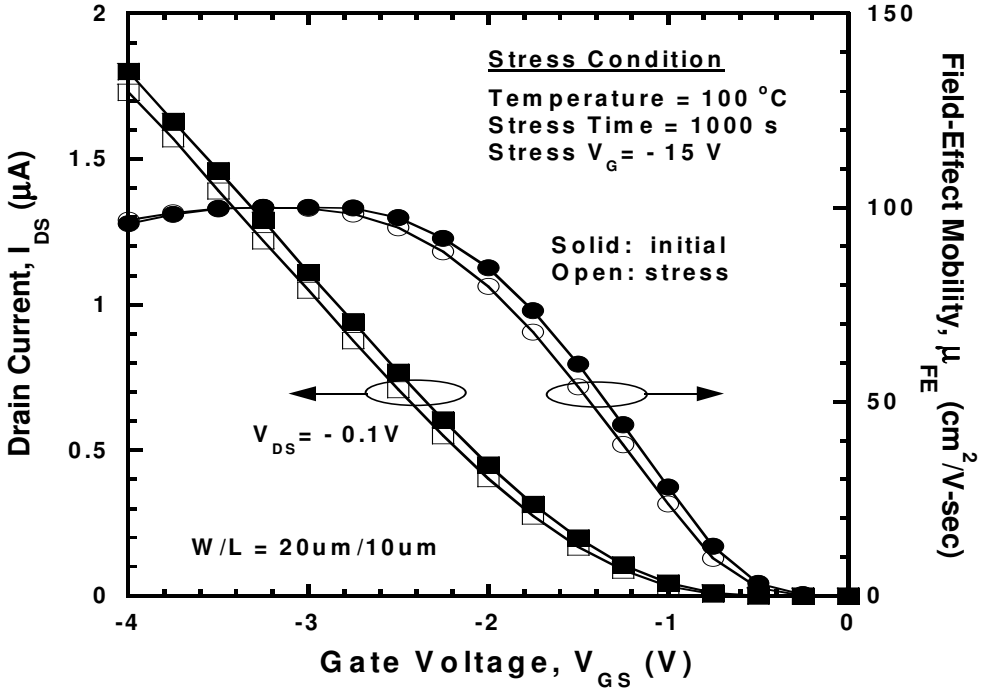


(f) Inter-layer dielectric deposition and dopant activation.

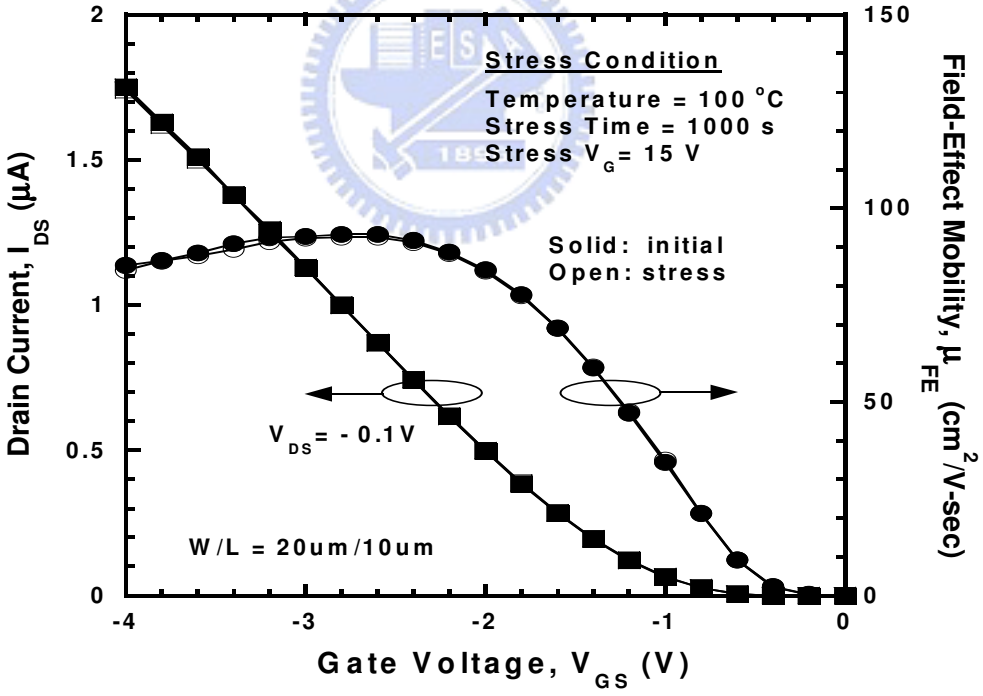


(g) Contact hole opening, and interconnection metal deposition and patterning.

Fig. 2.2 Process flow of the *p*-channel LTPS TFT.

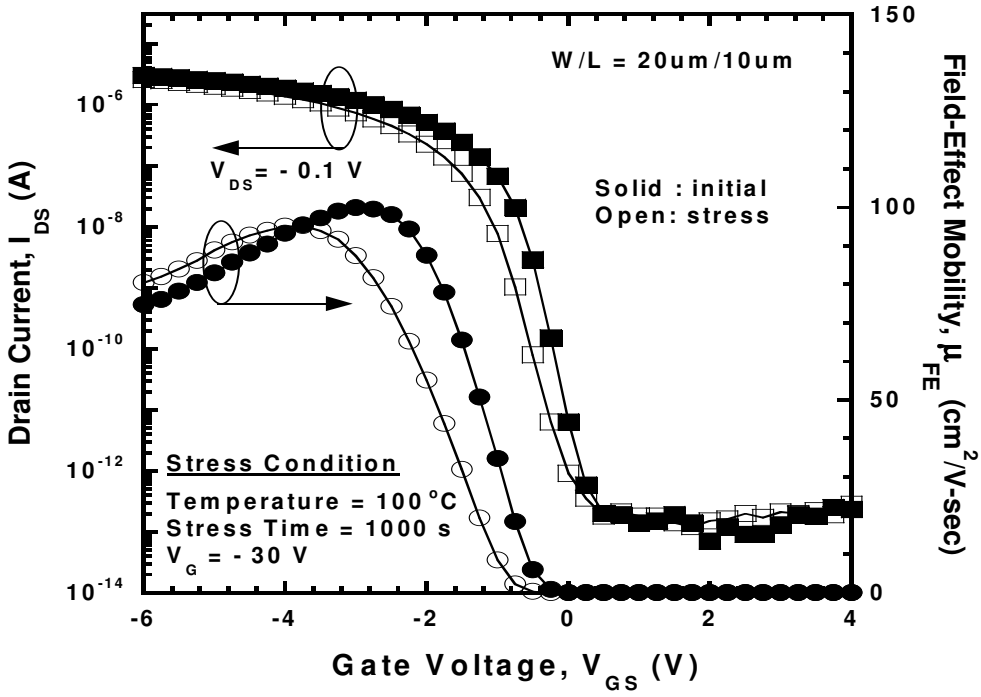


(a)

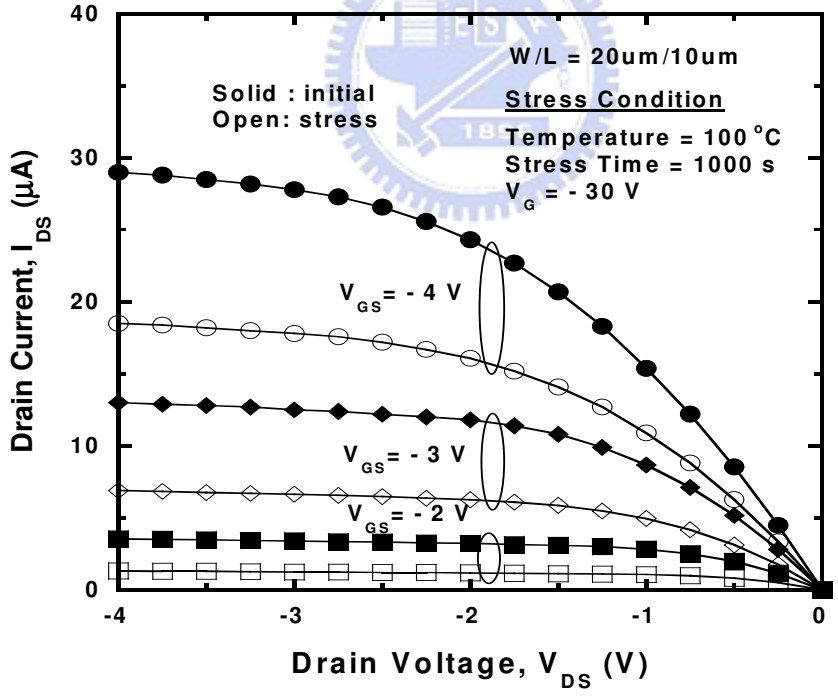


(b)

Fig. 2.3 Transfer characteristics in the linear scale of the LTPS TFTs before and after 1000 s (a) NBTI stress and (b) PBTI stress with stress voltages of ± 15 V.



(a)



(a)

Fig. 2.4 (a) Transfer characteristics and (b) output characteristics of the LTPS TFT both before and after 1000 s NBTI stress at 100 °C with a stress voltage of −30 V.

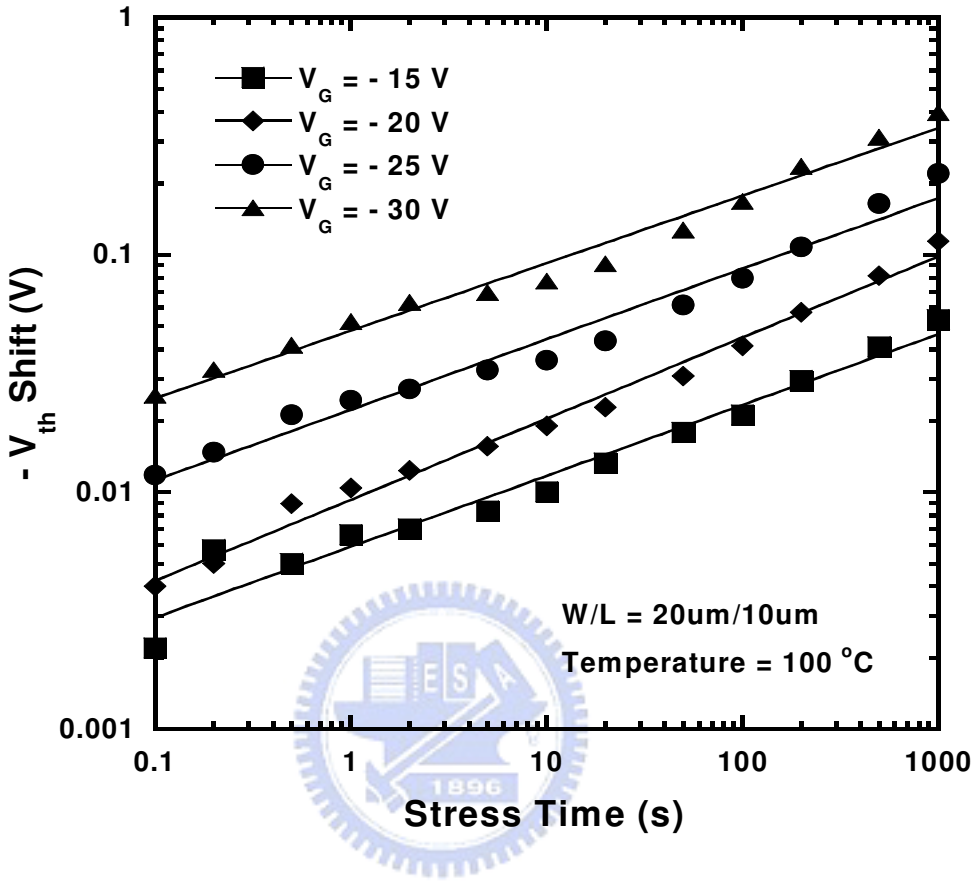


Fig. 2.5 (a) Dependence of the threshold-voltage shift on the stress time under various stress conditions.

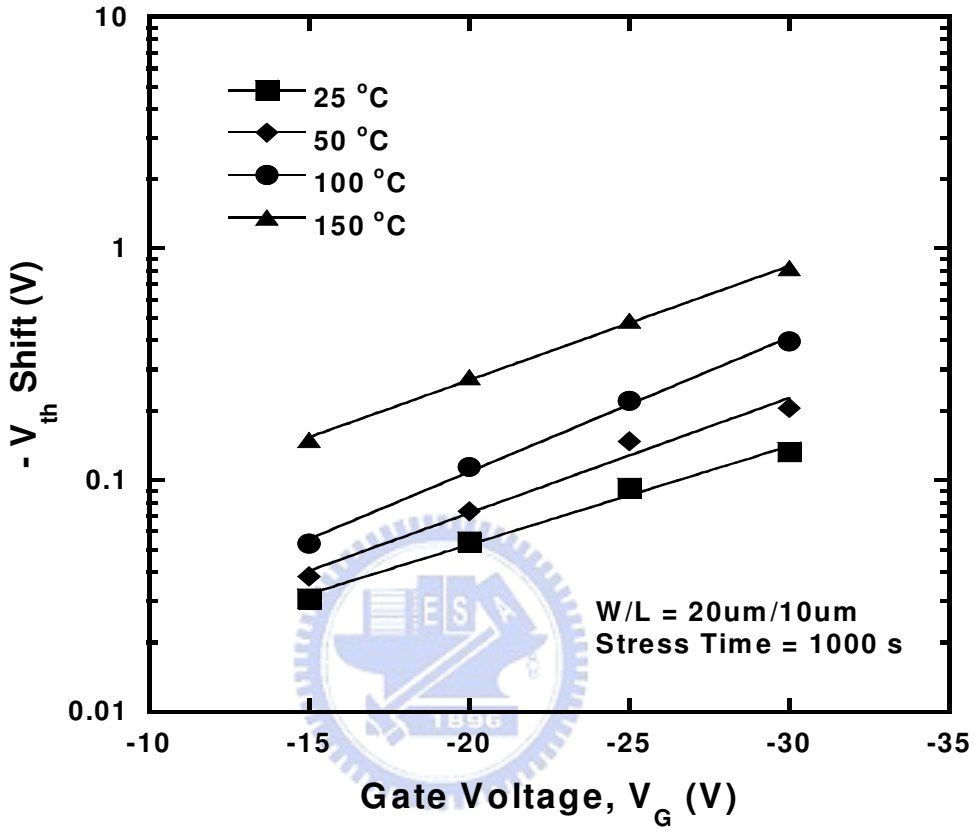


Fig. 2.5 (b) Dependence of the threshold-voltage shift on the stress voltage under various stress conditions.

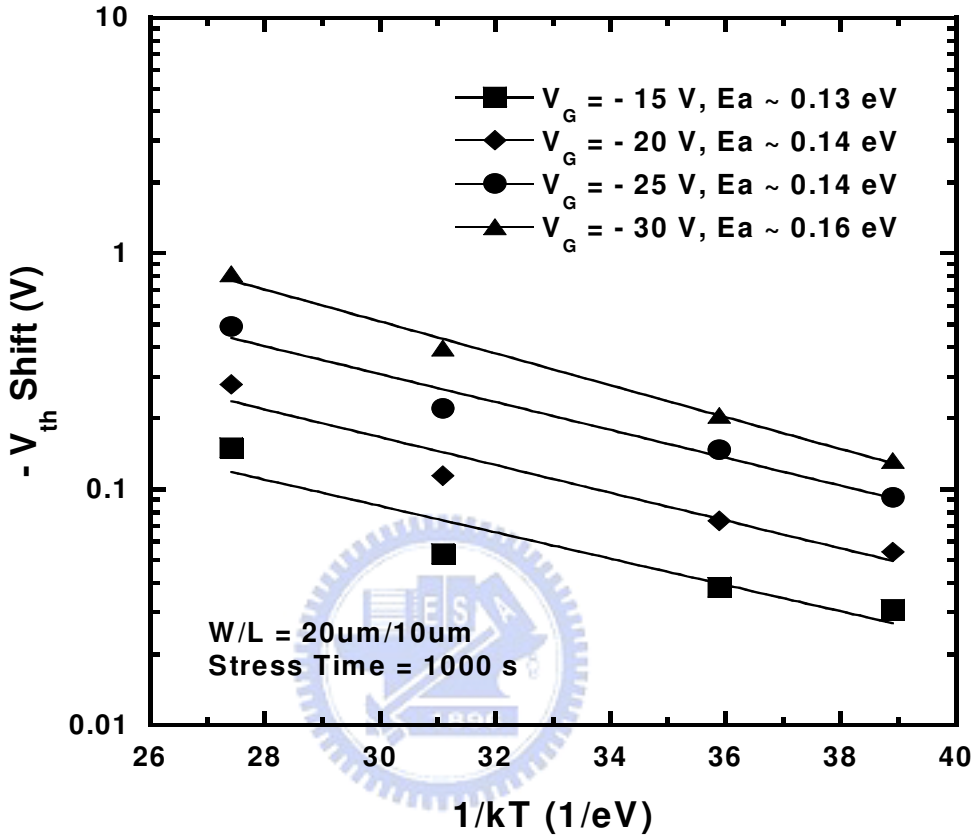
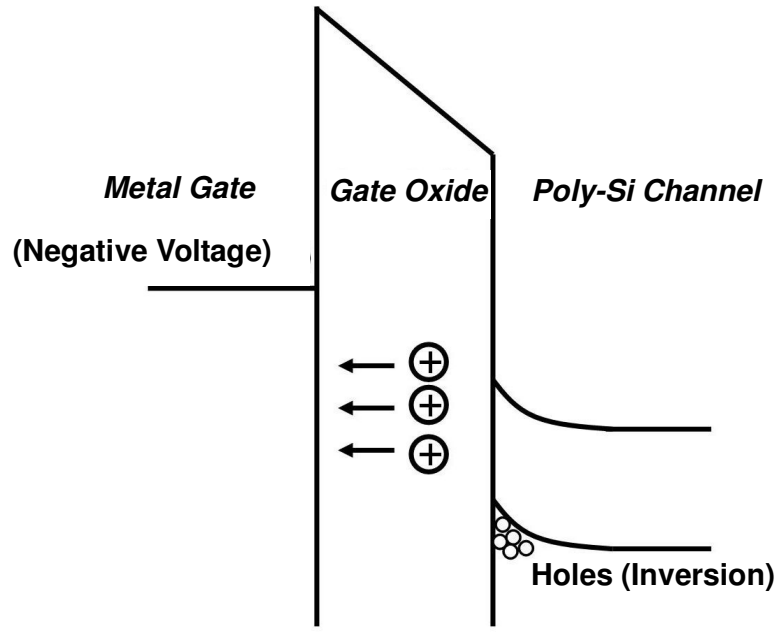
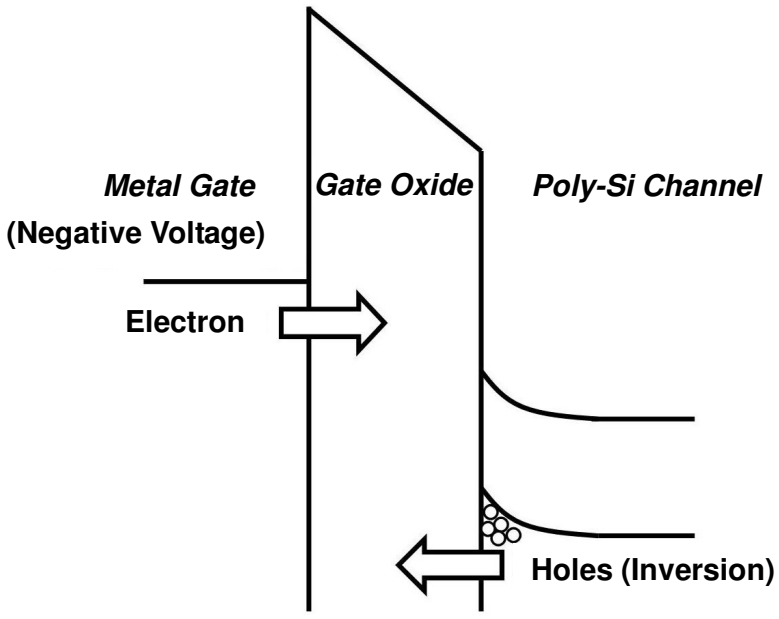


Fig. 2.5 (c) Dependence of the threshold-voltage shift on the stress temperature under various stress conditions.



(a)



(b)

Fig. 2.6 (a) Positive ion drift causes a reduction in the net amount of positive charge near the poly-Si/SiO_2 interface, resulting in a positive shift of the threshold voltage. (b) Injection of electrons or holes in to the gate dielectric leads to the threshold-voltage shift.

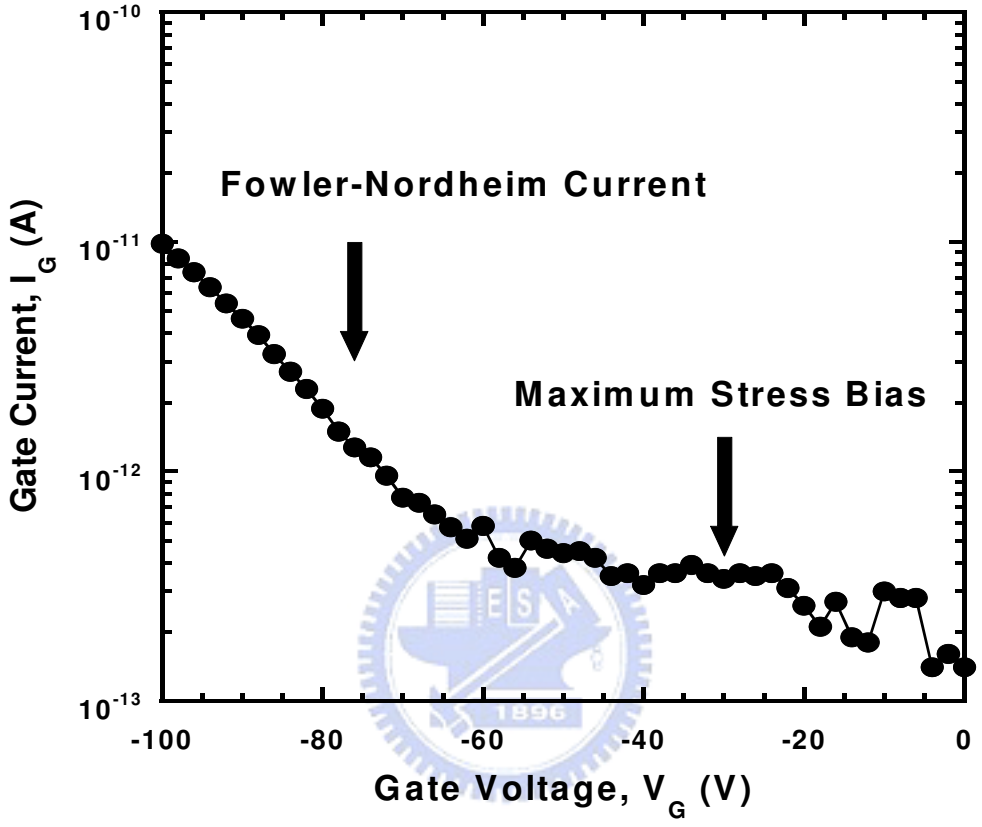


Fig. 2.7 Gate current of the LTPS TFT. Fowler－Nordheim current is not prominent at the maximum stress bias of －30 V. Therefore, the extra trap-state generation and device instability caused by small currents can be neglected.

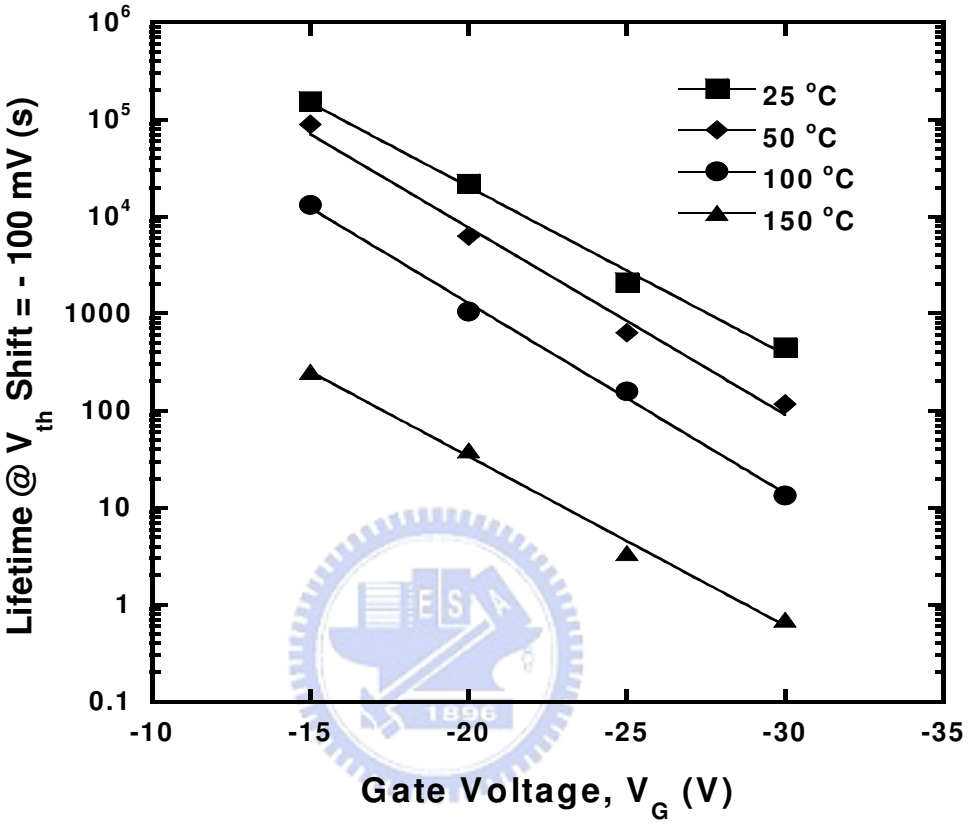


Fig. 2.8 Dependence of the lifetime on the stress voltage with various stress temperatures. The lifetime is defined as the time taken to reach a threshold-voltage shift of 100 mV.

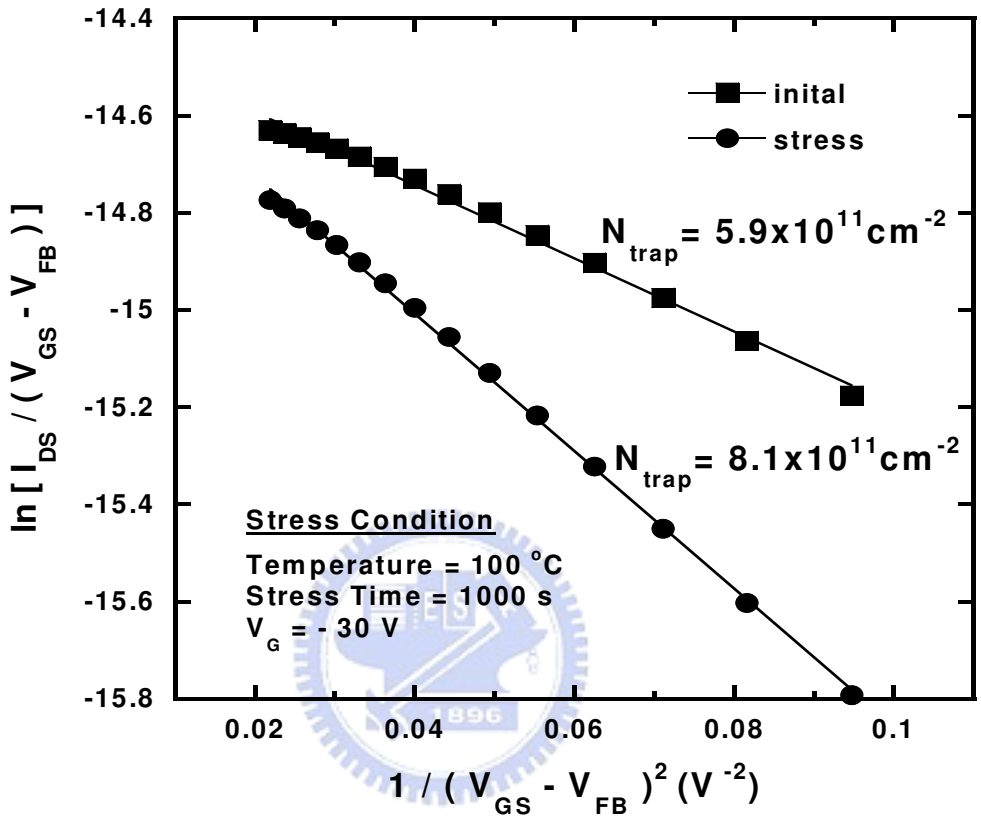


Fig. 2.9 Grain-boundary trap-state density extraction of the LTPS TFT before and after 1000 s NBTI stress at 100 °C with a stress voltage of −30 V.

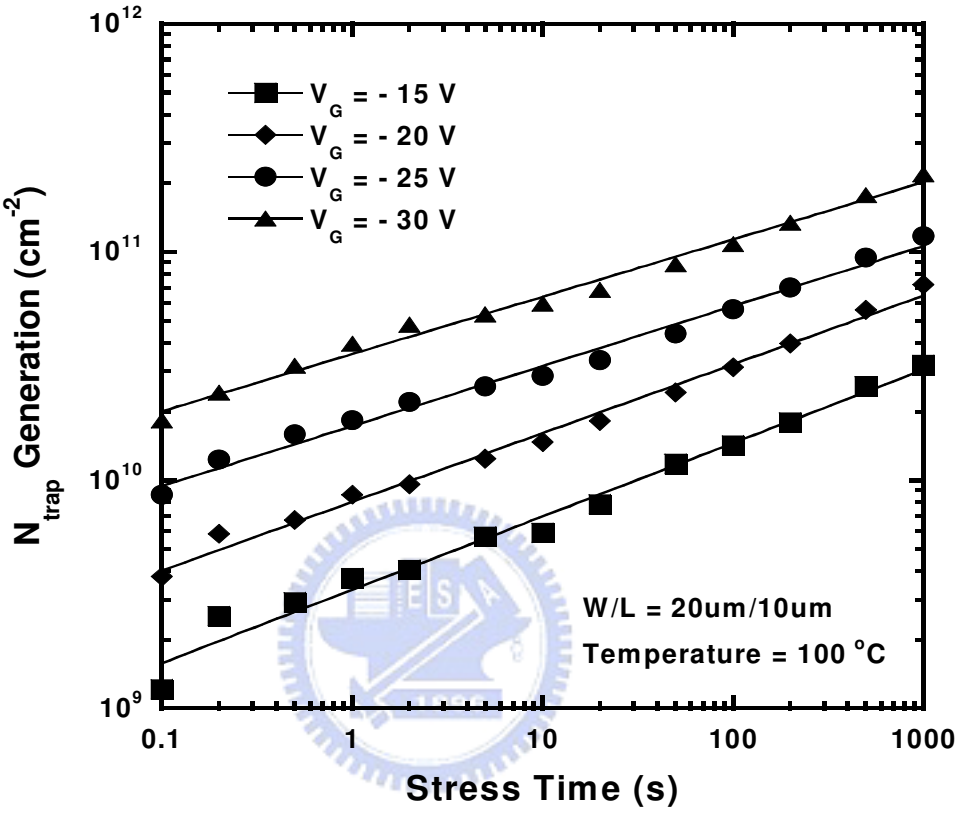


Fig. 2.10 (a) Dependence of the grain-boundary trap-state generation on the stress time under various stress conditions.

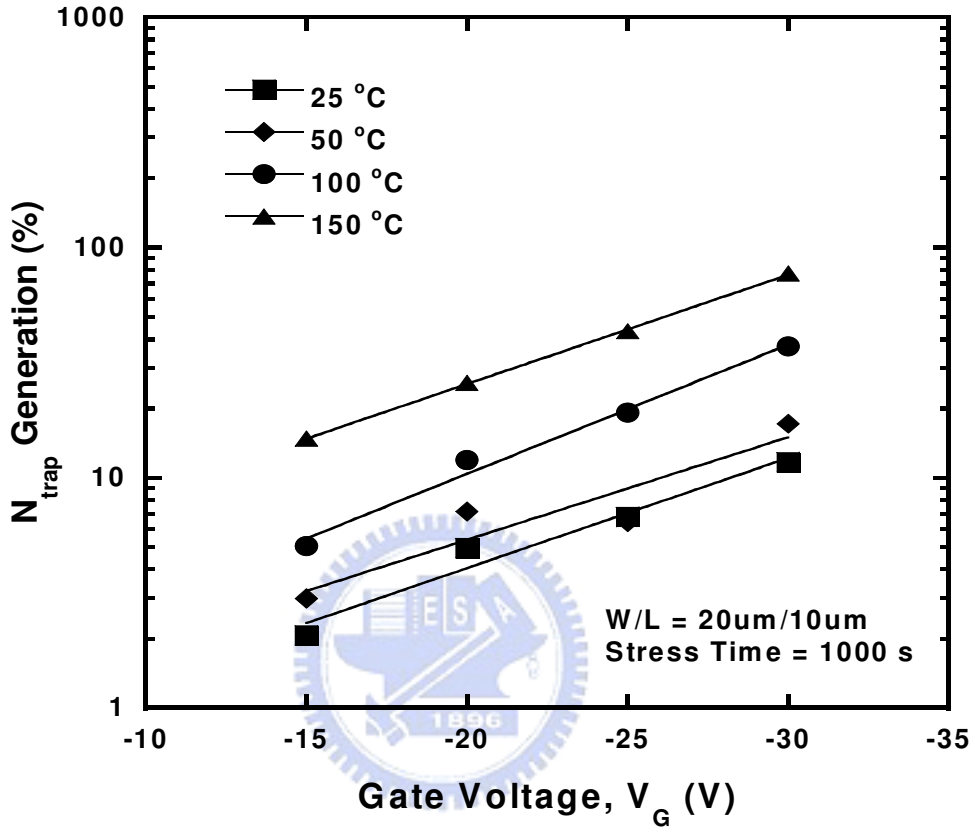


Fig. 2.10 (b) Dependence of the grain-boundary trap-state generation on the stress voltage under various stress conditions.

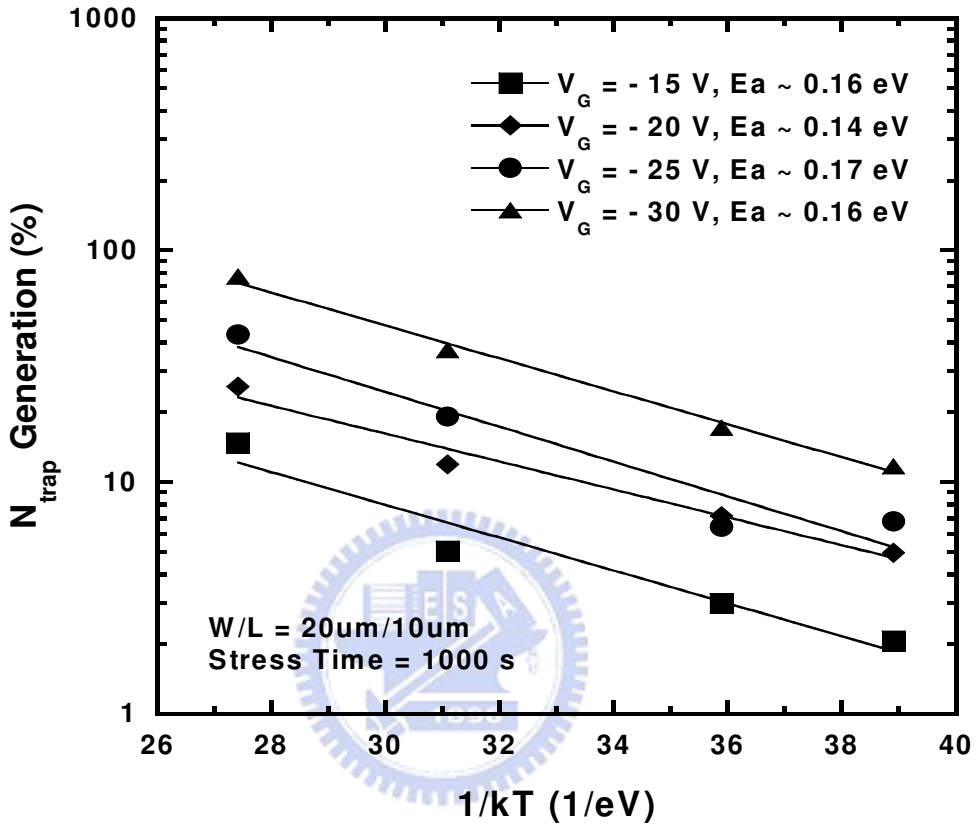


Fig. 2.10 (c) Dependence of the grain-boundary trap-state generation on the stress temperature under various stress conditions.

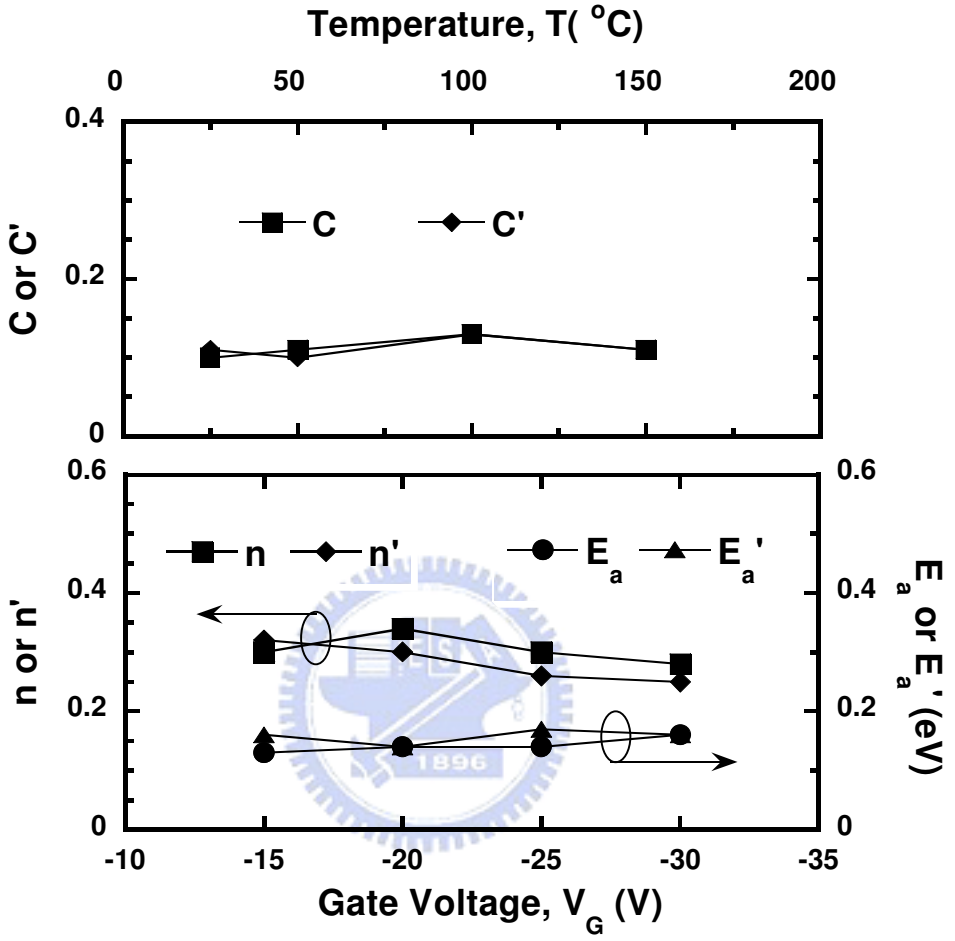


Fig. 2.11 Comparison of the parameters extracted from the grain-boundary trap-state generation and the threshold-voltage shift.

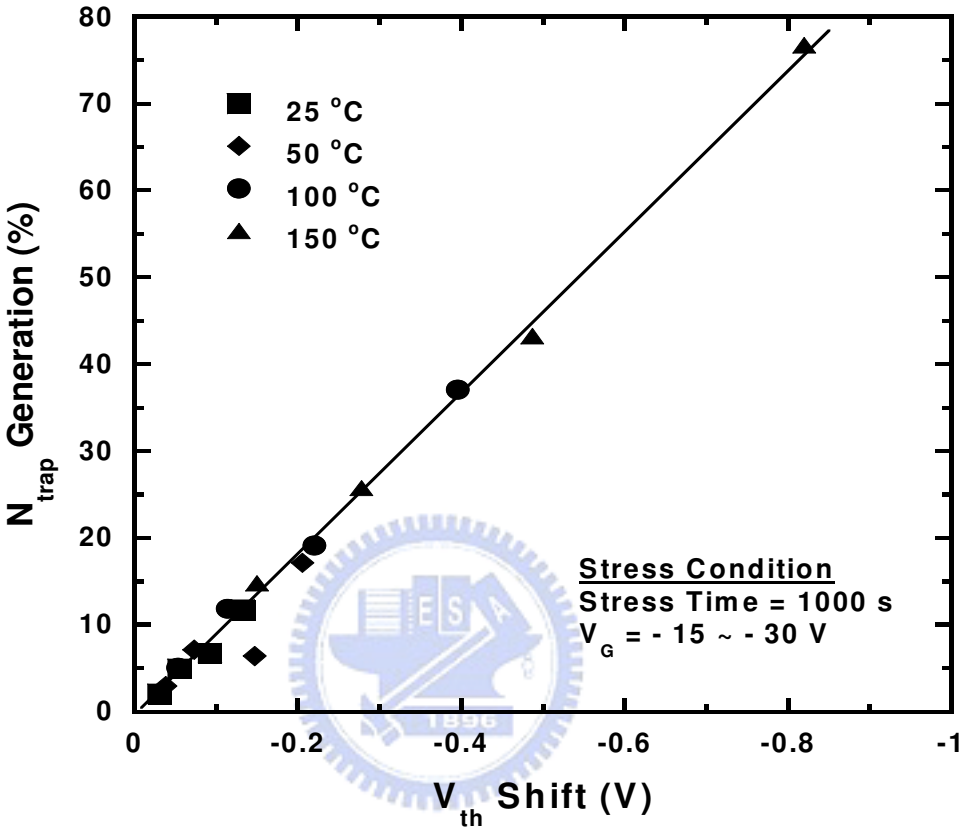
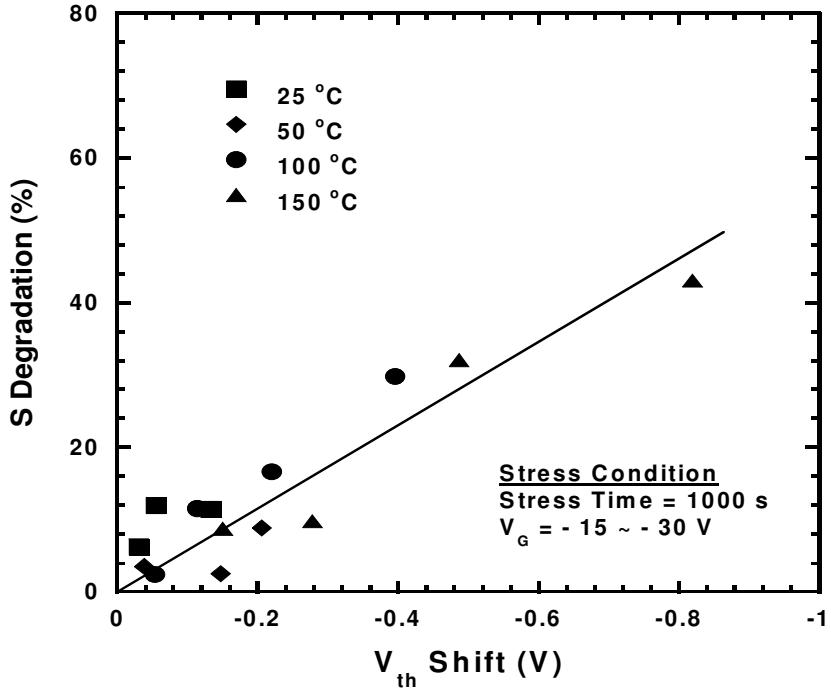
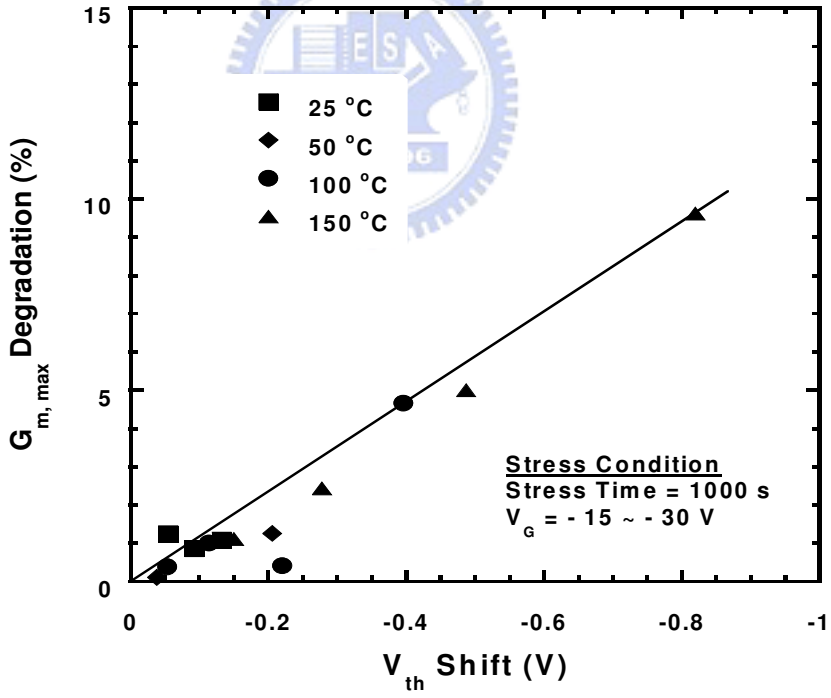


Fig. 2.12 Correlation between the grain-boundary trap-state generation and the threshold-voltage shift of the LTPS TFTs after NBTI stress.



(a)



(b)

Fig. 2.13 Correlation between the degradation of the (a) subthreshold swing, (b) maximum transconductance, and the threshold-voltage shift of the LTPS TFTs after 1000 s NBTI stress.

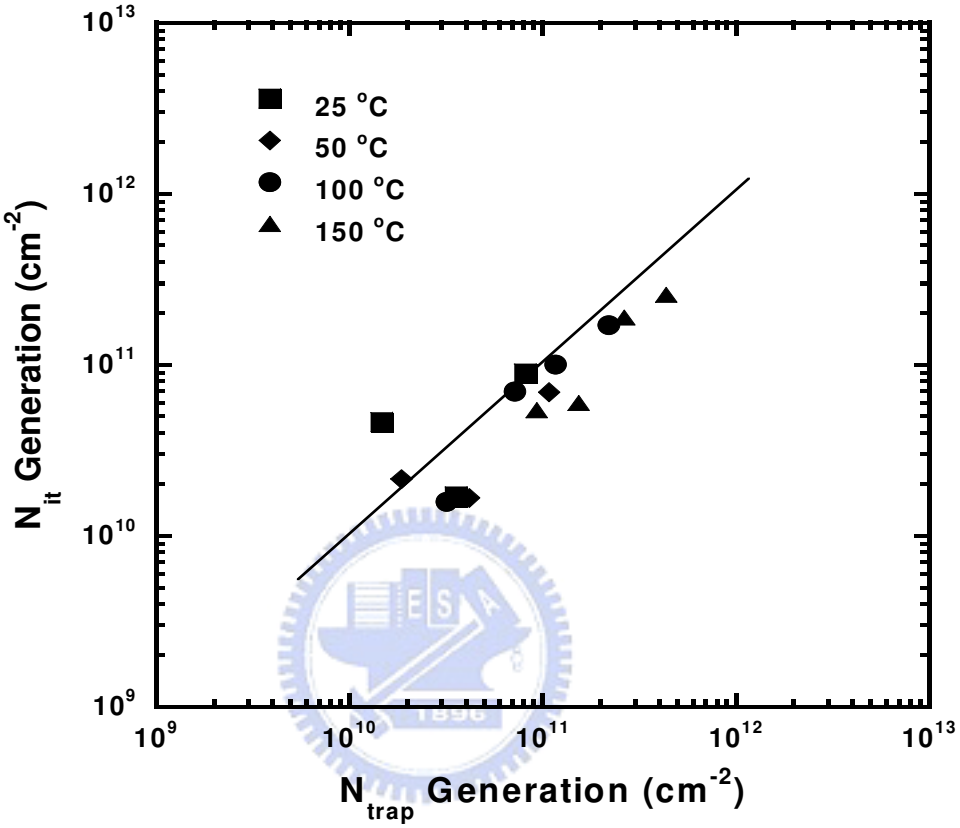


Fig. 2.14 Correlation between the generation of interface trap states and grain- boundary trap states of the LTPS TFTs after NBTI stress.

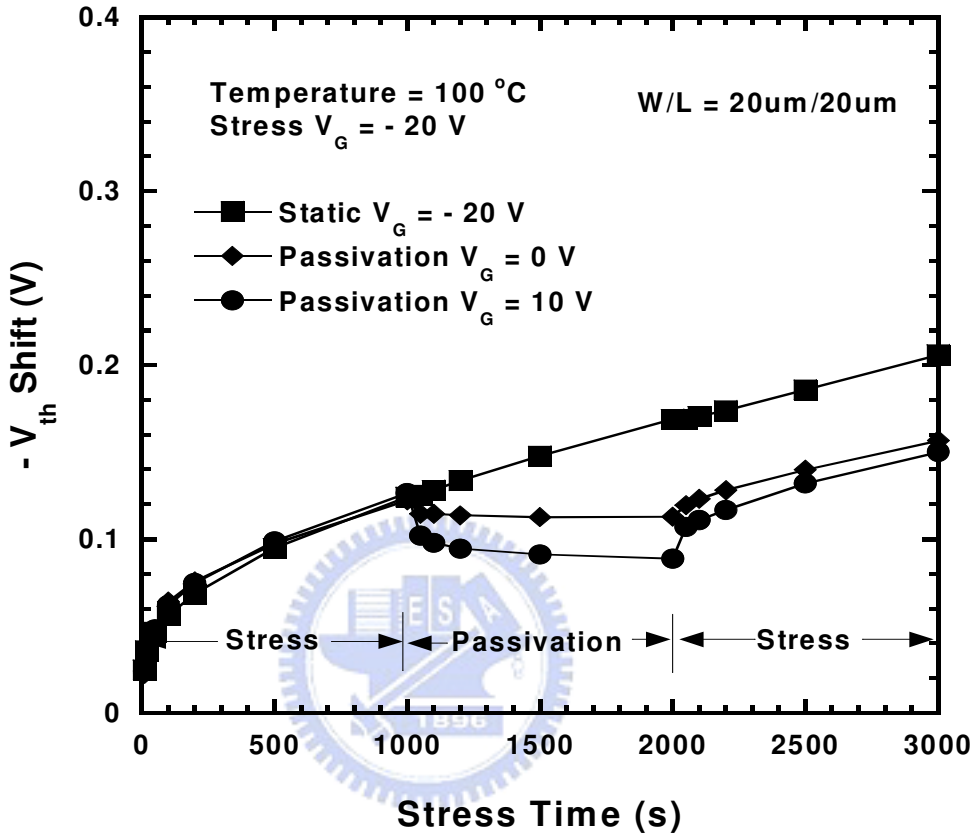


Fig. 2.15 Transfer characteristics of the devices under static stressing process and stressing-passivation-stressing process.

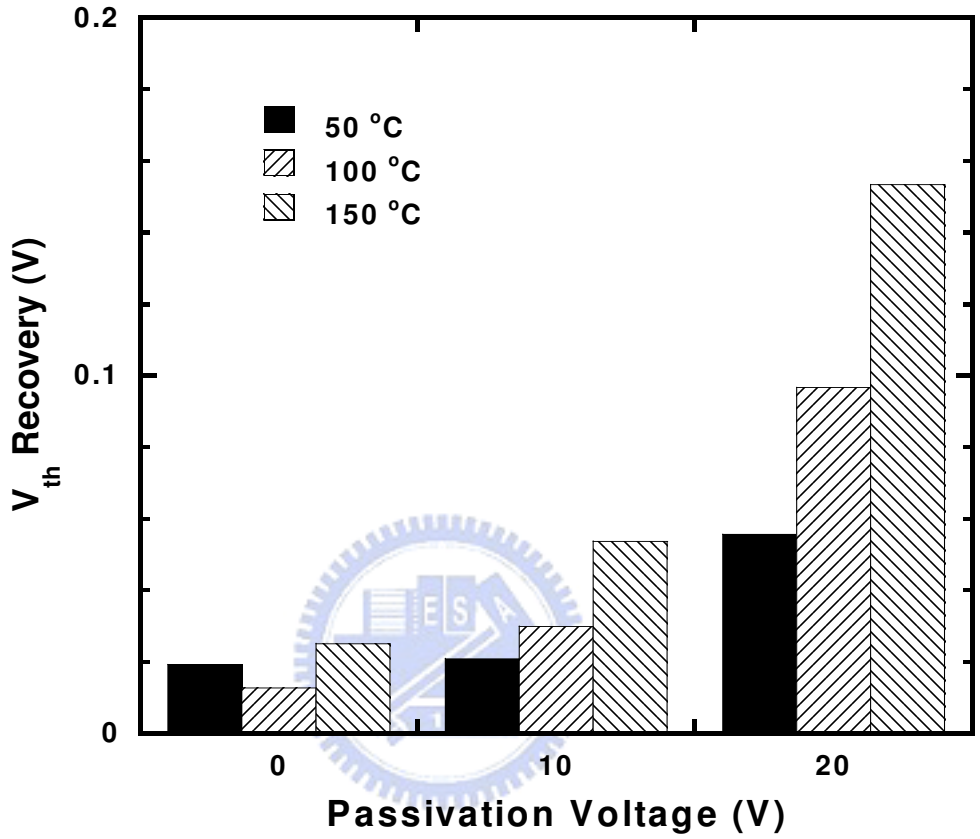
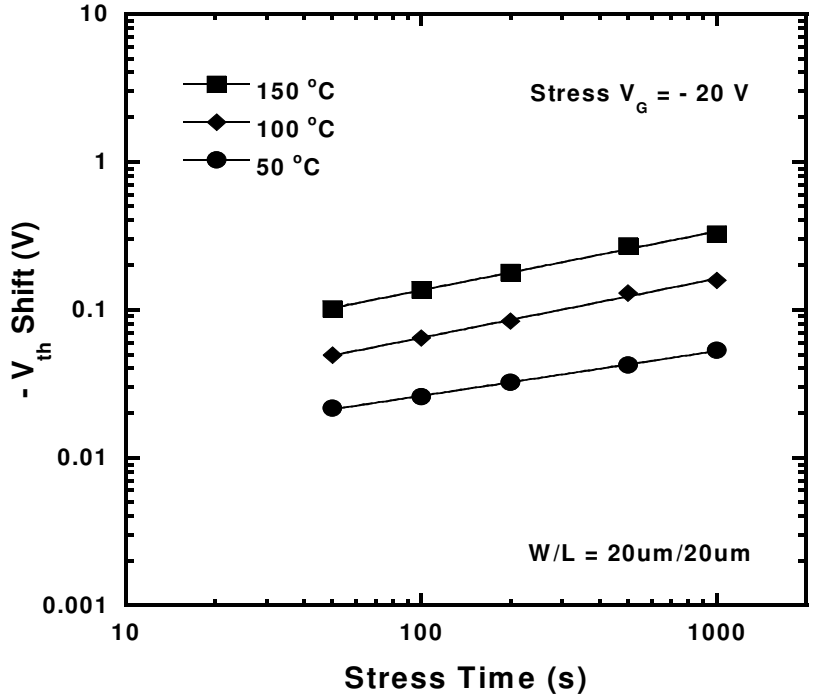
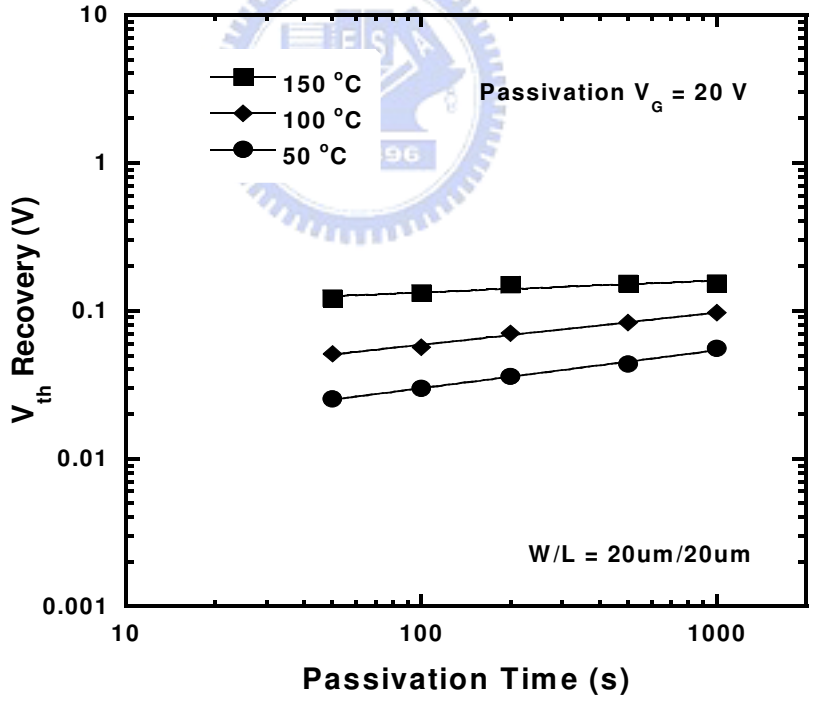


Fig. 2.16 Comparison of the threshold-voltage recovery under various temperatures and passivation voltages.



(a)



(b)

Fig. 2.17 Time dependence of the (a) threshold-voltage shift and (b) threshold- voltage recovery of the devices during the stressing-passivation process.

Table 2.1 Effect of different species on fractional time dependence of NBTI evolution for a diffusion-limited system.

(Ref. Chakravarthi *et al.*, in *Proc. IEEE Int. Reliab. Phys. Symp.*, 2004.)

Species	***Exponent***
$\mathbf{H^o}$	**0.25**
$\mathbf{H_2}$	**0.165**
$\mathbf{H^o, H_2}$	**0.165 – 0.25**
$\mathbf{H^+}$	**0.25 – 0.5**
$\mathbf{H^o, H_2, H^+}$	**0.165 – 0.5**

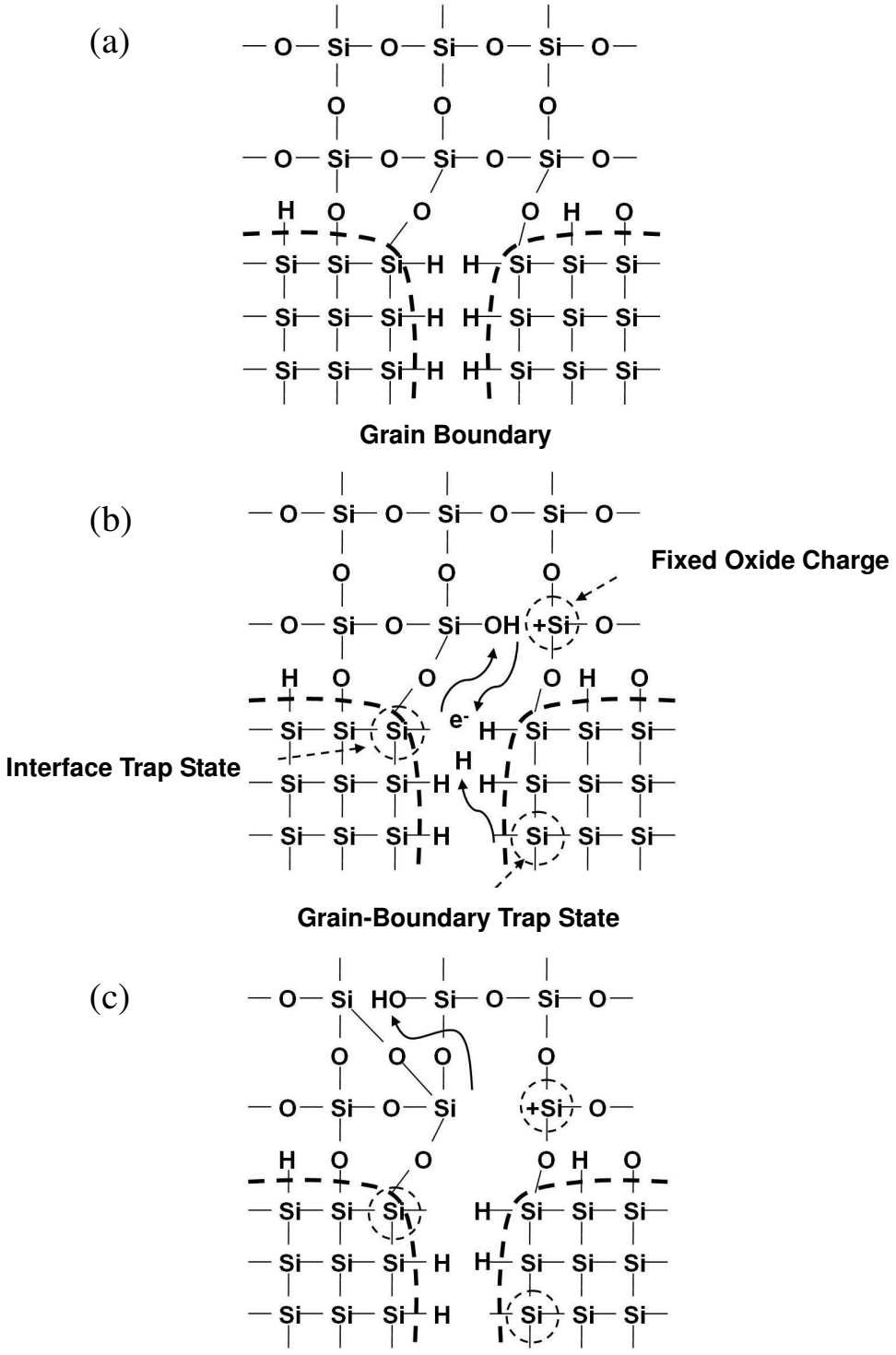


Fig. 2.18 Schematic illustration of the poly-Si/SiO_2 interface showing (a) the $\equiv Si-H$ defects at the poly-Si/SiO_2 interface and in the grain boundaries, (b) generation of the interface trap states, grain-boundary trap states, and fixed oxide charges, and (c) diffusion of the hydrogen species in the gate oxide.

Chapter 3

Analysis of Negative Bias Temperature Instability in Body-Tied Low-Temperature Polycrystalline Silicon Thin-Film Transistors

3.1 Introduction

In MOSFETs, NBTI refers to the generation of interface trap states and fixed oxide charges under negative bias stress, resulting in the threshold-voltage shift of the devices [3.1]－[3.5]. As described in Chapter 2, the greatest impact of NBTI occurs in *p*-FET devices, since it was only those types which experienced a negative bias condition during a typical CMOS circuit operation. It is well accepted that the NBTI degradation originates from the broken bond of the hydrogenated silicon (Si－H). In LTPS TFTs, due to the trap states in the grain boundaries and the poly-Si/SiO_2 interface, there are more Si-H bonds in the channel region compared to MOSFETs. Besides, due to the poor thermal conductivity of the glass substrate and high operation voltage, we suppose that NBTI can be an important reliability issue for LTPS TFTs. Therefore, it is important to study the NBTI behaviors and the related degradation mechanism of LTPS TFTs.

Some studies have pointed out that NBTI stress degrades the reliabilities of LTPS TFTs as well as MOSFETs, in which TFTs are held at a condition in which the gate electrodes are positively biased with the source and drain grounded at high temperatures [3.6]－[3.9]. As is known, the characteristics of LTPS TFTs are generally influenced by grain-boundary trap states. Therefore, it is important to investigate the degradation of the bulk channel region of LTPS TFTs under NBTI stress. Several studies of the bulk trap state

evaluation method have been reported so far, in which the channel properties are all derived from the current-voltage characteristics [3.10][3.11]. However, the channel current is affected only through the potential barrier formed by the trap states, and hence is not directly related to the bulk trap properties [3.12]. An important contribution to TFT characterization was made by Koyanagi and Balasinski *et al.*, who proposed a charge-pumping technique to directly characterize the bulk trap properties in poly-Si TFTs [3.12]—[3.16]. It is confirmed that a large number of donor-like and acceptor-like traps exist in the grain boundaries and at the poly-Si/SiO_2 interface. The bulk trap states can be revealed from the charge-pumping current because carriers are observed as the generation-recombination current, and hence the charge-pumping current directly indicates the trap properties.

The principle of a charge-pumping-current measurement was introduced by Brugler and Jespers [3.17]. During measurement, the gate of a transistor is connected to a pulse generator, and the source and drain are held at a certain reverse bias voltage with respect to the substrate, while the substrate current is measured. When a pulse voltage is applied to the gate of a *p*-channel LTPS TFT to invert the channel, holes will flow from the source and drain regions into the channel. Meanwhile, some of the holes will be captured by bulk trap states. When the pulse gate voltage is driving the channel surface back into accumulation, the holes in the channel drift back to the source and drain under the influence of a reverse bias. However, the holes trapped in the bulk trap states will recombine with the electrons from the substrate and give rise to a net flow of positive charge into the substrate. This is the so-called *charge-pumping effect* [3.18]. Figs. 3.1(a) and 3.1(b) show the schematic diagrams illustrating the pulse waveform and charge-pumping curve, respectively, of a *p*-channel transistor measured under fixed pulse amplitude and variable pulse base voltages (V_{GB}). The charge-pumping current is observed between the pulse base voltages corresponding to V_{FB} (flat-band voltage) and V_{th} (threshold voltage) plus ΔV (pulse amplitude) when the surface potential is switched between inversion and accumulation. Otherwise, no charge-pumping

current can be measured.

In MOSFETs, the charge-pumping technique has been widely adopted to identify the interface trap-state generation [3.19]－[3.21]. In LTPS TFTs, the grain-boundary trap states also give rise to a charge-pumping current. Consequently, the bulk trap states measured by a charge-pumping technique consist of both the grain-boundary trap states and interface trap states, as shown in Fig. 3.2(a). However, to our knowledge, this technique has not been reported to have investigated the NBTI effect in LTPS TFTs. Therefore, the aim of our study is to use a charge-pumping technique to investigate the real behavior of bulk trap states during NBTI stress. Also, since the relation between the fixed-oxide-charge generation and NBTI degradation has not been clearly identified, the role of fixed-oxide-charge generation during NBTI stress is also analyzed in this study. Finally, we also propose a NBTI-degradation mechanism for LTPS TFTs.

3.2 Experiments

LTPS TFTs were fabricated with both a channel length (L) and width (W) of 10μm. The detail process flow has been described in Chapter 2. NBTI stress was performed by heating a glass substrate to a temperature ranging from 75 ^{o}C to 150 ^{o}C, and a voltage in the range of －13 V to －20 V was then applied on the gate with the source, drain, and body grounded. During the measurement of charge-pumping current, a pulse train with a frequency of 100 kHz and a fixed pulse amplitude of 1.5 V was applied to the gate while the charge-pumping current was measured between the source/drain and substrate contact, and the base voltage was varied to tune the surface condition from inversion to accumulation. The schematic diagrams of the plane and cross-sectional views of the LTPS TFT and the setup of the charge-pumping current measurement are shown in Figs. 3.2(b) and 3.2(c).

3.3 Results and Discussion

3.3.1 Basic Charge-Pumping-Current Characteristics

Before we analyze the NBTI-degradation mechanism of LTPS TFTs, the basic charge-pumping current characteristics must be identified to optimize the measurement condition. In our experiment, the measurement was performed by varying the pulse base voltage from inversion to accumulation while keeping the amplitude of the pulse constant. Figs. 3.3－3.10 show the curves of charge-pumping currents and the dependence of the maximum charge-pumping currents and the bulk trap-state density on the measurement conditions, including frequency, pulse amplitude, raising time, falling time, source/drain bias, and duty ratio.

Fig. 3.3(a) shows the charge-pumping current measured with different frequencies. The charge-pumping current gradually increases with the pulse base voltage, then reaches the maximum value and finally gradually decreases. The curve is not as sharp as that seen in MOSFET. This is because the threshold-voltage distribution in the channel of the LTPS TFT is non-uniform due to the grain boundaries [3.16]. Fig. 3.3(b) indicates that the charge-pumping current increases with the frequency of the pulse voltage. However, the measured bulk trap-state density decreases. This may be due to the reduced time for the carrier to fill the trap states. In order to obtain more information of on the bulk trap-state properties, the pulse frequency in our charge-pumping measurement was set to be 100 kHz.

In Figs 3.4(a) and 3.4(b), the charge-pumping current and the measured bulk trap-state density increase with the pulse amplitude. This can be explained by the reduced emission time of electrons ($t_{em,\,e}$) and holes ($t_{em,\,h}$) as the pulse amplitude increases, as shown in Figs. 3.5(a) and 3.5(b). Furthermore, since only those regions can be sensed where $\Delta V > |V_{th} - V_{fb}|$, increasing the pulse amplitude permits to sense bulk traps further into the source and drain regions [3.22], as shown in Figs. 3.6(a) and 3.6(b). Although a larger value of pulse

amplitude is useful to get more information about the bulk trap-state properties, still, a larger range of pulse voltage is required to measure the charge-pumping curve, and this is time-consuming and may result in the recovery of the threshold-voltage shift during NBTI stress. Therefore, the pulse amplitude in our measurement was set to be 1.5 V.

In Figs. 3.7 and 3.8, the charge-pumping current and measured bulk trap-state density decrease as the rising time or falling time increases. This can be explained by the enlarged emission time of electrons ($t_{em,\,e}$) or holes ($t_{em,\,h}$) as the rising time or falling time increases, as shown in Figs. 3.9(a) and 3.9(b). Although a smaller value of the rising time or falling time is useful to get more information about the bulk trap-state properties, yet Uraoka *et al.* have pointed out that a smaller value of the rising time or falling time leads to device degradation in field-effect mobility [3.23]. Therefore, the values of both the rising time and falling time in our charge-pumping measurement were set to be 100 ns.

In Fig. 3.10(a) and 3.10(b), the charge-pumping current and measured bulk trap-state density decrease as the source/drain reverse bias increases. When a reverse bias is applied to the source and drain with respect to the substrate, body effect appears and results in the increase of the threshold voltage (modulus). It therefore limits the scanning into the source/drain regions, and hence decreases the maximum charge-pumping current. Therefore, in order to get more information about the bulk trap-state properties, the values of the reverse source/drain bias in our charge-pumping measurement were set to be -50 mV. Finally, the effect of the duty ratio is shown in Figs. 3.11(a) and 3.11(b). The duty ratio shows a negligible effect on the charge-pumping current and bulk trap-state density. Therefore, the duty ratio was set at 50 % in our measurement.

3.3.2 Device Degradation Due to NBTI

Figs. 3.12(a) and 3.12(b) show the transfer characteristics on a linear and logarithmic scale, respectively, of the LTPS TFT before and after NBTI stress at 150 ^{o}C with the stress

gate voltage of –20 V for 1000 s. The stress degrades the subthreshold swing and field-effect mobility, indicating that interface trap states were generated [3.24]. The threshold voltage (V_{th}) also shifts to the negative direction after the stress. The NBTI degradation can be attributed to the generation of bulk trap states (including grain-boundary and interface trap states) and fixed oxide charges. Detailed analysis of these trap-state generations will be discussed below.

Figs. 3.13(a)－3.13(c) show the charge-pumping current before and after 1000 s NBTI under the stress conditions of V_G = －15 V at 100 °C, V_G = －20 V at 100 °C, and V_G = －15 V at 150 °C, respectively. It is obvious that the charge-pumping current increases after NBTI stress; this directly indicates that bulk trap states are generated during the NBTI stress, and implies that bulk trap-state generation plays an important role in the NBTI-degradation mechanism of LTPS TFTs. In addition, the curve of the charge-pumping current shifts to the negative direction after the stress, and this implies that a net positive charge is clearly generated in the oxide or/and at the interface. As the stress voltage increases from －15 V to －20 V at 100 °C, the charge-pumping current variation increases from 3.4 % to 8.2 %; as the stress temperature increases from 100 °C to 150 °C under the stress voltage of －15 V, the charge-pumping current variation increases from 3.4 % to 10.3 %. The results confirm that the NBTI degradation becomes more serious as the stress voltage or stress temperature increases.

3.3.3 Analysis of the Bulk Trap-State Generation

Fig. 3.14(a) shows the time dependence of the bulk trap-state density (N_{bulk}) generation under various stress voltages and stress temperatures. The bulk trap-state density is calculated from the charge-pumping current. The generation of bulk trap states follows a power law dependence on the stress time with an exponent from 0.41 to 0.43. Such a power-law dependency is characteristic of NBTI [3.1], [3.2]. The values of the exponents are

slightly larger than those extracted from the conventional LTPS TFTs as shown in Chapter 1 (from 0.28 to 0.34). This indicates that the body-tied TFT has a faster degradation rate than the conventional TFT under NBTI stress. Fig. 3.2 may be used to explain this phenomenon. Our body-tied TFT is fabricated through the heavily doped n^+ region. When the device is turned on during the NBTI stress, the gate inverts the n^+ layer beneath it and the inverted n^+ layer is just like the normal *p*-channel formed beneath the normal gate. When the body tie is grounded, the extra *p*-layer (the inverted n^+ layer) can transport extra holes to the normal poly-Si/SiO_2 interface due to the potential drop. Therefore, the extra holes assist more bond dissociation and accelerate the NBTI degradation [3.25].

In addition, the atomic hydrogen model indicates that the release of a neutral hydrogen atom is the primary NBTI-degradation mechanism, which exhibits a power-law dependence on the stress time with an exponent of 0.25. The atomic hydrogen model can be expressed as:

$$SiH + h^+ \longleftrightarrow Si^+ + H^o. \qquad (Eq.\ 3.1)$$

On the other hand, the proton model clarifies that proton (H^+) participates in the NBTI degradation, in which the exponent approximates from 0.25 to 0.5. The proton model can be expressed as:

$$SiH + 2h^+ \longleftrightarrow Si^+ + H^+. \qquad (Eq.\ 3.2)$$

In addition to the diffusion component (H^o), the drift component (H^+) arises because the charged hydrogen species can also move under the influence of the electric field. Due to the additional drift component, therefore, the value of the exponent is larger than 0.25 [3.26]. In our experiments, we suggest that the extra *p*-layer (the inverted n^+ layer) provides extra holes to enhance the generation of proton and leads to the larger value of the exponent.

In our study, we found that the bulk trap-state density variation not only shows a power law dependence on the stress time, but also exhibits an exponential dependence on both the stress voltage (V_G) and the reciprocal of temperature (*1/T*). From our experimental results, the behavior of the bulk trap-state density variation can be expressed as the following

equation:

$$\Delta N_{bulk} \propto t^{n} e^{(-E_a/kT)} e^{C|V_G|}, \qquad (Eq.\ 3.3)$$

where n is the time dependent exponent. The voltage accelerated factor C extracted from Fig. 3.14(b) is between 0.14 and 0.19, which is dependent on the process and independent of the stress voltage [3.27]. The activation energy (E_a) extracted from the Arrhenius plot of Fig. 3.14(c) is between 0.25 to 0.30 eV. Moreover, Figs. 3.14(b) and 3.14(c) show that the bulk trap-state density increases with the stress voltage or stress temperature; this confirms that the bulk trap-state generation induced by NBTI stress can be electrically and thermally activated. Also, the charge trapping model can't explain the exponential dependence of threshold voltage shift on V_G and $1/T$ [3.28], [3.29]. Furthermore, the electric field across the gate dielectric (below 2 MV/cm) was not high enough to cause a hole injection. Therefore, we further confirm that the NBTI degradation in LTPS TFTs is attributed to the diffusion-controlled electrochemical reactions instead of the charge trapping model. Fig. 3.15 presents the correlation between the bulk trap-state density variation and the threshold-voltage shift. These two physical quantities are closely related and show linear relation, and this demonstrates that the bulk trap-state generation attributes to the NBTI degradation in LTPS TFTs.

3.3.4 Analysis of the Fixed-Oxide-Charge Generation

In MOSFETs, the NBTI degradation is generally explained by the generation of interface trap states and fixed oxide charges. In LTPS TFTs, because the NBTI degradation can be explained by the diffusion-controlled electrochemical reactions, we can assume that the threshold-voltage shift is caused by the generation of bulk trap-state density (N_{bulk}) and fixed-oxide-charge density (N_{ox}). Therefore, the threshold-voltage shift (ΔV_{th}) can be simply expressed as:

$$\Delta V_{th} = -\frac{q(\Delta N_{bulk} + \Delta N_{ox})}{C_{ox}}, \qquad (Eq.\ 3.4)$$

where q is the electron charge and C_{ox} is the oxide capacitance. According to *Eq.* 3.4, the fixed-oxide-charge density can be calculated from the measured threshold-voltage shift and bulk trap-state density generation.

Fig. 3.16(a) shows the time dependence of the fixed-oxide-charge density variation under various stress voltages at 100 °C. It is interesting that the increases of the fixed-oxide-charge density, like the bulk trap-state density, also follows a power law dependence on the stress time. The exponent ranges between 0.35 and 0.50. Besides, the increase of the fixed-oxide-charge density shows an exponential dependence on the stress voltage and reciprocal of the stress temperature. Accordingly, we can express the bulk trap-state density variation with the following equation:

$$\Delta N_{ox} \propto t^{n'} e^{(-E_a'/kT)} e^{C'|V_G|}. \qquad (Eq.\ 3.5)$$

The parameter *C'* extracted from Fig. 3.16(b) is between 0.24 and 0.27, while the activation energy (E_a') extracted from the Arrhenius plot of Fig. 3.16(c) is between 0.26 to 0.35 eV. Fig. 3.17 shows the comparison of the parameters extracted from the bulk trap-state generation and the fixed-oxide-charge generation. The correlation between the increase of fixed-oxide-charge density and the threshold-voltage shift is shown in Fig. 3.18. The increase of fixed-oxide-charge density is closely related to the threshold-voltage shift, implying that the generation of fixed oxide charges also participates in the NBTI degradation in LTPS TFTs. Therefore, we can conclude that the bulk trap states alone cannot explain the measured threshold-voltage shift and the oxide trap states must be taken into account.

3.3.5 Physical Model of NBTI

Fig. 3.19 shows the correlation between the increases of the fixed-oxide-charge density

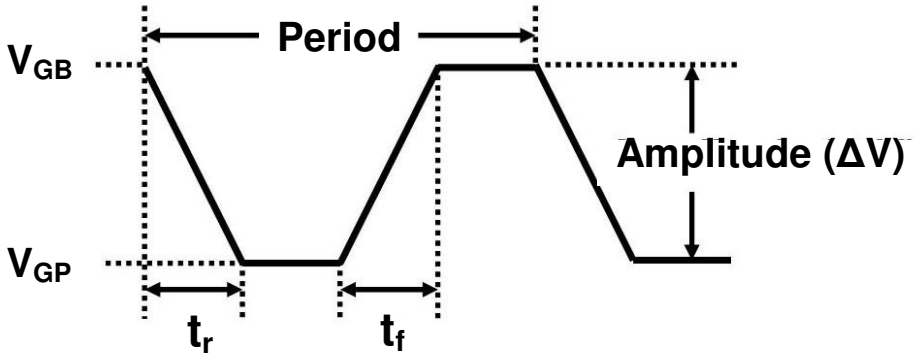
and the bulk trap-state density. Both the two parameters are close related and show a linear relation. The increases of the fixed-oxide-charge density and the bulk trap-state density are in the same order; therefore, we have demonstrated that the trap-state generation occurs both in the channel bulk region and in the gate dielectric for LTPS TFTs under NBTI stress.

As described in Chapter 2, we introduced a model to explain the NBTI-degradation mechanism for LTPS TFTs by expanding the model proposed for bulk-Si MOSFETs [3.30]. The model can be further explained from the energy band diagram as shown in Fig. 3.20. The Si dangling bonds in the bulk channel region are assumed to be initially passivated by hydrogen atoms. During NBTI stress, the hydrogen atoms react with the holes and dissociate from the Si atoms, resulting in the generation of bulk trap states. The released hydrogen species, including H^o and H^+, diffuse or drift into the gate oxide and react with it, forming OH groups bounded to oxide Si atoms. In the meantime, positive fixed oxide charges were generated in the gate oxide. Finally, the hydrogen species diffuse in the gate oxide, becoming a reaction-limiting factor.

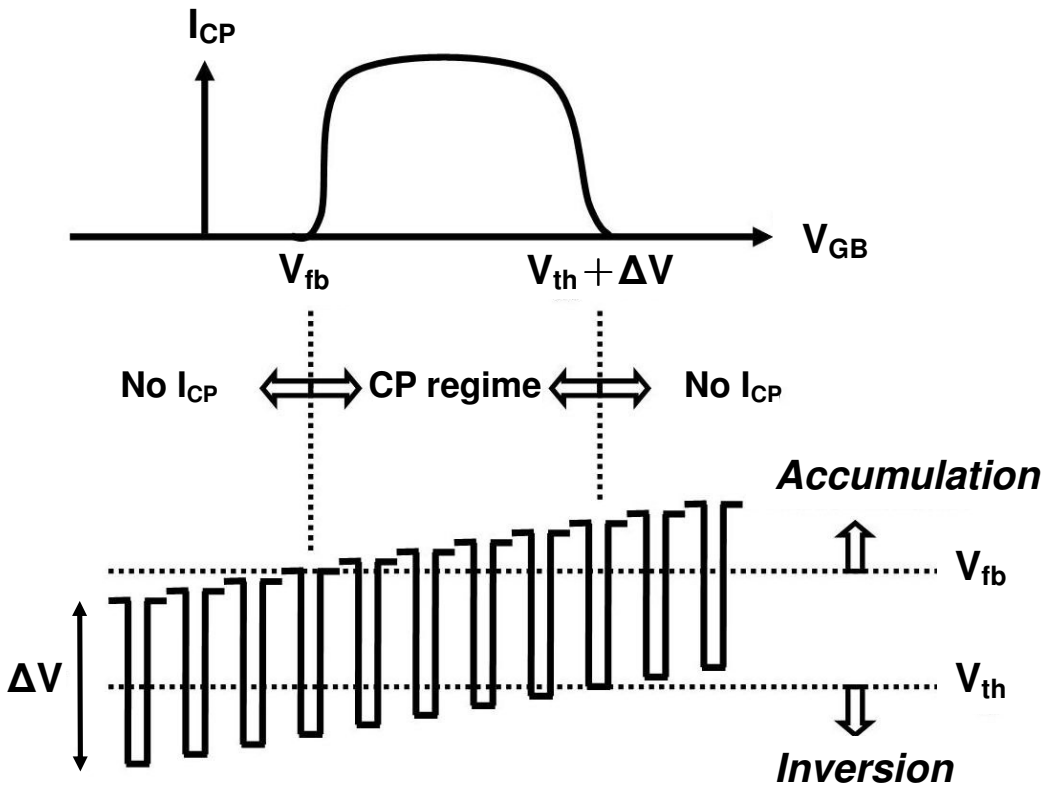
3.4 Summary

For the first time, the charge-pumping technique is utilized to analyze the NBTI-degradation mechanism in LTPS TFTs. The properties of bulk trap states can be directly characterized from the charge-pumping current. In addition, the increase of fixed-oxide-charge density is also extracted. Our results show that the increases of both bulk trap-state density and fixed oxide charges are closely related to the threshold-voltage shift, further confirming that the bulk trap states alone cannot explain the measured threshold-voltage shift, and the fixed oxide charges must be taken into account. In addition, the body-tied LTPS TFTs show a larger value of exponent factor compared to conventional LTPS TFT. This is because that the extra *p*-layer (inverted n^+ layer) provides extra holes to enhance the generation of proton and

leads to the larger value of the exponent factor. Furthermore, experimental results show that the NBTI degradation can be electrically and thermally activated. Therefore, the operation voltage and power consumption have to be well designed and new processes must be developed to suppress the NBTI degradation and to realize SOP.



(a)



(b)

Fig. 3.1 Schematic diagrams illustrating (a) the pulse waveform and (b) the charge-pumping-current curve of a *p*-channel transistor.

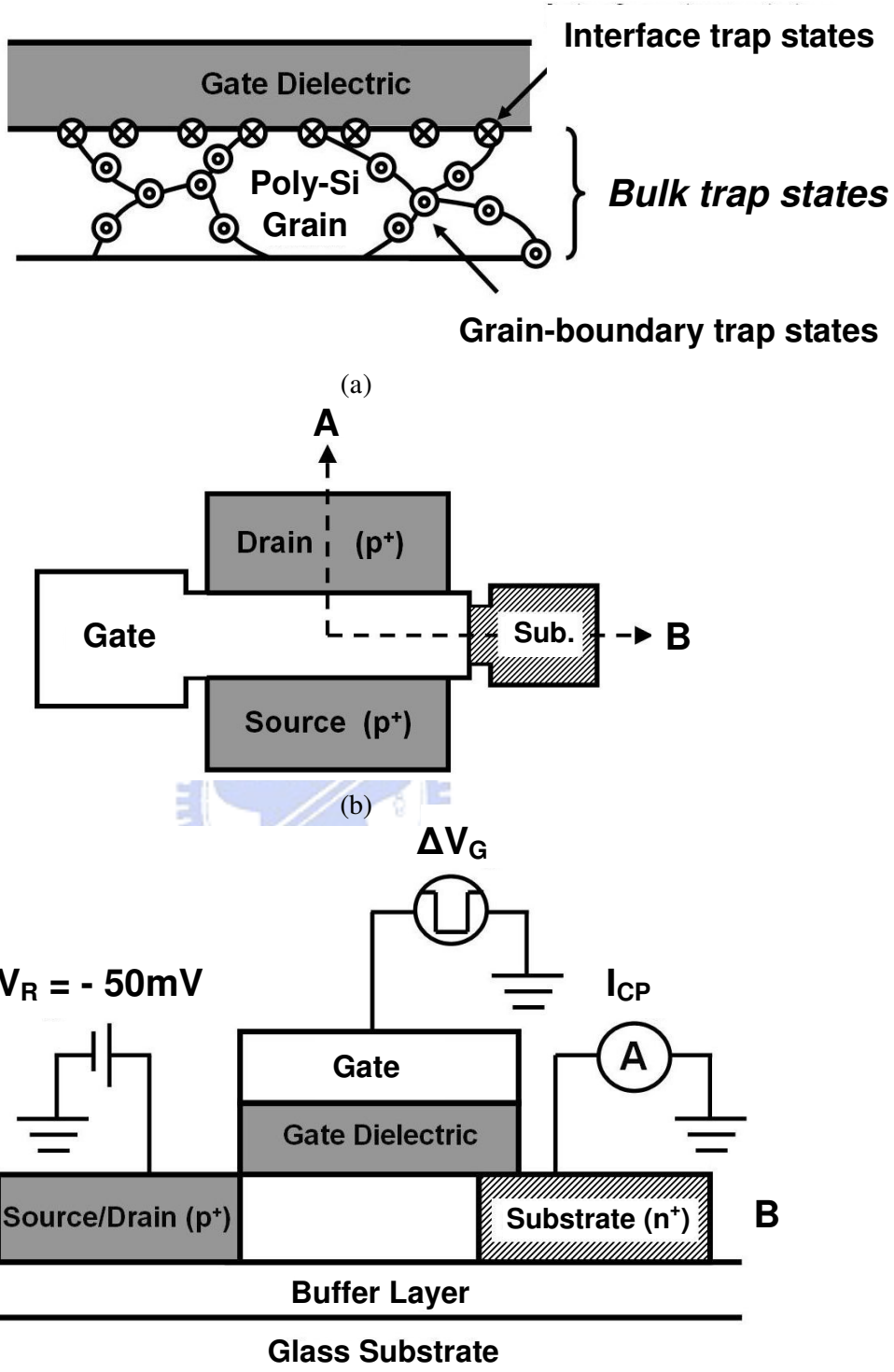
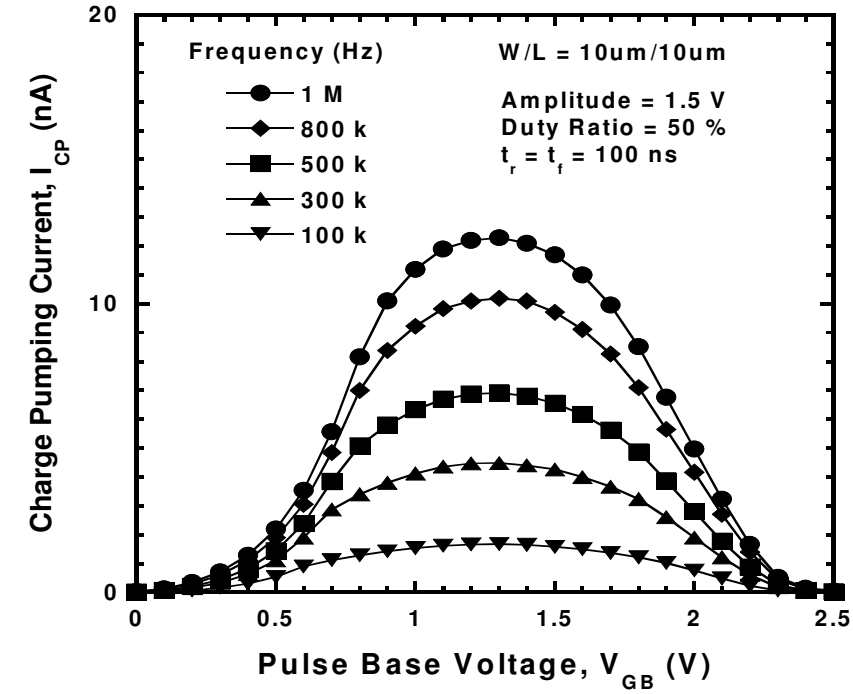
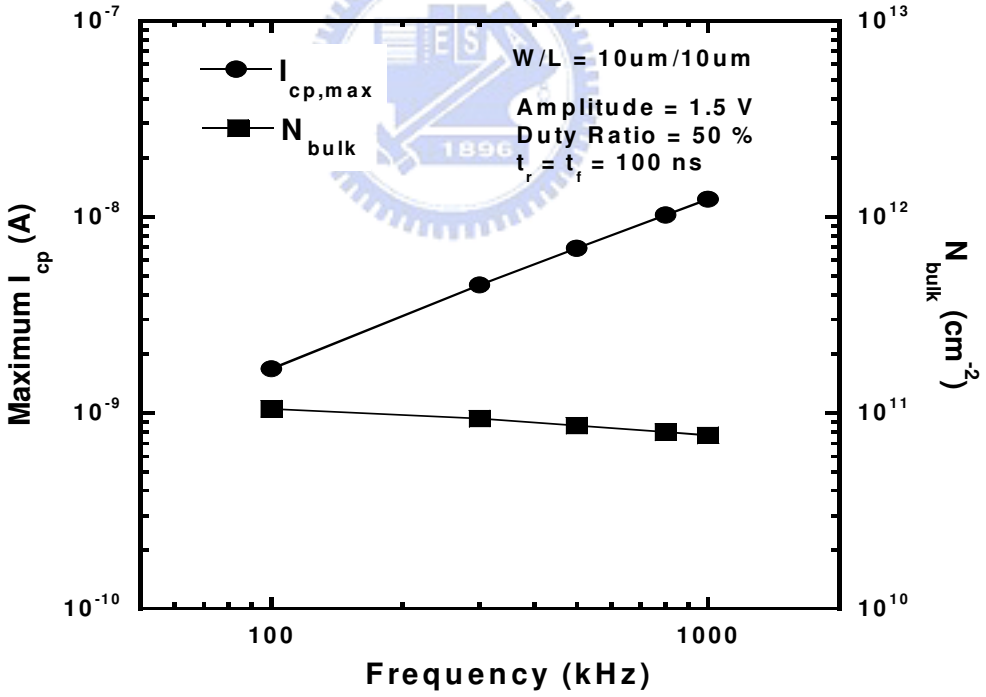


Fig. 3.2 (a) Schematic cross-sectional view of the critical poly-Si/SiO_2 interface showing interface trap states and grain-boundary trap states, and (b) cross-sectional and (c) top views of the LTPS TFT used in this study.

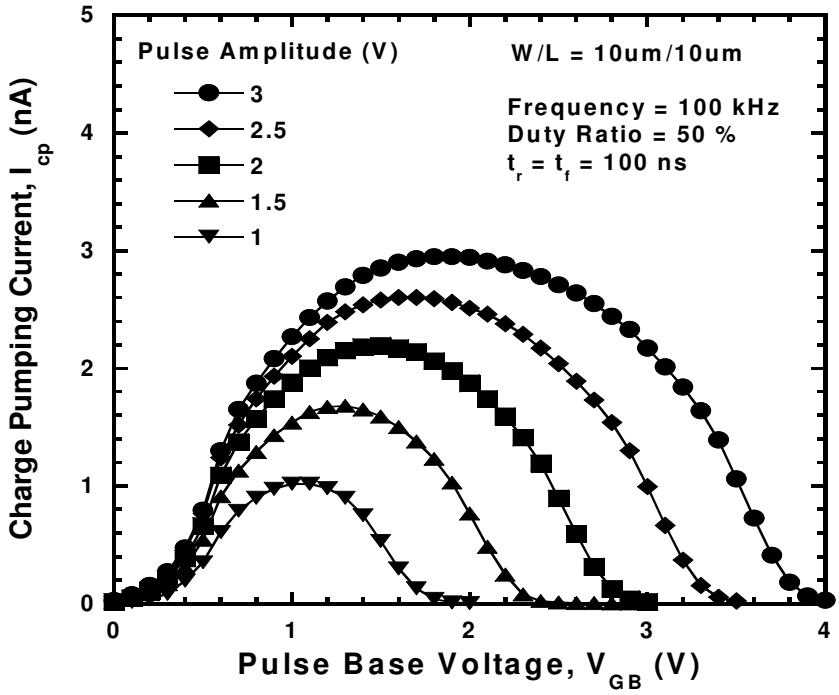


(a)

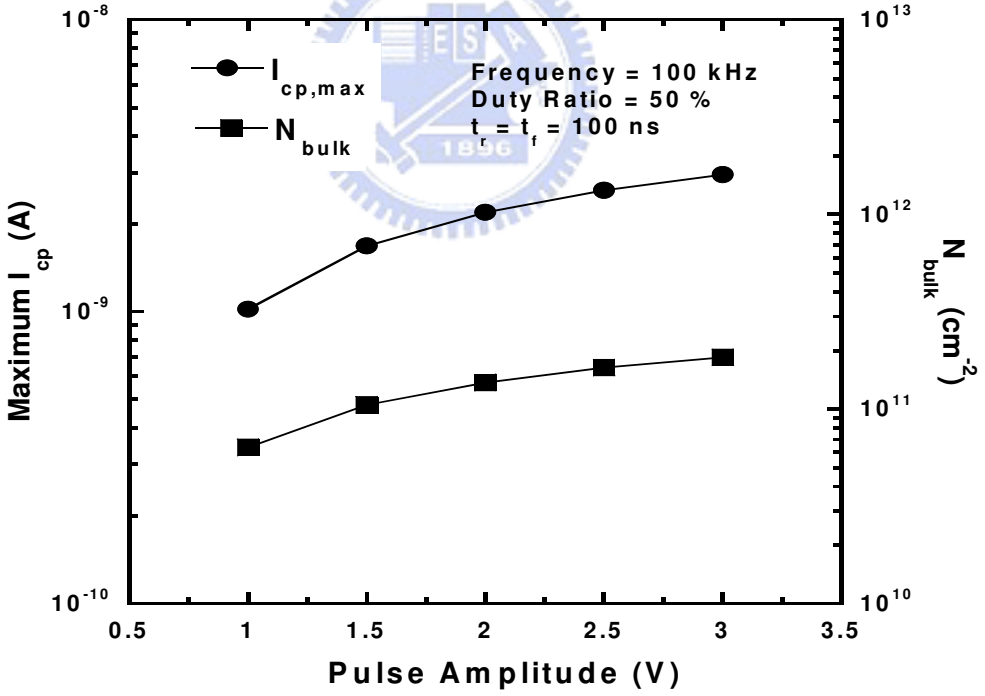


(b)

Fig. 3.3 (a) Charge-pumping current measured with different frequencies, and (b) dependence of the maximum charge-pumping current and the bulk trap-state density on the frequency.

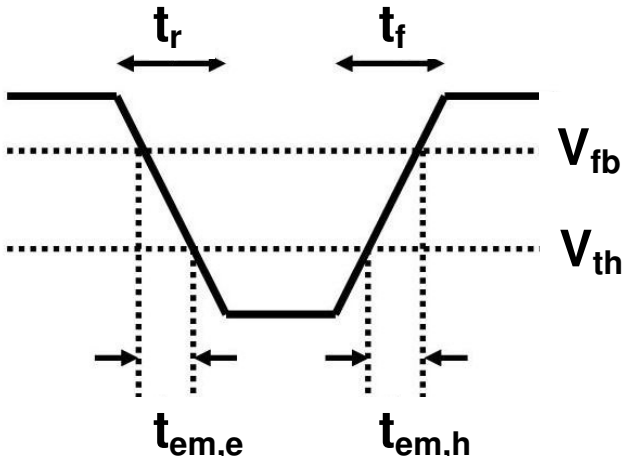


(a)

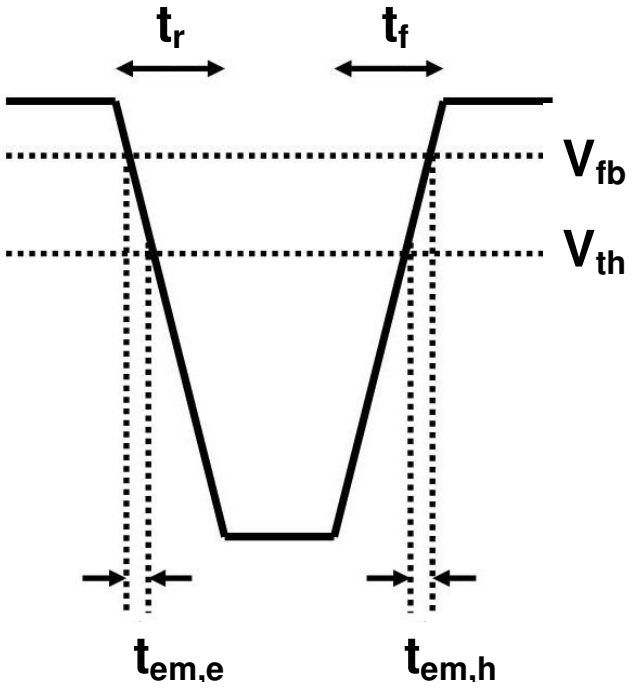


(b)

Fig. 3.4 (a) Charge-pumping current measured with different pulse amplitudes, and (b) dependence of the maximum charge-pumping current, and the bulk trap-state density on the pulse amplitude.



(a)



(b)

Fig. 3.5 Schematic diagrams of the pulse waveform with (a) a small and (b) a large pulse amplitude. The emission times of both electrons ($t_{em,e}$) and holes ($t_{em,h}$) decrease as the pulse amplitude increases.

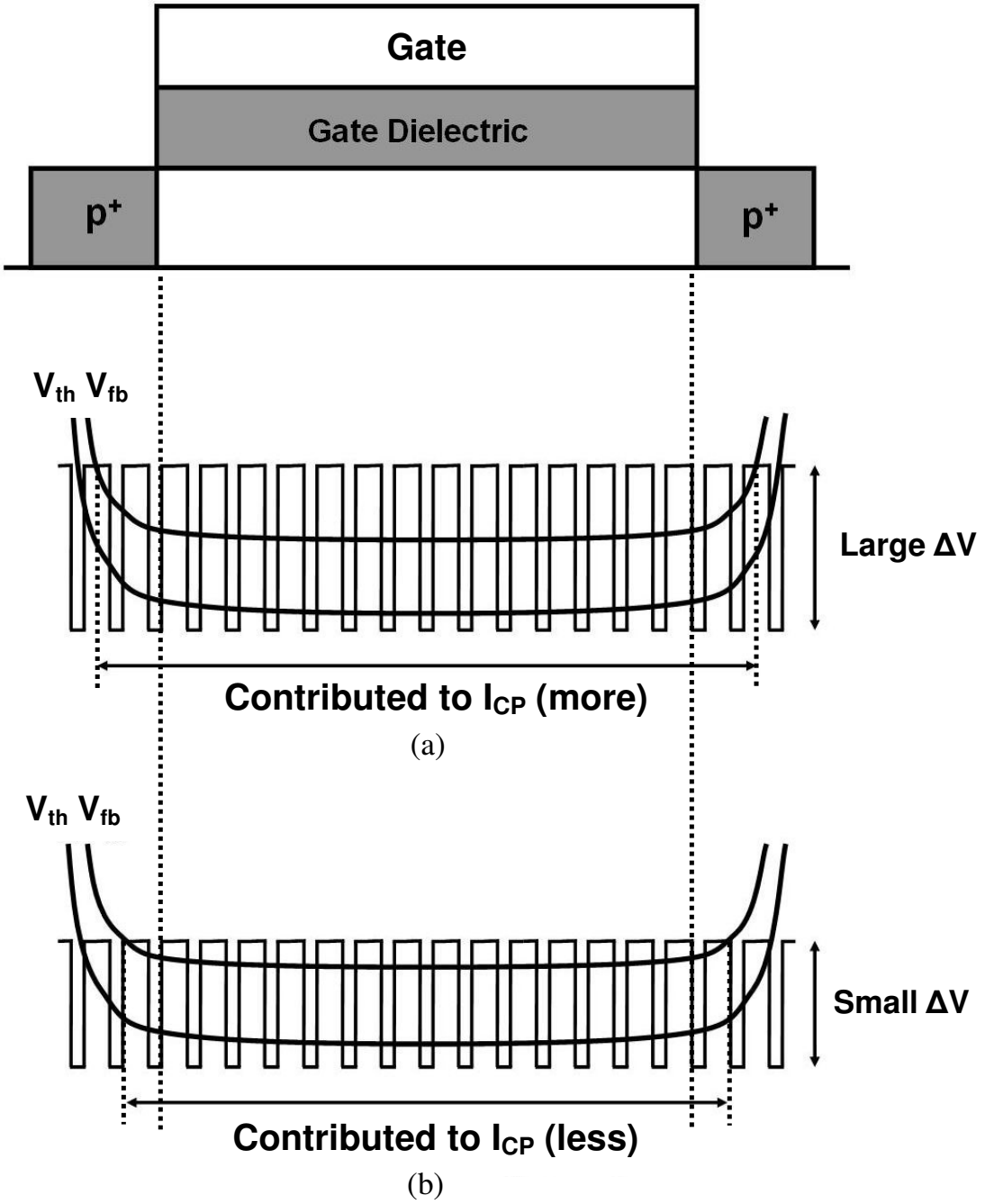
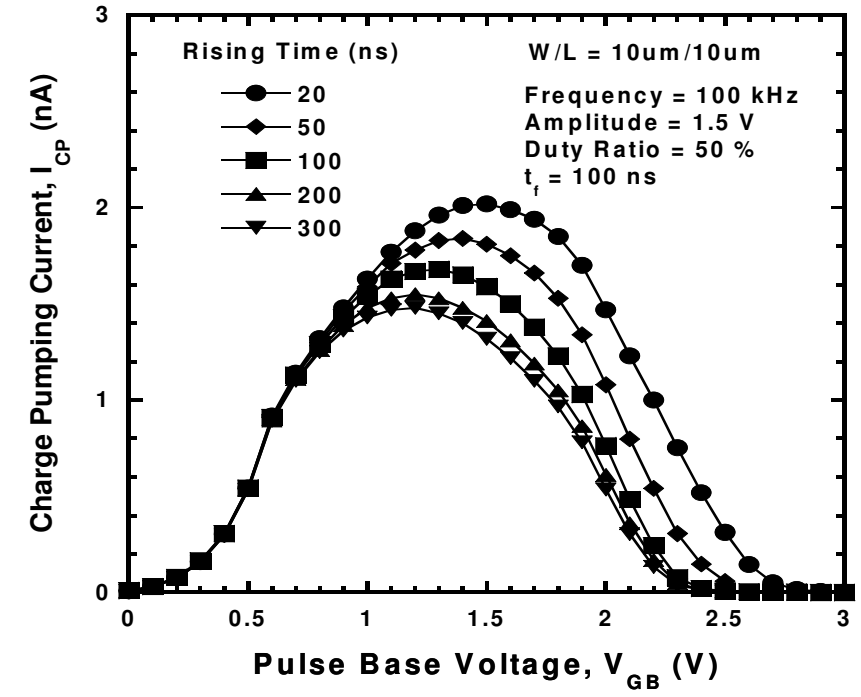
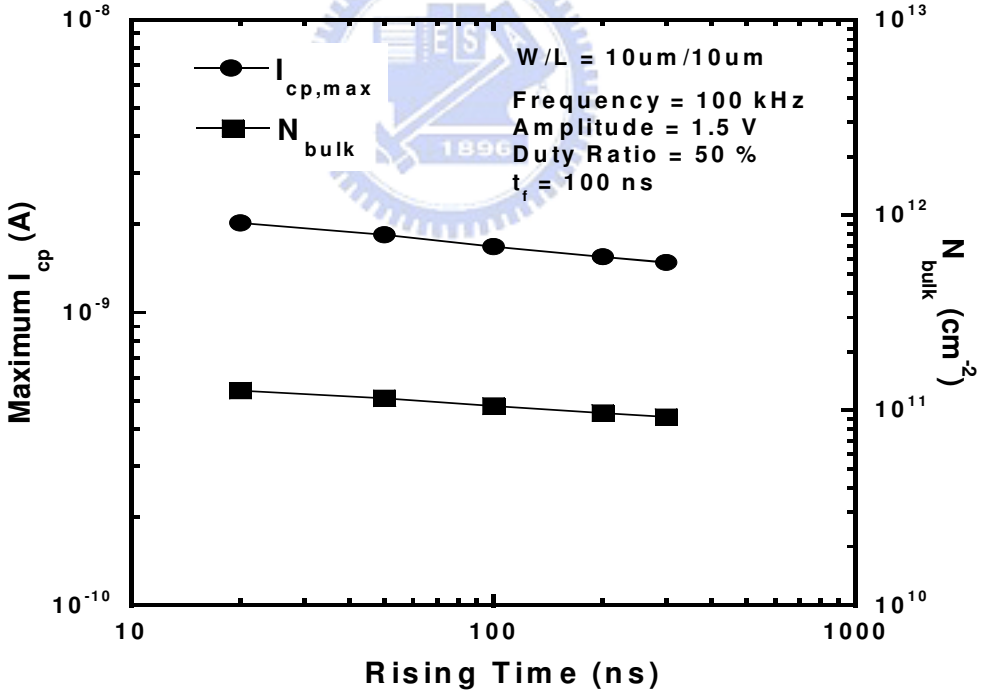


Fig. 3.6 Schematic diagram illustrating the effect of (a) a large and (b) a small pulse amplitude on the junction region that contributes to the charge-pumping current.

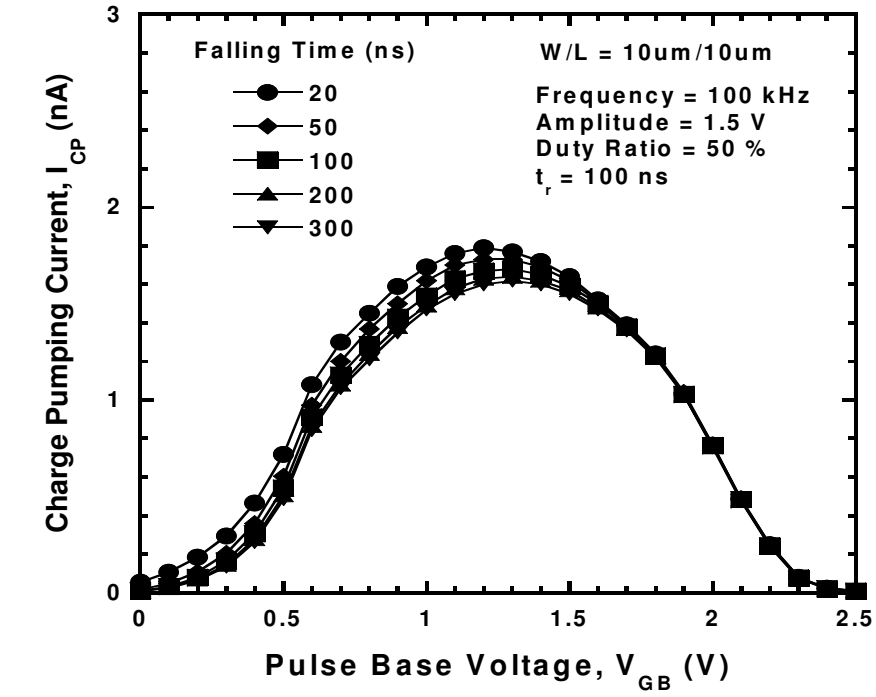


(a)

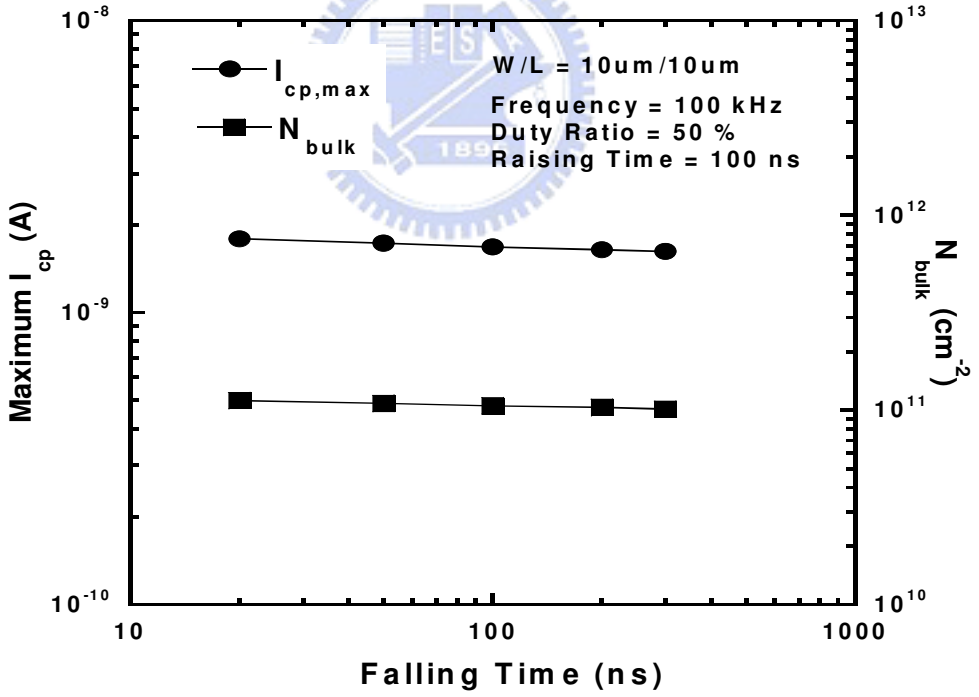


(b)

Fig. 3.7 (a) Charge-pumping current measured with different rising times, and (b) dependence of the maximum charge-pumping current and the bulk trap-state density on the rising time.

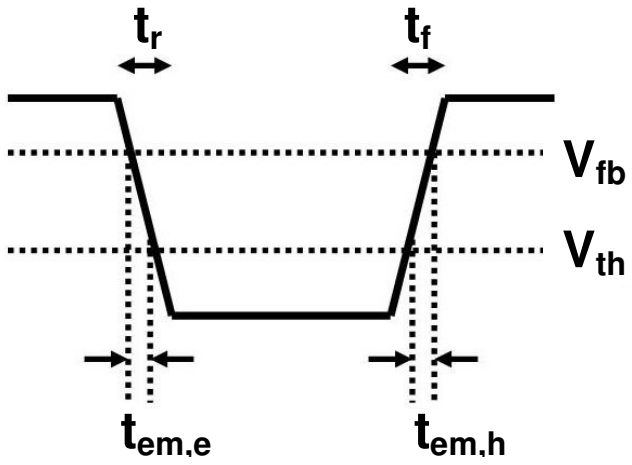


(a)

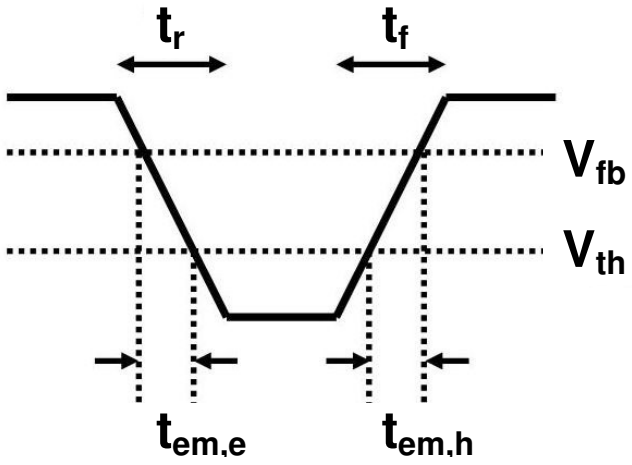


(b)

Fig. 3.8 (a) Charge-pumping current measured with different falling times, and (b) dependence of the maximum charge-pumping current and the bulk trap-state density on the falling time.

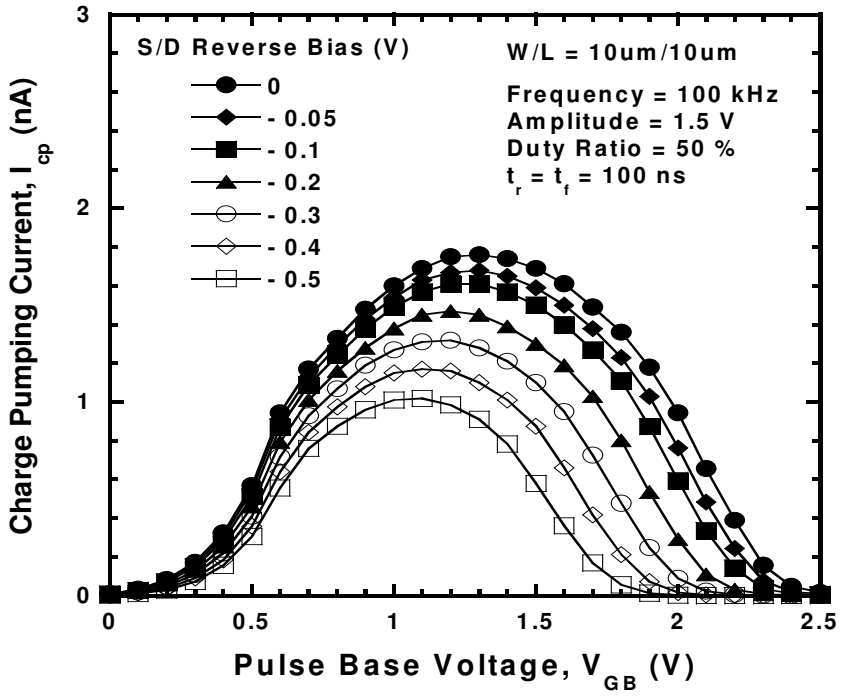


(a)

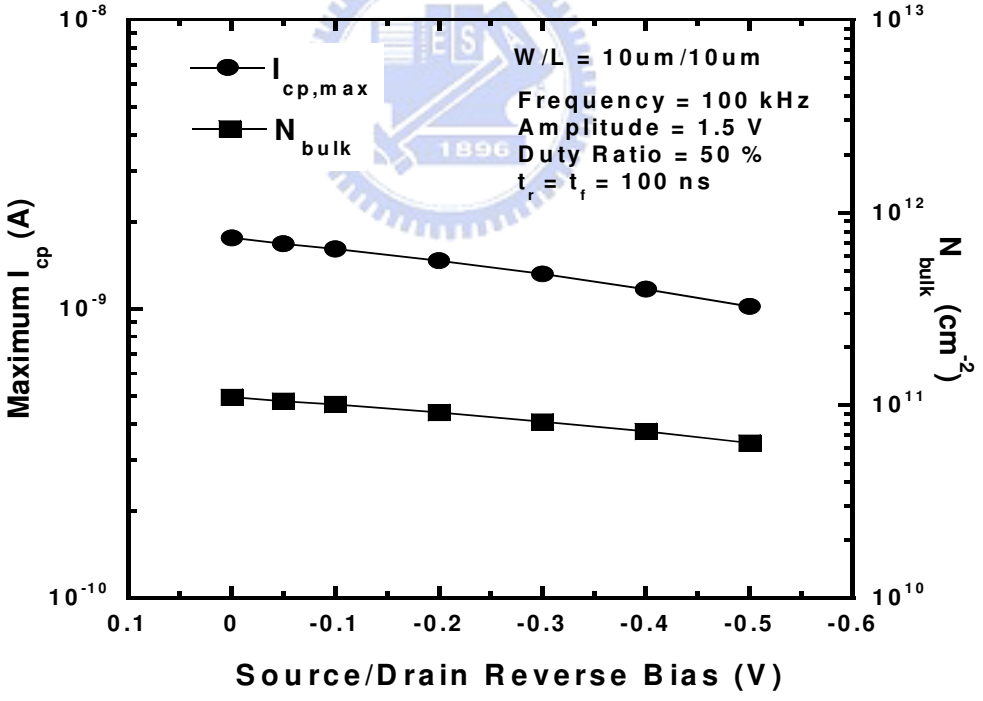


(b)

Fig. 3.9 Schematic diagrams of the pulse waveform with (a) a small and (b) a large rising/falling time. The emission times of electrons ($t_{em,e}$) and holes ($t_{em,h}$) increase with the rising time and falling time.

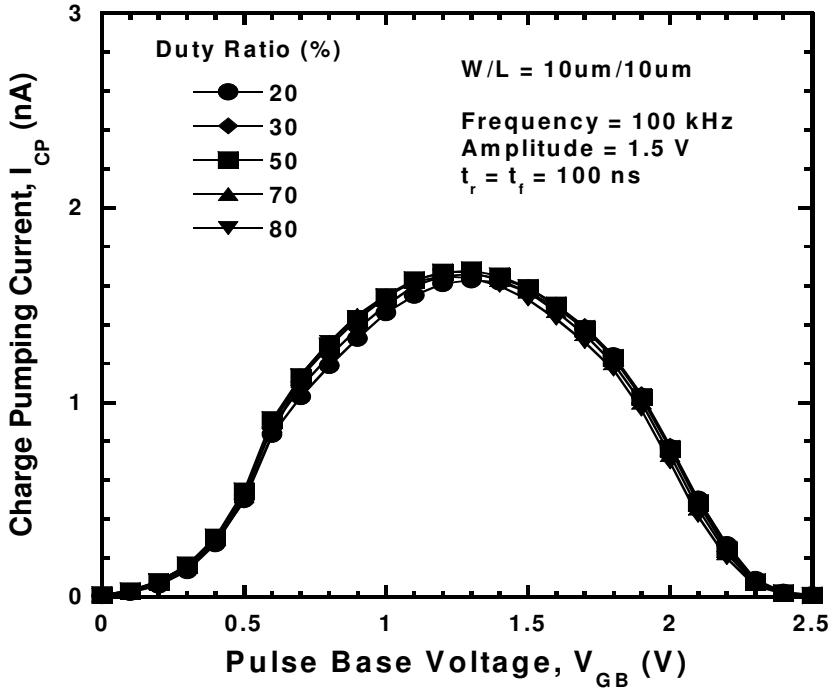


(a)

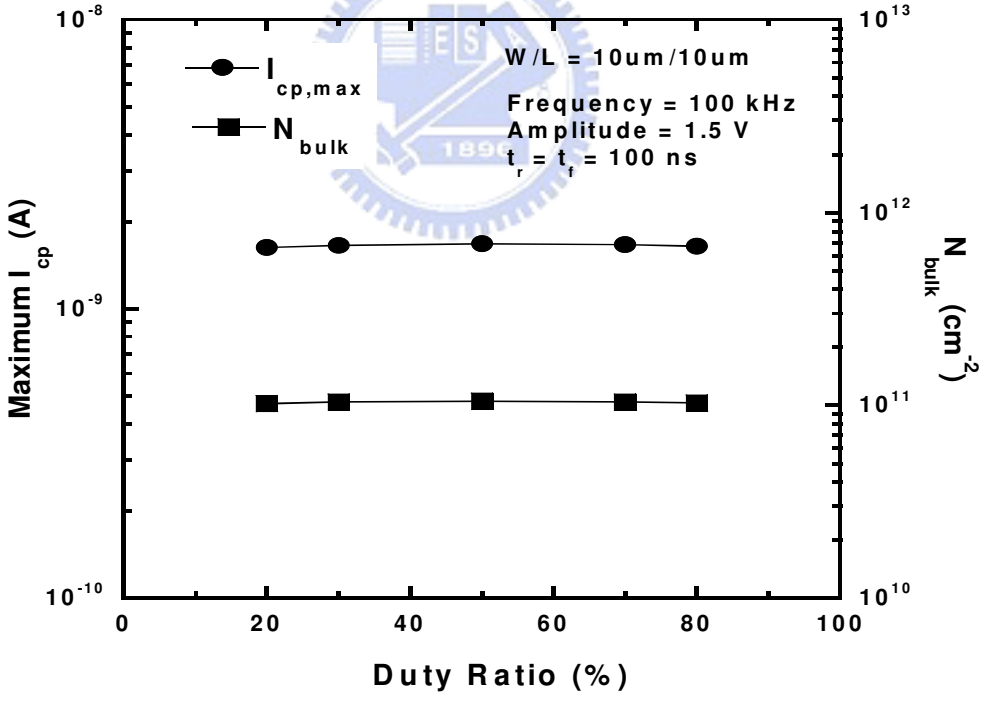


(b)

Fig. 3.10 (a) Charge-pumping current measured with different source/drain biases, and (b) dependence of the maximum charge-pumping current and the bulk trap-state density on the source/drain bias.

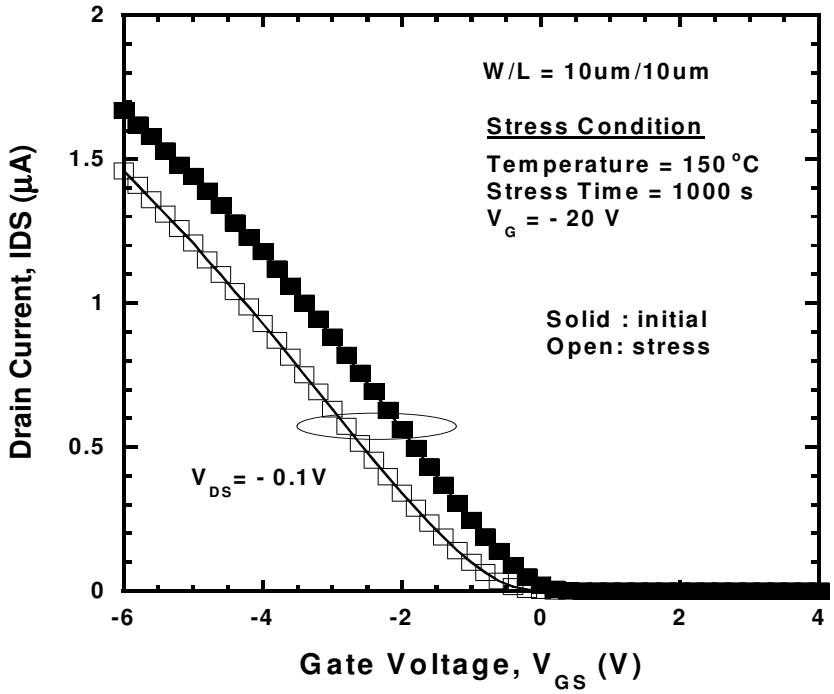


(a)

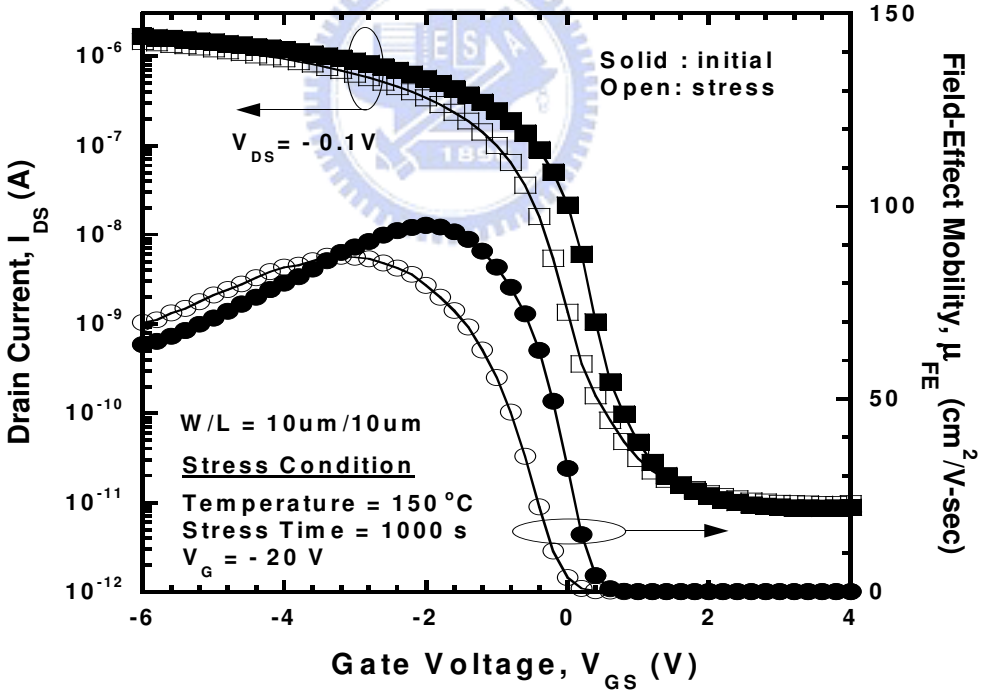


(b)

Fig. 3.11 (a) Charge-pumping current measured with different duty ratios, and (b) dependence of the maximum charge-pumping current and the bulk trap-state density on the duty ratio.



(a)



(b)

Fig. 3.12 Transfer characteristics in the (a) linear and (b) logarithmic scale of the LTPS TFT before and after 1000 s NBTI stress at 150 °C.

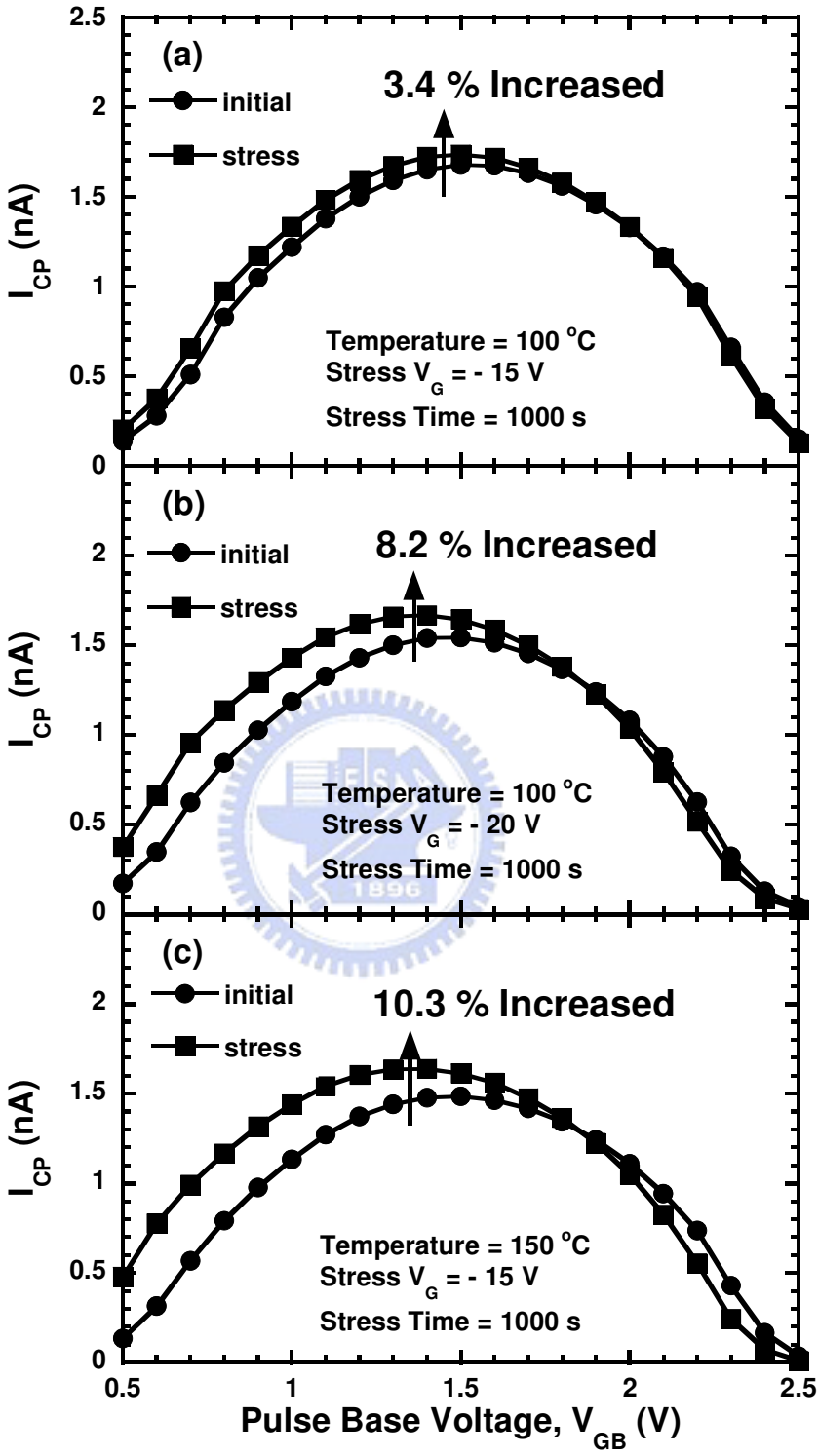


Fig. 3.13 Charge-pumping current before and after 1000 s NBTI stress under the stress conditions of (a) $V_G = -15$ V at 100 °C, (b) $V_G = -20$ V at 100 °C, and (c) $V_G = -15$ V at 150 °C.

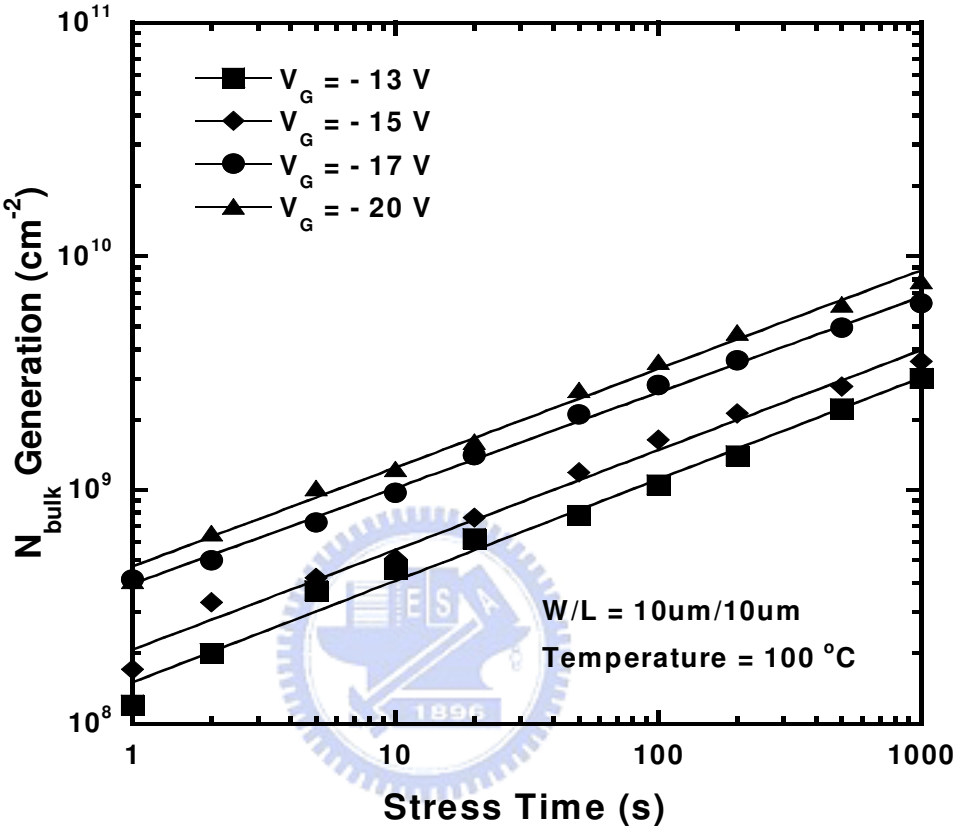


Fig. 3.14 (a) Time dependence of the bulk trap-state density generation under various stress voltages at 100 °C.

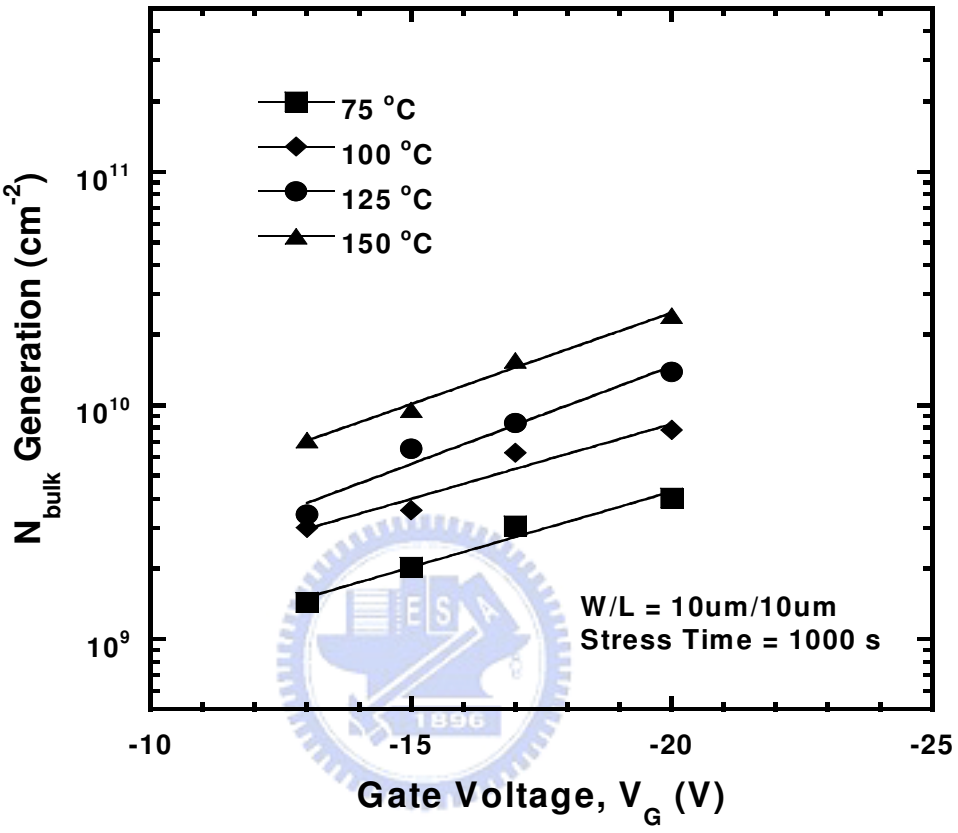


Fig. 3.14 (b) Dependence of the bulk trap-state density generation on the stress voltage of the LTPS TFTs under various stress conditions.

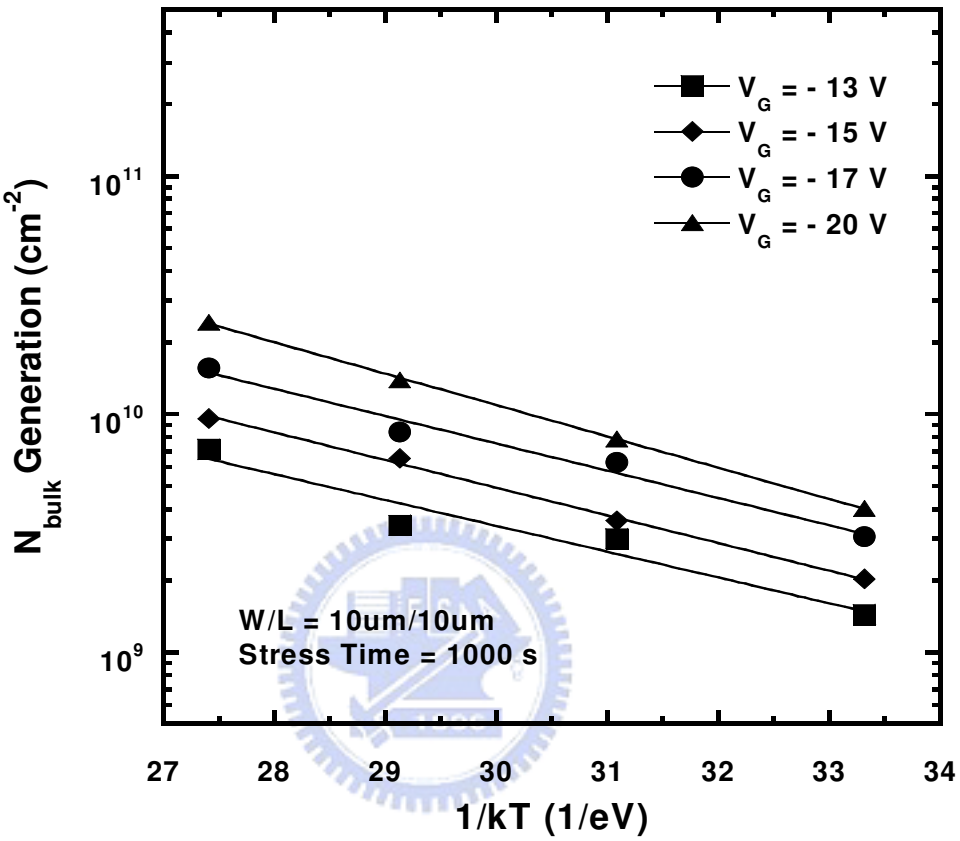


Fig. 3.14 (c) Dependence of the bulk trap-state density variation on the stress temperature of the LTPS TFTs under various stress conditions.

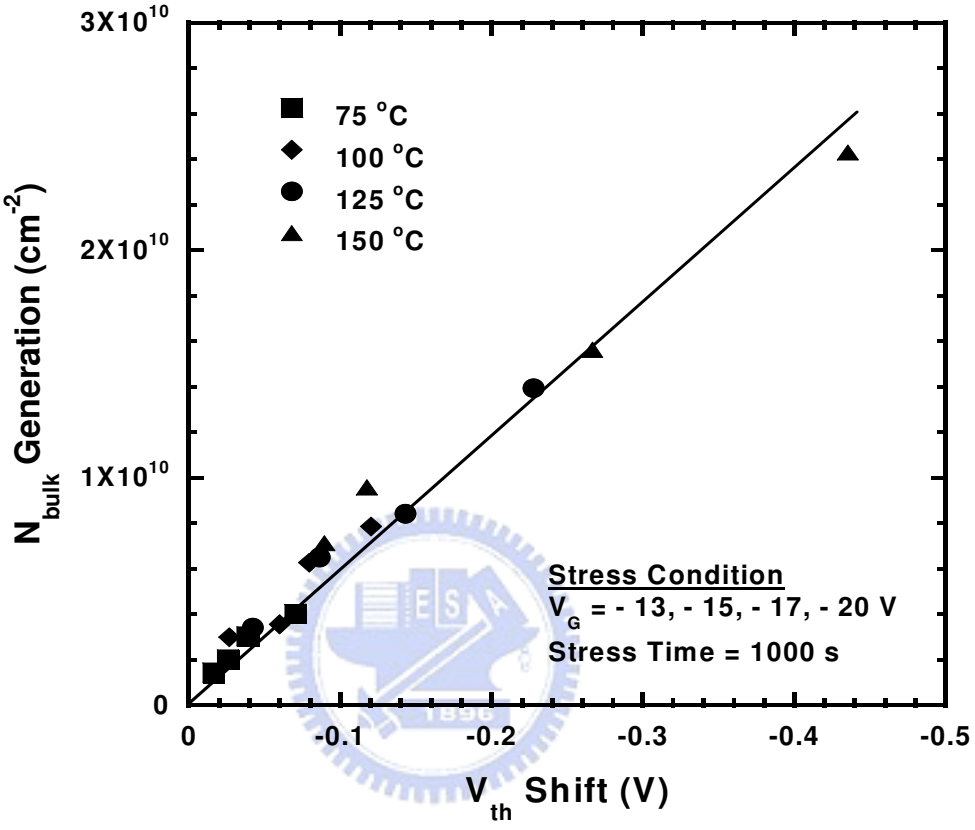


Fig. 3.15 Correlation between the increases of the bulk trap-state density and the threshold-voltage shift.

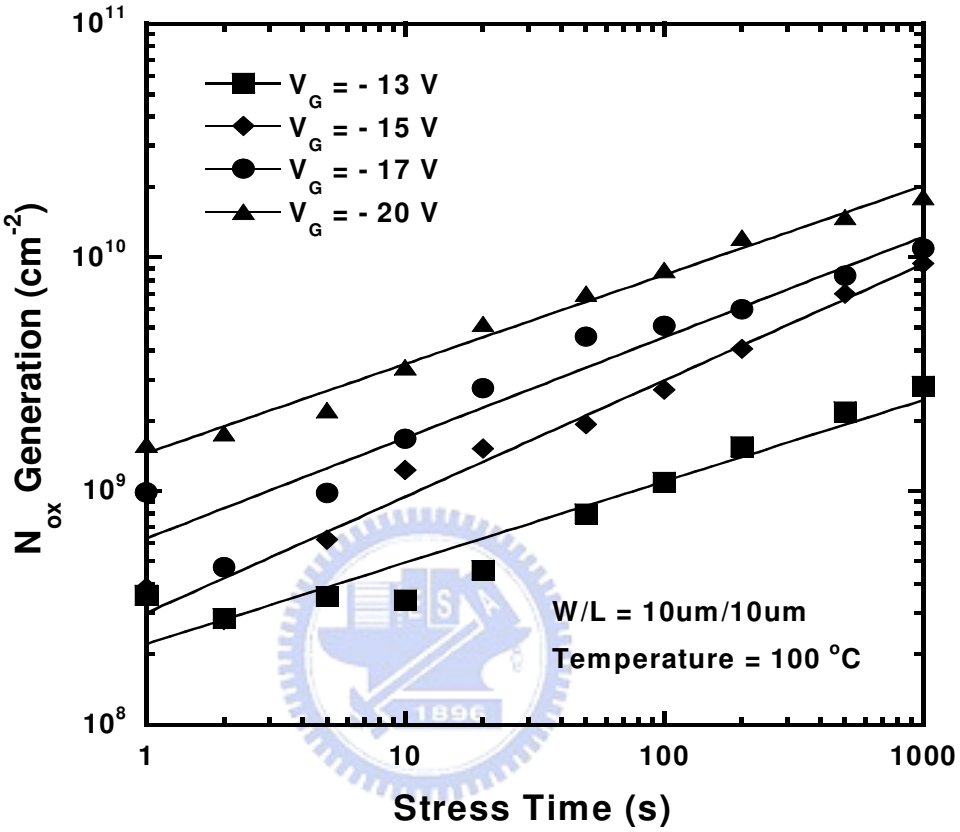


Fig. 3.16 (a) Time dependence of the variation of fixed-oxide-charge density under various stress voltages at 100 °C.

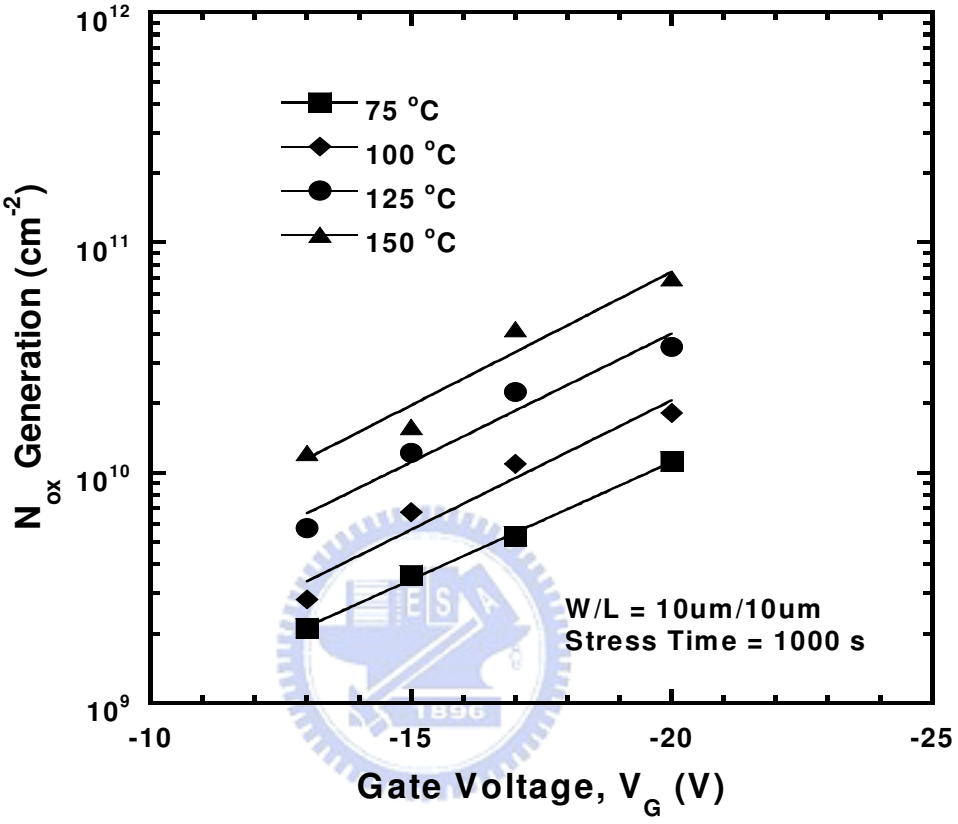


Fig. 3.16 (b) Dependence of the variation of fixed-oxide-charge density on the stress voltage of the LTPS TFTs under various stress conditions.

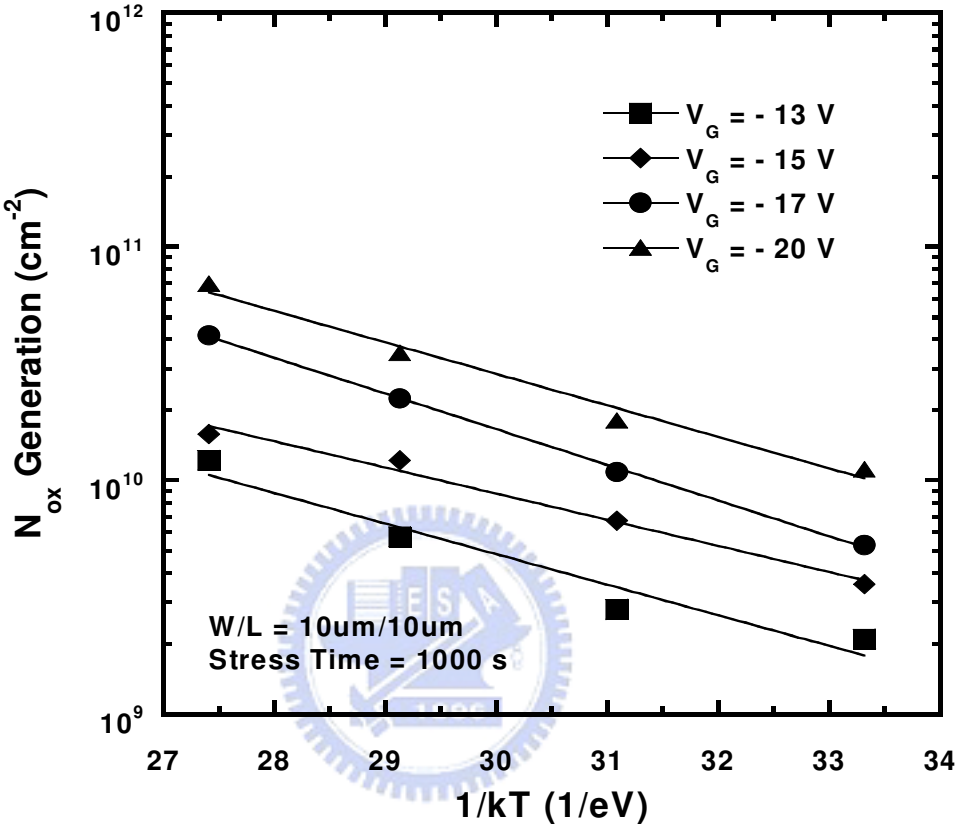


Fig. 3.16 (c) Dependence of the variation of fixed-oxide-charge density on the stress temperature of the LTPS TFTs under various stress conditions.

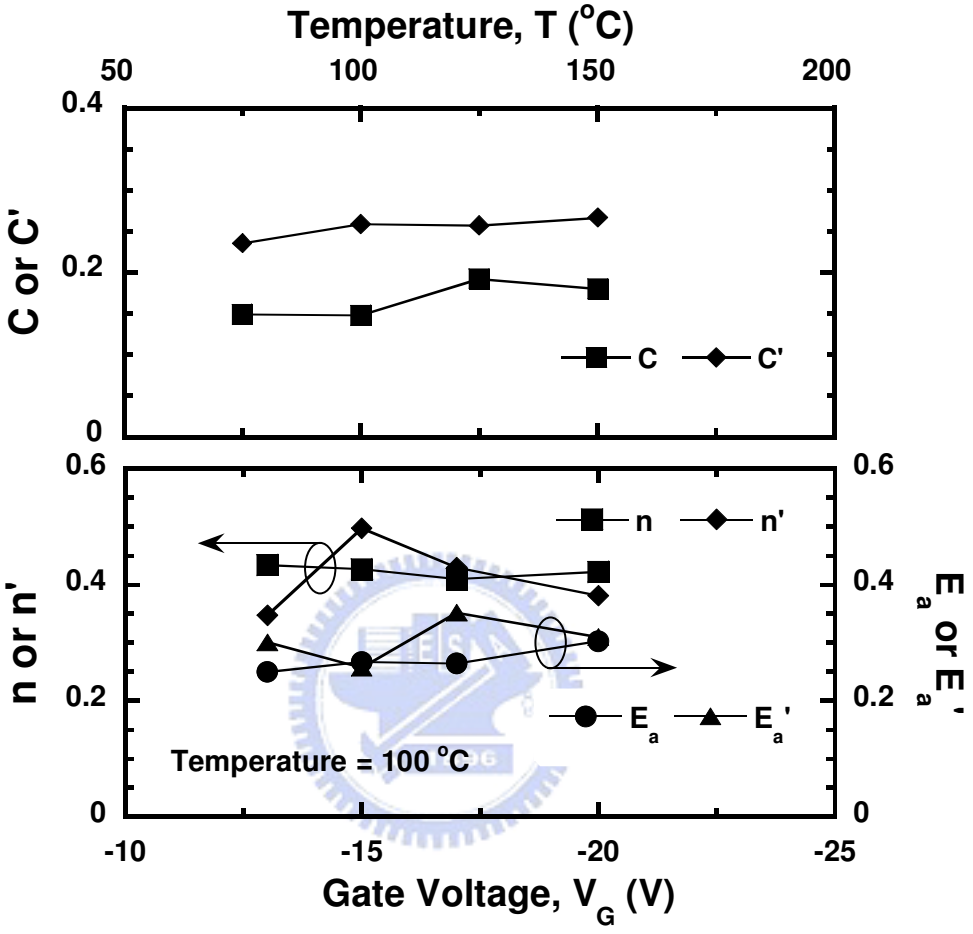


Fig. 3.17 Comparison of the parameters extracted from the bulk trap-state generation and the fixed-oxide-charge generation.

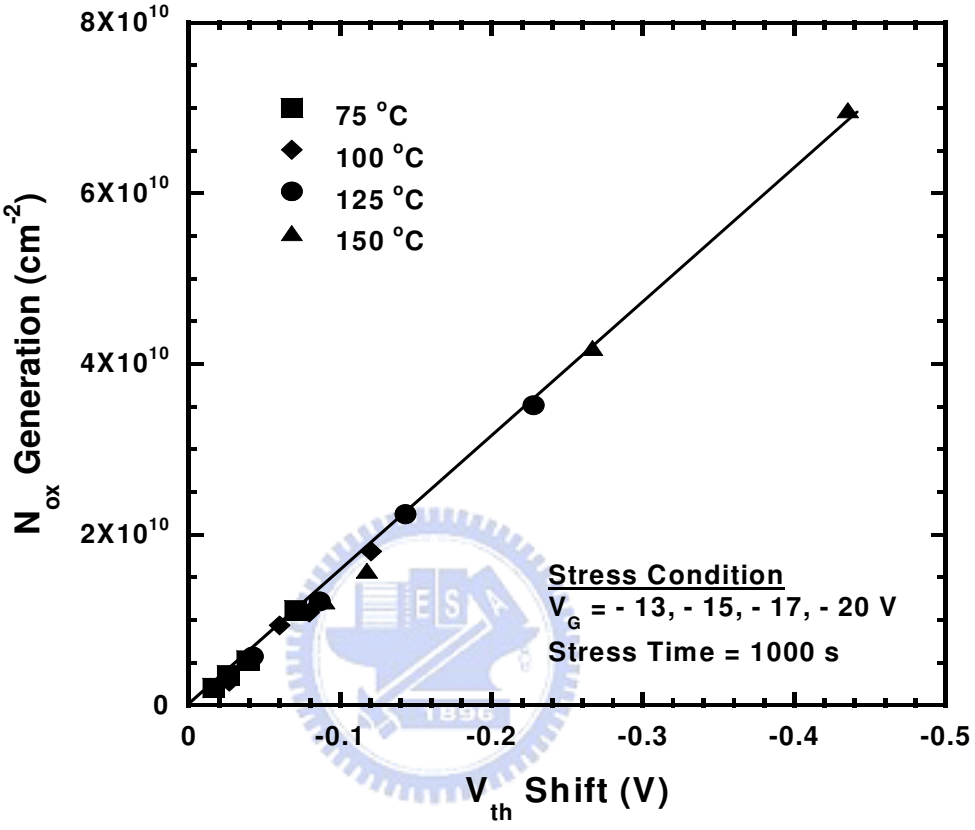


Fig. 3.18 Correlation between the increases of the fixed-oxide-charge density and the threshold-voltage shift.

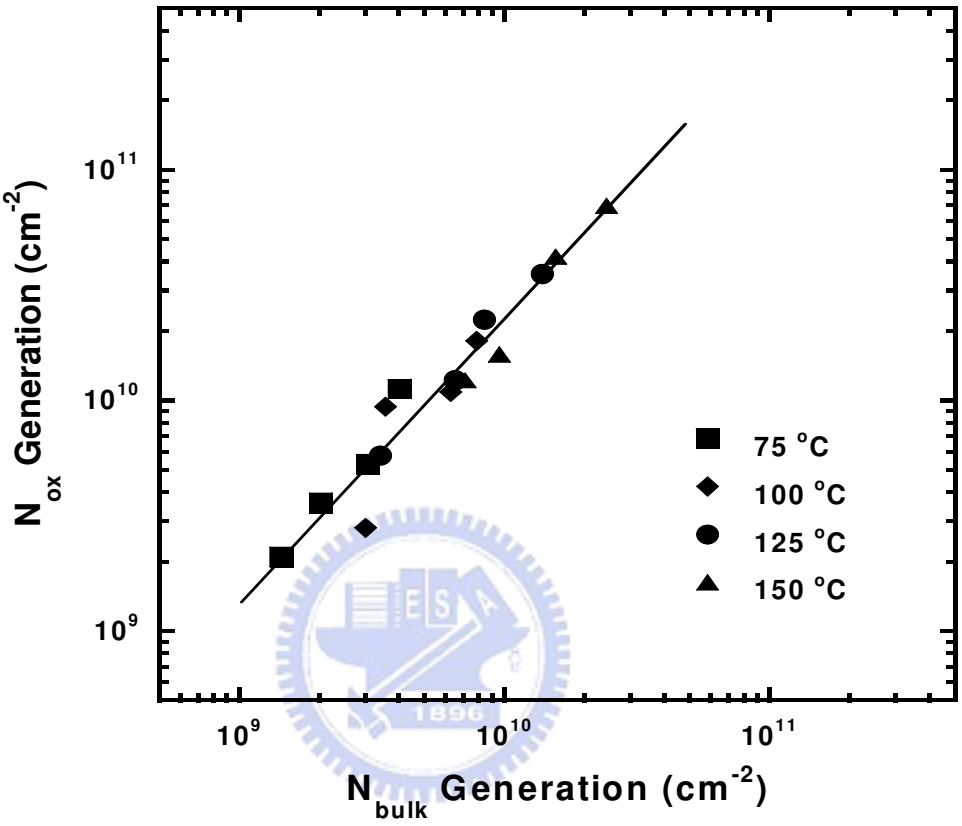


Fig. 3.19 Correlation between the increases of the fixed-oxide-charge density and the bulk trap-state density.

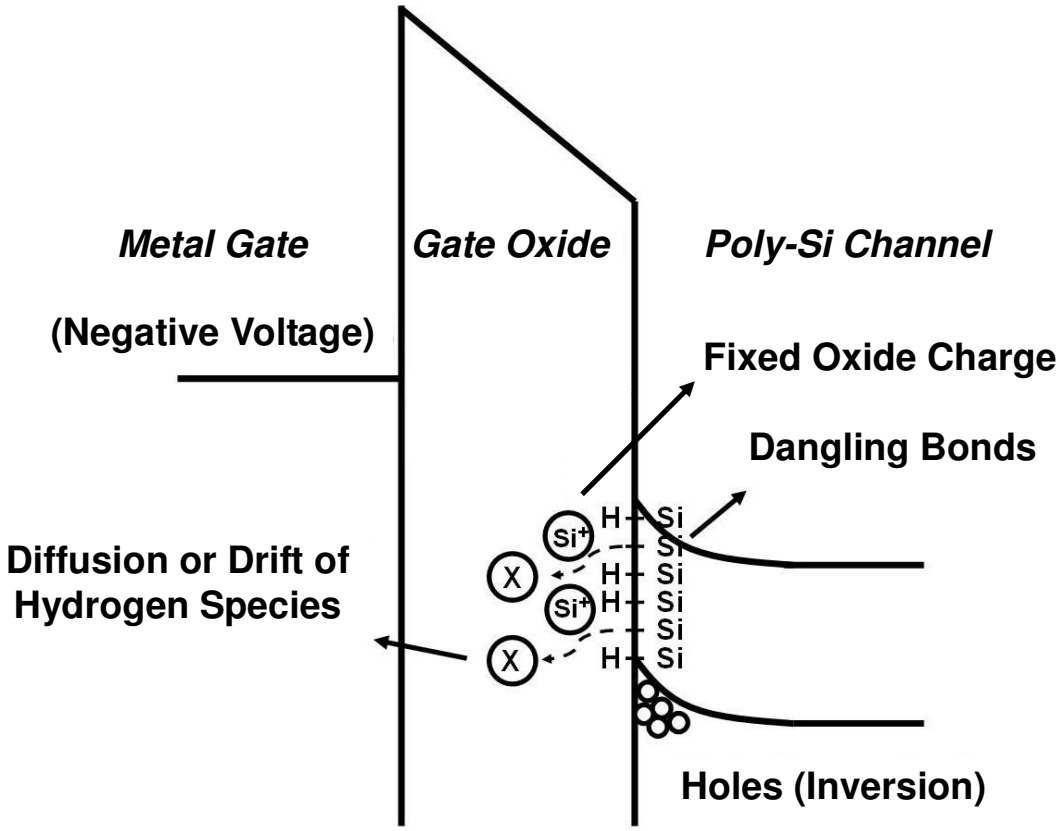


Fig. 3.20 Energy band diagram of the *p*-channel LTPS TFT under NBTI stress.

Chapter 4

Impacts of the Antenna Effect on Low-Temperature Polycrystalline Silicon Thin-Film Transistors

4.1 Introduction

In the fabrication of very-large-scale integration (VLSI) and poly-Si TFTs, plasma-etching processes are widely adopted to achieve good process repeatability and precise control over the feature sizes in the insulators, semiconductors, and metals. However, the impact of plasma processing on device reliability has been a cause for concern since many reports have highlighted that plasma processing during the VLSI manufacturing, including aluminum etching, poly-silicon etching, and resist ashing, may induce reliability issues such as the degradation of threshold voltage, transconductance, gate leakage current, and oxide reliability [4.1]－[4.4].

When an isolated object comes into contact with plasma, negative charges accumulate very rapidly on the object because electrons are the lightest and hottest particles. This situation leads to the buildup of negative potential, called the *floating potential* (V_f), with respect to the plasma potential (V_p). The floating potential continues to increase until the net flux of arriving negative charges on the isolated object is equal to the net flux of the positive charges [4.5]. However, plasma non-uniformity leads to a local imbalance between the flux of the positive and negative charges, causing a charge accumulation by the isolated object [4.6]. If a conducting layer is connected to the gate oxide and then subjected to plasma etching, the layer completely covers the wafer during most of the etching process; charges flow through the layer to balance the local non-uniformity of the charge flux such that no

charge accumulates on the layer. When the conducting layer is nearly completely etched, however, the layer eventually becomes discontinuous, leading to the onset of local charge accumulation and damage to the gate oxide [4.7]. In addition, during the over-etching step of the photoresist stripping process, the entire wafer surface is exposed to the plasma, causing charge accumulation on the conducting layer. The charges collected by the conducting layer cause stress to the gate oxide. When the plasma non-uniformity is sufficiently large, and the electric field across the gate oxide exceeds a critical value, electrons inject through the gate oxide via FN tunneling, causing deterioration of the oxide quality and integrity [4.8]. The injection process could occur through either substrate injection or gate injection, depending upon the potential distribution at the wafer surface during the plasma process [4.9].

The degree of plasma damage is strongly related to the topography of the gate interconnection. It is reported that plasma damage occurs when the gate electrode is longer [4.10], or when the gate electrode is connected to a longer metal line [4.11]. In addition, the charging effect is amplified by the ratio of the areas of the conducting layer and the gate, the so-called *antenna-area ratio* (AR). This phenomenon is referred as the *antenna effect*. For LTPS TFTs, because they have a high potential to be used in the driving circuit, the antenna structure will be very common in circuit layout, and the antenna effect will be an important reliability issue. However, it has only rarely been investigated in LTPS TFTs. Some studies have indicated that the plasma processing may degrade the performance of poly-Si TFTs through such phenomena as crystal damage, exposure damage, radiation damage, and charging damage [4.12], [4.13]; however, the impacts of the antenna effect on the performance and reliability of LTPS TFTs have not been explored to an appropriate degree.

In this chapter, we investigated the impacts of the antenna effect on the LTPS TFTs having various antenna structures. Moreover, to investigate the influence of an antenna effect on the reliability of the LTPS TFTs, we applied both gate-bias stress and hot-carrier stress to the samples.

4.2 Experiments

LTPS TFTs having a lightly-doped drain (LDD) were fabricated on the glass substrates having top-gate structures. The process flow of the *n*-channel LTPS TFT is shown in Figs. 4.1(a)—4.1(g). A 400-Å amorphous-Si layer was deposited by plasma-enhanced chemical-vapor deposition (PECVD) at 300 ^{o}C on a buffer layer, and then crystallized into a poly-Si film by excimer laser annealing. After source and drain formation through plasma doping, the gate dielectric was deposited having 1000-Å SiO_2 by PECVD at 300 ^{o}C**.** Mo was deposited having a thickness of 3000 Å and patterned as the gate electrode. After gate formation, an LDD having a length of 1.5 μm was formed by a self-aligned process. Then, 5000-Å SiO_2 was deposited as the inter-layer dielectric and densified through rapid thermal annealing (RTA) at 700 ^{o}C for 30 s. The dopants were also activated during the densification process. Finally, after contact-hole opening, 5000-Å Al was deposited and patterned as the interconnection metal.

The antenna geometry of the test structure is presented in Fig. 4.2, and the antenna-area ratio (AR) is defined as:

$$AR = \frac{Antenna\ Area}{Gate\ Area\ on\ Active\ Region\ (L \times W)}. \qquad (Eq.\ 4.1)$$

To study the effects of the antenna structures on the characteristics of the LTPS TFTs, two sets of antenna patterns were designed; their parameters are detailed in Tables 4.1 and 4.2. The first series of devices were designed having a fixed channel width (W) and a channel length (L) of 20 μm and 10 μm, respectively; their values of AR were varied from 36 to 1000. The second series of devices were designed having a fixed AR of 1000, and the channel widths were varied from 5 to 30 μm at a fixed channel length of 5 μm.

4.3 Results and Discussion

4.3.1 Fixed Device Size/Various ARs

There are many device parameters that can be used to check plasma-induced damage, such as the threshold voltage, drive current and gate-leakage current [4.1], [4.2]. In our experiments, we found that the threshold-voltage distribution of the LTPS TFTs displays a clear dependence on the AR, as shown in Fig. 4.3. The threshold-voltage distribution degrades as the AR increases to 1000. When the devices are exposed to plasma, local charges accumulate on the conducting layer and create a voltage across the gate dielectric. Such stress causes charge injection through the gate oxide, and creates numerous trap states in it [4.13], [4.14]. Therefore, as a result of the enhanced degree of plasma damage, the LTPS TFTs, having larger values of AR, exhibit a greater instability in their threshold voltages than those having smaller values of AR.

Fig. 4.4(a) displays the transfer characteristics of the LTPS TFTs before and after gate-bias stress for 1000 s. The gate-bias stress was performed by applying a voltage of 30 V to the gate, while the source and drain were grounded. Obviously, the threshold voltage shifts to the positive direction after the gate-bias stress, while the subthreshold swing changes only slightly. It has been reported that the subthreshold-swing degradation is closely related to the generation of interface trap states located near the mid-gap region (deep interface trap states); on the other hand, the threshold-voltage shift is closely related to both a deep interface trap-state generation and a charge injection into the gate oxide [4.15]. Because the subthreshold swing remains almost unchanged in our experiment after the gate-bias stress, the generation of deep interface trap states can be ruled out. As a result, we conclude that the threshold-voltage shift is due mainly to a charge injection into the gate dielectric. Fig. 4.4(b) displays the time dependence of the threshold-voltage shift of the LTPS TFTs having various values of AR under gate-bias stress. Although the rates of threshold-voltage shift for the three devices are almost identical, the LTPS TFT having the largest AR exhibits the largest threshold-voltage shift, indicating that more charges are trapped in the gate dielectric.

Because we applied a stress voltage of 30 V to the gate, there are probabilities that holes could be injected into the gate dielectric from the metal gate and that holes could be generated in the gate dielectric. However, holes have a much higher tunneling barrier and a larger effective mass than do electrons. Therefore, the tunneling effects of holes are small and can be ruled out. Furthermore, due to the thick gate dielectric, the oxide field (ca. 3MV/cm) was not sufficiently high enough to make the electrons tunnel into the gate oxide and generate electron-hole pairs in it. Therefore, the generation of holes in the gate oxide can be ruled out. The experimental results show that the threshold voltage moves in the positive direction after stress; this further confirms that the degradation mechanism was not dominated by hole injection or generation in the gate oxide.

It has been reported that plasma-induced damage creates numerous trap states in the gate dielectric and that the number of these trap states depends on the degree of damage [4.16]. The LTPS TFTs, having larger values of AR, experienced a greater degree of plasma damage; therefore, more trap states were generated in the gate dielectric. When a gate bias of 30 V is applied to stress the device, the oxide field (ca. 3MV/cm) is not sufficiently high to damage the gate dielectric; this situation, however, is true for the oxide that has not been subjected to plasma damage. The plasma processes induce many trap states in the gate dielectric. Those trap states enhance the probabilities of both electron injection and trapping in the gate dielectric through trap-assisted tunneling, which results in a threshold-voltage shift during gate-bias stress [4.17]. Therefore, because of the greater number of trap states in the gate dielectric, we suggest that during the gate-bias stress for the device having a large value of AR, more electrons were trapped in the gate dielectric through trap-assisted tunneling, resulting in a large threshold-voltage shift.

In this study, hot-carrier stress (V_{GS} = 10 V; V_{DS} = 20 V) was also applied to identify the impacts of the antenna effect. Fig. 4.5(a) displays the transfer characteristics of the LTPS TFTs having AR values of 36 and 100, both before and after hot-carrier stress. Fig. 4.5(b)

presents the time dependence of the drive-current degradation, defined as $-\Delta I_{DS}/I_{DS} \times 100\%$, of the LTPS TFTs having various values of AR under hot-carrier stress. Although the threshold voltage and subthreshold swing remains almost unchanged after stress, the drive current decreases accordingly. When a hot-carrier stress is applied to the device, a high field is induced near the drain junction, causing impact ionization and leading to the generation of electron-hole pairs. The generated hot carriers create trap states near the drain junction and reduce the field-effect mobility - by increasing the potential barrier for the carriers to migrate from the source to the drain [4.18], [4.19]. Moreover, because the drive current and the field-effect mobility degrade similarly in our experiments, the drive-current degradation can be attributed to the degradation of the field-effect mobility. We found that the LTPS TFTs having larger values of AR exhibit a greater degree of drive-current degradation; therefore, we conclude that plasma damage affected the immunity of the LTPS TFTs against hot-carrier stress.

4.3.2 Fixed AR/Various Device Sizes

Figs. 4.6—4.9 show the results of the same series of experiments performed using a second series of devices. The devices were designed to have a fixed AR of 1000, having a varied channel width from 5 to 30 μm at a fixed channel length of 5 μm. Fig. 4.6 presents the threshold-voltage distribution of these devices. The antenna area was proportional to the gate area on the active region ($L \times W$) to maintain the values of AR constant at 1000. As the channel width increases, the antenna area increases. The larger antenna area may induce a greater degree of plasma damage on the gate dielectric. Therefore, those TFTs having a 30-μm-wide channel exhibit a poorer threshold-voltage distribution than those having a smaller channel width since different antenna areas were exposed to the plasma.

Fig. 4.7 reveals the time dependence of the threshold-voltage shift of the LTPS TFTs under gate-bias stress. The LTPS TFTs having a larger channel width exhibits a larger

threshold-voltage shift. Because a larger antenna area enhances the plasma damage and creates more trap states in the gate dielectric, electrons are more likely to be injected into the gate dielectric through trap-assisted tunneling, leading to a larger threshold-voltage shift. Therefore, the device having a larger channel width displays a greater threshold-voltage shift under gate-bias stress.

Fig. 4.8 shows the threshold-voltage shift of the LTPS TFTs under hot-carrier stress. The LTPS TFT having the smallest channel width exhibits the smallest threshold-voltage shift. The threshold-voltage shifts of the devices having channel widths of 20 and 30 μm exhibit two degradation regimes. In the first regime, the threshold-voltage shifts move increasingly more toward negative values upon increasing the stress time; in the second regime, however, the threshold-voltage shifts move more toward positive values after a certain time. To explain these phenomena, the output characteristics of the pre-stress devices were monitored and shown in Fig. 4.9. We found that the drain current increases upon increasing the drain voltage in the saturation region; this phenomenon is referred to as the so-called *kink effect* [4.20], [4.21]. The small circles (O) in this figure mark the hot-carrier stress conditions that we used in this study. The kink effect increases upon increasing the channel width under hot-carrier stress conditions (V_{GS} = 10 V; V_{DS} = 20 V).

For the devices having channel widths of 20 and 30 μm, we believe that the kink effect is responsible for the negative shift of the threshold voltages. During hot-carrier stress, the impact-ionization-generated holes accumulate in the channel region. These holes may be initially trapped or compensate the trapped electrons that are pre-existing at the Si/SiO_2 interface and grain boundaries. Besides, at a fixed AR of 1000, the plasma damage is enhanced for the device having a larger channel width, which may also create larger amounts of both hole traps and pre-existing trapped electrons. Therefore, a device having a larger channel width exhibits a larger threshold-voltage reduction in the first stress regime. As impact ionization continues, both hole trapping and the compensation of pre-trapped charge

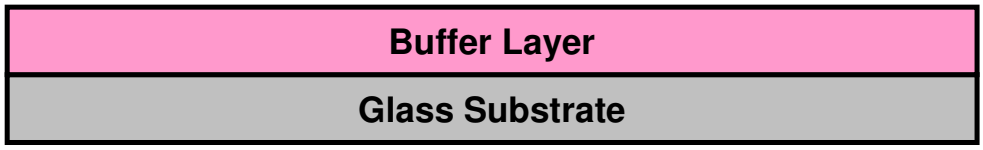
effect will soon reach saturation [4.22]. Therefore, hot-electron injection becomes the degrading factor in the second stress regime, leading to positive shifts of the threshold voltages.

The kink effect shown in Fig. 4.9 could be explained from the mechanism proposed by Pretet *et al* [4.23]. They have reported that those defects which had arisen from mechanical stress shorten the lifetime of carriers along the channel edges and therefore suppress the kink effect for narrow-width devices. The effect can be neglected for the devices having larger channel widths. As a result, in comparing the devices having a larger channel width with those having a narrow width, the amount of the impact-ionization-generated holes is relatively reduced for the narrow-width devices under the hot-carrier stress condition. Because of the suppressed impact ionization during hot-carrier stress, the 5-μm device has a much smaller current density than the others. Therefore, the device having a 5-μm-wide channel has a better immunity against hot-carrier degradation.

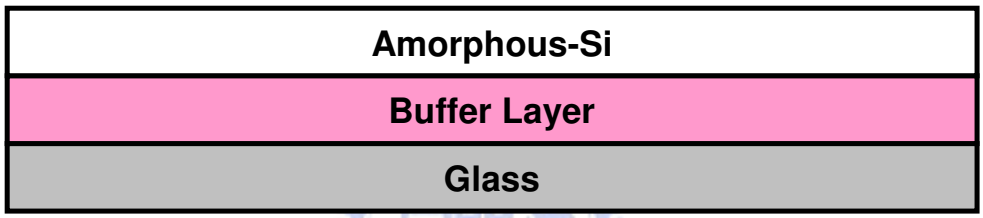
Figs. 4.10(a) and 4.10(b) show the transfer characteristics of the LTPS TFTs having channel widths of 5 and 30 μm, respectively, under hot-carrier stress. The channel length was fixed at 5 μm and the AR was fixed at 1000. For the device having a channel width of 5 μm, the threshold voltage and subthreshold swing change insignificantly after hot-carrier stress for 10^4 s, as shown in Fig. 4.10(a). For the device having a channel width of 30 μm, however, the device characteristics degrade with an increased stress time. The instability of threshold voltage has been explained in the former section. In addition, we found that the subthreshold swing degrades with an increased stress time; this phenomenon can be explained by the enhanced impact ionization that generates more interface trap states during hot-carrier stress. Therefore, we conclude that devices having larger channel widths at a fixed AR are more susceptible to hot-carrier degradation than those having smaller channel widths.

4.4 Summary

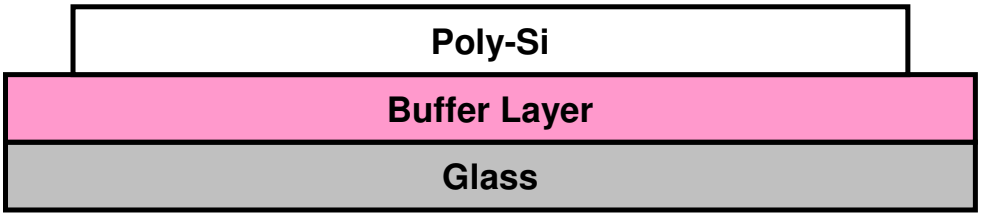
In this chapter, we investigated the impacts of the antenna effect on the performance and reliability of LTPS TFTs. Devices having larger values of AR exhibit a greater instability in their threshold voltage relative to devices having smaller values of AR. This phenomenon is due to the enhanced plasma damage for large-value AR devices during the fabrication process. The enhanced damage generates more trap states in the gate dielectric and degrades the reliability of these devices. For devices having a fixed value of AR at 1000 and various channel widths, we found that the device reliability degrades as the channel width increases. The antenna effect is demonstrated to affect both the performance and reliability of LTPS TFTs.



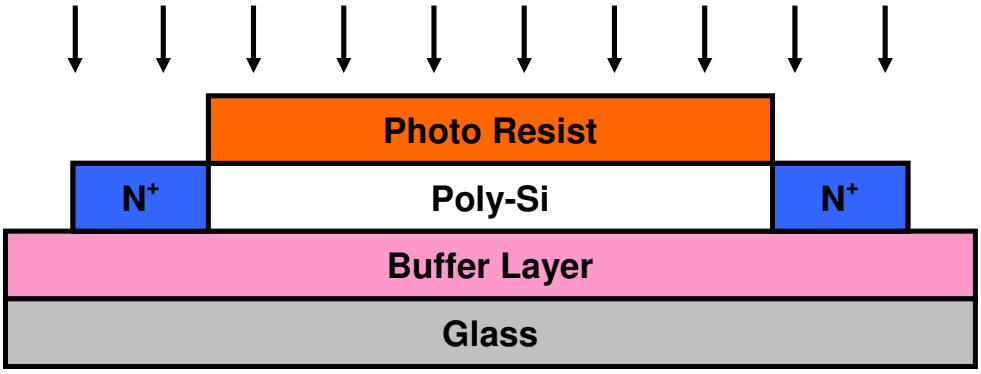
(a) Buffer layer deposition on the glass substrate.



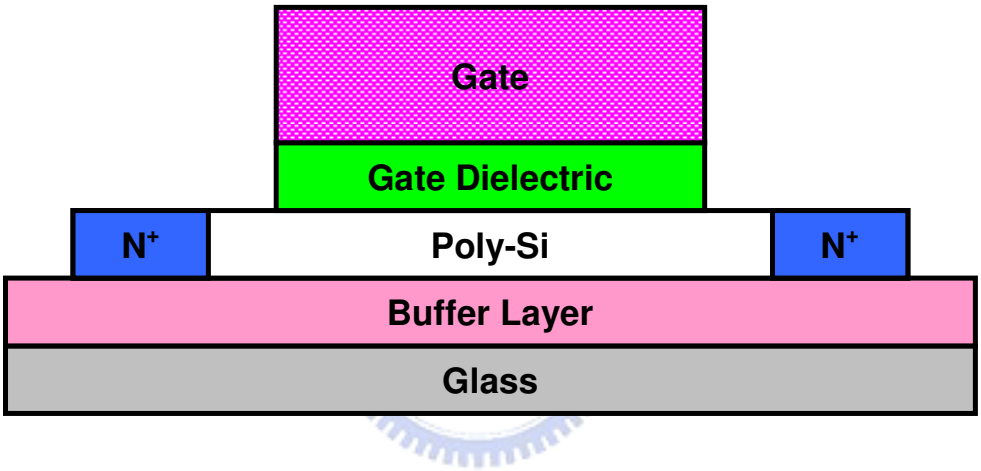
(b) Amorphous-Si layer deposition by PECVD.



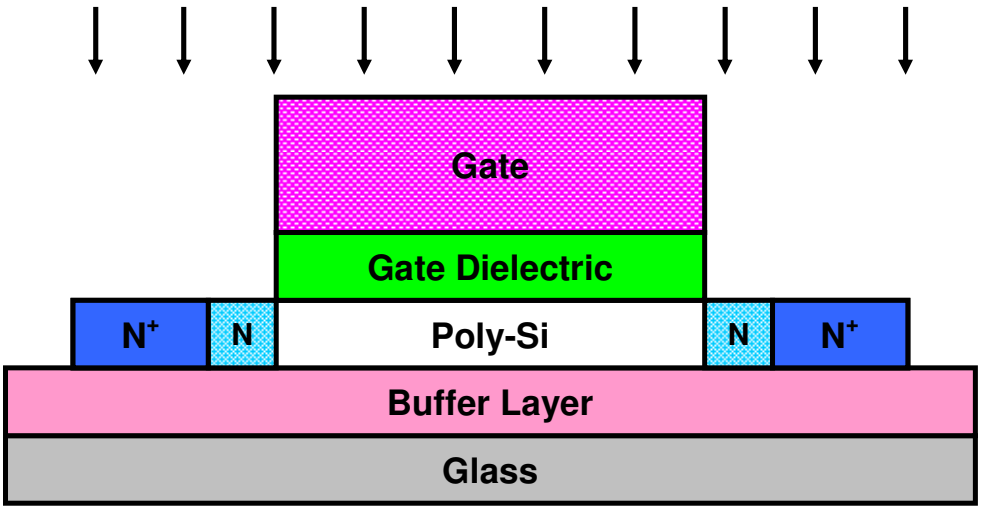
(c) Crystallization of the amorphous-Si film followed by active region definition.



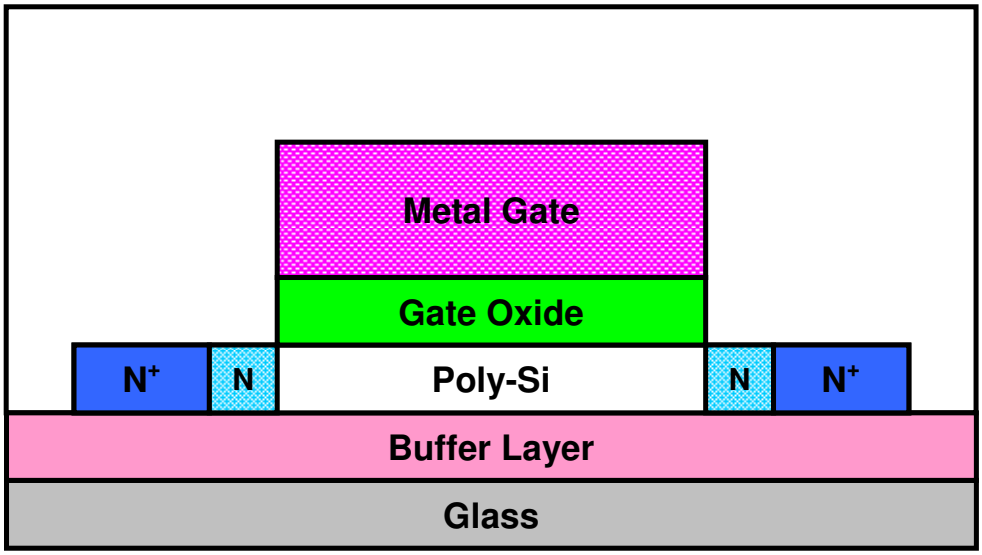
(d) Source and drain dopping.



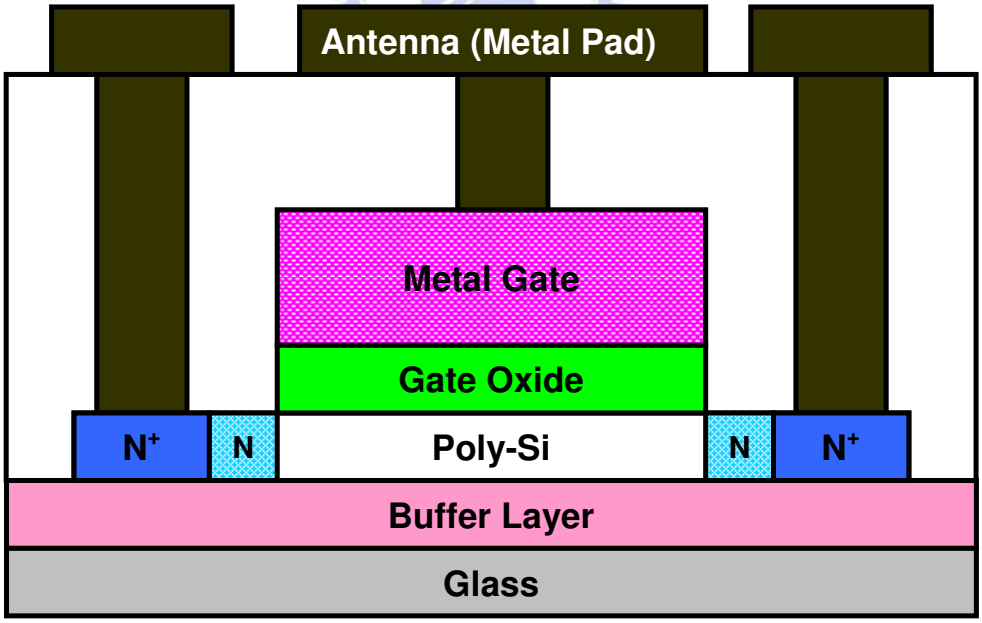
(d) Gate dielectric and Mo deposition followed by patterning as the gate electrode.



(e) Self-aligned lightly doped source/drain formation followed by hydrogenation.



(f) Inter-layer dielectric deposition and dopant activation..



(g) Contact hole opening, and interconnection metal deposition and patterning.

Fig. 4.1 Process flow of the *n*-channel LTPS TFT.

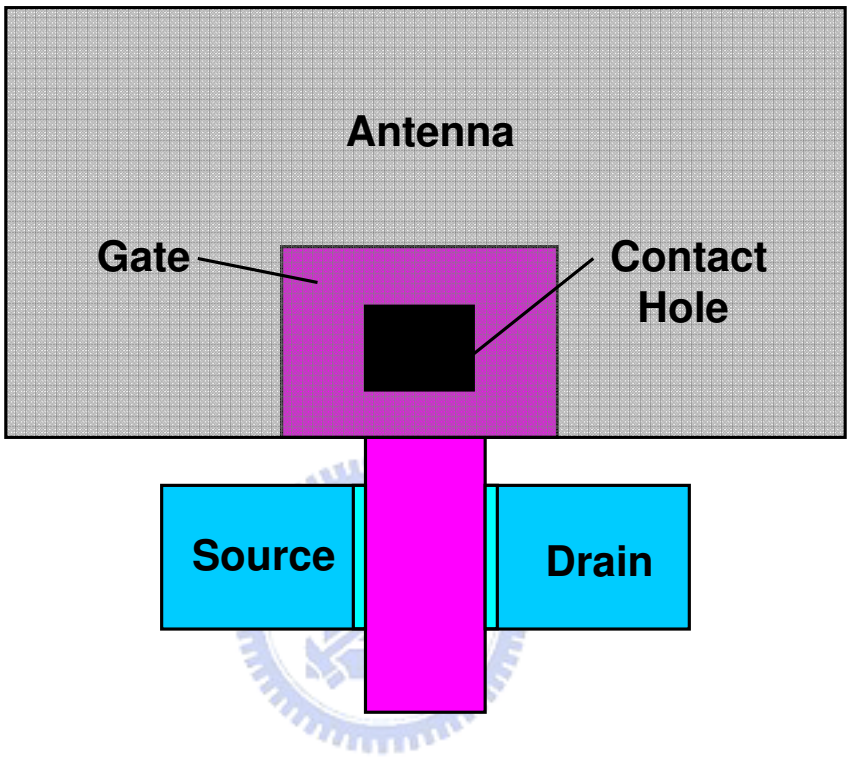


Fig. 4.2 Antenna geometry of the device structure used in this study. The AR is defined as the antenna area divided by the gate area on the active region.

Table 4.1 Antenna patterns having a fixed gate area on the active region and various values of AR.

W/L (μm/μm)	AR	Antenna Area = (W×L) ×AR (μm^2)
20/10	36	7200
20/10	100	20000
20/10	1000	200000

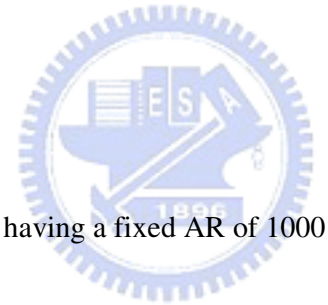


Table 4.2 Antenna patterns having a fixed AR of 1000 and various channel widths.

W/L (μm/μm)	AR	Antenna Area=(W×L)×AR (μm^2)
5/5	1000	25000
20/5	1000	100000
30/5	1000	150000

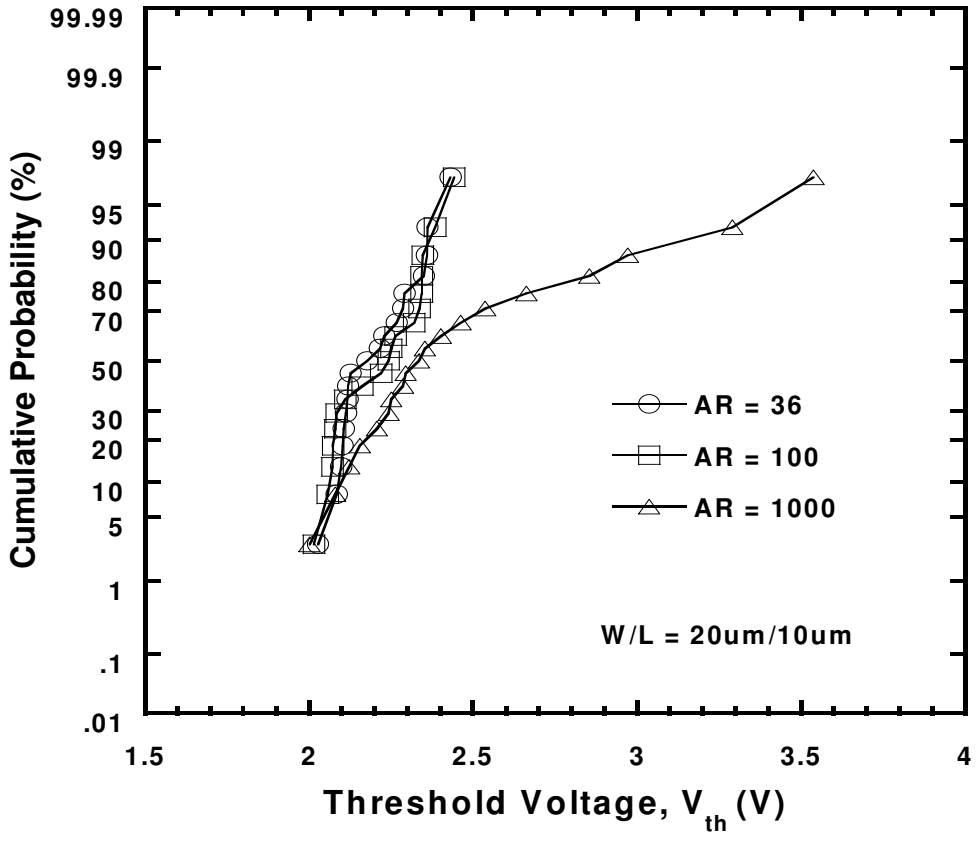
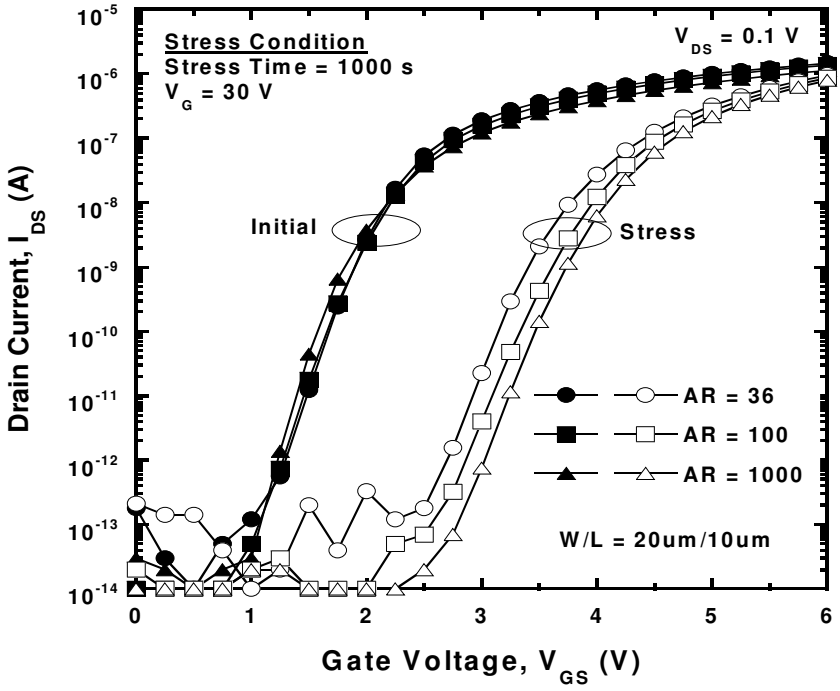
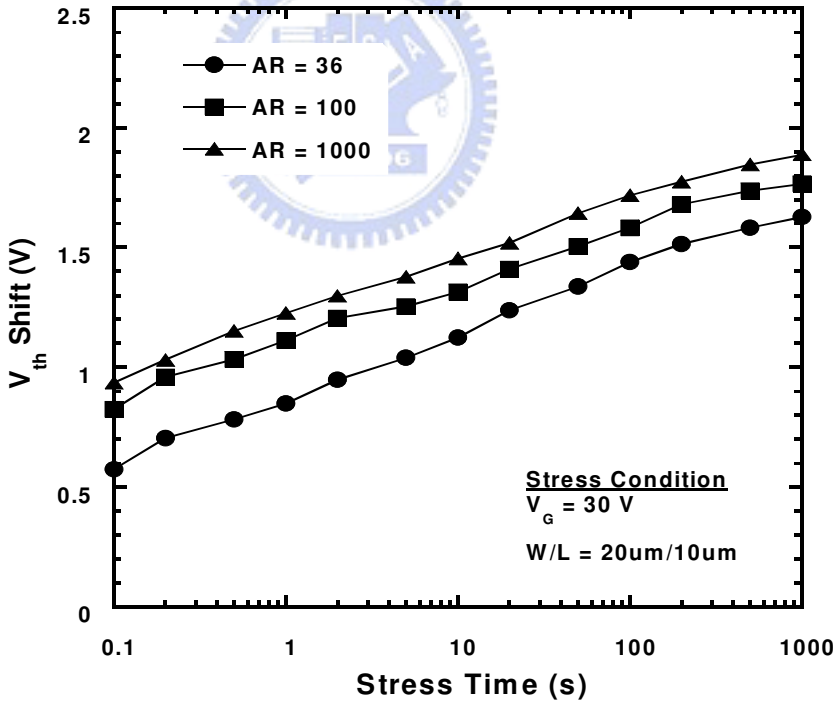


Fig. 4.3 Cumulative probability of the threshold voltages for the LTPS TFTs having various ARs. The threshold voltage was measured at a constant drain current I_{DS} of 10 nA × (*W*/*L*) at a value of V_{DS} of 0.1 V.

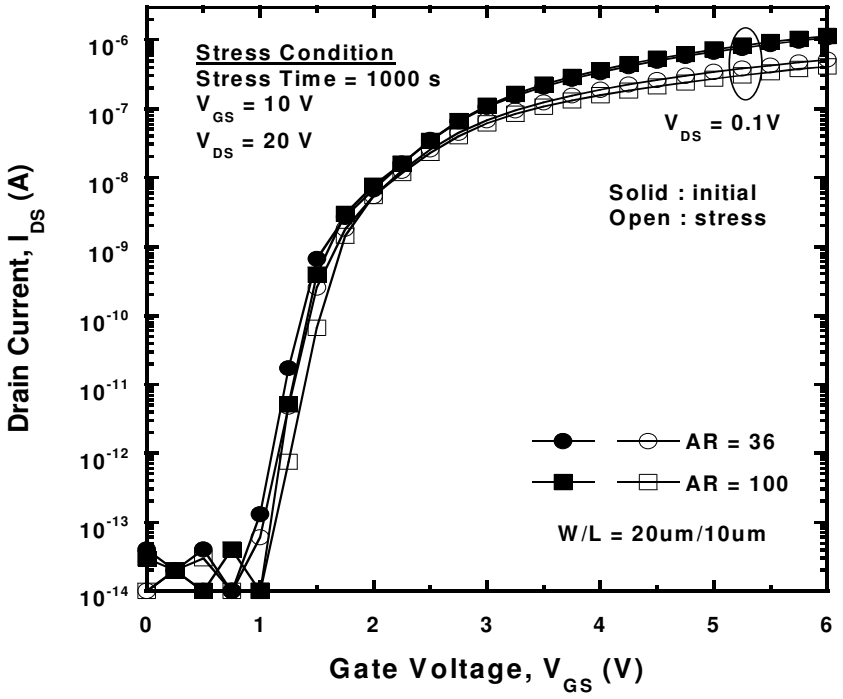


(a)

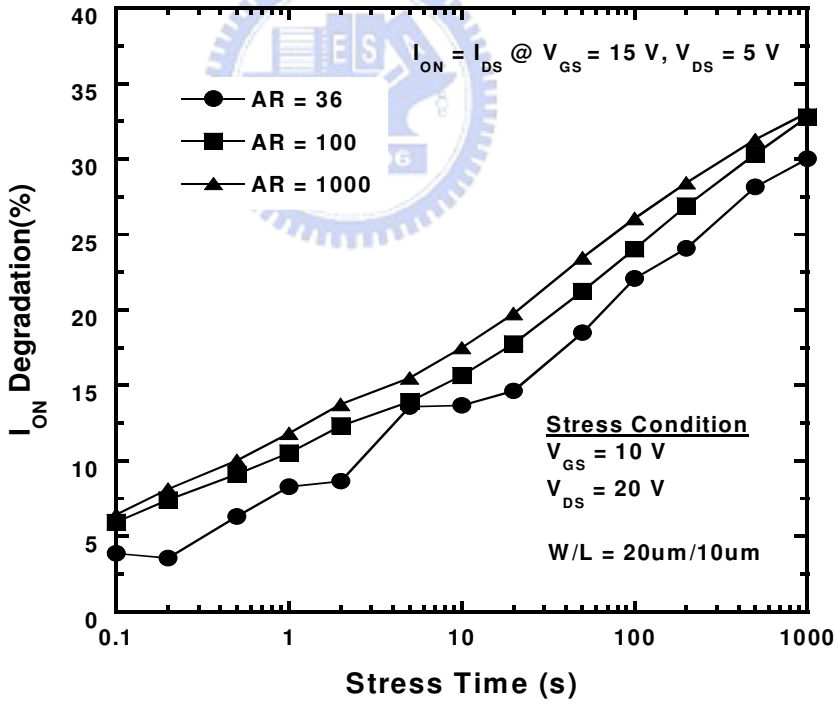


(b)

Fig. 4.4 (a) Transfer characteristics and (b) time dependence of the threshold- voltage shift of the LTPS TFTs having various values of AR under a gate-bias stress. Stress condition: $V_D = V_S = 0$ V; $V_G = 30$ V.



(a)



(b)

Fig. 4.5 (a) Transfer characteristics and (b) drive-current degradation of the LTPS TFTs having various values of AR under a hot-carrier stress. Stress condition: V_{GS} = 10 V; V_{DS} = 20 V.

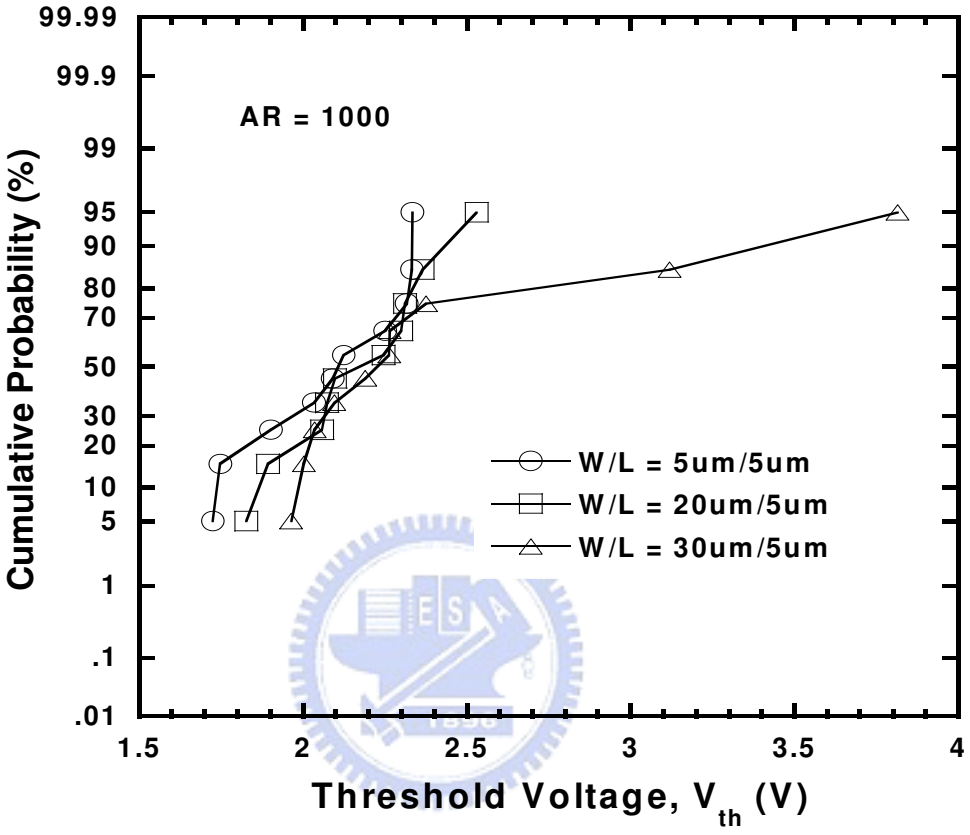


Fig. 4.6 Cumulative probability of the threshold voltages for the LTPS TFTs having different channel widths and a fixed AR of 1000.

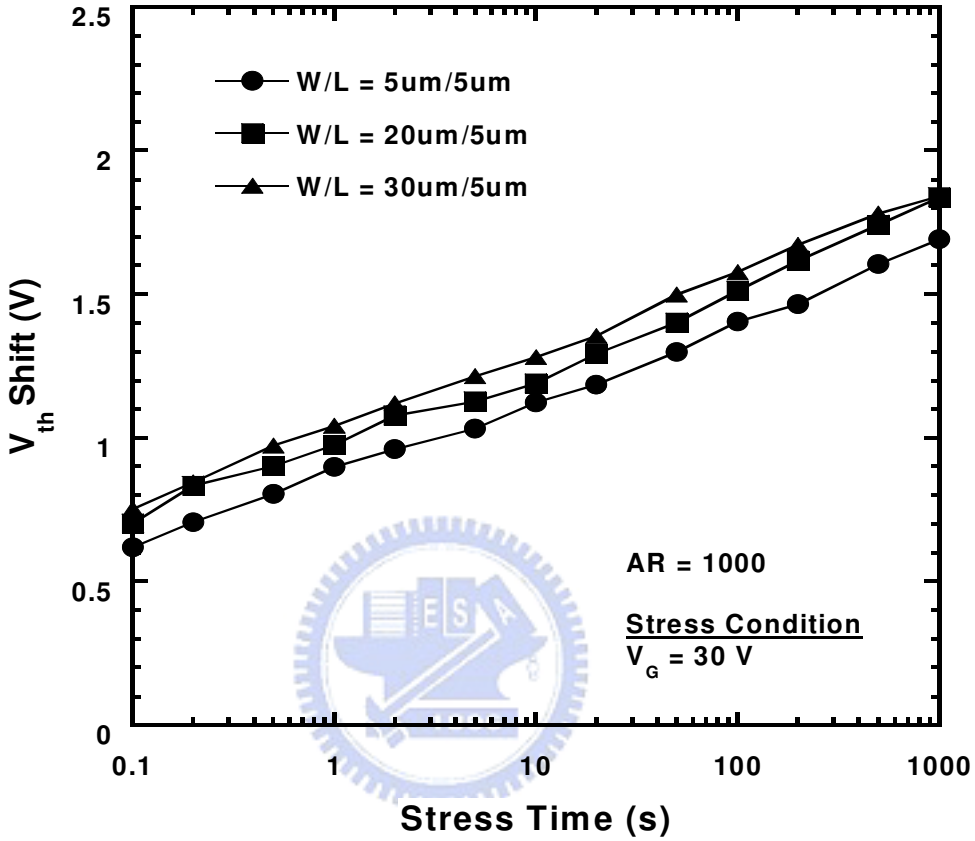


Fig. 4.7 Time dependence of the threshold-voltage shift for the LTPS TFTs having different channel widths and a fixed AR of 1000 under a gate-bias stress. Stress condition: $V_D = V_S = 0$ V; $V_G = 30$ V.

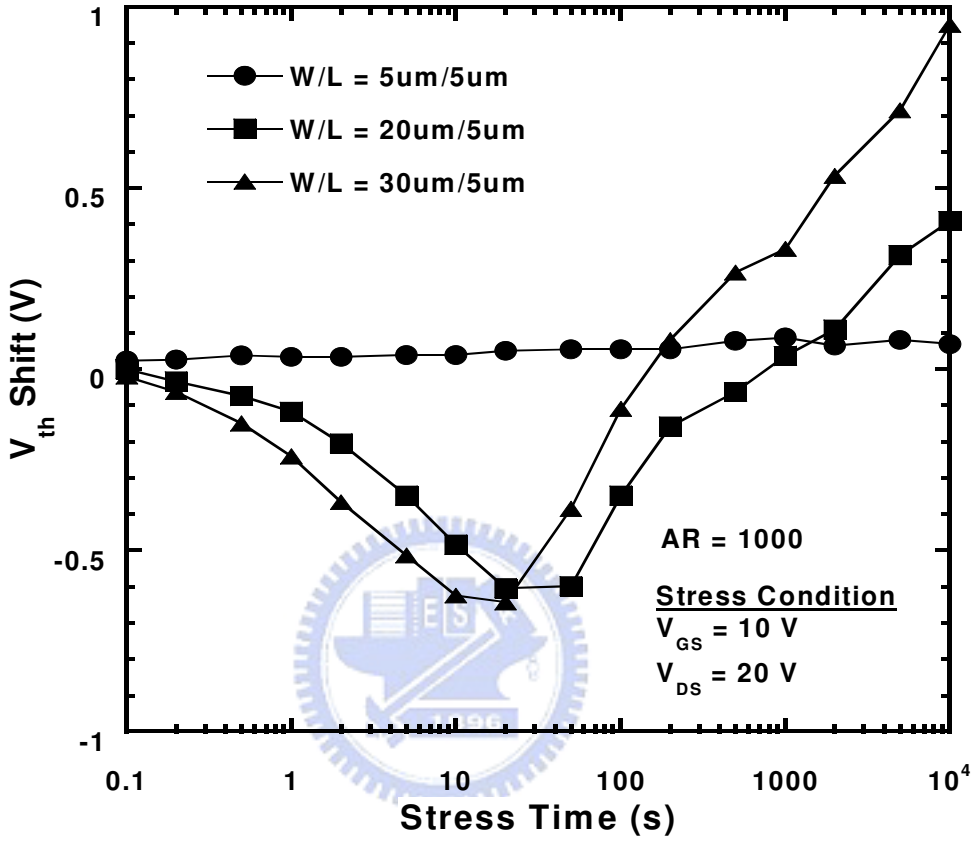


Fig. 4.8 Time dependence of the threshold-voltage shifts for the LTPS TFTs having various channel widths and a fixed AR of 1000 under a hot-carrier stress.

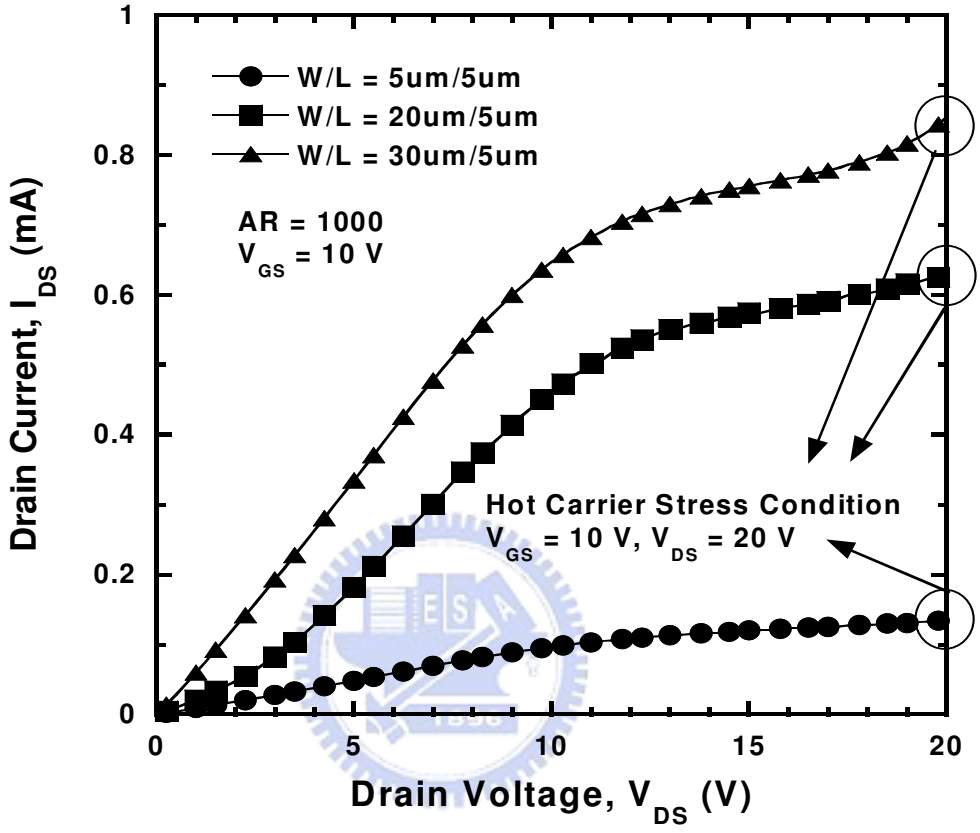
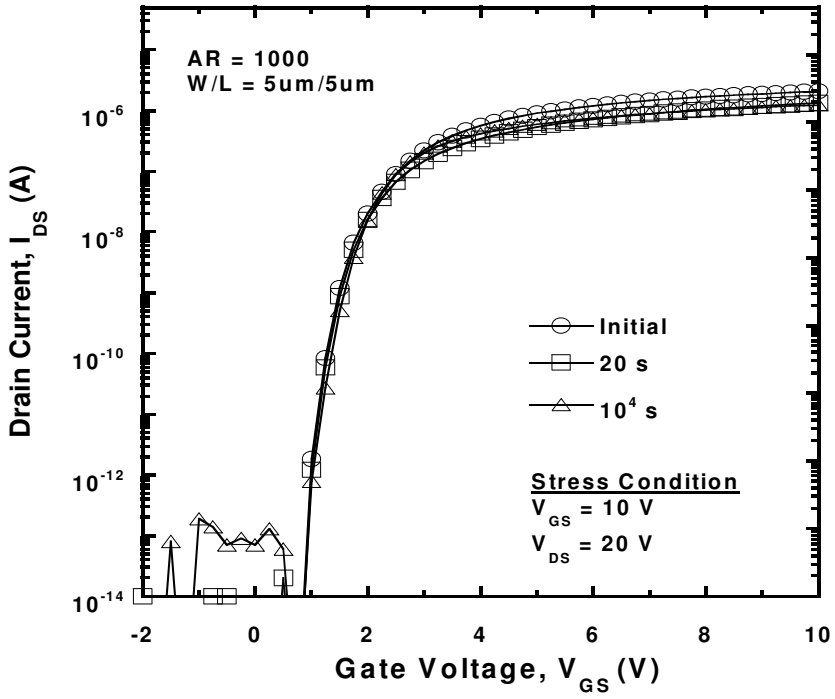
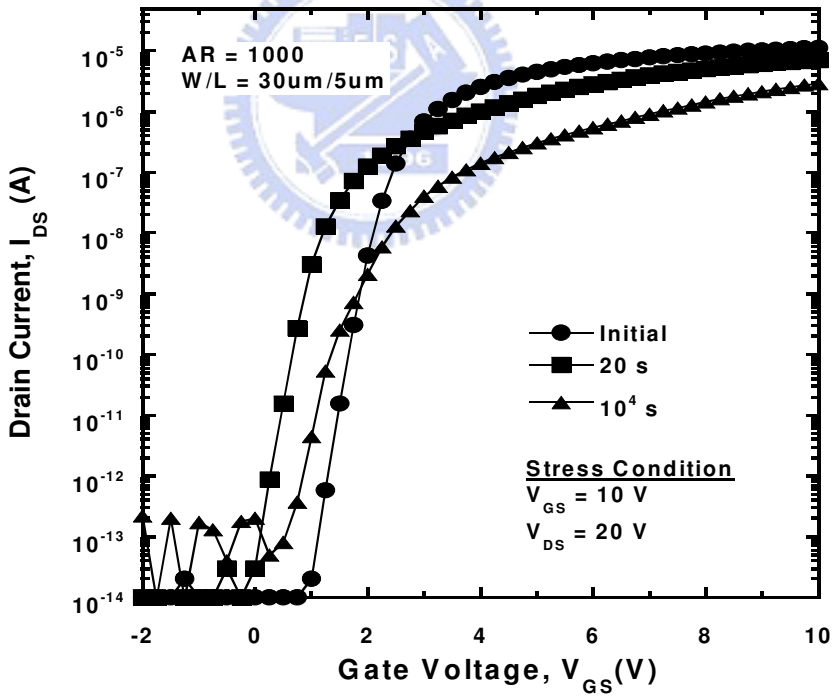


Fig. 4.9 Output characteristics of the LTPS TFTs having different channel widths and a fixed AR of 1000 prior to hot-carrier stress. The small circles (O) mark the hot-carrier stress conditions used in this study.



(a)



(b)

Fig. 4.10 Transfer characteristics of the LTPS TFTs having channel widths of (a) 5 μm and (b) 30 μm and a fixed AR of 1000 at various hot-carrier stress times.

Chapter 5

Antenna Effect Enhanced Negative Bias Temperature Instability in Low-Temperature Polycrystalline Silicon Thin-Film Transistors

5.1 Introduction

Recently, bias temperature instability (BTI) is considered a most serious obstacle for securing the reliability of CMOS devices [5.1]—[5.7] and poly-Si TFTs [5.8], [5.9]. BTI is observed mainly on *p*-FETs, in which a negative gate voltage is applied, but a negligible BTI is observed on *n*-FETs, which requires a positive gate bias voltage. Therefore, much attention has been given to the negative bias temperature instability (NBTI) in the *p*-MOSFETs rather than to the positive bias temperature instability (PBTI) in the *n*-MOSFETs. To realize system on panel (SOP), as we mentioned before, LTPS TFTs must be used and designed using the CMOS configuration. Therefore, NBTI becomes an important reliability issue for LTPS TFTs during the inverter operation. In Chapters 2 and 3, we have demonstrated that the NBTI-degradation mechanism in LTPS TFTs can be explained by the generation of fixed oxide charges, interface trap states, and grain-boundary trap states, resulting in the device degradation in the threshold voltage, subthreshold swing, and transconductance.

Plasma damage has been reported to degrade the performance and reliability of thin-film transistors [5.10]—[5.12]. In Chapter 4, the impacts of the antenna effect on the performance and reliability of LTPS TFTs have been studied. It has been shown that the antenna effect degrades the device lifetime under hot-carrier or gate-bias stress. However, the correlation between the antenna effect and NBTI in LTPS TFTs has not been explored.

In this study, *p*-channel LTPS TFTs with various antenna structures were designed and a NBTI measurement was performed. The impact of an antenna effect on the NBTI behaviors of LTPS TFTs is explored. In our experiments, the antenna effect is demonstrated to have a significant detrimental effect on NBTI behaviors of devices.

5.2 Experiments

LTPS TFTs were fabricated with channel lengths (L) and widths (W) of 10 and 20 μm, respectively. The detailed process flow has been described in Chapter 2. The metal pads attached to the gate were designed with antenna-area ratios (AR) of 100, 500, and 1000, respectively. The AR is defined as the ratio between the antenna area and gate area on the active region ($L \times W$). The schematic cross-sectional diagram of the test structure is shown in Fig. 5.1. NBTI stress was performed at 150 °C, and a stress voltage of −30 V was applied to the gate with the source/drain grounded. All the measurements were taken at stress temperatures, and the stress was periodically stopped to measure the basic device characteristics. The delay time between the stress and measurement was set at 1 s.

5.3 Results and Discussion

Figs. 5.2(a) and 5.2(b) show the NBTI-induced transfer-characteristic degradation in the linear and logarithmic scale, respectively, for the LTPS TFTs with ARs of 100, 500, and 1000. The antenna devices chosen for the NBTI stress were indistinguishable from each other in their transfer characteristics. We found that NBTI stress makes the threshold voltage (V_{th}) shift to the negative direction and simultaneously degrades the subthreshold swing (S); additionally, the effects worsen for the devices with larger ARs. Figs. 5.3(a)−5.3(c) show the output characteristics of the LTPS TFTs with ARs of 100, 500, and 1000, respectively, before and after 1000-s NBTI stress. The device with a larger AR shows more reduction in

the saturation current after NBTI stress. Therefore, it is reasonable to suppose that the NBTI in LTPS TFTs is modulated by the antenna effect. The correlations can further be observed from the threshold-voltage shift versus the stress time for the LTPS TFTs with different ARs, as shown in Fig. 5.4(a). It significantly confirms that the device with a larger AR does indeed induce a greater threshold-voltage shift under NBTI stress. Therefore, compared with the threshold-voltage shift, the drive-current (I_{ON}) degradation revealed in Fig. 5.4(b) presents the same trend that confirms antenna-effect-enhanced NBTI.

Owing to the fact that LTPS TFTs have a lot of grain boundaries in the channel region, the NBTI-degradation mechanism of the LTPS TFTs will be different from that of MOSFETs. Figs. 5.5(a)－5.5(c) show the grain-boundary trap-state density (N_{trap}) estimated by the Levinson and Proano method [5.13], [5.14]. Under NBTI stress, the grain-boundary trap-state density increases from 42.7 % to 96.3 % for the devices with ARs of 100, 500, and 1000, respectively. The overall increase of the grain-boundary trap-state density is enhanced for the device with a larger AR; this signifies that the antenna effect accelerates the generation of grain-boundary trap states during NBTI stress.

It is well known that the threshold-voltage shift of *p*-MOSFETs under NBTI stress shows a power-law dependence on the stress time with exponents (n) from 1/3 to 1/4 ($\Delta V_{th} \sim t^{n}$), which can be illustrated by the diffusion-controlled electrochemical reactions. These reactions are usually explained by the generation of fixed oxide charges and interface trap states in MOSFETs, leading to the threshold-voltage shift [5.15]－[5.17]. Fig. 5.6(a) shows the linear fit of the log-log plot of the threshold-voltage shift versus the stress time of the LTPS TFTs with ARs of 100, 500, and 1000 under NBTI stress. The experimental results also follow a similar power-law dependence on the stress time. Fig. 5.6(b) exhibits the extracted n values for the LTPS TFTs with different values of AR. It is interesting to note that the n value is larger for the devices with larger ARs. This implies that devices with a larger antenna area would degrade more, for a given NBTI stress voltage and stress time, even

though their initial characteristics may be the same. We suggest that the antenna effect degrades the oxide quality that the diffusion of the hydrogen species is enhanced. Therefore, the devices with larger ARs exhibit larger exponents due to the enhanced NBTI-degradation rate.

Table 5.1 compares the parameter variation of those LTPS TFTs which were stressed by NBTI for 1000 s; the ARs of those devices are 100, 500, and 1000, respectively. As the AR increases, the devices have a higher degree of degradation in field-effect mobility (μ_{FE}), subthreshold swing, threshold voltage, grain-boundary trap-state density, and drive current. All of the results confirm that the antenna effect enhances the NBTI degradation in LTPS TFTs.

5.4 Summary

In this chapter, we confirmed that the antenna effect is a significant factor for NBTI reliability in LTPS TFTs. The experimental results confirm that the LTPS TFTs with a larger antenna area ratio will have a higher degree of degradation in threshold voltage, field-effect mobility, and drive current under NBTI stress. The enhanced degradation can be attributed to the faster diffusion rate of the hydrogen species in the damaged oxide for the devices with larger ARs. It could be concluded that the antenna effect will speed up the NBTI, and should be avoided for LPTS TFT circuitry designs.

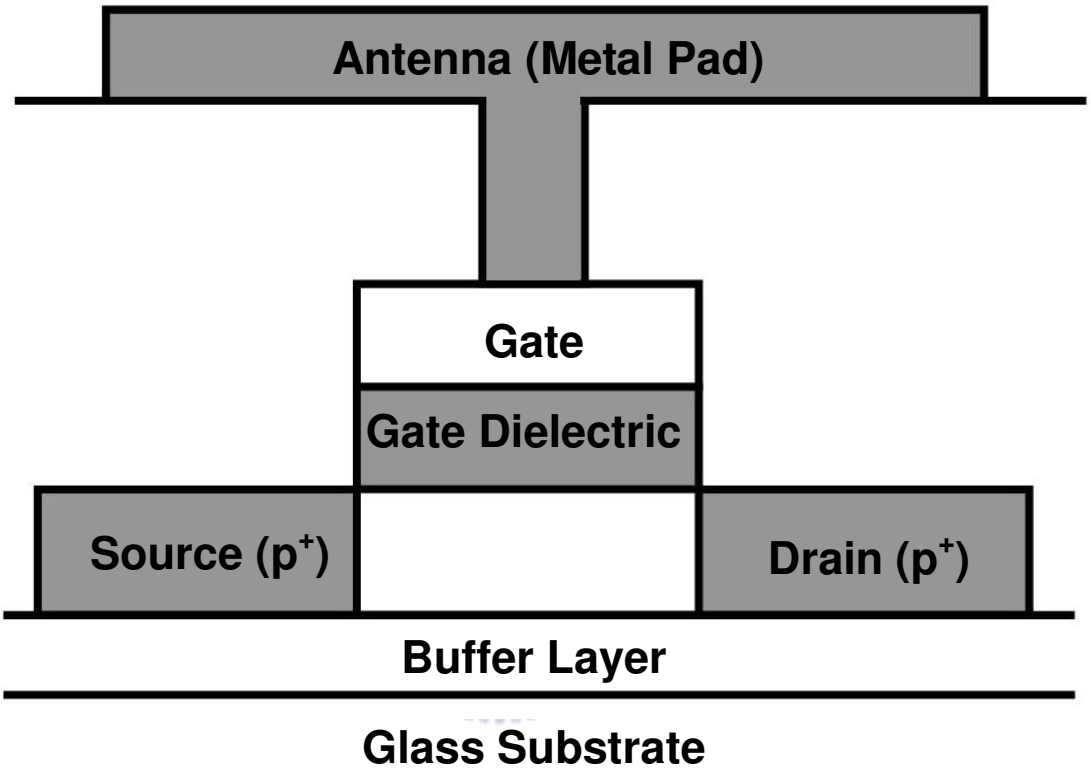
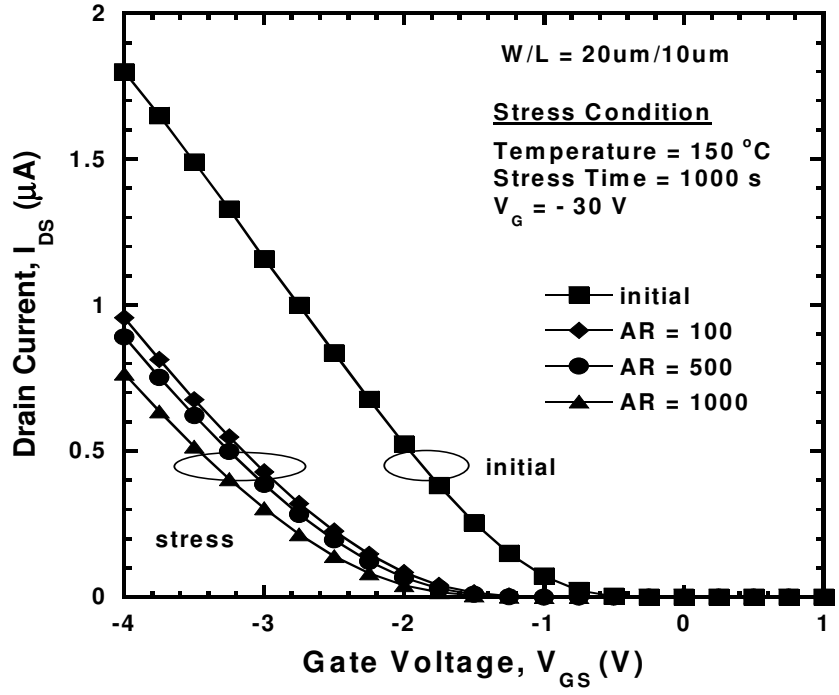
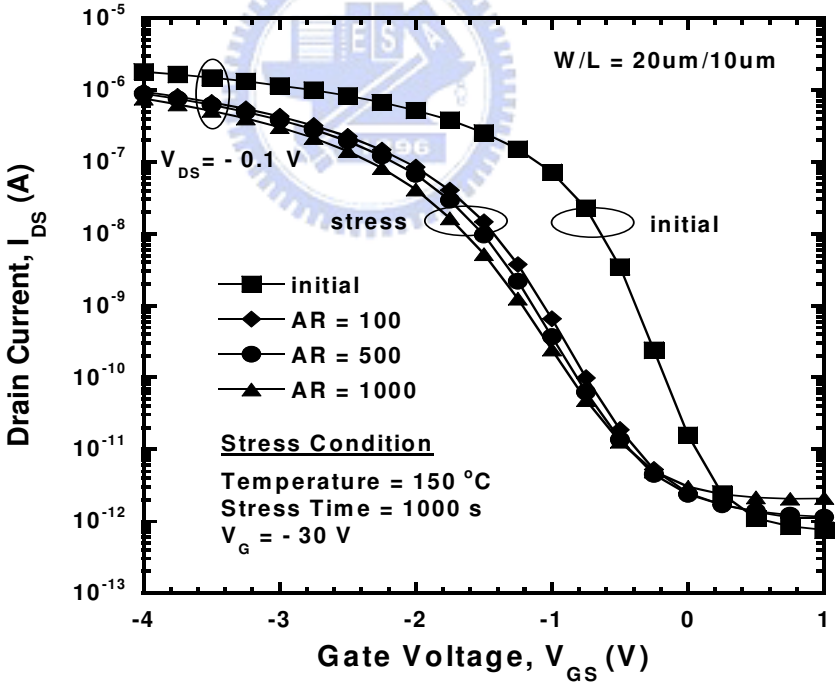


Fig. 5.1 Schematic cross-sectional diagram of the device structure.



(a)



(b)

Fig. 5.2 Transfer characteristics in the (a) linear and (b) logarithmic scale of the LTPS TFTs with an AR of 100, 500, and 1000 before and after 1000 s NBTI stress.

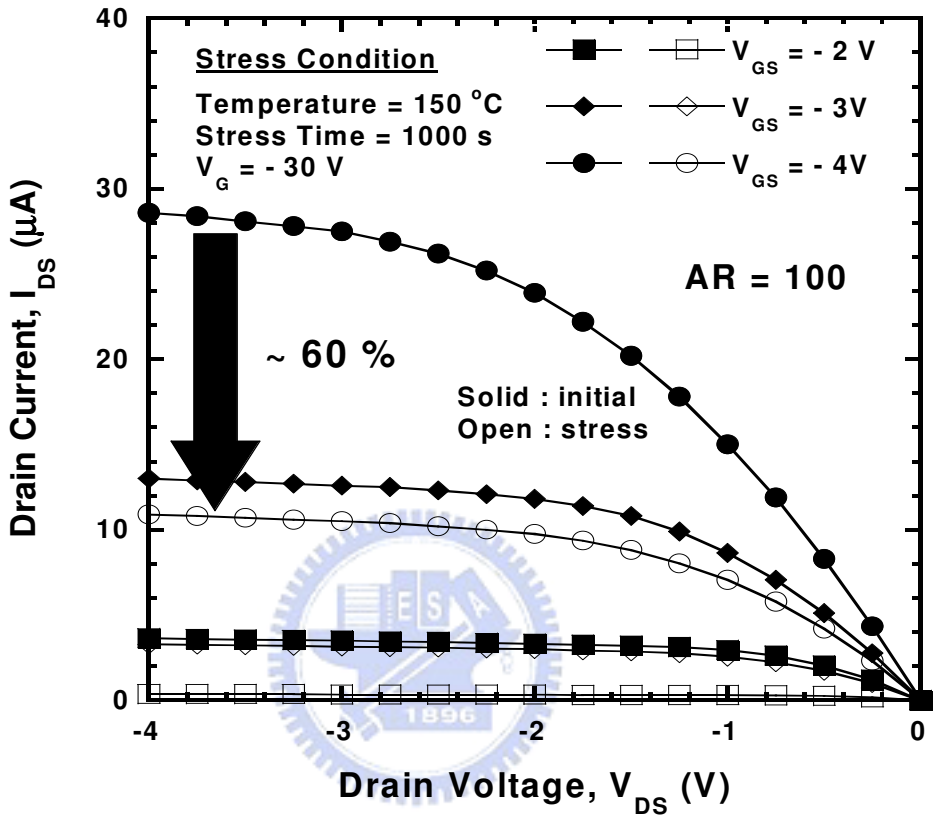


Fig. 5.3 (a) Output characteristics of the LTPS TFTs with an AR of 100 before and after 1000 s NBTI stress.

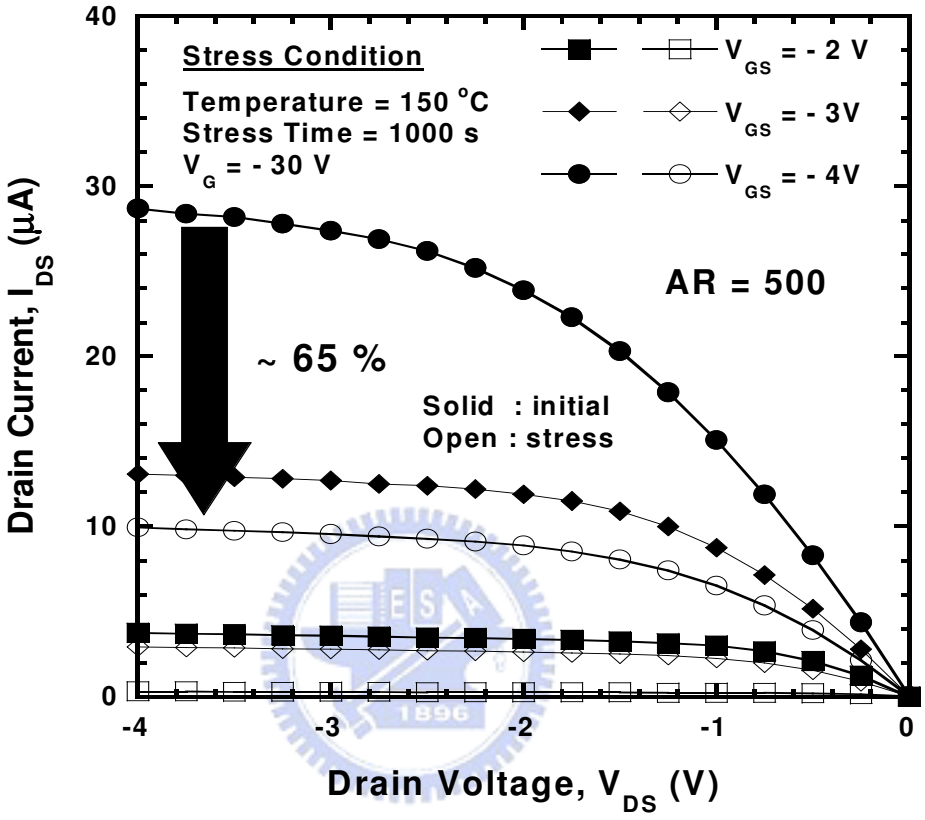


Fig. 5.3 (b) Output characteristics of the LTPS TFTs with an AR of 500 before and after 1000 s NBTI stress.

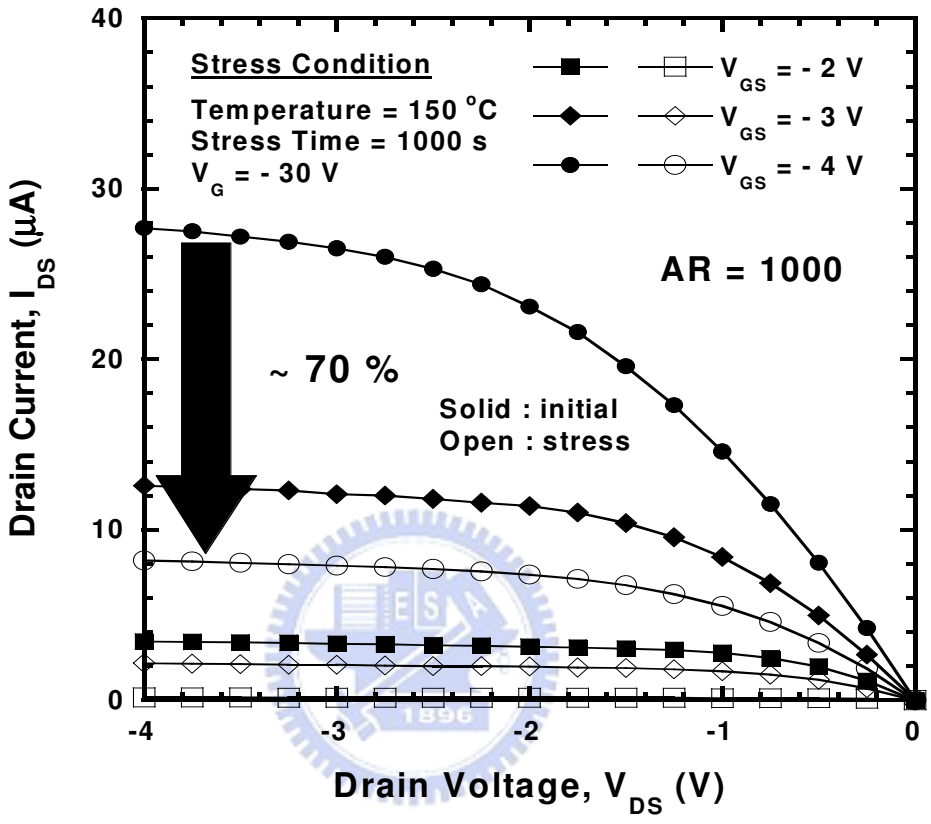
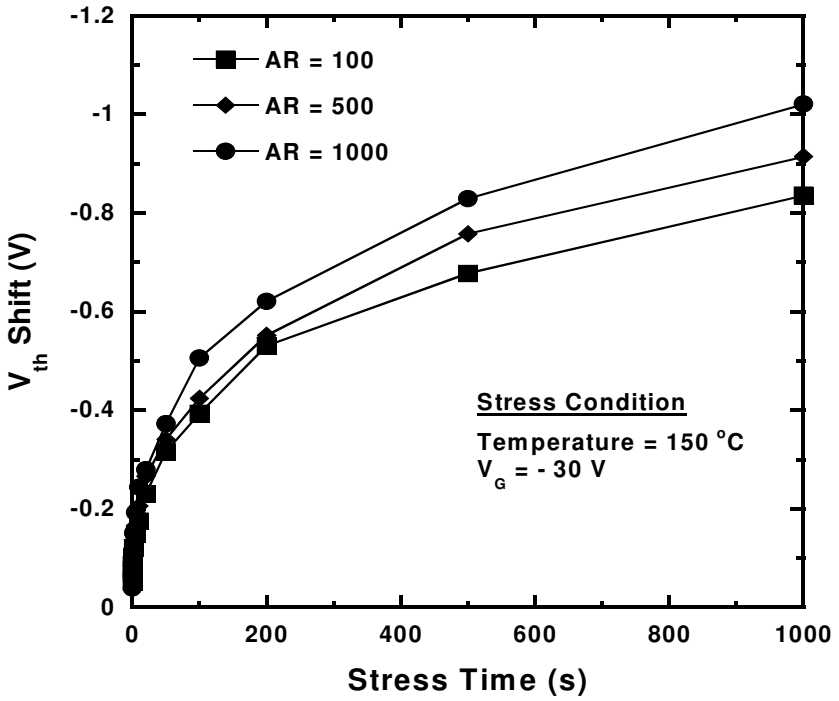
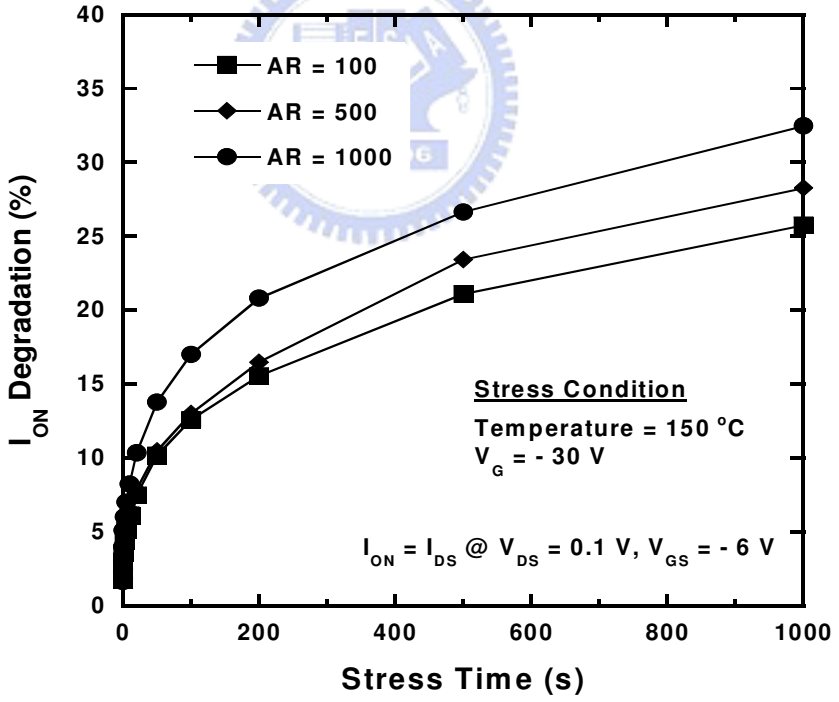


Fig. 5.3 (c) Output characteristics of the LTPS TFTs with an AR of 1000 before and after 1000 s NBTI stress.



(a)



(b)

Fig. 5.4 Dependence of the (a) threshold-voltage shift and (b) drive-current degradation on the stress time for the LTPS TFTs with an AR of 100, 500, and 1000.

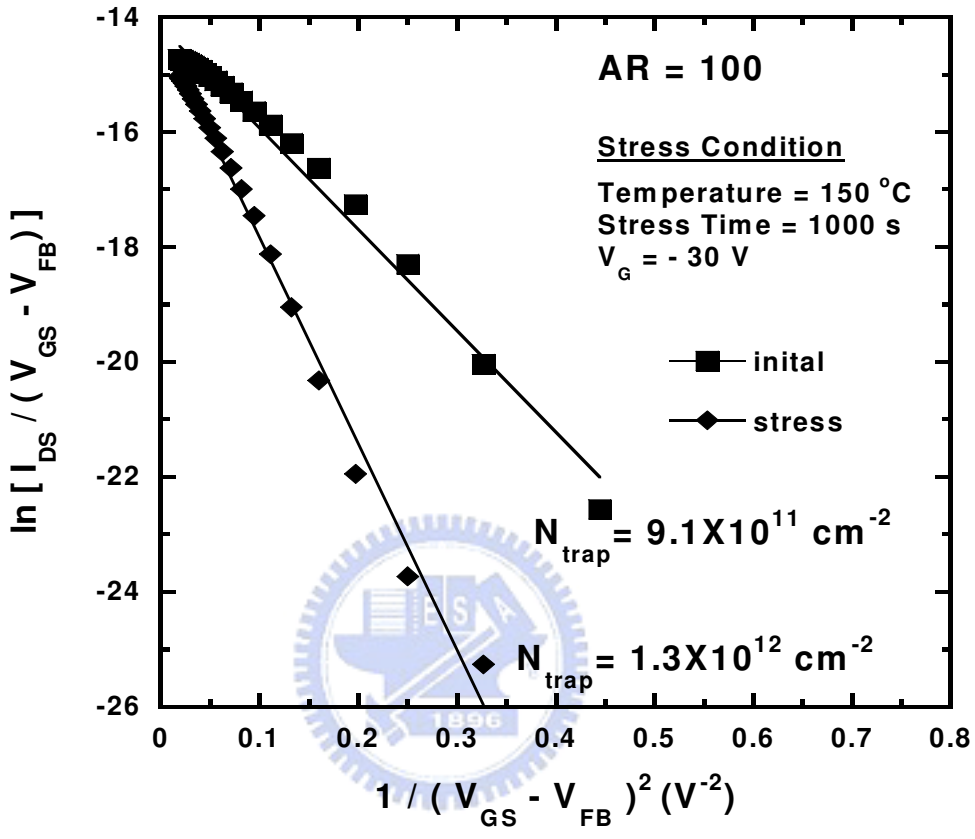


Fig. 5.5 (a) Extraction of the grain-boundary trap-state density of the LTPS TFT with an AR of 100 before and after 1000 s NBTI stress.

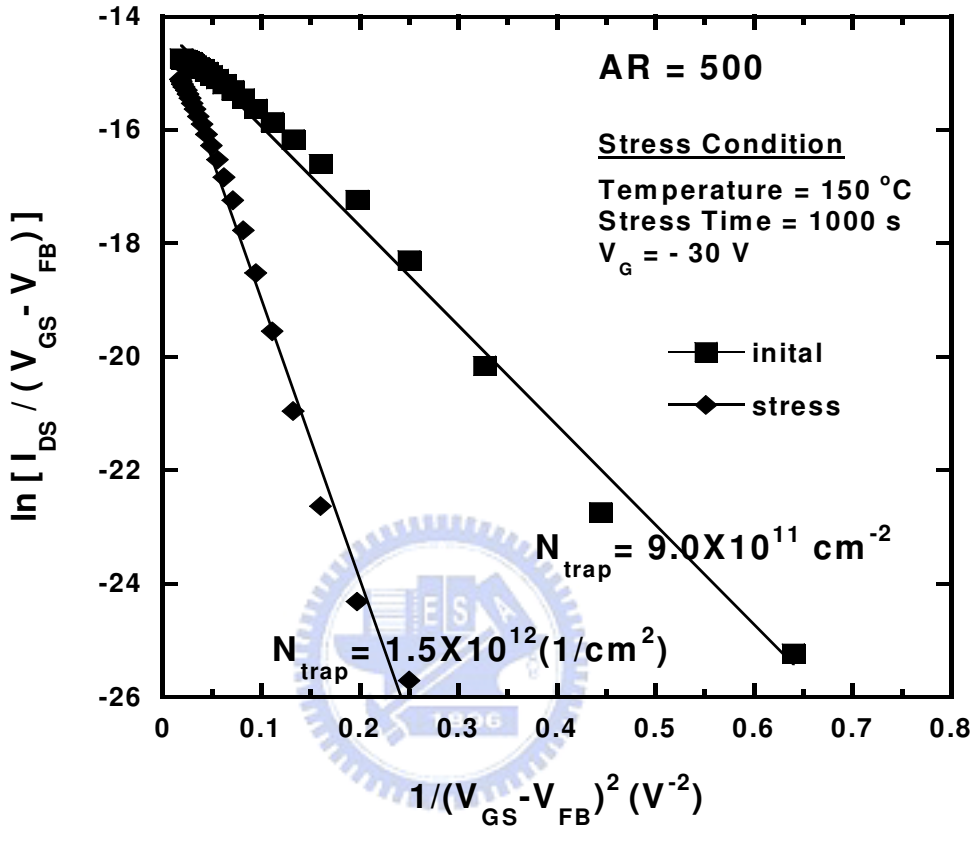


Fig. 5.5 (b) Extraction of the grain-boundary trap-state density of the LTPS TFT with an AR of 500 before and after 1000 s NBTI stress.

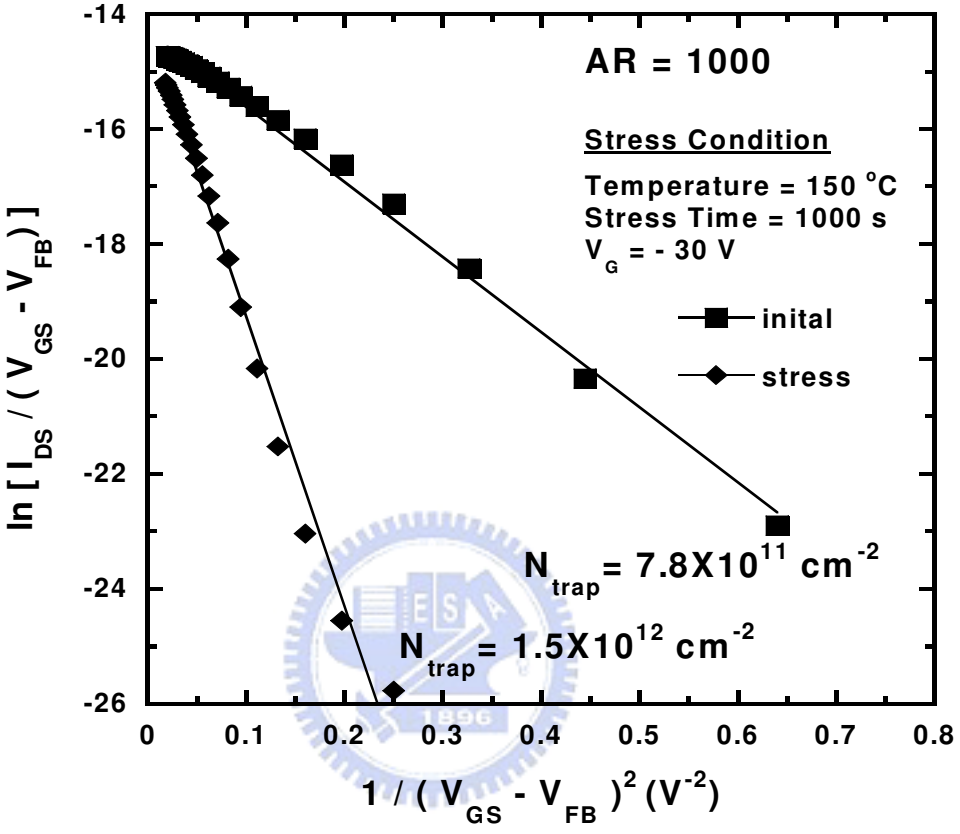
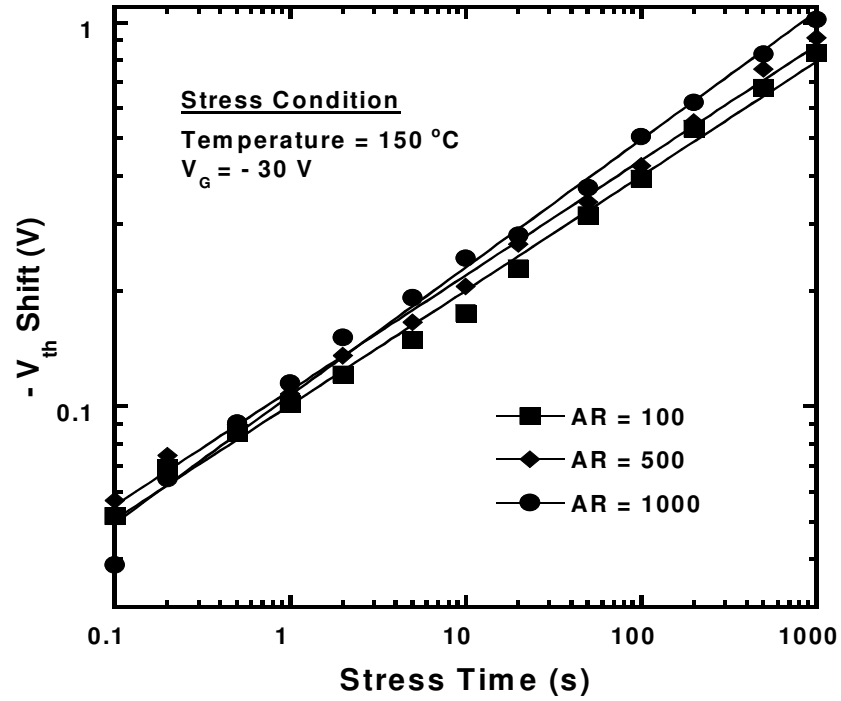
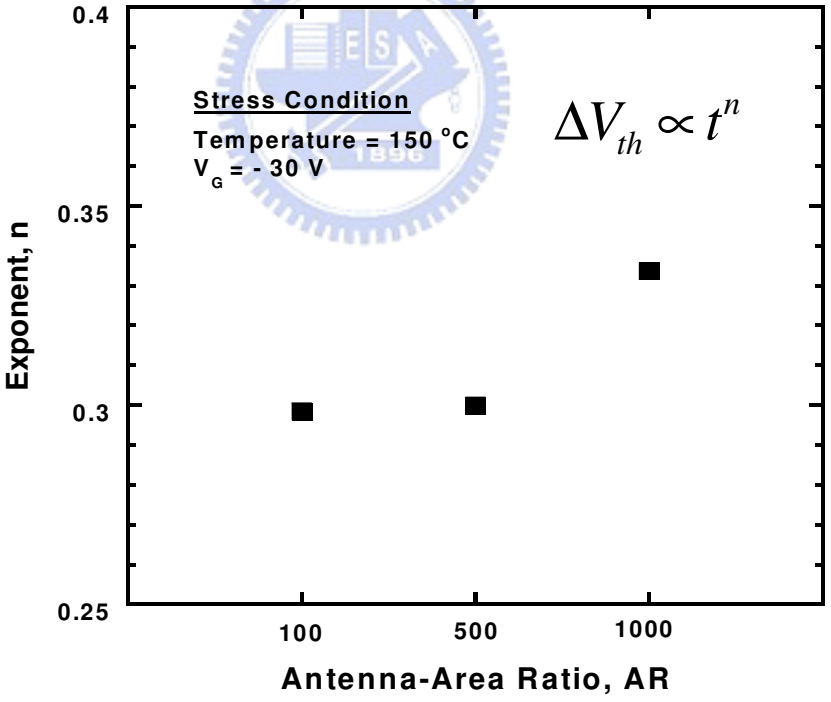


Fig. 5.5 (c) Extraction of the grain-boundary trap-state density of the LTPS TFT with an AR of 1000 before and after 1000 s NBTI stress.



(a)



(b)

Fig. 5.6 (a) Linear fit of the log-log plot of the threshold-voltage shift versus the stress time of the LTPS TFTs with an AR of 100, 500, and 1000 under NBTI stress. (b) Exponents (n) of the LTPS TFTs with various ARs.

Table 5.1 Comparison of parameter variation of the LTPS TFTs with an AR of 100, 500, and 1000 after 1000 s NBTI stress.

Stress Condition: V_G = −30 V, 150 °C			
	AR = 100	**AR = 500**	**AR = 1000**
$\triangle\mu_{FE}$ (%)	**−6.7**	**−7.9**	**−9.0**
$\triangle S$ (%)	**52.3**	**64.2**	**78.7**
$\triangle V_{th}$ (V)	**−0.84**	**−0.91**	**−1.02**
$\triangle I_{ON}$ (%)	**−25.8**	**−28.3**	**−32.5**
$\triangle N_{trap}$(%)	**42.7**	**67.8**	**96.3**

Chapter 6

Combined Negative Bias Temperature Instability and Hot-Carrier Effect in Low-Temperature Polycrystalline Silicon Thin-Film Transistors

6.1 Introduction

As we have mentioned in Chapter 1, LTPS TFTs have a high potential of integrating the driver circuitry on the display's substrate to achieve system on panel (SOP). Different from the requirements for pixels, electrical stability is greatly needed for driving circuitry, which operates under a high pulse voltage [6.1]. Negative bias temperature instability (NBTI) has been introduced into the reliability insurance process for the very large scale integration circuit, and the related model has been comprehensively developed [6.2]－[6.4]. NBTI arises at high temperatures under the influence of negative voltages on the gate of the devices. In LTPS TFTs, the effect seen is a negative shift in the threshold voltage, and a decrease in the subthreshold swing of the transistor due to an increase in the amount of positive oxide trapped charges, interface trap states, and grain-boundary trap states, as shown in Chapters 2 and 3. In addition to NBTI, hot-carrier stress (HCS) has been widely studied and commonly used for reliability assurance [6.5]－[6.7]. The hot-carrier effect which originates from a high electric field near the drain junction mainly causes the variation of threshold voltages. The threshold-voltage variation during stress is important for circuit designers in order to integrate TFTs into flat-panel displays.

Because the LTPS TFT driving circuit is designed using the CMOSFET structure, HCS becomes a transient phenomenon that mixes with the effect of NBTI [6.8]. Unfortunately, the

mixed effects of NBTI and HCS are rarely explored for LTPS TFTs. Therefore, in this chapter, we demonstrate here a reliability model for *p*-channel LTPS TFTs that considers both the effects of NBTI and HCS. From the experimental results and the model we proposed, the combined NBTI and HCS effects can be clearly identified, and this may be useful for circuit designers.

6.2 Experiments

LTPS TFTs fabricated on glass substrates were used in this study. The devices were fabricated with a channel width (W) of 20 μm and channel lengths (L) of 10 or 20 μm. The detailed process flow has been described in Chapter 2. The constant current method is used for threshold voltage (V_{th}) extraction, where the V_{th} is defined as the bias of gate voltage that forces drain current to (W/L) × 10 nA at V_{DS} = −0.1 V. Under the extraction method, the initial threshold voltages of all the devices were about −1 V at room temperature. We used HP 4156B for both the NBTI and HCS measurements. The stress was performed at various stress temperatures with a gate voltage (V_{GS}) of −20 V and a drain voltage (V_{DS}) ranging from 0 to −20 V, to study the combined NBTI and HCS effects. The schematic cross-sectional diagram of the LTPS TFT and stress setup is shown in Fig. 6.1.

6.3 Results and Discussion

Figs. 6.2(a) and 6.2(b) show the transfer characteristics of the devices before and after stress at 100 °C under different stress biases. In Fig. 6.2(a), the stress was performed under a stress V_{GS} of −20 V and a stress V_{DS} of 0 V, and the stress condition corresponds to NBTI stress. In Fig. 6.2(a), it is obvious that the threshold voltage shifts to the negative direction after the stress, and the subthreshold swing and maximum transconductance slightly degrades. In Fig. 6.2(b), the stress was performed under a hot-carrier stress condition, in

which both V_{GS} and V_{DS} were equal to -20 V. The subthreshold swing and maximum transconductance degrade after the hot-carrier stress, implying that interface trap states were generated.

Fig. 6.3 shows the threshold-voltage shift (ΔV_{th}) of the devices, stressed with a fixed V_{GS} of -20 V and a V_{DS} ranging from 0 to -20 V. The temperature was kept at 25, 75, and 100 ^{o}C. It was found that the measured $|\Delta V_{th}|$ exhibits two degradation regimes. In the low $|V_{DS}|$ stress condition, the $|\Delta V_{th}|$ decreases with an increase of $|V_{DS}|$. On the other hand, the $|\Delta V_{th}|$ increases upon increasing the $|V_{DS}|$ at high $|V_{DS}|$ bias. We speculate that the NBTI, which is induced by a vertical-electric field, is suppressed at a low $|V_{DS}|$ bias. The suppression of the NBTI is soon taken over by the influence of a horizontal electric field when the V_{DS} continuously decreases to be smaller than -2.5 V. The phenomenon is caused by the fact that an increment of the horizontal electric field will enhance the hot-carrier generation; this is particularly true for the stress conditions in which the V_{DS} and V_{GS} are equal to -20 V. Furthermore, the degradation is found to be highly temperature dependant; this is because both the NBTI and HCS can be thermally accelerated [6.9], [6.10].

The effect of the vertical-electric field on NBTI behavior can be further explained from Fig. 6.4. The stress was performed on devices with a fixed V_{GS} of -20 V, and $V_D = V_S$ ranging from 0 to -10 V. Because the source and drain were kept at the same bias, the hot carrier effect can be neglected; therefore, the device degradation is only attributed to the NBTI stress. As the absolute values of the source and drain biases increase, the effective vertical-electric field and the overall carrier number are decreased. This results in a reduced threshold-voltage shift and a retarded NBTI effect as shown in Fig. 6.4. Therefore, in Fig. 6.3, the drain-bias retarded NBTI effect is demonstrated to be attributed to the reduced vertical-electric field and overall carrier number.

The effect of the lateral-electric field on the device degradation can be further verified from Fig. 6.5(a). This figure shows the substrate currents of LTPS TFTs measured at 25 and

100 °C under a fixed V_{GS} of −20 V and a V_{DS} ranging from 0 to −20 V. As the device is turned on and a negative voltage is applied to the drain, holes are accelerated and move toward the drain. When the drain bias is large enough, electron-hole pairs are generated by impact ionization. The generated holes flow to the drain while the electrons flow to the substrate. Therefore, the substrate current can be used as a correlating parameter and monitor for hot-carrier-induced degradation. In Fig. 6.5(a), the substrate current is found to increase with the drain voltage, which indicates that more and more hot carriers were generated. Therefore, in the high $|V_{DS}|$ stress, the device degradation can be attributed to the increase of hot-carrier effect. The substrate current is also found to increase with the temperature. This can be further explained by Fig. 6.5(b) proposed by Li *et al.* [6.10], which shows that the carrier energy distribution at elevated temperature has a broader high-energy tail than at room temperature because of the thermal excitation. At the same time, the threshold energy for impact ionization (Φ_{II}) is smaller due to band-gap narrowing. For *p*-channel LTPS TFTs, most carriers do not have sufficient energy for impact ionization. Carriers with sufficient energy predominantly belong to a highly temperature sensitive tail of the energy distribution. Therefore, at a higher temperature, even though the field-effect mobility and drain current are degraded, the substrate current is increased.

In Fig. 6.3, it is also found that the device with a channel length of 10 μm shows a larger $|\Delta V_{th}|$ than those with channel lengths of 20 μm, even at a lower stress temperature. We suggest that there are two possible reasons to explain this phenomenon. First, the hole concentration is higher near the source/drain (S/D) edge and the gate-S/D overlap region than in the channel region. Second, many oxide defects exist near the S/D region because of the damage induced by the fabrication processes, such as gate etching and S/D formation. Due to these two reasons, NBTI degradation is enhanced locally in these regions [6.11]. Therefore, the local degradation is less effective for devices with longer channels. In contrast, for shorter-channel devices, this local degradation significantly affects the device

characteristics.

To develop a reliability model, we introduced the parameter of V_{DS} into the physical model of NBTI. In considering the mechanism of NBTI, the ΔV_{th} can be expressed in the following equation [6.12], [6.13]:

$$\Delta V_{th} = At^n \exp(-\frac{E_a}{kT}) \exp(C|V_G|) = A' \exp(C|V_G|) , \qquad (Eq.\ 6.1)$$

where A, n and C are the fitting parameters, and k, T and E_a are the Boltzmann constant, temperature, and activation energy, respectively. Here we defined that $A' = At^n exp(-E_a/kT)$. Fig. 6.6(a) shows the schematic diagram illustrating the vertical-electric field when the stress drain voltage is grounded. The vertical-electric field is uniformly distributed in the channel region. By measuring the NBTI degradation under a different stress V_{GS}, the parameter C can be extracted as shown in Fig. 6.7. Instead of the grounded drain, V_{DS} was applied to incorporate the HCS effects into the NBTI model; accordingly, the expressive equation must be modified with respect to the theoretical calculations. Fig. 6.6(b) shows the schematic diagram illustrating the vertical-electric field when a negative voltage is applied on the drain. The vertical-electric field decreases from the source region to the drain region. The channel potential at the location y from the p^+ source approximates a linear function of the location at a low $|V_{DS}|$, which can be concisely expressed as $V(y) = (y/L) \times V_{DS}$ [6.14]. Furthermore, the vertical-electric field becomes a function of $[|V_{GS}| - |V(y)|]$, and the ΔV_{th} can be rewritten as:

$$\Delta V_{th} = A' \frac{1}{L} \int_0^L \exp[C(|V_{GS}| - |V(y)|)] dy$$

$$= \frac{A'}{C|V_{DS}|} \exp(C|V_{GS}|)[1 - \exp(-C|V_{DS}|)] . \qquad (Eq.\ 6.2)$$

This simple and analytical model can be used to interpret and quantify the NBTI effect under different V_{DS} biases, as shown in Figs. 6.8(a)－6.8(c). For the HCS at high $|V_{DS}|$, the ΔV_{th} can

be experimentally expressed by the formula constructed by Takeda and Suzuki [6.15]:

$$\Delta V_{th} = Bt^{n} \exp(-\frac{\alpha}{|V_{DS}|}). \qquad (Eq.\ 6.3)$$

The parameters α can be extracted from the linear fitting of Figs. 6.8(a), 6.9(a) and 6.10(a). The ΔV_{th} that we used here to extract the parameter α is derived from subtracting the calculated ΔV_{th} of *Eq.* (6.2) from the measured ΔV_{th}. In these figures, the ΔV_{th} under low $|V_{DS}|$ stress conditions show division from the linear fitting, implying that the generation of hot carriers can be neglected and the HCS model is not valid in the low $|V_{DS}|$ bias region. The overall ΔV_{th} caused by NBTI and HCS can be predicted by combining *Eqs.* (6.2) and (6.3), as shown below:

$$\Delta V_{th} = \frac{A'}{C|V_{DS}|}\exp(C|V_{GS}|)[1-\exp(-C|V_{DS}|)] + B'\exp(-\frac{\alpha}{|V_{DS}|}). \qquad (Eq.\ 6.4)$$

The proposed model is highly consistent with the experimental results, as shown in Figs. 6.8(b), 6.9(b), and 6.10(b). Besides, the model we proposed is valid for devices with different gate lengths and under different stress temperatures.

Figs. 6.11(a) and 6.11(b) display the degradations of the subthreshold swing (*S*) and maximum transconductance, respectively. The degradation of the subthreshold swing reflects the generation of deep interface states, while the degradation of maximum transconductance reflects the tail interface states [6.16]. We found that the degradations of the subthreshold swing and maximum transconductance show similar trend with the degradations of the ΔV_{th}; this means that the interface state generation is suppressed at low $|V_{DS}|$ stress conditions, and further enhanced at high $|V_{DS}|$ stress conditions.

Fig. 6.12 shows the correlations between the drive current (I_{ON}) degradations and acceleration stresses. The I_{ON} is defined as the drain current measured at V_{GS} = −10 V and V_{DS} = −5 V. The degree of I_{ON} degradation is extracted from the methods of both the forward and reverse measurement modes. For the forward mode, we obtained the transfer

current-voltage characteristic by defining the drain, gate, and source electrodes exactly the same as with the definition in the acceleration stresses. In contrast, the biases of source and drain were exchanged in the reverse mode. At low $|V_{DS}|$ conditions, the difference of the I_{ON} degradation between the forward and reverse modes is insignificant. This indicates that the NBTI-induced degradation has geometrical symmetry. However, at high $|V_{DS}|$ conditions, the I_{ON} degradation in the reverse mode is significantly larger than that in the forward mode, implying that the damage caused by HCS is mainly located on the drain side.

6.4 Summary

We demonstrate here a reliability model that could be successfully used to predict the performance of the LTPS TFT's driving circuit. The model mainly includes both NBTI and the HCS effects that are responsible for the performance degradation. Experimental results confirm that the model could precisely describe the reliability behaviors of the *p*-channel LTPS TFTs. A significant feature of the model is that the ΔV_{th} exhibits two degradation regimes: in the low $|V_{DS}|$ regime, the device degradation is dominated by NBTI; after that, the HCS dominates the degradation mechanism in the high $|V_{DS}|$ regime. We conclude that the proposed model shows a good capability in expressing the entire reliability behavior of CMOSFET operations. Consequently, it is very attractive for the LTPS TFT circuitry design.

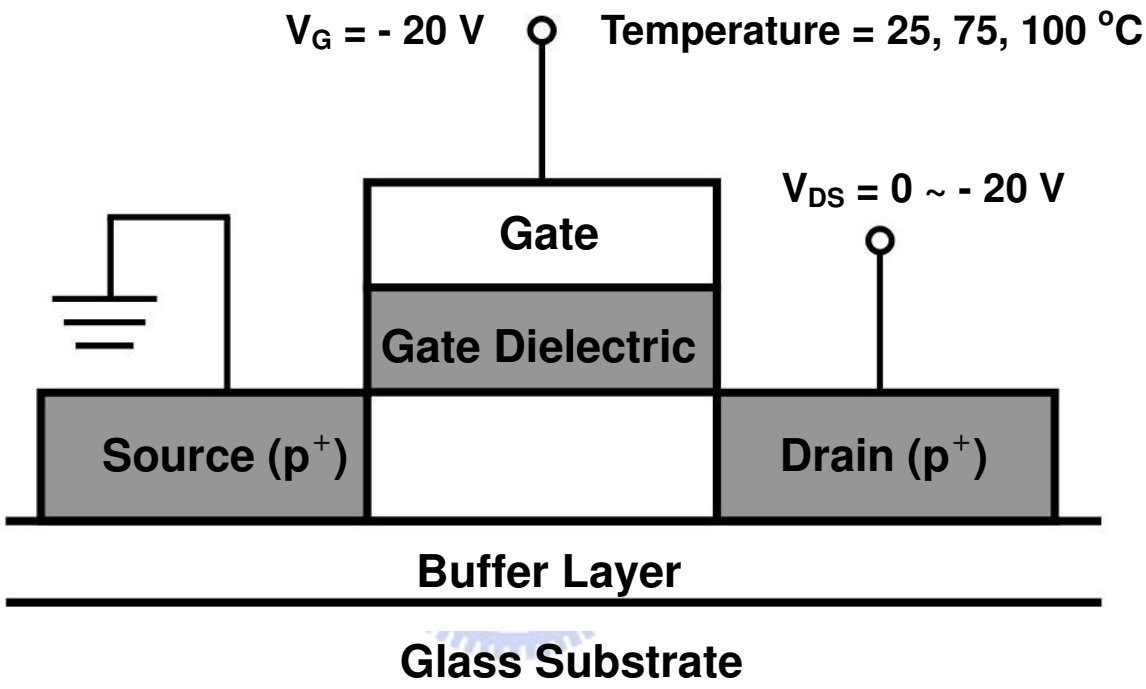
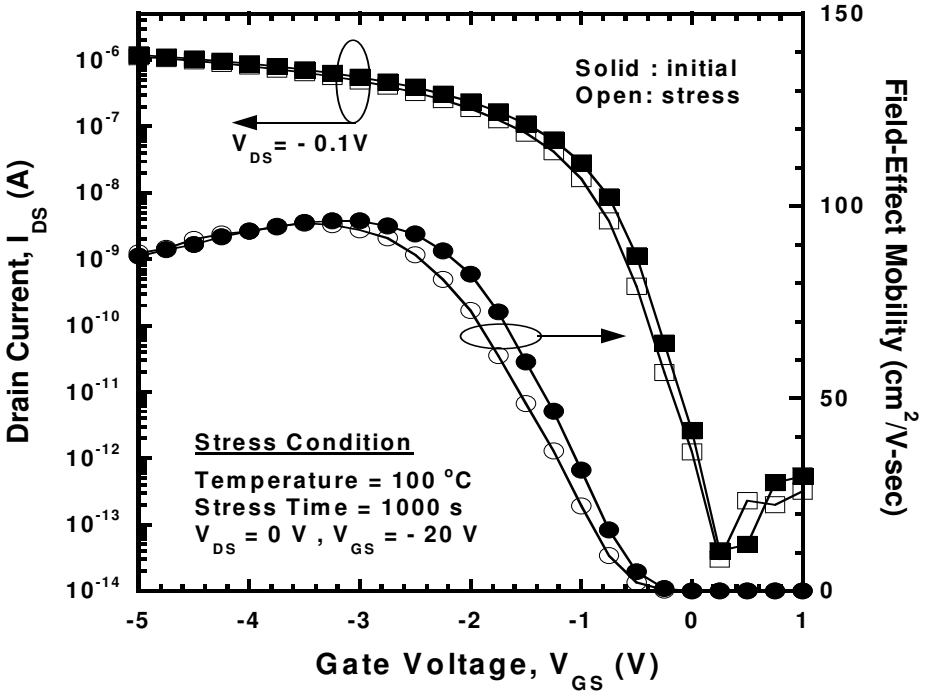
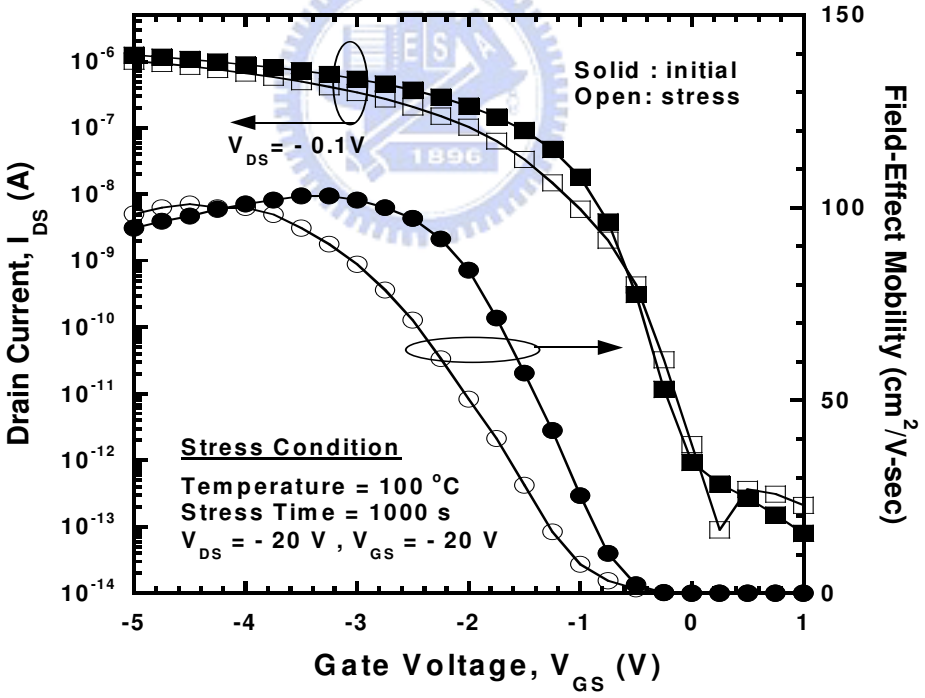


Fig. 6.1 Schematic cross-sectional diagram of the LTPS TFT and stress setup. The stress was performed at various stress temperatures with a stress gate voltage (V_{GS}) of −20 V, and a stress drain voltage (V_{DS}) ranging from 0 to −20 V.



(a)



(b)

Fig. 6.2 Transfer characteristics of the LTPS TFTs before and after stress. The stress was performed with a stress gate voltage of −20 V, and stress drain voltages of (a) 0 V and (b) −20 V.

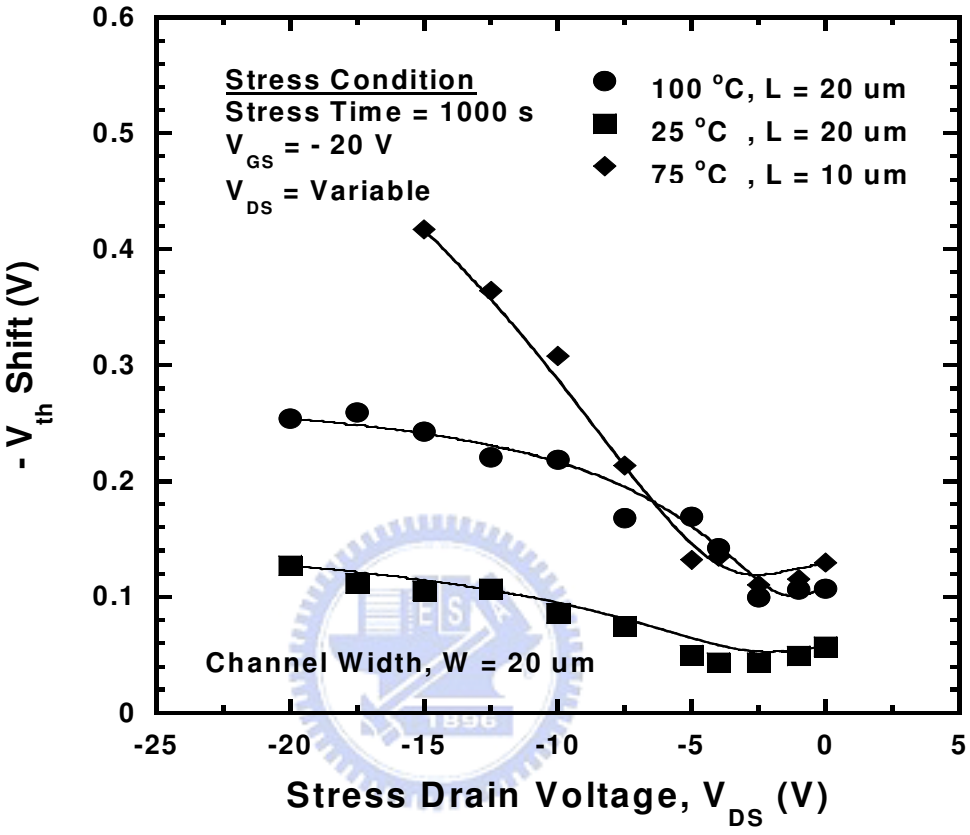


Fig. 6.3 Threshold-voltage shift of the LTPS TFTs after various stress conditions. The stress was performed with a fixed stress gate voltage of −20 V, and a stress drain voltage ranging from 0 to −20 V; the temperature was fixed at 25, 75, and 100 °C.

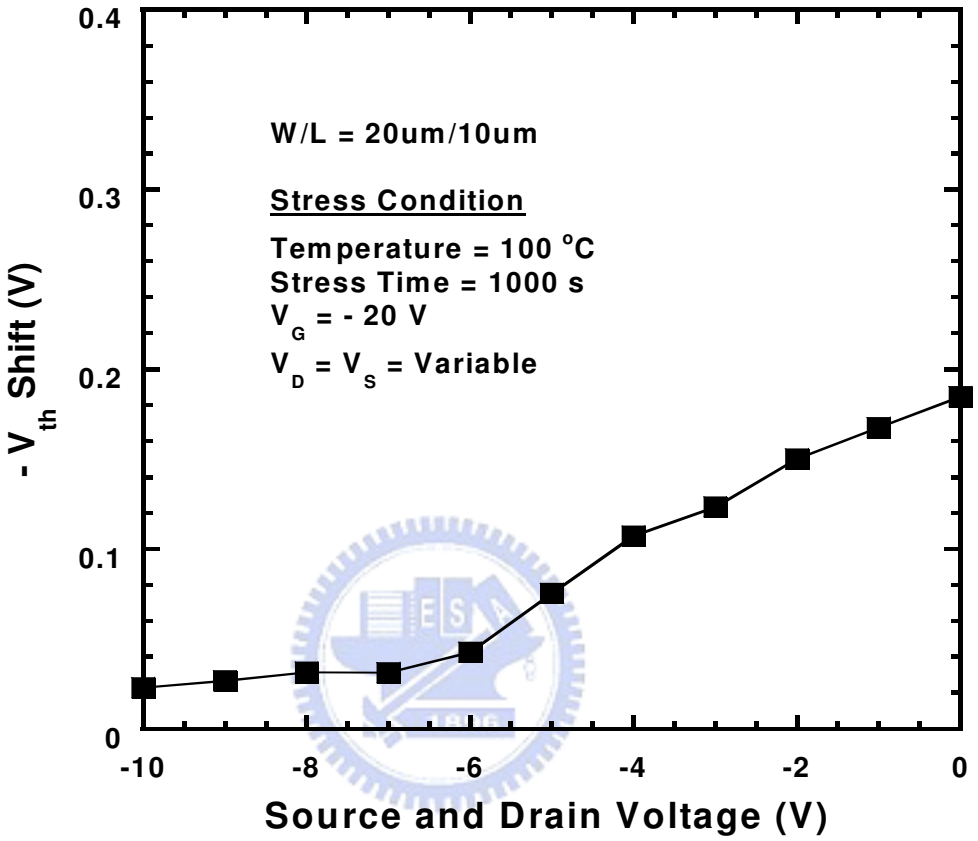
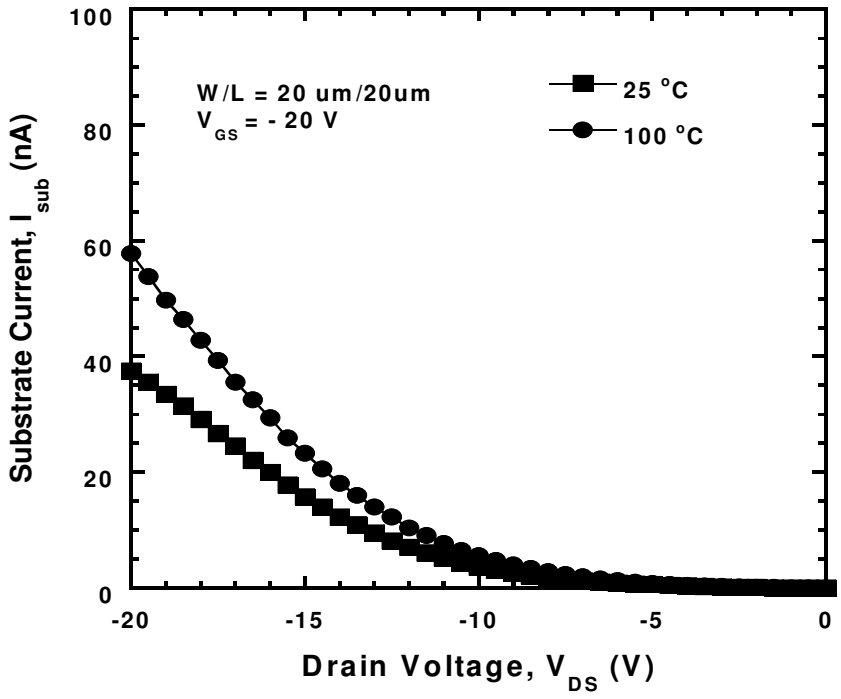
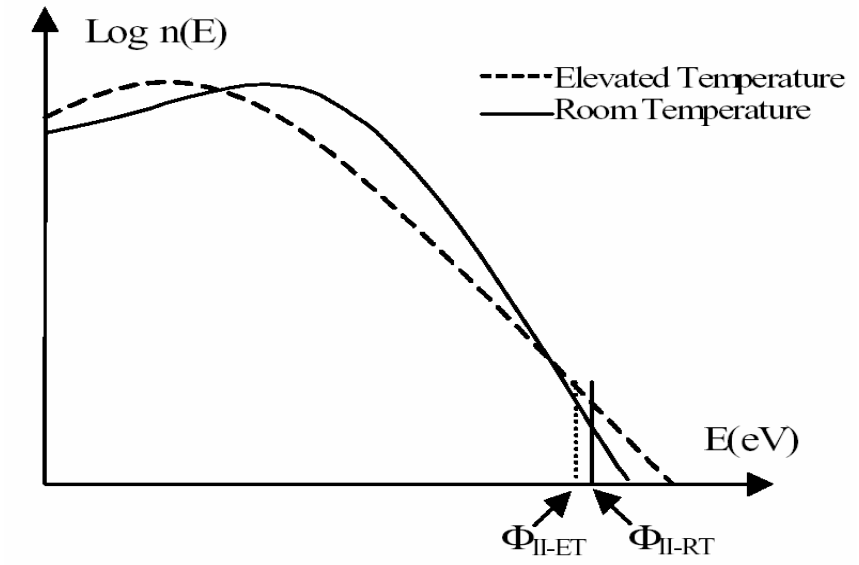


Fig. 6.4 Threshold-voltage shift of the LTPS TFTs after various stress conditions at 100 °C. The stress was performed with a fixed stress gate voltage of -20 V, and $V_D = V_S$ ranging from 0 to -10 V.



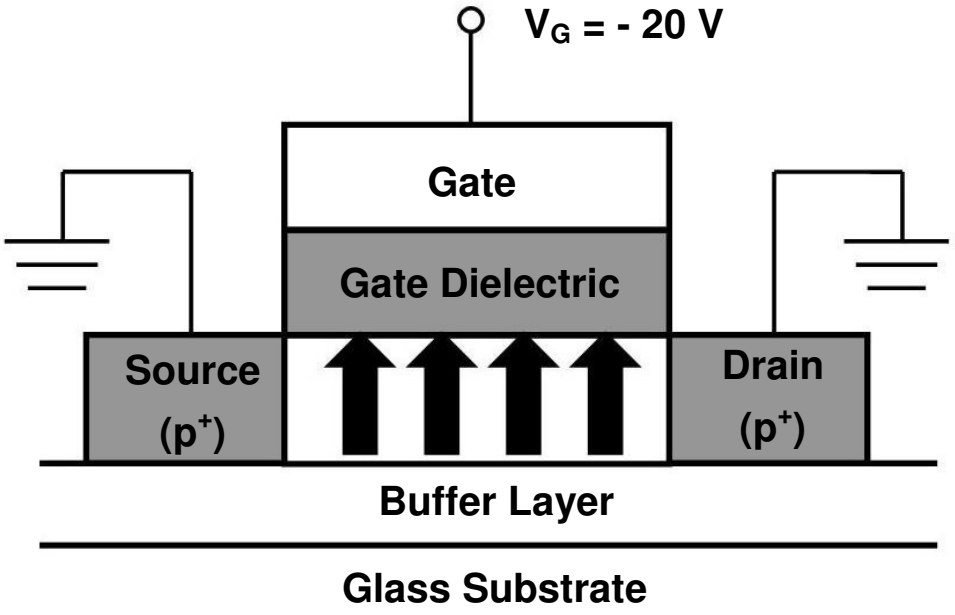
(a)



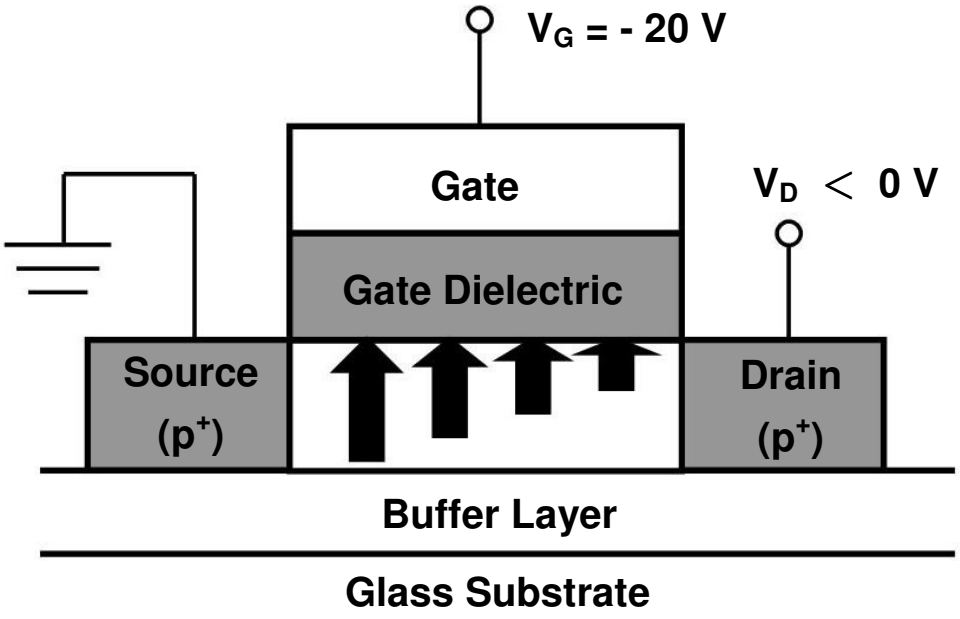
(b)

Fig. 6.5 (a) Substrate current of the LTPS TFT measured at 25 and 100 °C under a fixed stress gate voltage of −20 V, and a stress drain voltage ranging from 0 to −20 V. (b) A simplified sketch of the carrier energy distribution near the drain-end at room temperature and an elevated temperature.

(Ref. Li *et al.*, in *Proc. IEEE Int. Reliab. Phys. Symp.*, 2000.)



(a)



(b)

Fig. 6.6 Schematic diagrams illustrating the vertical-electric field (a) when the stress drain voltage is grounded and (b) when a negative voltage is applied on the drain.

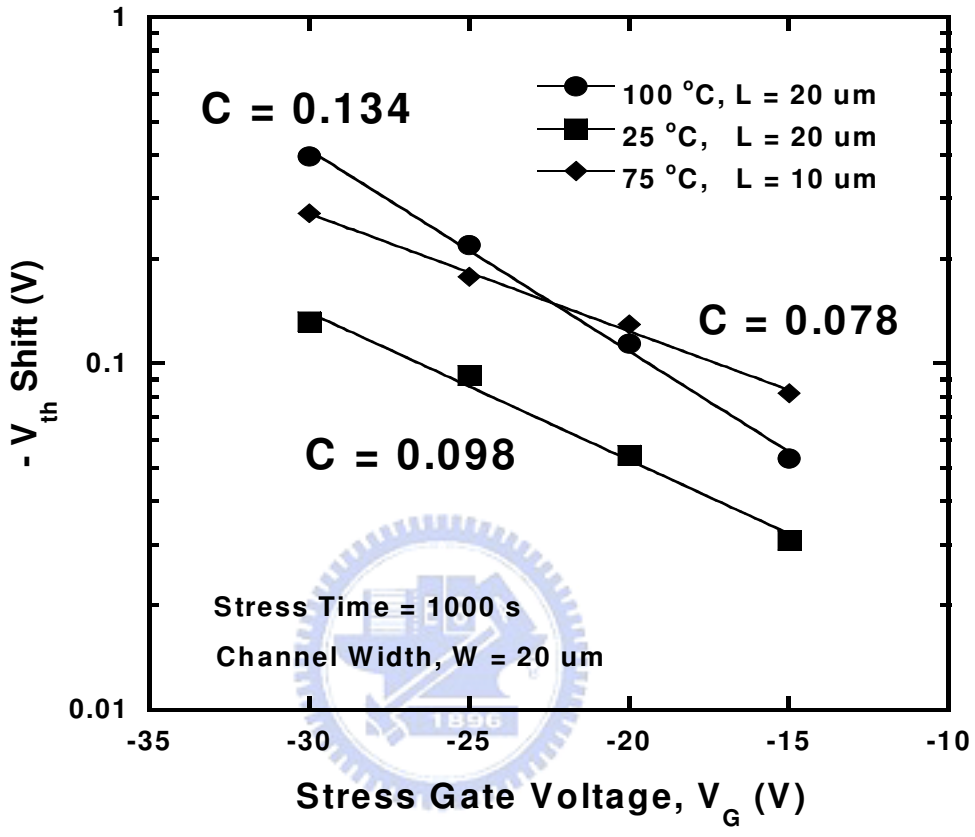
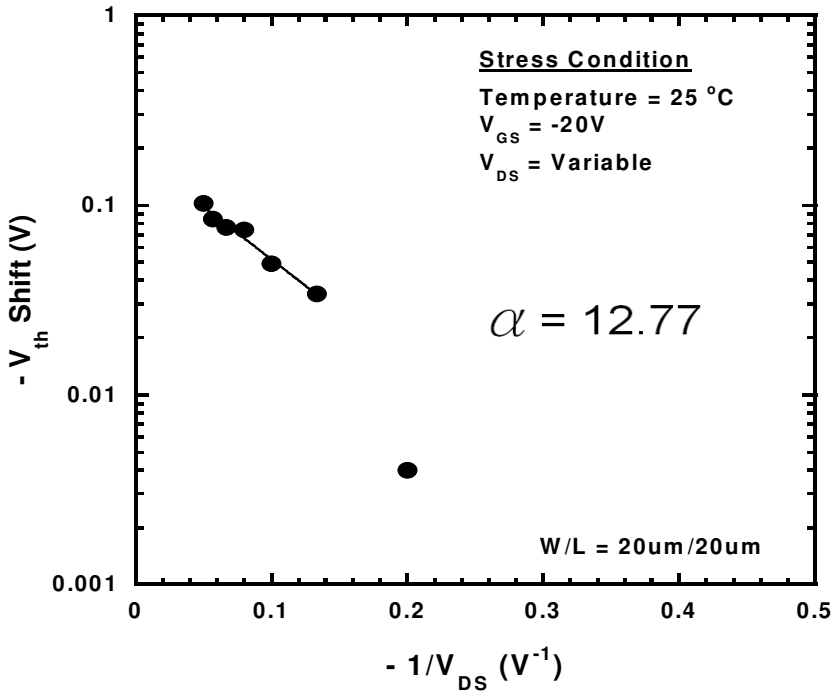
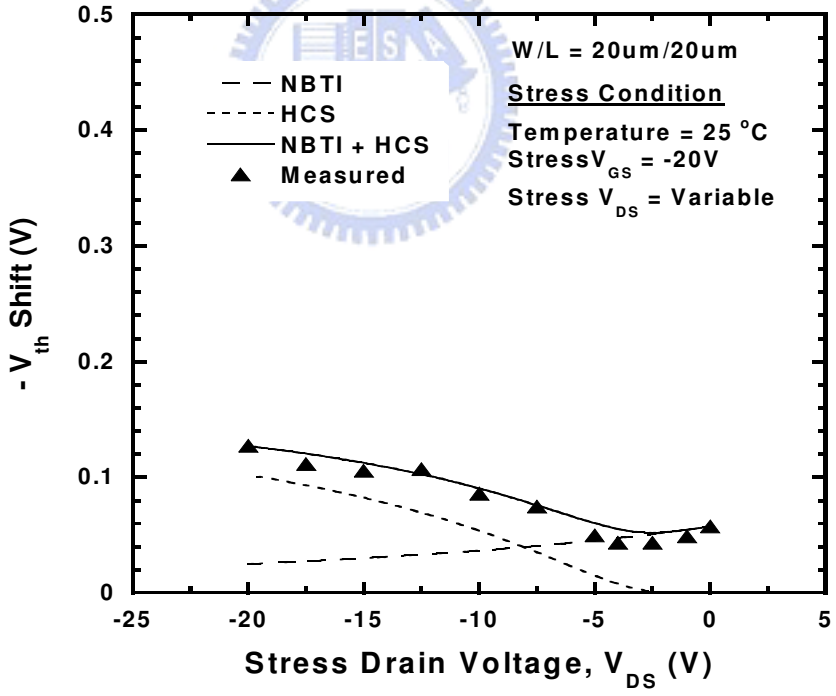


Fig. 6.7 Extraction of the parameter *C* from the fitting of the threshold-voltage shift and the stress voltage.

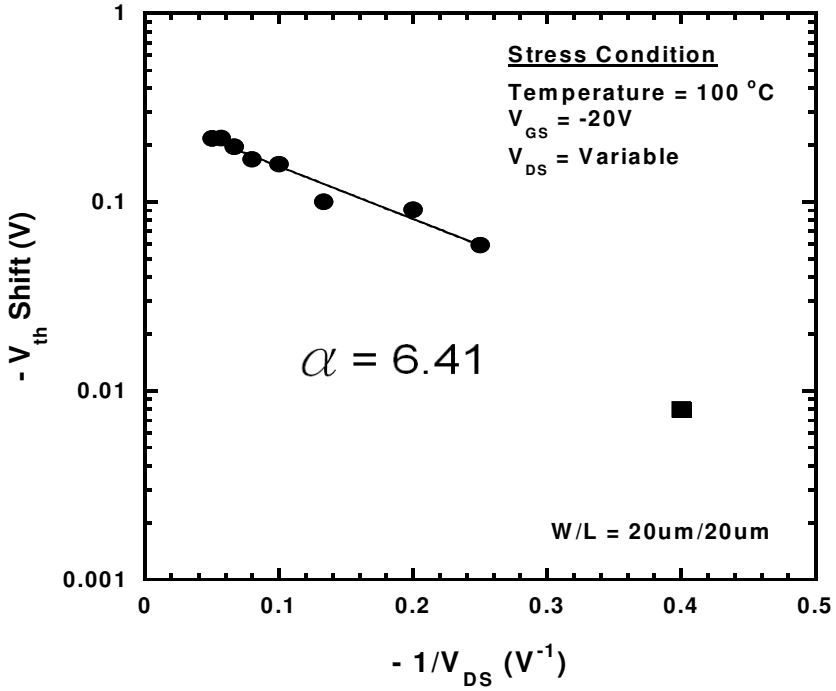


(a)

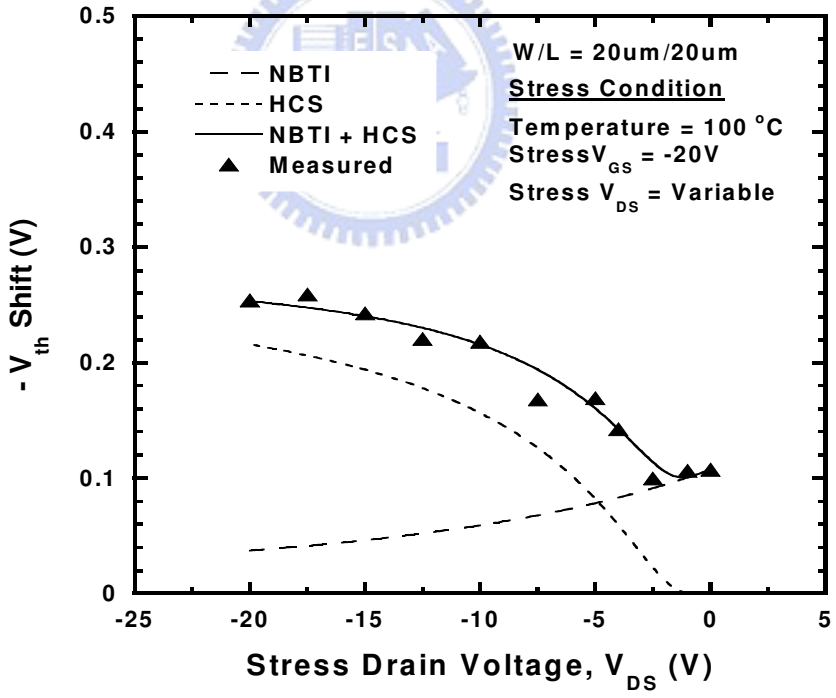


(b)

Fig. 6.8 Correlation between the threshold-voltage shift and $1/V_{DS}$ of the device (W/L = 20μm/20μm) stressed at 25 °C, and (b) comparison of the measured data with the predicted NBTI and HCS effects.

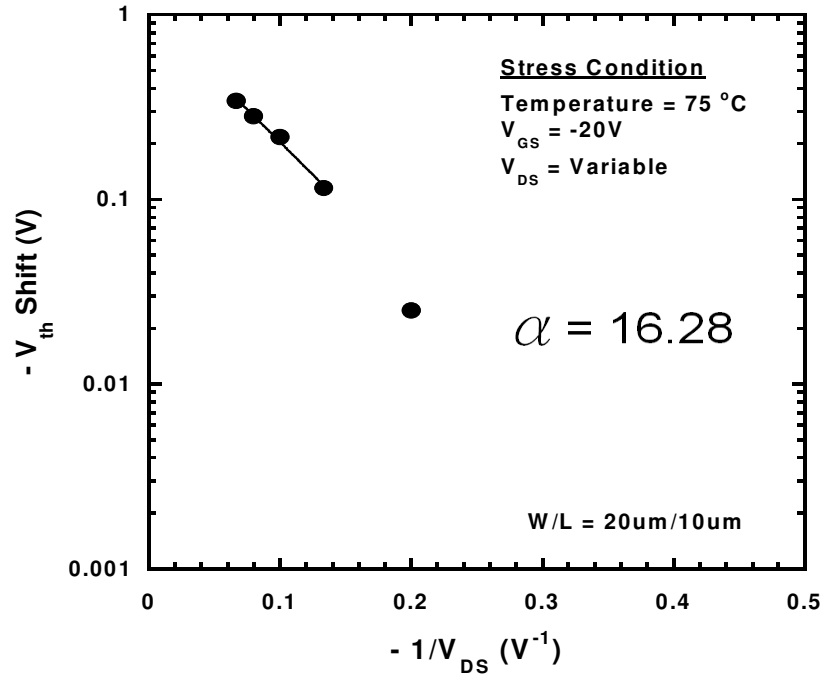


(a)

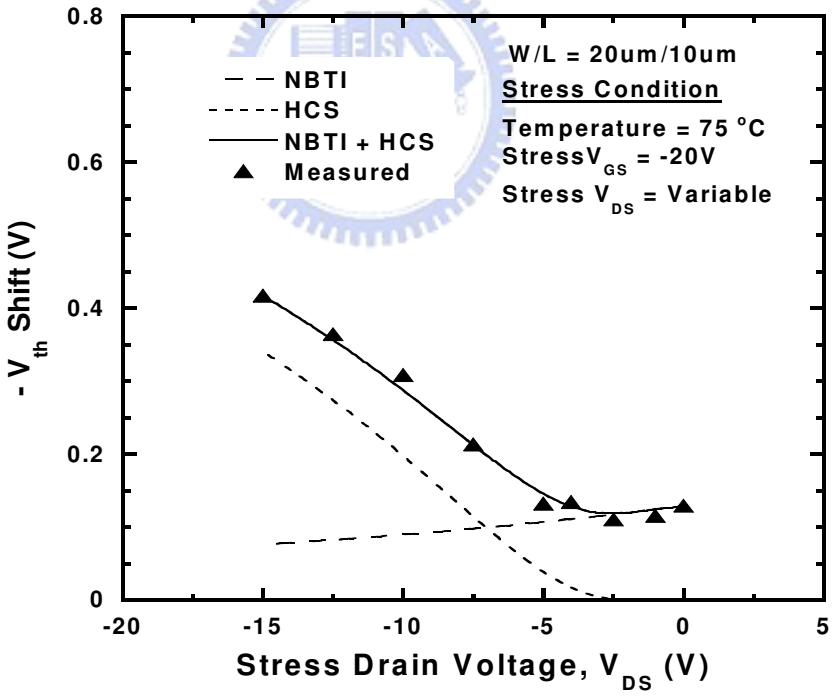


(b)

Fig. 6.9 Correlation between the threshold-voltage shift and $1/V_{DS}$ of the device (W/L = 20μm/20μm) stressed at 100 °C, and (b) comparison of the measured data with the predicted NBTI and HCS effects.

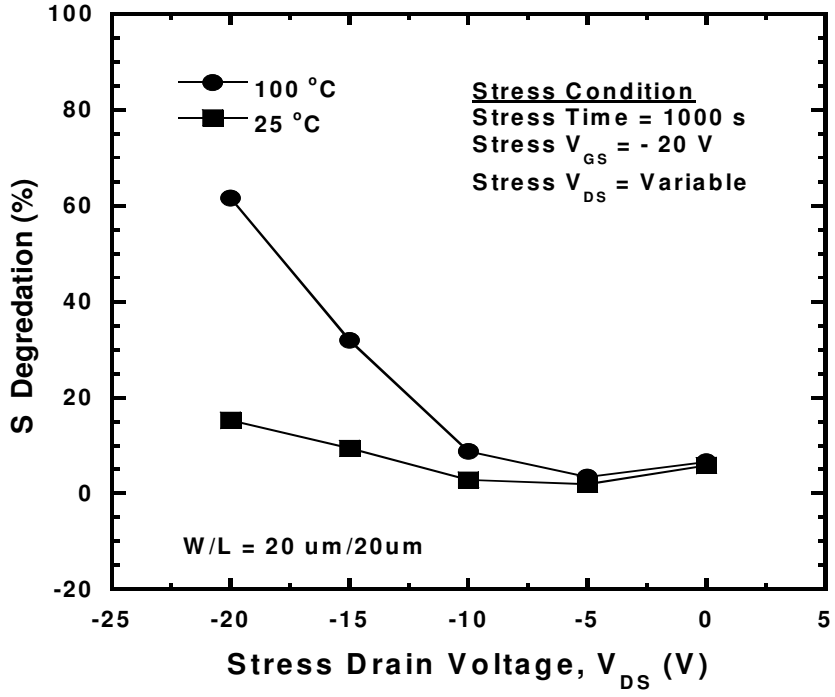


(a)

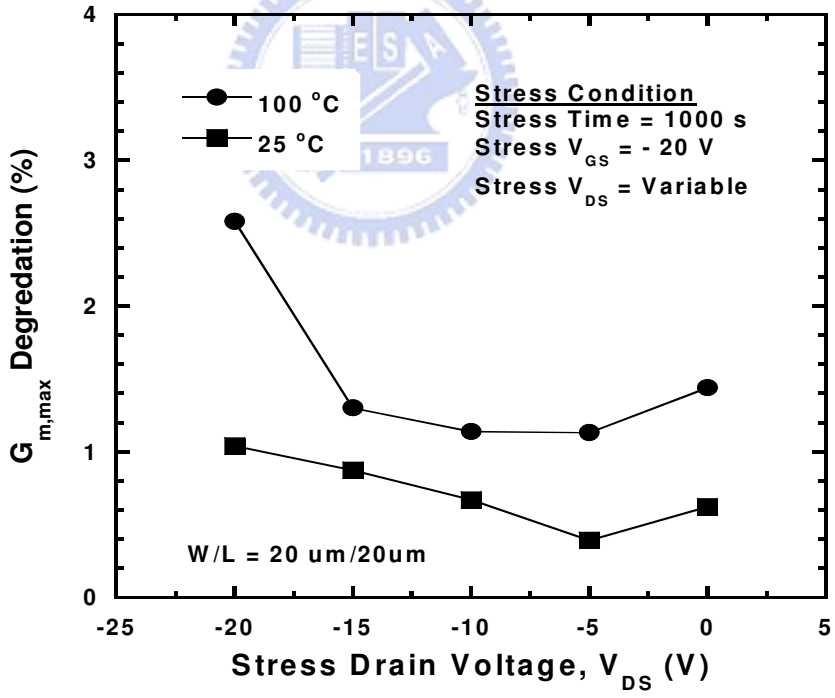


(b)

Fig. 6.10 Correlation between the threshold-voltage shift and $1/V_{DS}$ of the device (W/L = 20μm/10μm) stressed at 75 °C, and (b) comparison of the measured data with the predicted NBTI and HCS effects.



(a)



(b)

Fig. 6.11 Degradation of the (a) subthreshold swing (*S*) and (b) maximum transconductance as a function of the stress drain voltage with a fixed stress gate voltage of −20 V.

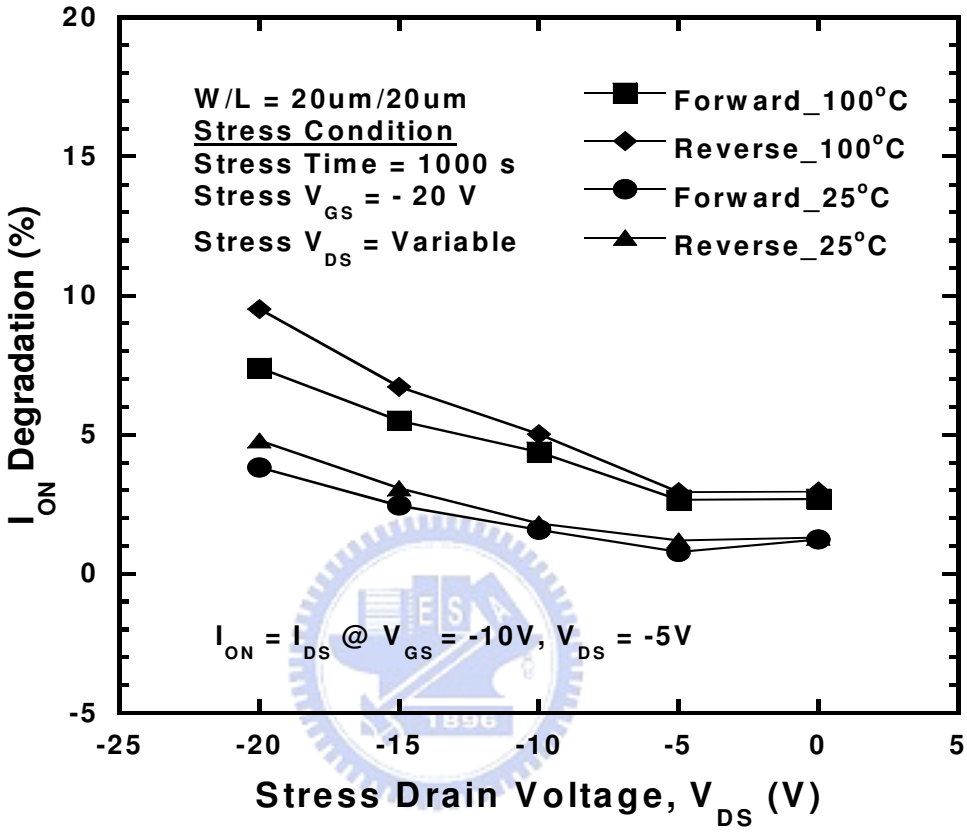


Fig. 6.12 Degradation of the drive current as a function of the stress drain voltage with a fixed stress gate voltage of −20 V for the devices having a channel length of 20 μm.

Chapter 7

Conclusions and Further Recommendations

7.1 Conclusions

Various reliability issues and degradation mechanisms of LTPS TFTs were studied in this thesis, including the NBTI and the antenna effect. Both the NBTI and the antenna effect degrade the performance and reliability of the device. Besides this, the antenna effect is also confirmed to accelerate NBTI degradation. Finally, the drain bias dependence of the threshold-voltage shift under NBTI stress was investigated and a new model was proposed to explain the experimental results. The main results of these studies are summarized below.

In Chapter 2, NBTI effects on *p*-channel LTPS TFTs were thoroughly studied and the degradation mechanism is confirmed from the experimental results. Due to the grain boundaries in the channel film, the NBTI degradation in LTPS TFTs was found to be highly correlated to the generation of grain-boundary trap states, because experimental results show that the threshold-voltage shift and the grain-boundary trap-state generation follow similar power-law dependence on the stress time, and similar exponential dependence on the stress voltage and on the reciprocal of the ambient temperature. The exponent of the power-law dependence on the stress time approximates from 1/3 to 1/4, which can be explained by the diffusion-controlled electrochemical reactions. In addition, the threshold-voltage shift is closely associated with the subthreshold swing degradation, which originates from dangling bond formation. From the experimental results, NBTI degradation in LTPS TFTs can be attributed to the generation of fixed oxide charges, interface trap states, and grain-boundary trap states. Furthermore, during the stressing-passivation-stressing process, the recovery of

the threshold voltage is found to have similar power-law dependence on the stress time as on the threshold-voltage shift. Therefore, the threshold-voltage recovery can be explained by the reverse processes of the diffusion-controlled electrochemical reactions.

In Chapter 3, for the first time, the charge-pumping technique is utilized to analyze the NBTI-degradation mechanism in *p*-channel LTPS TFTs. The properties of bulk trap states (including interface and grain-boundary trap states) can be directly characterized from the charge-pumping current. In addition, the increase of fixed oxide charges is also extracted, which has not been quantified in previous studies of NBTI degradation in LTPS TFTs. The experimental results show that both the increases of bulk trap-state density and of fixed oxide charges show similar power-law dependence on the stress time, and similar exponential dependence on the stress voltage and on the reciprocal of temperature. Furthermore, these two parameters are found to be proportional to the threshold-voltage shift. Therefore, the NBTI degradation in LTPS TFTs can be furthermore confirmed to be caused by the generation of interface trap states, grain-boundary trap states, and fixed oxide charges.

In Chapter 4, the antenna effect on the performance and reliability of LTPS TFTs is studied. Instability of threshold voltages occurs in the LTPS TFTs having relatively large-area antennas presumably because of charge trapping in the gate dielectric during the plasma etching process. The reliabilities of the LTPS TFTs, having larger antenna areas, are found to be more degraded under gate-bias stress and hot-carrier stress than those of the samples having smaller antenna areas. Because of their enhanced plasma damage, LTPS TFTs having larger antenna areas are supposed to possess more trap states in the gate dielectrics. Therefore, during gate bias stress or hot carrier stress, charges can be injected into the gate dielectric through trap-assisted tunneling, resulting in a significant degradation of both the performance and reliability.

In Chapter 5, a NBTI acceleration mechanism in LTPS TFTs is proposed. The experimental results confirm that the mechanism traditionally found in thin gate-oxide

devices do indeed also enhance the NBTI degradation in LTPS TFTs; which exhibits the fact that LTPS TFTs with a larger antenna area ratio under NBTI stress will have a higher degradation in the threshold voltage, subthreshold swing, field-effect mobility, and drive current. By extracting the related device parameters, the enhanced NBTI degradation was proven to be mainly attributed to the accelerated generation of interface states, grain-boundary trap states and fixed oxide charges. It could be concluded that antenna effect will strongly accelerate the NBTI degradation and should be avoided for LPTS TFT circuitry designs.

In Chapter 6, a reliability model was proposed that successfully introduces both the physical mechanisms of NBTI and the HCS for *p*-channel LTPS TFTs. The voltage of stress drain bias was introduced into the conventional NBTI degradation model to develop a drain-bias-modulated NBTI degradation model. By combining the drain-bias-modulated NBTI degradation model and the HCS model, the drain bias dependence of the threshold-voltage shift under NBTI stress can be predicted. The significant feature of the reliability model is that the threshold-voltage shift exhibits two degradation regimes: in the low-stress drain-voltage regime, the device degradation is dominated by NBTI; after that, the HCS dominates the degradation mechanism in the high-stress drain-voltage regime. The model provides a comprehensive way to predict the lifetime of *p*-channel LTPS TFTs, which is especially necessary for SOP circuitry design.

7.2 Further Recommendations

There are some interesting and important topics about LTPS TFTs that are worthy to be further investigated:

(1) As described in Chapters 1, 2 and 3, NBTI is an important reliability issue of LTPS TFTs especially for SOP applications. Although details of the degradation mechanism were

studied in this thesis, the process effects on the NBTI behaviors have not been discussed. Hydrogen passivation has been widely adopted for the fabrication of LTPS TFTs to passivate the silicon dangling bonds and improve the device performance; however, the dissociation of the hydrogen atoms from the Si—H bonds is the origination of the NBTI degradation. Therefore, different passivation methods such as the incorporation of fluorine or deuterium could be done to study the process effects on the NBTI degradation.

(2) In this thesis, the study of NBTI degradation is based on DC voltage stressing; that is, on a constant negative bias applied to the gate electrode of a LTPS TFT at an elevated temperature with source and drain grounded. However, during circuit operations, the applied gate voltage is a pulse voltage switching between "high" and "low" voltages. Therefore, the dynamic NBTI degradation, taking into account the transient effects, is a topic worthy to be investigated. Besides, the scaling down of the LTPS TFT size is the future trend for the driving circuit application. The dependence of the NBTI degradation of LTPS TFTs on the gate length or channel width is therefore recommended to be studied.

(3) In Chapter 4, the antenna effect was studied for *n*-channel LTPS TFTs. It is worthy to further investigate the impacts of antenna effects on the performance and hot-carrier immunity of *p*-channel LTPS TFTs. Antenna structures with different peripheral ratio can also be studied, and the influence of area ratio and peripheral ratio can be compared. Furthermore, protection structures such as protection diodes can be used to study their impacts on the antenna effect.

(4) During the circuit operation of LTPS TFTs, NBTI occurs in *p*-channel TFTs while PBTI takes place in *n*-channel TFTs. Our studies mainly focus on the NBTI of *p*-channel LTPS TFTs and the related degradation mechanism. However, until now, the effects of PBTI on *n*-channel LTPS TFTs have not been investigated. Therefore, it is recommended that the

effects of PBTI and the related degradation mechanism should be thoroughly studied. Besides, the impacts of the antenna effect on PBTI behaviors can also be studied. In Chapter 6, the drain-bias-modulated NBTI effect was also studied, and a reliability model is proposed; we think it is worthy to investigate the drain bias dependence of the PBTI degradation in *n*-channel LTPS TFTs in order to develop a unified reliability model for both *p*- and *n*-channel LTPS TFTs.

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論文題目: 低溫複晶矽薄膜電晶體負偏壓溫度不穩定與天線效應之研究

Study on Negative Bias Temperature Instability and Antenna Effect of Low-Temperature Polycrystalline Silicon Thin-Film Transistors

Publication Lists

1. International Journal:

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