國立交通大學

電子工程學系電子研究所碩士班

碩士論文

新穎的金氧半電晶體雜訊模型與應用於超寬頻系統低雜訊放大器之設計

Novel Noise Modeling of RF MOSFETs and the Design of an UWB LNA with Modified L-degenerate Input Matching

研究生: 賴照民

指導教授: 荊鳳德 博士

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摘要

我們已經發展出新穎的微帶線結構用來直接量得 NFmin 而不需要複雜的校正手續(de-embedding)，以取代傳統的 CPW 結構。在 10GHz、0.18μm MOSFET 8 gate fingers 條件下，非常低的 NFmin，0.9dB，可以直接量測得而不需要任何的校正。在精準的雜訊量測結果為基準下，我們發展出新穎的金氧半電晶體雜訊模型可以來預測元件的雜訊表現與特性。此外，我們修改了窄頻低雜訊放大器所使用的源極電感回授匹配方式，並且將它應用於設計超寬頻低雜訊放大器。該放大器採用台積電 0.18 微米製程，在 3~10GHz 的範圍裡達到輸入與輸出的阻抗匹配並提供 10dB 的功率增益。在 1.8V 的供應電壓下消耗 27mW 的功率，而第一級放大及僅銷耗 15mW。在這篇論文中，我們將會說明如何修改源極電感回授匹配及其原理，以及如何將之應用於超寬頻低雜訊放大器中。

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Student: Zhaomin Lai **Advisor: Dr. Albert Chin**

Department of Electronics Engineering

And Institute of Electronics

Nation Chiao Tung University

Abstract

A novel micro-strip line layout is developed to direct measure the min. noise figure (NFmin) accurately instead of the complicated de-embedding procedure in conventional CPW line. Very low NFmin of 0.9 dB at 10 GHz is directly measured in 8 gate fingers 0.18μm MOSFETs without any de-embedding. Based on the accurate NFmin measurement, we have developed the novel NFmin model to predict device noise characteristics. Besides, we also designed an UWB LNA with Modified Source L-degenerate by using TSMC 0.18μm technology. The LNA provides a forward gain (S_{21}) of 10dB over the 3 ~ 10 GHz range with a low noise figure of 3.5dB (at 6 GHz) while consuming 27mW from 1.8V power supply. To achieve its wide-band characteristics, a novel input matching mechanism is proposed, which modifies L-degenerate approach for the wide-band matching. We will present a detail analysis of this LNA architecture.

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2.2 Noise Analysis

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Chapter 4 UWB LNA Design

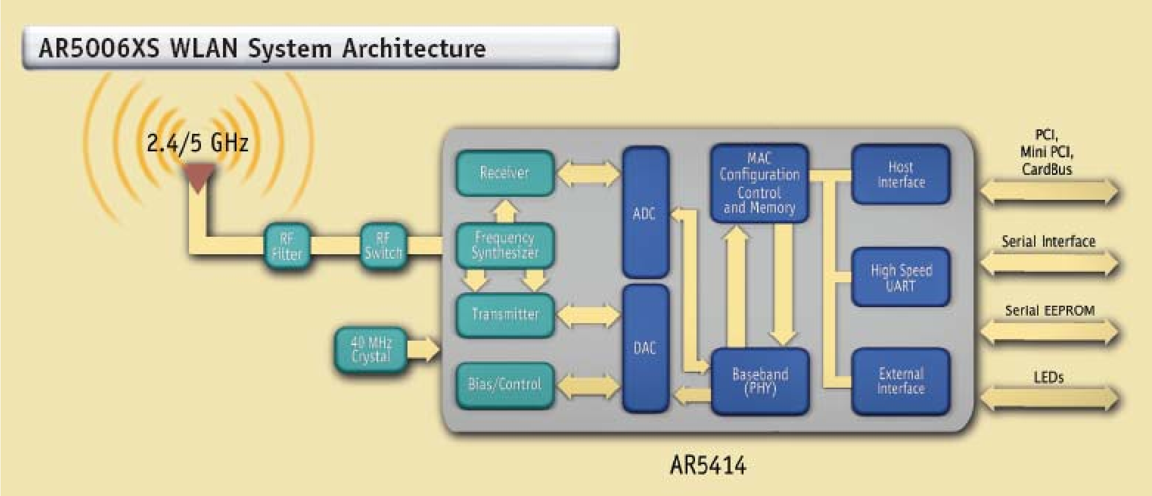
Figure Caption

I. Introduction

Si RF MOSFETs [1]-[5] are now widely used for wireless communication due to the continuously improved RF noise and high frequency gain with technology downscaling evolution. The increasing operation frequency to higher band with wider bandwidth is the technology trend for communication system. The demand of high performance low noise MOSFET becomes more urgent for ultra-wide band (UWB) (3.1-10.6 GHz) beyond current W-LAN (5.2-5.8 GHz), since the noise also increases monotonically with increasing frequency. However, accurate RF noise modeling of the nm-scale MOSFETs is challenging due to the limited understanding of noise sources and the large parasitic effect from low resistance Si substrate [5]-[7]. Another problem for the nm-scale MOSFET is the large gate resistance where a parallel multiple gate fingers layout is used to reduce the Rg generated thermal noise [5]. Unfortunately, the consumed DC and RF power also increase with increasing finger number that is contradictory to the low power trend.

To accurately model the MOSFETs noise performance, in this paper we first developed a novel micro-strip line layout that can directly measure the NFmin with good accuracy. Very low as-measured NFmin of 0.9 dB is measured at 10 GHz in 8 gate fingers 0.18μm MOSFETs without any de-embedding, where the new micro-strip line design was used to screen out the RF noise generated by the resistance from low resistance Si substrate. Such low NFmin is comparable with de-embedded 0.13 μm node MOSFETs (80 nm gate length) [3]-[4].

At RF frequencies, the MOSFET 1/f noise becomes negligible and thermal noise is the dominant source of noise. The topic of this paper is about the high frequency thermal noise of RF MOSFETs. Thermal noise is due to the random thermal motion of charge carriers. It not only manifests itself in the drain current noise spectrum, but due to the capacitive coupling between channel and gate, also in the gate current noise spectrum. In the next section, we will analyze the mechanism of the noise sources of MOSFETs, and derive many theoretically equations about the RF MOSFETs noise performance. In the section three, we will extract the important noise coefficients, like the correlation factor *c* and γ, from our accurate measurement and further develop our noise model of RF MOSFETs. Then, the forth section, is the second major topic about the UWB LNA design. We will represent how to achieve wideband matching by modified the famous source L-degenerate which can make good input matching and also yield nearly optimal noise figure at the response frequency in narrow band LNA. Finally, in the section five, we will summarize a conclusion to our study.



Total 801.11 a/b/g single chip by CMOS.

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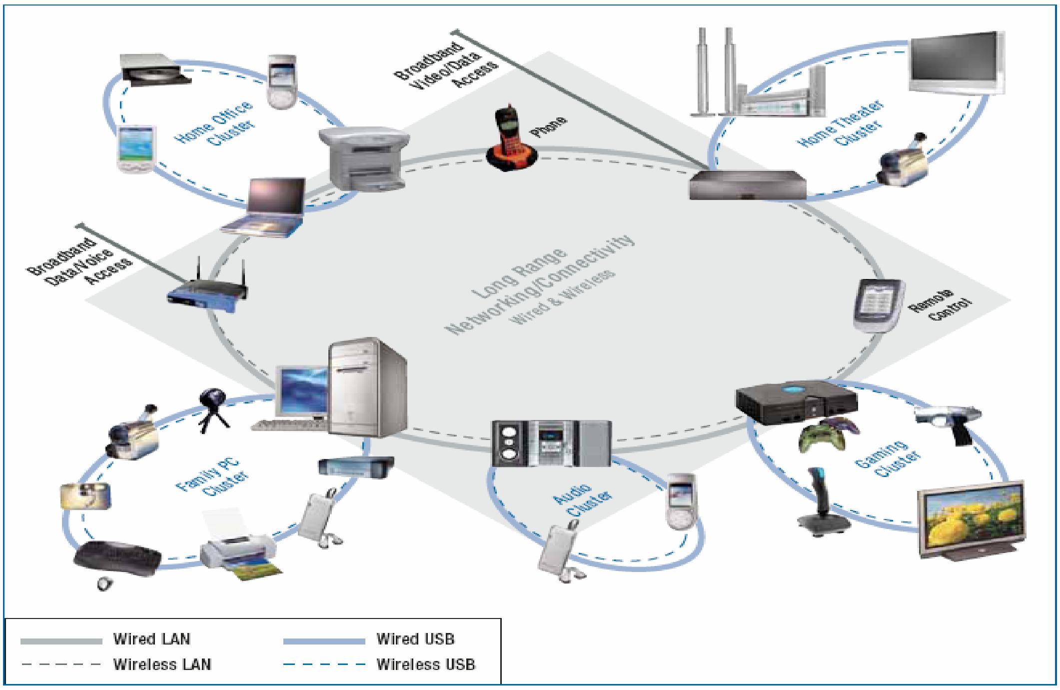

Figure 1. Home usage scenarios that could be "unwired" with Wireless USB.

UWB applications.

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II. Thermal Noise in MOSFETs

2.1 Noise Sources in MOSFETs

（a）Drain Current Noise

There are three main sources which contribute the thermal noise of MOSFETs [8]. And the dominate noise source of RF MOSFETs is the drain current noise which is expressed as:

$$\overline{i_{nd}^{2}} = 4KT\gamma g_{d0}\Delta f$$

where g_{d0} is the drain-source conductance at zero V_{DS}. The coefficient γ has a vale of unity at zero V_{DS} and, in long channel devices, decrease toward a value of 2/3 in saturation [9]. Some measurements show that short-channel devices exhibit noise considerably in excess of values predicted by long-channel theory, sometimes by an order of magnitude in extreme cases. Some of the literature attributes this excess noise to carrier heating by the large electric fields commonly encountered in such devices. In this view, the high fields produce carriers with abnormally high energies. No longer in quasi-thermal equilibrium with the lattice, these hot carriers produce abnormal amount of noise. But in contrast to other groups, we find only a moderate enhancement of the drain current noise for short-channel MOSFETs by our good measurements. The details will be illustrated in the section three.

（b）Substrate Thermal Noise

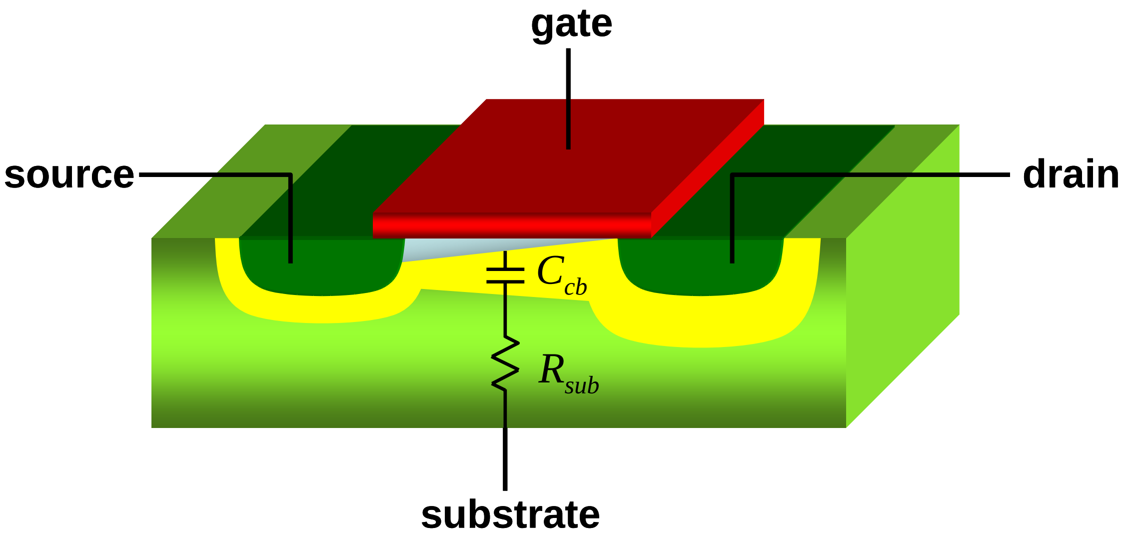


Figure 1 Substrate thermal noise.

Figure 1 shows a simplified picture of how the thermal noise associated with the substrate resistance can produce measurable effect at the main terminals of the devices. At frequencies low enough that we may ignore C_{cb} (open), the thermal noise of R_{sub} modulates the potential of the back gate, contributing some noisy drain current:

$$\overline{i_{nd,sub}^{2}} = 4KTR_{sub}g_{mb}^{2}\Delta f$$

Depending on bias conditions – and also on the magnitude of the effective substrate resistance and size of the back-gate transconductance – the noise generated by this mechanism may actually exceed the thermal noise contribution of the ordinary channel charge. In this regime, layout strategies that reduce the substrate resistance have a noticeable and beneficial effect on noise.

At frequencies well above the pole formed by C_{cb} and R_{sub}, however, the substrate thermal noise becomes unimportant, as is readily apparent from inspection of the physical structure and the corresponding frequency-dependent expression for the substrate noise contribution [9]:

$$\overline{i_{nd,sub}^2} = \frac{4KTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{cb})^2}\Delta f$$

The characteristics of many IC processes are such that this pole is often around 1 GHz. Excess noise produced by this mechanism consequently will be most noticeable below about 1 GHz.

（c） Drain Induced Gate Noise

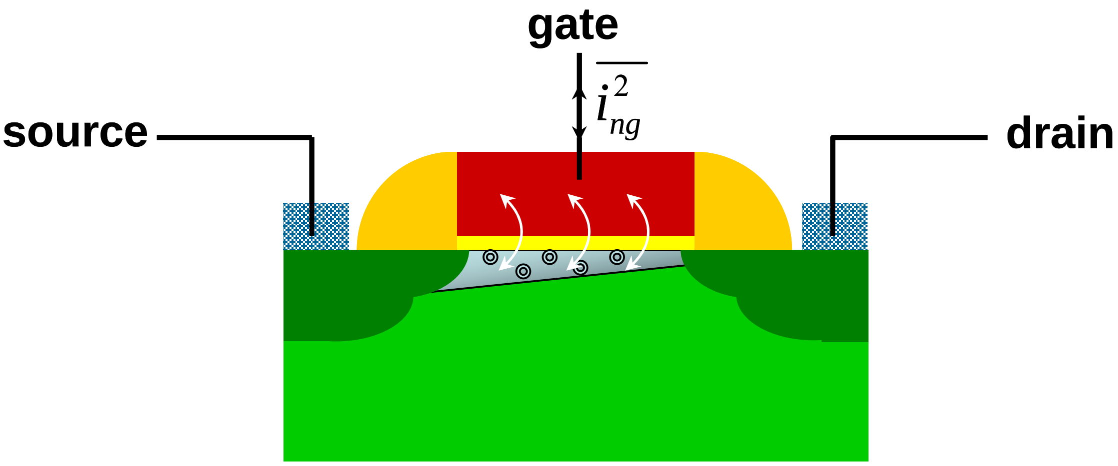


Figure 2 Drain induced gate noise.

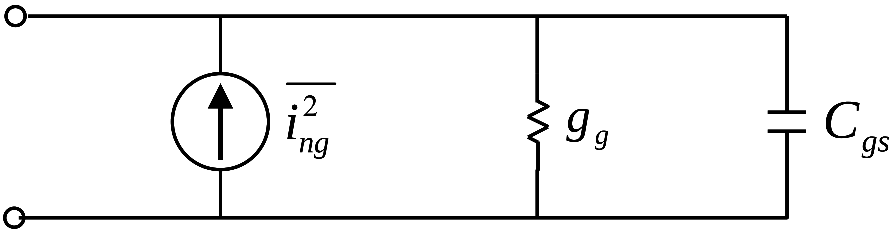


Figure 3 Equivalent circuits.

In addition to drain noise, the thermal agitation of channel charge has another important consequence: gate noise. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current (see figure 2). Noisy gate current may also be produced by thermally noisy resistive gate material. But this noise source will be separately discussed later, even though it is more and more important in nano-scale devices. Although the drain-induced-gate-noise is negligible at low frequencies, it can dominate at radio frequencies. Van der Ziel has shown that the drain-induced-gate-noise may be expressed as:

$$\overline{i_{ng}^2} = 4KT\delta g_g \Delta f$$

where the parameter g_g is:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}}$$

Van der Ziel gives a value of 4/3 (twice γ) for the gate noise coefficient, δ, in long channel devices [9].

The circuit model for the drain-induced-gate-noise is a conductance connected between gate and source, shunted by a noise current source (see figure 3). This noise current clearly has a spectral density that is not constant. In fact, it increases with frequency, so perhaps it ought to be called "blue noise" to continue the optical analogy. Because the drain thermal current noise and the drain-induced-gate-noise do share a common origin, they are correlated. That is, there is a component of the gate noise current that is proportional to the drain noise current on an instantaneous basis.

Although the noise behavior of long-channel devices is fairly well understood, the precise behavior of δ and γ in the short-channel regime is still unknown at present. That's why we have to do more research on the thermal noise of MOSFETs. Thermal noise of deep sub-micrometer MOSFETs has received considerable attention lately, which is mainly triggered by publications that report a severe enhancement of the thermal noise with respect to long-channel theory [10]–[14]. In the earliest of these publications [10], thermal noise was found to be enhanced by a factor up to 12 in n-channel devices with 0.7μm gate length and hot electrons were proposed to explain these results. Evidently, the reported noise enhancements would seriously limit the viability of RF CMOS and a detailed study is called for. Therefore, in this paper, we perform an extensive study of the RF noise in 0.18μm RF CMOS technology.

2.2 Noise Analysis

2.2.1 Review

To analyze the relationship between noise performance and the characteristics of MOSFETs, we have derived the NFmin based on the intrinsic MOSFETs with additional Rg and following the procedure in reference [3]:

$$\frac{\overline{v_i^{\,2}}}{\Delta f} = 4kT\gamma\frac{1}{g_m} + \frac{K_f}{WLC_{ox}f} + 4kTR_g \cong 4kT\left(\frac{\gamma}{g_m} + R_g\right) \tag{1}$$

$$\frac{\overline{i_i^{\,2}}}{\Delta f} = 2qI_G + \frac{\omega^2 C_{gs}^2}{g_m^{\,2}}\left(4kT\gamma g_m + K\frac{I_D}{f}\right) \cong 4kT\omega^2 C_{gs}^2\frac{\gamma}{g_m} \tag{2}$$

$$NF = 1 + \frac{\overline{v_i^{\,2}}}{4kTR_S\Delta f} + \frac{\overline{i_i^2}}{4kT\frac{1}{R_s}\Delta f} = 1 + \frac{1}{R_S}\left(\frac{\gamma}{g_m} + R_g\right) + R_s\omega^2 C_{gs}^2\left(\frac{\gamma}{g_m}\right) \tag{3}$$

$$R_{s(opt)}^2 = \frac{\overline{v_i^2}}{\overline{i_i^2}} \tag{4}$$

$$NF_{\min} \approx 1 + 4\pi f\frac{C_{gs}}{g_m}\sqrt{\gamma^2 + \gamma\cdot g_m R_g} = 1 + 2\gamma\frac{f}{f_t}\sqrt{1 + g_m R_g/\gamma} \tag{5}$$

In above equations, the 1/f terms are neglected due to high RF frequency. The γ is the proportional constant of the drain current noise, which was previously attributed to hot electron effect in short channels. The derived NFmin in equation (5) has exactly the same dependence of f, Cgs and gm with Fukui's experimental equation [15] for GaAs FETs that suggests the good accuracy of the derived equation.

But the noise equations which we derive just before still have some loss and unreasonable parts. Those are the “lacking of drain-induced-gate-noise” and the “wrong optimized source impedance - Y_{opt}”. We did not account the drain-induced-gate-noise in the noise sources. And the Y_{opt} is also incorrect since it has merely the real part, which is inconsistent with usual measurements. We will fix the bugs and further enhance the accuracy of our noise equations, but we need to do more study on noise theory, two-port noise theory at first.

2.2.2 Two-port noise theory

The noise factor is defined as:

$$F \equiv \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} \tag{6}$$

The noise factor is a measure of the degradation in signal-to-noise ratio that a system introduces. The larger the degradation, the larger the noise factor. If a system adds no noise of its own then the total output noise is due entirely to the source, and the noise factor is therefore unity.

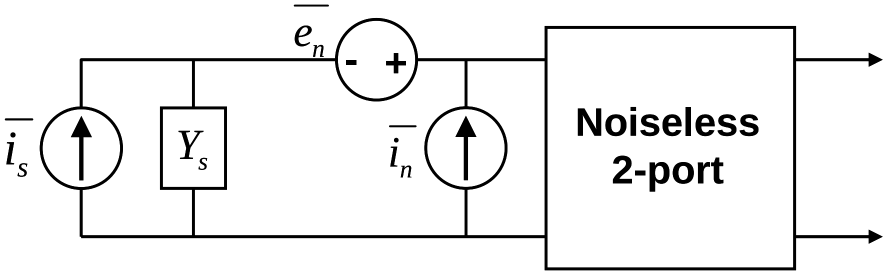


Figure 4 Equivalent noise model.

In the model of figure 4, all of the noise appears as input to the noiseless network, so we may compute the noise figure there. A calculation based directly on Eqn. 6 requires the computation of the total power due to all of the sources, and dividing that result by the power due to the input source. An equivalent and simpler method is to compute the total short-circuit mean-square noise current and then divide that total by the short-circuit mean-square noise current due to the input source. This alternative method is equivalent because the individual power contributions are proportional to the short-circuit mean-square current, with a proportionality constant (which involves the current division ratio between the source and two-port) that is the same for all the terms.

In carrying out this computation, one generally encounters the problem of combining noise sources that have varying degree of correlation with one another. In the special case of zero correlation, the individual powers superpose. For example, if we assume, as seems reasonable, that the noise powers of the source and of the two-port are

Uncorrelated, then the expression for noise figure becomes [8]:

$$F = \frac{\overline{i_s^2 + \left| i_n + Y_s e_n \right|^2}}{\overline{i_s^2}} \qquad (7)$$

Note that, although we have assumed that the noise of the source is uncorrelated with the two equivalent noise generators of the two-port, Enq. 7 does not assume that the two-port's generators are also uncorrelated with each other.

In order to accommodate the possibility of correlations between e_n and i_n, express i_n as the sum of two components. One, i_c, is correlated with e_n, and the other, i_u, isn't:

$$i_n = i_c + i_u \tag{8}$$

Since i_c is correlated with e_n, it may be treated as proportional to it through a constant whose dimensions are those of an admittance:

$$i_c = Y_c e_n \tag{9}$$

The constant Y_c is known as the ***correlation admittance***. Combining Eqn. 7, 8, and 9, the noise factor becomes:

$$F = \frac{\overline{i_s^2} + \overline{\left| i_u + (Y_c + Y_s) e_n \right|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_u^2} + \left| Y_c + Y_s \right|^2 \overline{e_n^2}}{\overline{i_s^2}} \tag{10}$$

The expression in Eqn. 10 contain three independent noise sources, each of which may be treated as thermal noise produced by an equivalent resistance or conductance (whether or not such a resistance or conductance actually is the source of the noise):

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} \tag{11}$$

$$G_u \equiv \frac{\overline{i_u^2}}{4KT\Delta f} \tag{12}$$

$$G_s \equiv \frac{\overline{i_s^2}}{4KT\Delta f} \tag{13}$$

Using these equivalences, the expression for noise factor can be written purely in terms of impedances and admittances:

$$\begin{aligned} F &= 1 + \frac{G_u + \left|Y_c + Y_s\right|^2 R_n}{G_s} \\ &= 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s} \end{aligned} \tag{14}$$

where we have explicitly decomposed each admittance into a sum of a conductance G and a susceptance B.

once a given two-port's noise has been characterized with its four noise parameters (G_c, B_c, R_n, and G_u), Eqn. 14 allows us to identify the general conditions for minimizing the noise factor. Taking the first derivative with the respect to the source admittance and setting it equal to zero yield:

$$B_s = -B_c = B_{opt} \tag{15}$$

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \tag{16}$$

Hence, to minimize the noise factor, the source susceptance should be made to equal to the inverse of the correlation susceptance, while the source conductance shoule be set equal to the value in Eqn. 16.

The noise factor corresponding to this choice is found by direct substitution of Eqn. 15 and 16 into Eqn. 14:

$$F_{\min} = 1 + 2R_n(G_{opt} + G_c) = 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c\right] \tag{17}$$

Thus, contours of constant noise factor are non-overlapping circles in the admittance plane.

It is important to recognize that, although minimizing the noise factor has something of the flavor of maximizing power transfer, the source admittance leading to these condition are generally not the same – as is apparent by inspection of Eqn. 15 and 16. For example, there is no reason to expect the correlation susceptance to equal to the input susceptance (except by coincidence). As a consequence, one must generally accept less than maximum power gain if noise performance is to be optimized, and vice versa.

2.2.3 Further analysis

Now, we start to derive the new noise equations of the relationship between noise performance and the characteristics again. Recall that the MOSFETs noise model consists of two generators. The mean-square drain current noise from the thermal current noise and the substrate thermal noise is:

$$\overline{i_{nd}^2} = 4KT\gamma g_{d0}\Delta f + \frac{4KTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{cb})^2}\Delta f \tag{18}$$

We will ignore the second term of the drain thermal current noise since it will drop quickly at the high frequencies range.

The drain-induced-gate-noise is:

$$\overline{i_{ng}^2} = 4KT\delta g_g \Delta f \tag{19}$$

where

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{20}$$

Further recall that the drain-induced-gate-noise is correlated with the drain noise, with a correlation coefficient defined formally as:

$$c \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \tag{21}$$

The long-channel value of c is theoretically –*j*0.395. Precise measurements of the correlation coefficient are difficulty to carry out (especially in the deep sub-micron regime), but the best published measurements reveal that its magnitude stays within a factor of 2 of this theoretically value, even for devices with drawn channel lengths as small as 0.13μm.

To derive the four equivalent two-port noise parameters, repeated here for convenience,

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} \tag{11}$$

$$G_u \equiv \frac{\overline{i_u^2}}{4KT\Delta f} \tag{12}$$

$$Y_c \equiv \frac{i_c}{e_n} = G_c + jB_c \tag{22}$$

We first reflect the two fundamental MOSFETs noise source back to the input as a different pair of equivalent input generator (one voltage and one current source).

The equivalent input noise voltage generator accounts for the output noise observed when the input port is short-circuited. To determine its value, reflect the drain current noise back to the input as a noise voltage source and recognize that the ratio of these quantities is simply g_m. But there is one more important noise source which should be added in account. That is the gate resistance thermal noise which becomes more and more significant effect on the noise performance in recently deep sub-micron technology. Thus, the over all equivalent input noise voltage generator including gate resistance and the reflected noise current is equal to:

$$\overline{e_n^2} = \frac{\overline{i_{nd}^2}}{g_m^2} + \underline{\underline{4KTR_g\Delta f}} = \frac{\overline{i_{nd}^2}}{g_m^2} \cdot \underline{\underline{\frac{\gamma g_{d0} + R_g g_m^2}{\gamma g_{d0}}}} \tag{23}$$

from which it is apparent that equivalent input noise voltage is completely correlated, and in phase, with the drain current noise. Thus, we can immediately determine the equivalent noise resistance that:

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} = \frac{\gamma g_{d0}}{g_m^2} + \underline{\underline{R_g}} = \frac{\gamma g_{d0}}{g_m^2} \cdot \underline{\underline{\frac{\gamma g_{d0} + R_g g_m^2}{\gamma g_{d0}}}} \tag{24}$$

The equivalent input noise voltage generator by itself does not fully account foe the drain current noise, however, because a nosy drain current also flows even when the input is open-circuits and the drain-induced-gate-noise is ignored. Under this open-circuit condition, dividing the drain current noise by the transconductance yields an equivalent input which, when multiplied by the input admittance, gives us the value of an equivalent input current noise that completes the modeling of i_{nd}:

$$\overline{i_{n1}^2} = \frac{\overline{i_{nd}^2}(j\omega C_{gs})^2}{g_m^2} = \overline{e_n^2}(j\omega C_{gs})^2 \cdot \underline{\underline{\frac{\gamma g_{d0}}{\gamma g_{d0} + R_g g_m^2}}} \tag{25}$$

In this step of the derivation, we have assumed that the input impedance of a MOSFET is purely capacitive. This assumption is a good approximation for frequencies well below ω_T, if appropriate high-frequency layout practice is observed to minimize gate resistance. Given this assumption, Eqn. 25 shows that the input noise current i_{n1} is in quadrature, and therefore completely correlated, with the equivalent input noise voltage, e_n.

The total equivalent input current noise is the sum of the reflected drain noise contribution of Eqn. 25 and the induced gate current noise. The induced gate noise current itself consists of two terms. One, which we'll denote i_{ngc}, is fully correlated with the drain current noise, while the other, i_{ngu}, is completely uncorrelated with the drain current noise. Hence, we may express the correlation admittance as follows:

$$\begin{aligned}
Y_c &\equiv \frac{i_c}{e_n} = G_c + jB_c \\
&= \frac{i_{n1} + i_{ngc}}{e_n} = j\omega C_{gs}\sqrt{\frac{\gamma g_{d0}}{\gamma g_{d0} + R_g g_m^2}} + \frac{i_{ngc}}{e_n} \\
&= j\omega C_{gs}\sqrt{\frac{\gamma g_{d0}}{\gamma g_{d0} + R_g g_m^2}} + \frac{g_m}{\sqrt{\dfrac{\gamma g_{d0} + R_g g_m^2}{\gamma g_{d0}}}} \cdot \frac{i_{ngc}}{i_{nd}} \\
&= \underline{\underline{Z}} \cdot \left(j\omega C_{gs} + g_m \cdot \frac{i_{ngc}}{i_{nd}} \right)
\end{aligned} \tag{26}$$

For simplifying the expression, we define a ***gate-resistance coefficient***, **Z**, with the following relation:

$$\underline{\underline{Z = \sqrt{\frac{\gamma g_{d0}}{\gamma g_{d0} + R_g g_m^2}}}} \tag{27}$$

So we can redraw some of the formulas which we just derived before as:

$$\overline{e_n^2} = \frac{\overline{i_{nd}^2}}{g_m^2} + \underline{\underline{4KTR_g \Delta f}} = \frac{\overline{i_{nd}^2}}{g_m^2} \cdot \underline{\underline{\frac{\gamma g_{d0} + R_g g_m^2}{\gamma g_{d0}}}} = \frac{\overline{i_{nd}^2}}{g_m^2} \cdot \frac{1}{\underline{\underline{Z^2}}} \tag{28}$$

$$\overline{i_{n1}^2} = \frac{\overline{i_{nd}^2}(j\omega C_{gs})^2}{g_m^2} = \overline{e_n^2}(j\omega C_{gs})^2 \cdot \underline{\underline{\frac{\gamma g_{d0}}{\gamma g_{d0} + R_g g_m^2}}} = \overline{e_n^2}(j\omega C_{gs})^2 \cdot \underline{\underline{Z^2}} \tag{29}$$

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} = \frac{\gamma g_{d0}}{g_m^2} + \underline{\underline{R_g}} = \frac{\gamma g_{d0}}{g_m^2} \cdot \frac{\gamma g_{d0} + R_g g_m^2}{\gamma g_{d0}} = \frac{\gamma g_{d0}}{g_m^2} \cdot \frac{1}{\underline{\underline{Z}}^2} \tag{30}$$

To express Y$_c$ in a more useful form, we need to incorporate the induced gate noise correlation factor explicitly. To do so, we must manipulate the last term of Eqn. 26 in ways that will initially appear mysterious. First, we express it in terms of cross-correlations by multiplying both numerator and denominator by the conjugate of the drain noise current and then averaging each:

$$\begin{aligned} g_m \cdot \frac{i_{ngc}}{i_{nd}} &= g_m \cdot \frac{\overline{i_{ngc} \cdot i_{nd}^*}}{\overline{i_{nd} \cdot i_{nd}^*}} = g_m \cdot \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\overline{i_{nd}^2}} = g_m \cdot \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{nd}^2}}\sqrt{\overline{i_{ng}^2}}}\sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} \\ &= g_m \cdot c\sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} = \frac{g_m}{g_{d0}} \cdot c\sqrt{\frac{\delta}{5\lambda}} \cdot \omega C_{gs} \end{aligned} \tag{31}$$

If we assume that *c* continues to be purely imaginary, even in the short-channel regime, we finally obtain a useful expression for the correlation admittance by combining Eqn. 26 and 31 as that:

$$Y_c = \underline{\underline{Z}} \cdot \left(j\omega C_{gs} + g_m \cdot \frac{i_{ngc}}{i_{nd}} \right) = j\underline{\underline{Z}}\omega C_{gs}\left(1 - \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right) \tag{32}$$

where we have used the substitution:

$$\alpha = \frac{g_m}{g_{d0}} \tag{33}$$

Since α is unity for long-channel devices and progressively decrease as channel lengths shrink, it is one measure of the departure from the long-channel regime.

We see from Eqn. 32 that the correlation admittance is purely imaginary, so that $G_c=0$. more significant, however, is the fact that Y_c does not equal the admittance of C_{gs}, although it is some multiple of it. Hence, one cannot maximize power transfer and minimize noise figure simultaneously. To investigate further the important implications of this impossibility, though, we need to derive the last remaining noise parameter, G_u.

Using the definition of the correlation coefficient, we may express the induced gate noise as follows:

$$\overline{i_{ng}^2} = \overline{(i_{ngc} + i_{ngu})^2} = 4KT\Delta f \delta g_g |c|^2 + 4KT\Delta f \delta g_g (1-|c|^2) \tag{34}$$

The last term in Eqn. 34is uncorrelated portion of the induced gate noise current, so that, finally:

$$G_u \equiv \frac{\overline{i_u^2}}{4KT\Delta f} = \frac{4KT\Delta f \delta g_g (1-|c|^2)}{4KT\Delta f} = \frac{\delta \omega^2 C_{gs}^2 (1-|c|^2)}{5 g_{d0}} \tag{35}$$

With these parameters, we can determine both the source impedance that minimizes the noise figure as well as the minimum noise figure itself:

$$B_{opt} = -B_c = -\underline{\underline{Z}}\omega C_{gs}\left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{36}$$

From Eqn. 36, we see that the optimum source susceptance is essentially inductive in character, except that it has the wrong frequency behavior. Hence, achieving a broadband noise matching is fundamentally difficult.

Continuing, the real part of the optimum source admittance is:

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = \underline{\underline{Z}}\alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \qquad (37)$$

And the minimum noise figure is given by:

$$\begin{aligned} F_{\min} &= 1 + 2R_n(G_{opt} + G_c) = 1 + \frac{2}{\sqrt{5}}\frac{\omega C_{gs}}{\underline{\underline{Z}}g_m}\sqrt{\gamma\delta(1-|c|^2)} \\ &\approx 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\underline{\underline{Z}}\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \end{aligned} \qquad (38)$$

In Eqn. 38, the approximation is exact if one threats ω_T as simply the ratio of g_m to C_{gs}. Note that if there were no the drain-induced-gate-noise current (i.e., if δ were zero), the minimum noise figure would be 0 dB. That unrealistic prediction along should be enough to suspect that the induced gate noise must indeed exist. Also note that, in principle, increasing the correlation between drain and gate current noise would improve noise figure, although correlation coefficient unrealistic near unity would be required to effect large reductions in noise figure.

Another important observation is that improvements in ω_T that accompany technology scaling also improve the noise figure at any given frequency. However, the rapid pace of change in IC technology virtually guarantees an incomplete understanding of the behavior of transistors of the most recent generations of technology. Because the detailed behavior of some of the coefficients in the short-channel regime is still unknown, we will have to make accurate noise measurement and then carefully extract the important MOSFETs noise coefficients.

III. MOSFETs Noise Coefficients Extraction

3.1 Introduction

The RF noise is difficult to measure in Si MOSFETs due to the strong parasitic substrate loss (shown in fig. 5) that dominates the noise in as-measured NFmin. De-embedding is required to give the much smaller intrinsic NFmin [3]-[5] - this can produce errors. To overcome this problem we used a novel microstrip transmission line layout, which is shown in figure 6. Figures 7(a) and 7(b) show the as-measured NFmin of different gate fingers devices, respectively. The as-measured NFmin using the standard CPW transmission line design is also shown for comparison. A large NFmin reduction over the whole frequency range is observed using the microstrip line design, even without de-embedding. At 10 GHz, the as-measured NFmin is only 0.9 dB for the 8 gate-finger MOSFET. This is the lowest reported NFmin for a 0.18 μm MOSFET and is comparable with the data for 0.13 μm devices (Lg= 80nm) [4]-[5]. The low NFmin of 0.9 dB at 10 GHz is sufficient for UWB (3.1-10.6 GHz) applications.

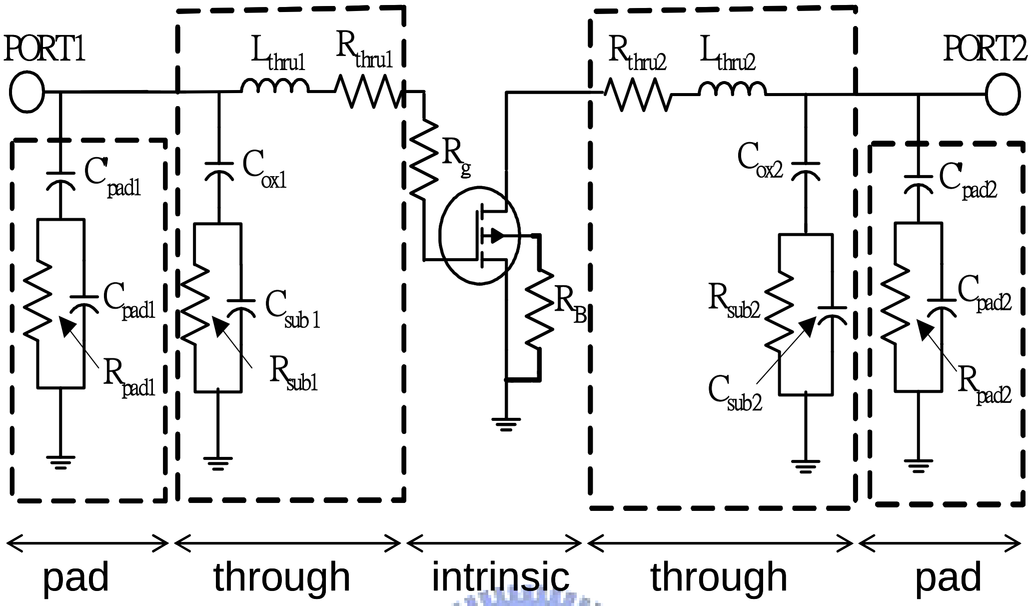


Figure 5 Complex parasitic circuits of CPW layout.

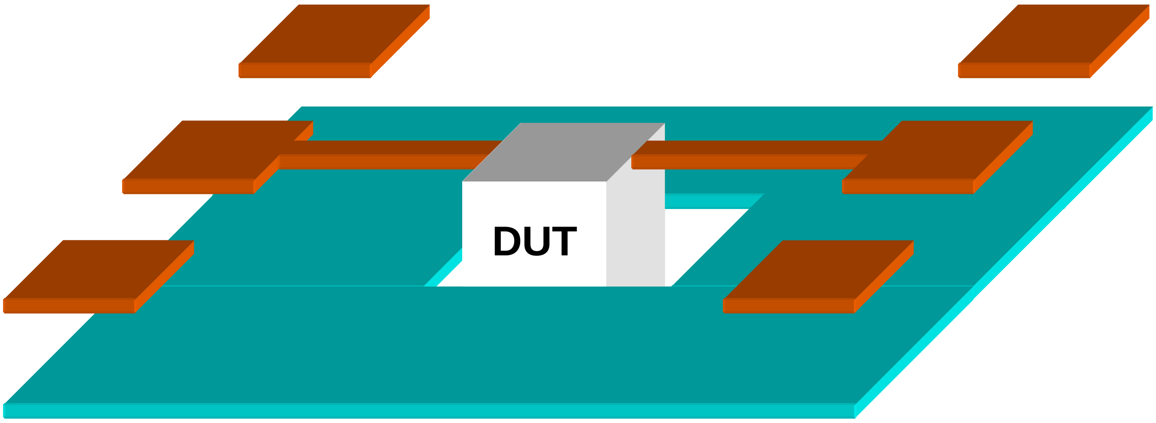


Figure 6 Developed microstrip line structure.

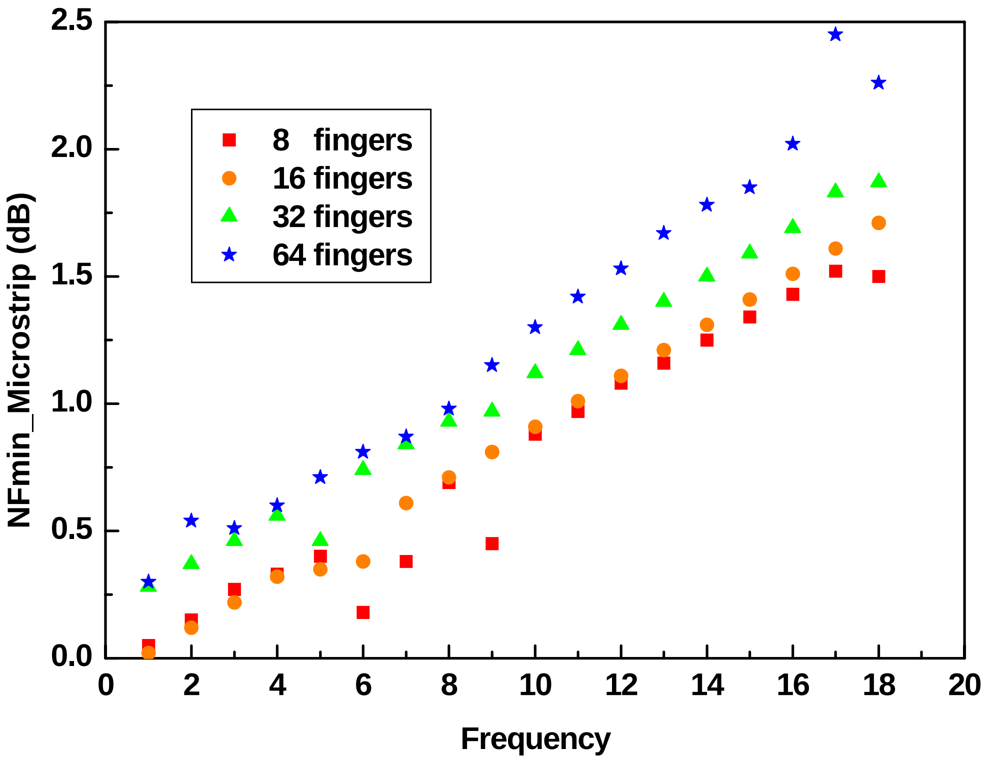


Figure 7(a) NFmin of different fingers on microstrip.

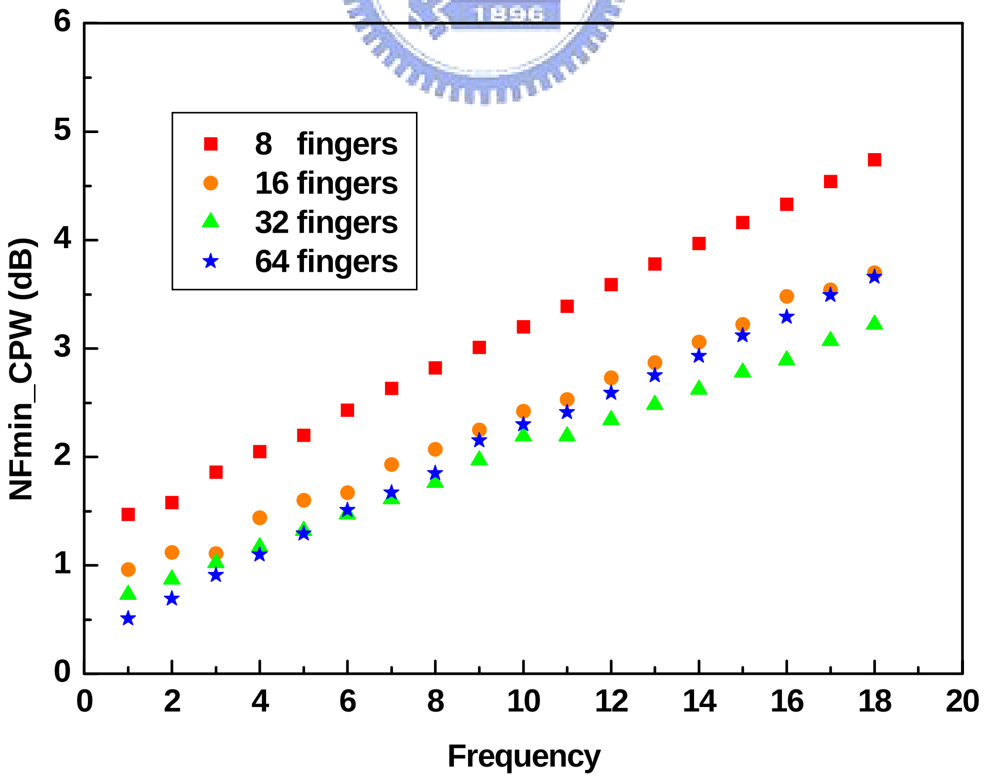


Figure 7(b) NFmin of different fingers on CPW.

The equivalent noise resistance of the two-port, which is shown in figure 8, decreases slightly with increasing frequencies. This is because that the substrate thermal noise which we ignore in our noise equations contributes some the equivalent noise resistance. As a result, we will extract the noise coefficients, such as γ and δ, at high frequencies range (10GHz) in order to get the better accuracy.

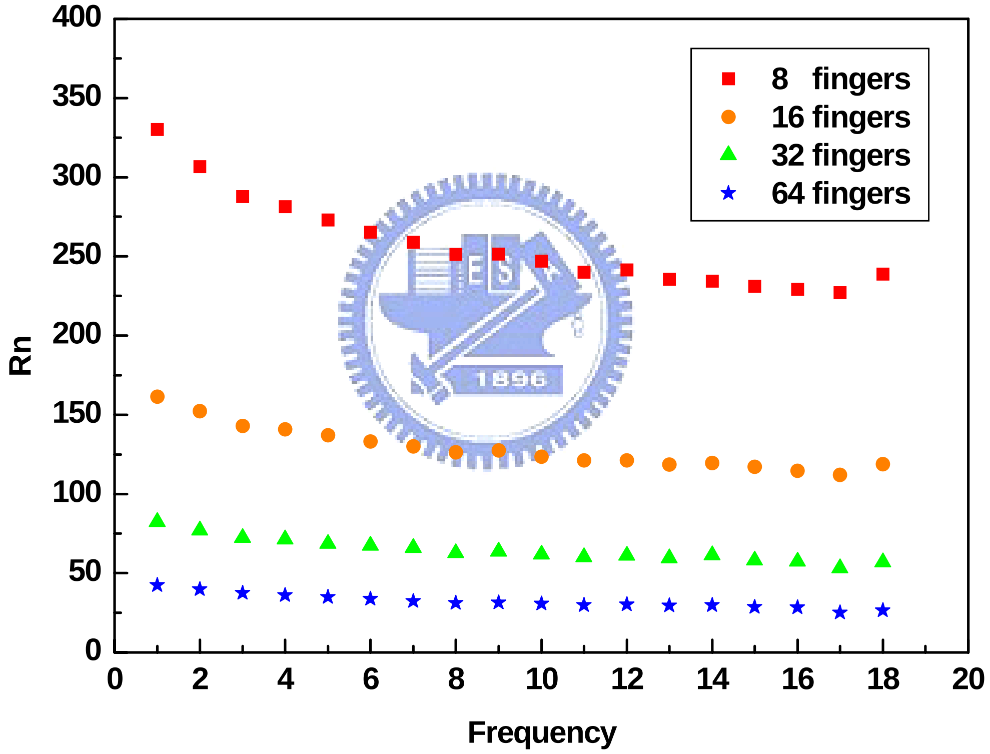


Figure 8 Equivalent noise resistance of different fingers versus freq.

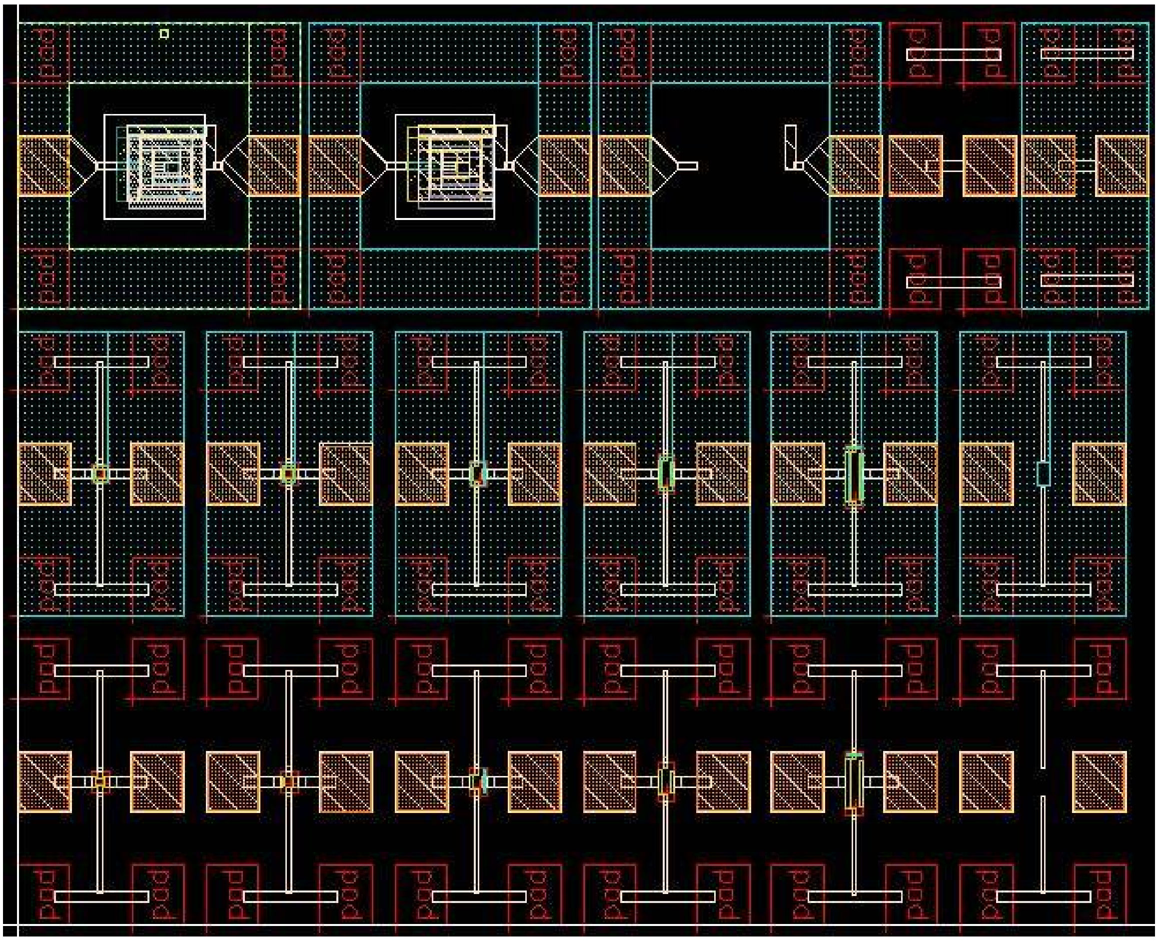


Figure 9 Test-key layout.

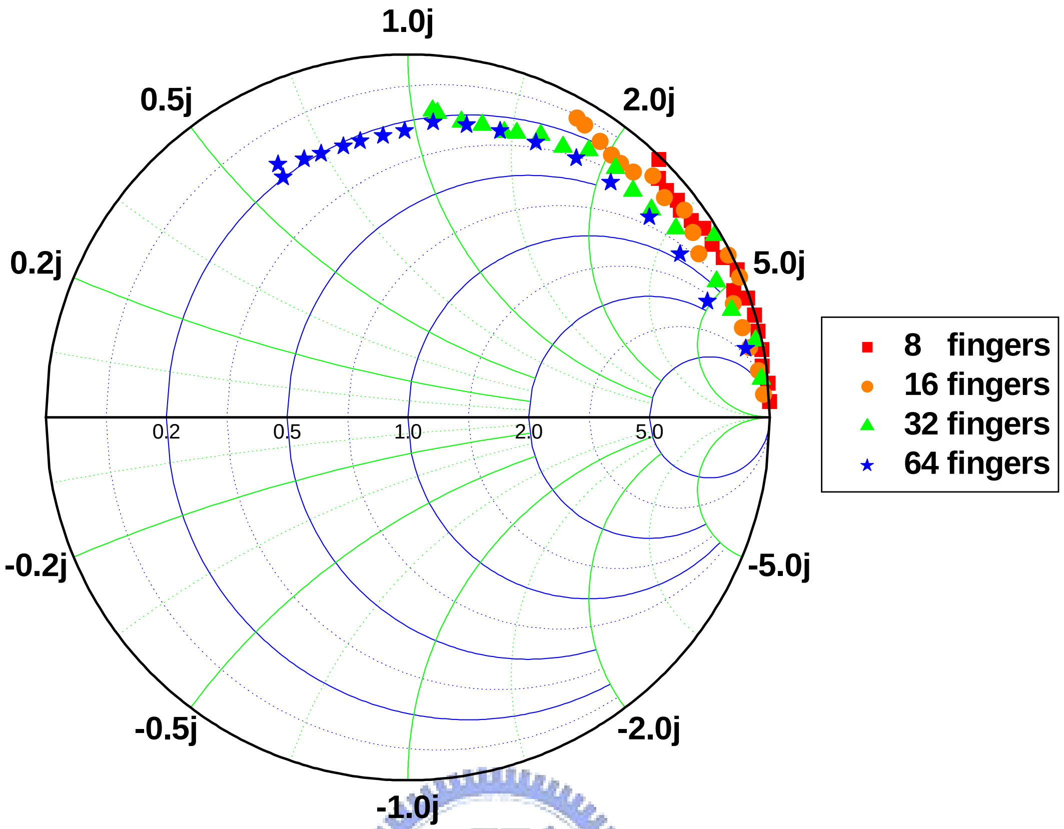


Figure 10 Γ_{opt} of different fingers on smith chart.

The figure 9 is the layout of the ultra-low noise MOSFETs, which includes the conventional CPW and our microstrip layout of MOSFETs and two more 3D inductors. And the figure 10 shows the optimum source impedance of the ultra-low noise MOSFETs. Sine we have derived the accurate noise data, we will start to extract the noise coefficients in the next step.

3.2 Extraction Results

According to our noise equations, we can extract the thermal drain current noise factor, γ, from R_n which is shown in the equation 30.

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} = \frac{\gamma g_{d0}}{g_m^2} + \underline{\underline{R_g}} = \frac{\gamma g_{d0}}{g_m^2} \cdot \frac{\gamma g_{d0} + R_g g_m^2}{\gamma g_{d0}} = \frac{\gamma g_{d0}}{g_m^2} \cdot \frac{1}{\underline{\underline{Z^2}}} \qquad (30)$$

By our extraction, the thermal drain current noise factor, γ, is about to 0.9, which is shown in figure 11. In contrast to some other groups, we find only a moderate enhancement of the drain current noise for short channel MOSFETs. The abnormal among of noise from other group’s results maybe due to inaccuracy measurements, lacking of gate and substrate thermal noise, or inappropriate layout.

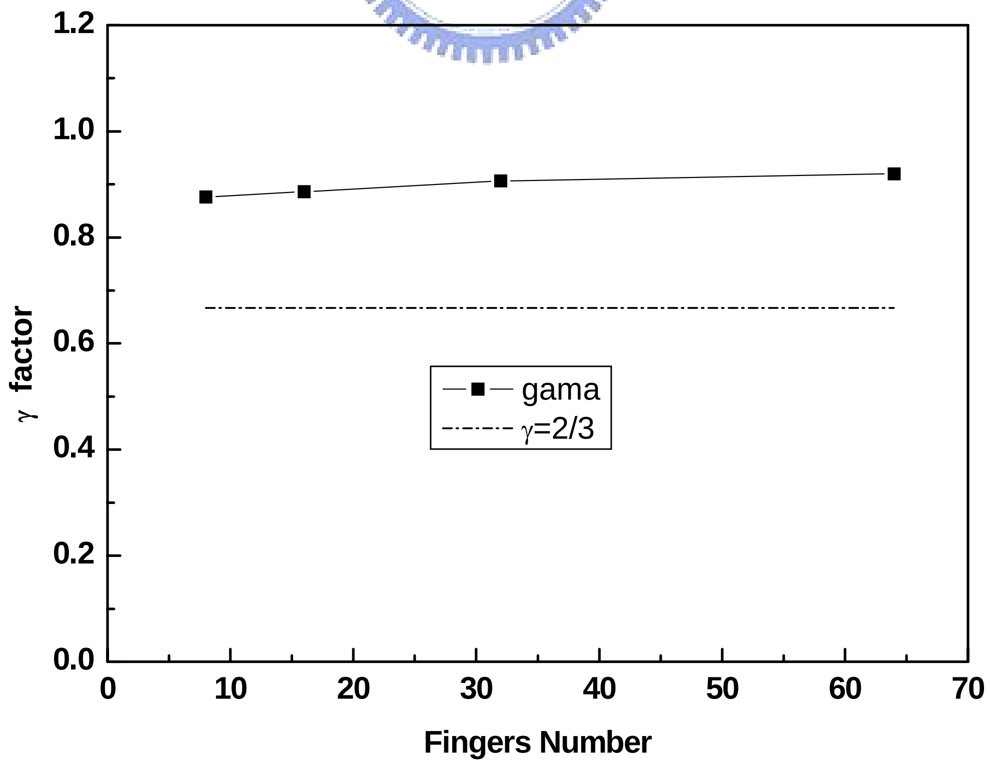


Figure 11 Extracted γ factor of different fingers at 10GHz.

The other two coefficients, c and δ, can be extract from equation 36~38 which are recalled again here for convenience.

$$B_{opt} = -B_c = -\underline{\underline{Z}}\omega C_{gs}\left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{36}$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n}+G_c^2} = \underline{\underline{Z}}\alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{37}$$

$$\begin{aligned} F_{\min} &= 1+2R_n(G_{opt}+G_c) = 1+\frac{2}{\sqrt{5}}\frac{\omega C_{gs}}{\underline{\underline{Z}}g_m}\sqrt{\gamma\delta(1-|c|^2)} \\ &\approx 1+\frac{2}{\sqrt{5}}\frac{\omega}{\underline{\underline{Z}}\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \end{aligned} \tag{38}$$

By the extraction, the correlation factor, ***c***, remains the value of –*j*0.395 as it in the long-channel regime theory [9], while δ is twice the value of γ. This value of δ is reasonable since it comes from the thermal drain current noise.

Figure 12 ~ 17 show the extraction results. Figure 12 and 13 represent the measured and modeling optimum source impedance respectively at 10GHz, while figure 14 is the measured and modeling NFmin at 10GHz. And figure 15 demonstrate the measured and modeling optimum source versus frequencies with 32 gate fingers, while figure 16 is the measured and modeling NFmin versus frequencies with 32 gate fingers. Very Good agreement between the measurements and our modeling is achieved by using our derived noise equations. Figure 17 tabulates the relative characteristics of the RF MOSFETs that we measured.

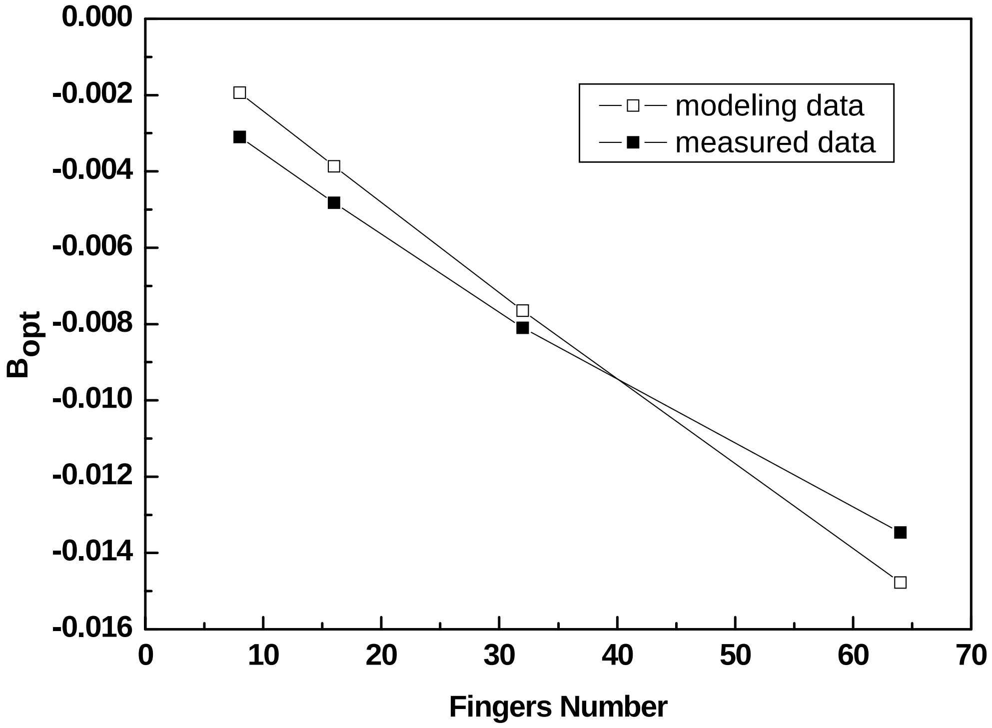


Figure 12 Modeling and measured B_{opt} of different fingers at 10GHz.

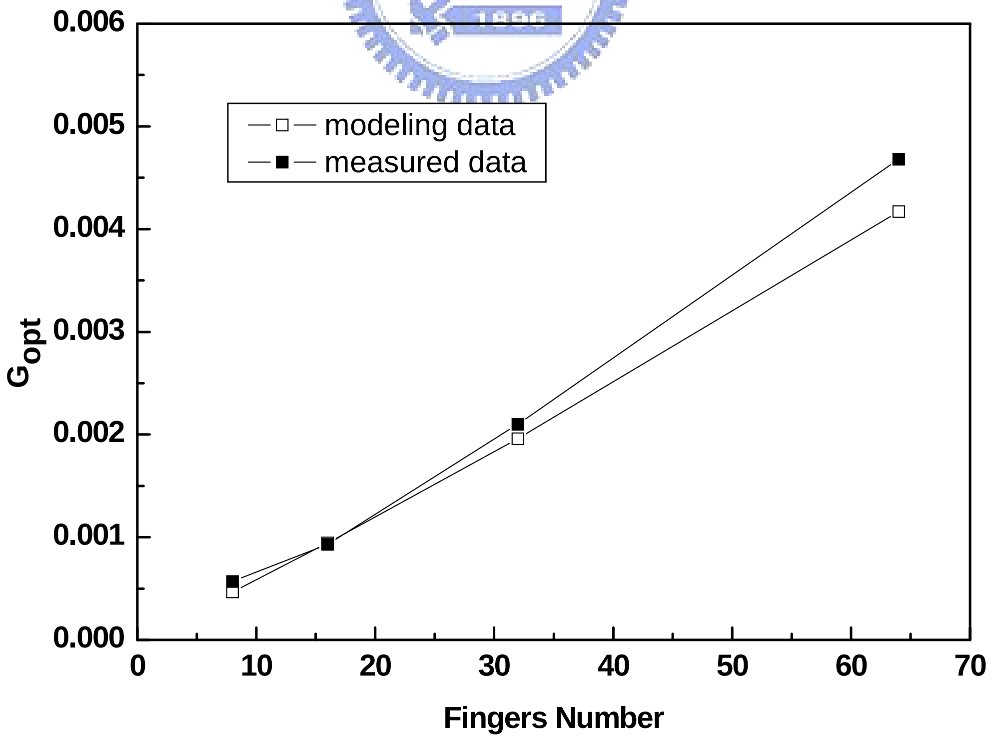


Figure 13 Modeling and measured G_{opt} of different fingers at 10GHz.

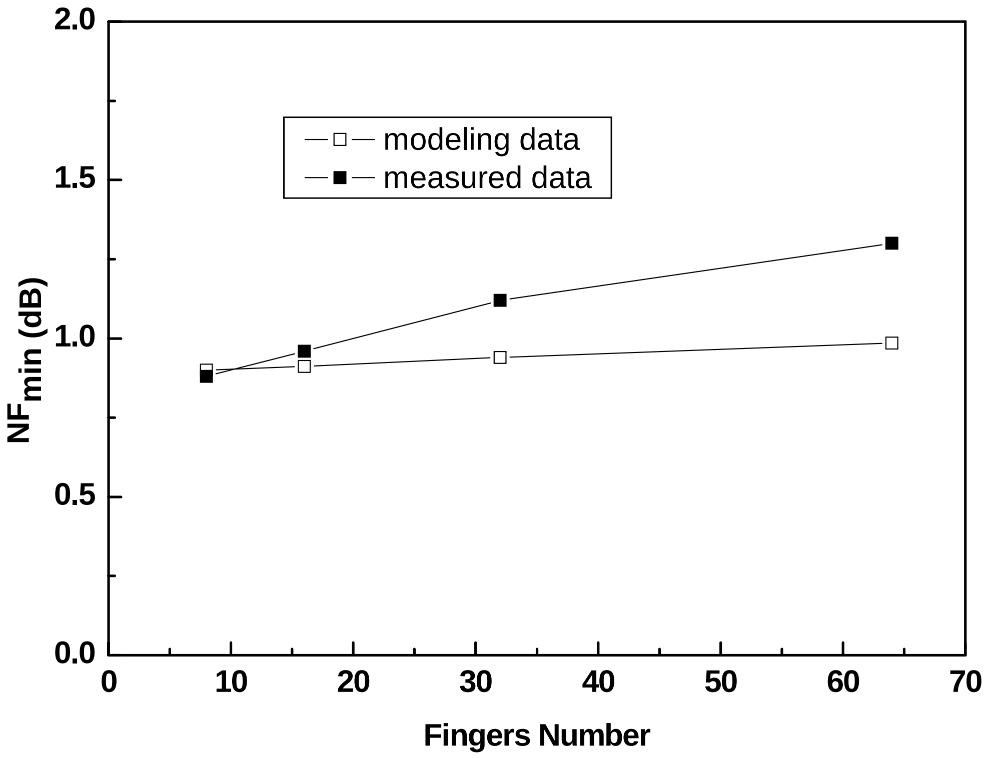


Figure14 Modeling and measured NFmin of different fingers at 10GHz.

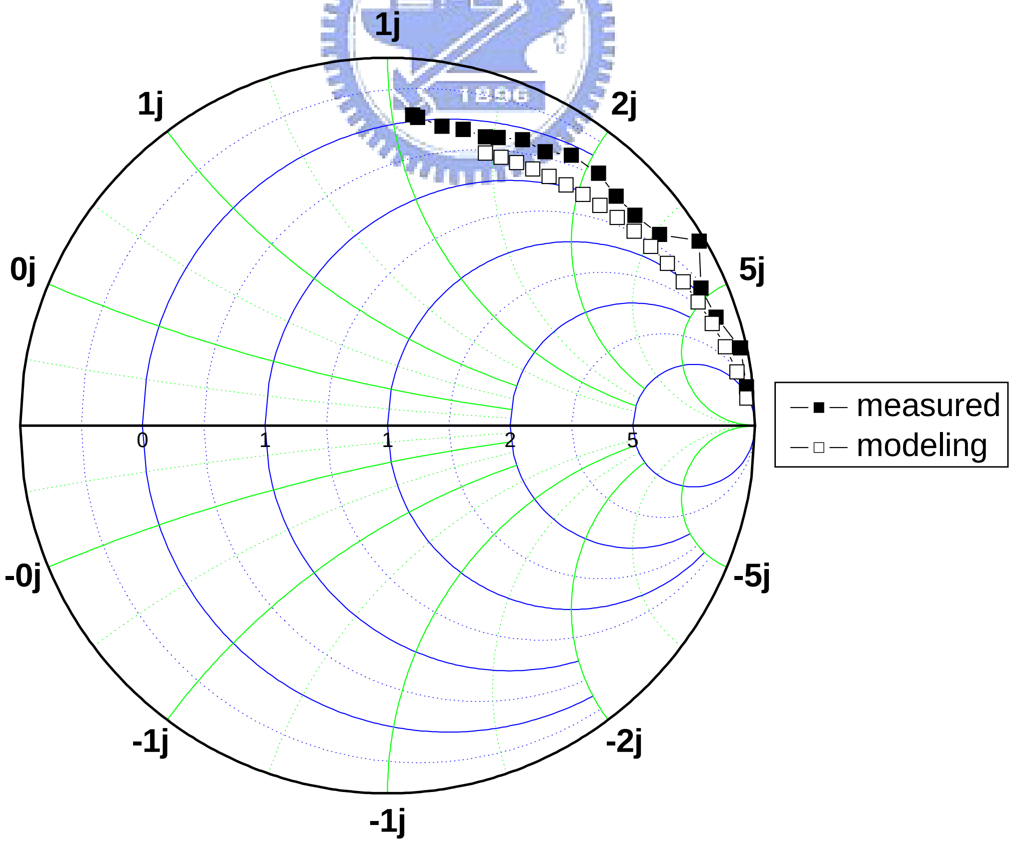


Figure 15 the optimum source impedance versus frequencies of 32 gate fingers.

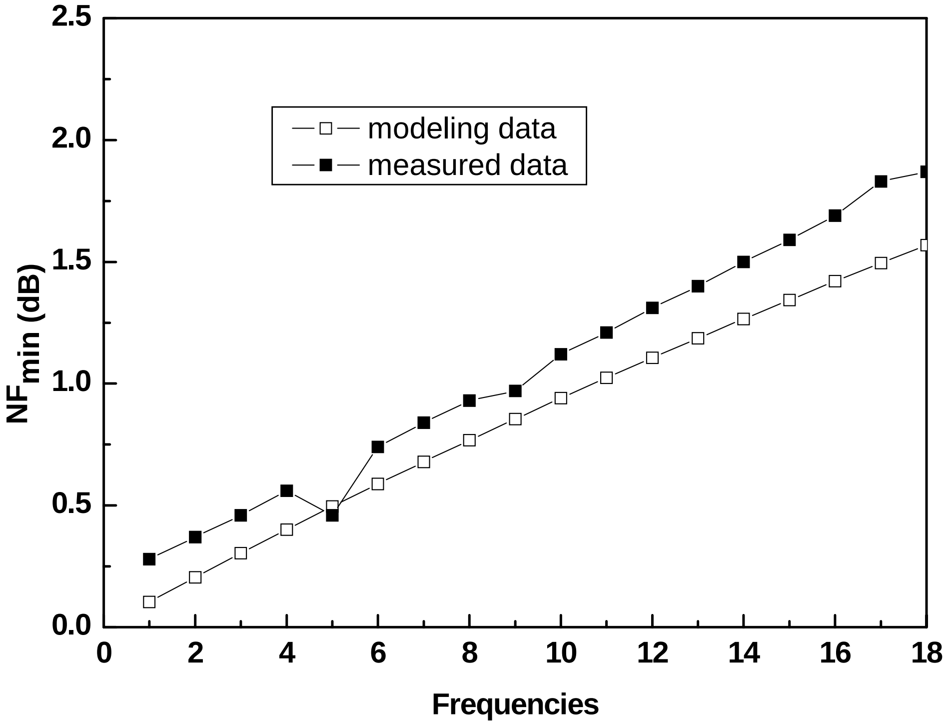


Figure 16 the NFmin versus frequencies of 32 gate fingers.

Characteristics\F.N.	**8**	**16**	**32**	**64**
gm (A/V)	0.00996	0.0199	0.0392	0.0741
gdo (A/V)	0.0265	0.0523	0.0987	0.171
α	0.375849	0.380497	0.397163	0.433333
Rn (Ω)	246.91	123.62	61.67	30.55
Rg (Ω)	12.74	6.55	3.45	1.9
γ	0.876605	0.886442	0.906415	0.919952
Z	0.973859	0.973147	0.971626	0.968404
δ	2γ	2γ	2γ	2γ
c	*j*0.395	*j*0.395	*j*0.395	*j*0.395
ft (GHz)	49	49	49	48.5

Figure 17 Summary of MOSFETs characteristics.

3.3 Conclusions

We have developed a new microstrip line design to measure NFmin accurately without the need for complicated de-embedding. Based on the accurate NFmin measurement and analytical NFmin equation, close agreements to the measurements with modeling data are all obtained that is important for further circuit application.

IV. UWB LNA Design

4.1 Introduction

Ultra wideband (UWB) systems are a new wireless technology capable of transmitting data over a wide spectrum of frequency bands with very low power and high data rates. Among the possible applications, UWB technology may be used for imaging systems, vehicular and ground penetrating radars, and communication systems. Although the UWB standard (IEEE 802.15.3a [16]) has not been completely defined, most of the proposed applications are allowed to transmit in a band between 3.1 and 10.6 GHz. In this work, the design of a low noise amplifier (LNA) in a 0.18μm CMOS technology for the receiver path of a UWB system is discussed. Such an amplifier must feature wide-band input matching to a 50Ω antenna, flat gain over the entire bandwidth, good linearity, minimum possible noise figure and low power consumption.

In recent years, narrow-band CMOS LNA designs have employed inductive source degeneration to achieve good input matching. This technique also yields nearly optimal noise figure at the resonance frequency of the input network [17]. In the proposed wide-band design in Figure 16 (at the next section), the inductively degenerated common source topology is further explored. The input impedance Zin is embedded in a two-section band-pass filter to resonate its reactive part over the whole band. The cascode configuration improves the reverse isolation and the frequency response of the amplifier. Source-follower buffer of the second stage is intended for measurement purposes, i.e. to drive an external 50Ω load.

4.2 Design Procedures

In this work, we first use inductive source degeneration to achieve good matching to 100Ω in stead of the conventional 50Ω to decrease the Q value of the serial resonance circuits. This is because that the lower Q value implies the wider bandwidth, which makes a broadband matching. Then we add an L-section circuit to transfer the 100Ω to the source impedance 50Ω. Finally by using CAD tool to optimize the circuits, we can achieve an input reflection coefficient to smaller than -10dB in-band: Ls=0.9nH, Lg=1.6nH, L1=0.9nH and C1=0.25pF. The size of M1 is chosen as 128 gate fingers to minimize the inductance values. The bias of M1 is set for balance between gain and power consumption.

The cascode device is chosen as small as possible to reduce the parasitic capacitances. A lower limit to the width of M2 (24 gate fingers) is set by its reasonable Vds. Both M1 and M2 are minimum length devices. The load is designed to achieve flat gain over the whole bandwidth. In-band, M1 acts as a current amplifier, the input current being Vin/Rs, and the current gain $\beta(\omega)=gm/(j\omega Cgs)$. To compensate for the roll-off of β(ω), a shunt-peaked load is used. The value of the inductance L2 (2.3nH) is limited by acceptable power gain over shooting. Resistance R_L (60Ω) improves the gain at lower frequency. All the design and the layout are shown in figure 18 and figure 19 respectively.

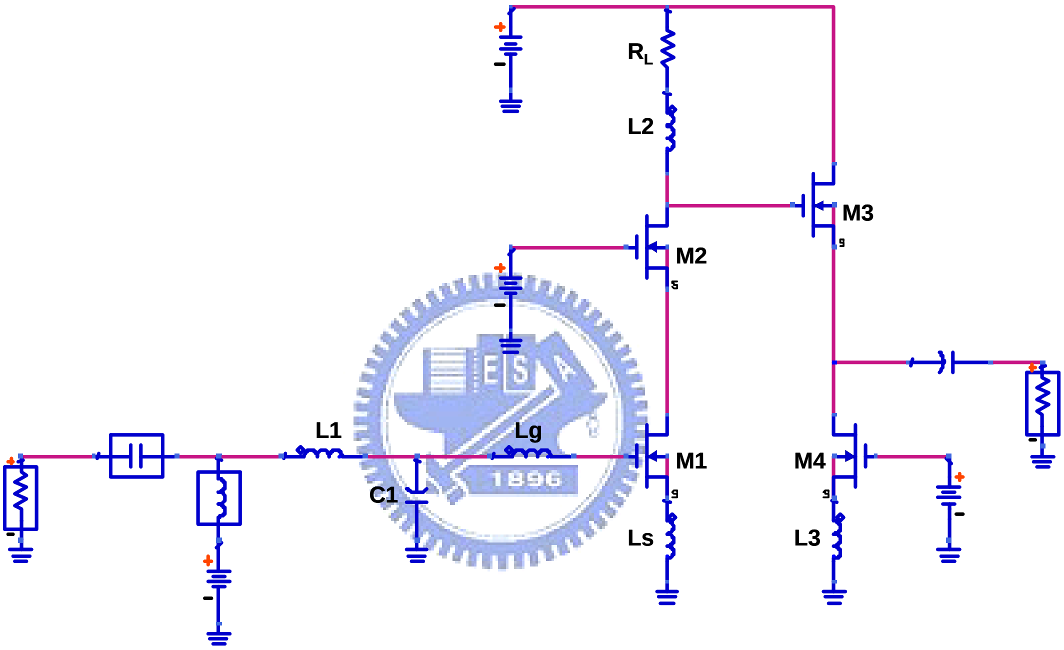


Figure 18 Circuits diagram.

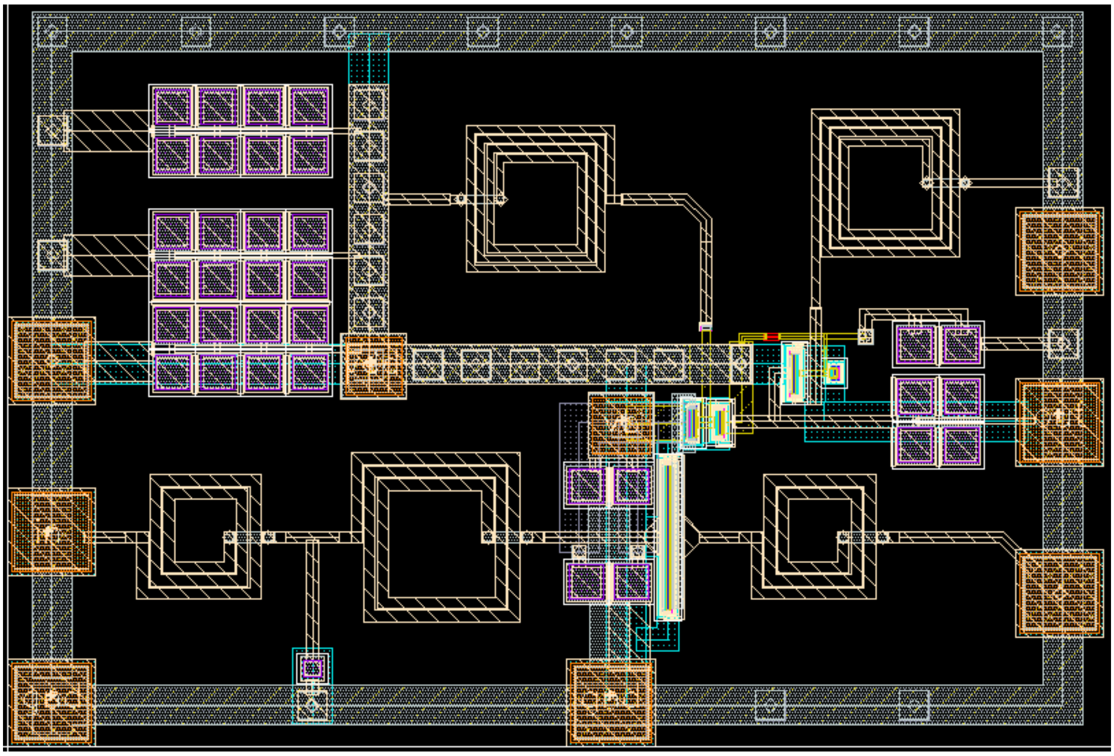


Figure 19 Chip layout.

4.3 Simulation results

Figure 20 shows the simulated input and output reflection coefficients. S11 is lower than -8dB between 3.1 and 12GHz. The output buffer achieves excellent matching such that S22 is lower than -10dB from 1.7GHz to 15.9 GHz. Figure 21 is the power gain versus frequencies, and the maximum power gain is 10.4dB in our simulation results. Since the output source follower drives a matched load, the voltage gain of the core amplifier is exactly 6dB higher than S21. The -3dB bandwidth is 0.4~9.9GHz for the simulation. The noise figure (NF) of this UWB LNA is shown in Figure 22. The noise figure is as low as 3.3dB at 6GHz which is the center frequency of UWB system, while the average noise figure in-band is about 4dB. Figure 23 and 24 show the simulated reverse isolation S12 and stability factor respectively. The two-tone test results for third-order intermodulation distortion are shown in Figure 25. The test is performed at 6GHz. IIP3 is to 3.3dBm, and the input referred 1-dB compression point (ICP) is -9dBm. These results imply excellent linearity of our LNA. The proposed UWB LNA dissipate 27mW (15mW for first stage) with a power supply of 1.8V. Figure 27 summarizes the performance of the presented amplifiers,

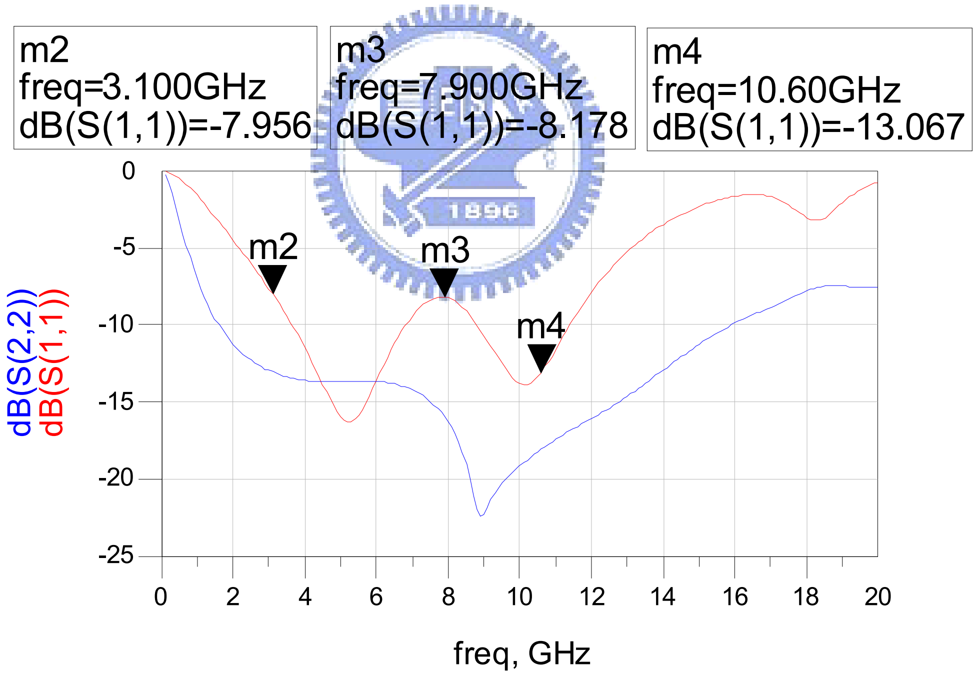


Figure 20 Simulated S11 & S22.

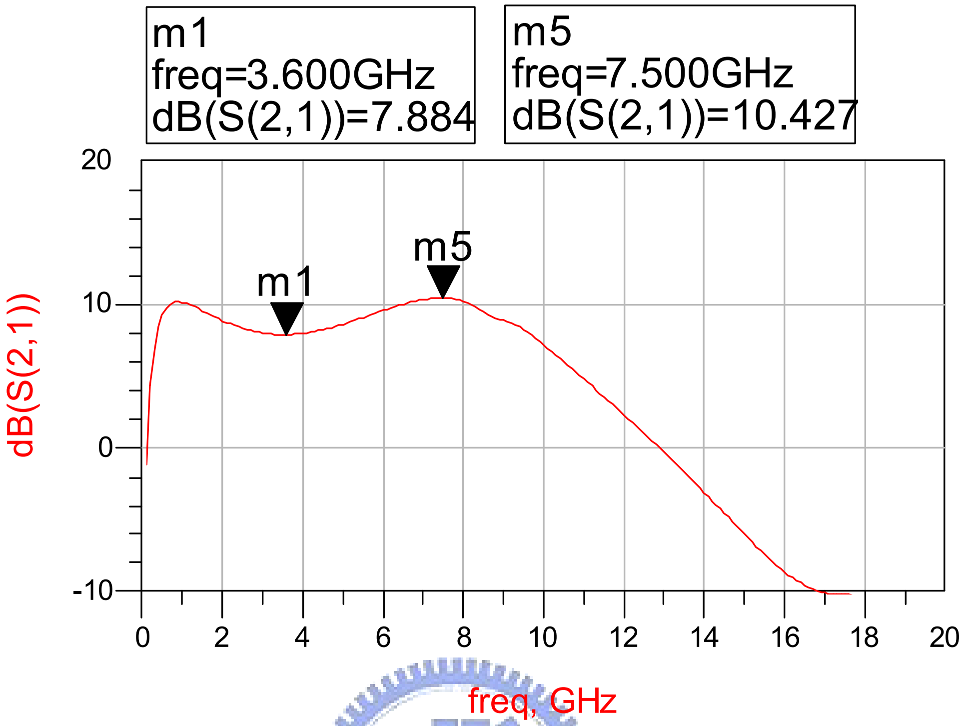


Figure 21 Simulated power gain.

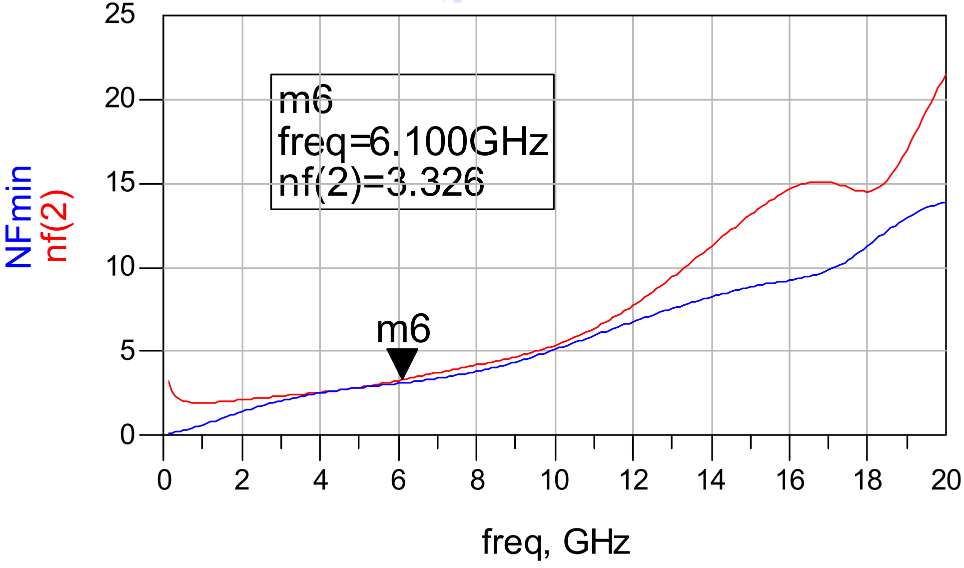


Figure 22 Simulated NF and NFmin.

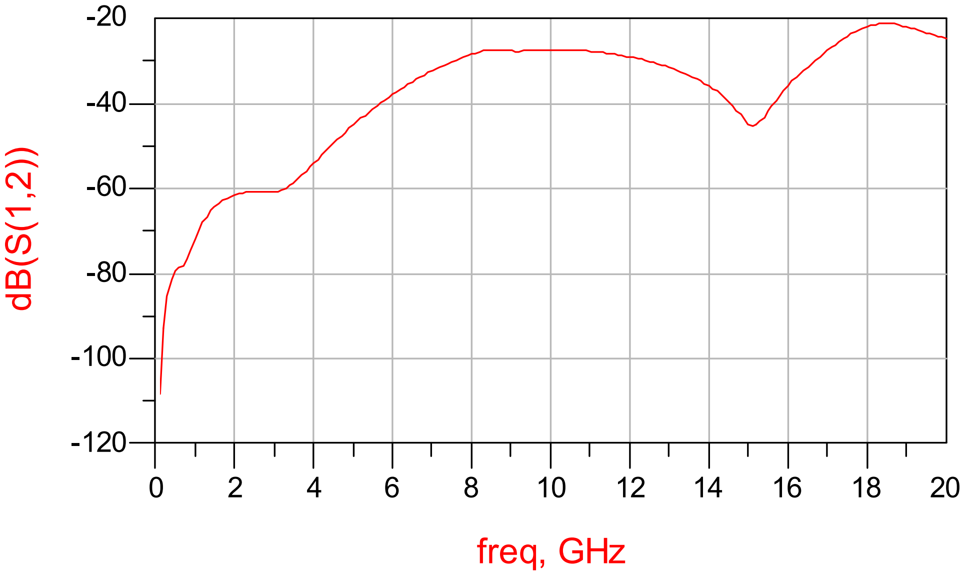


Figure 23 Simulated reverse isolation.

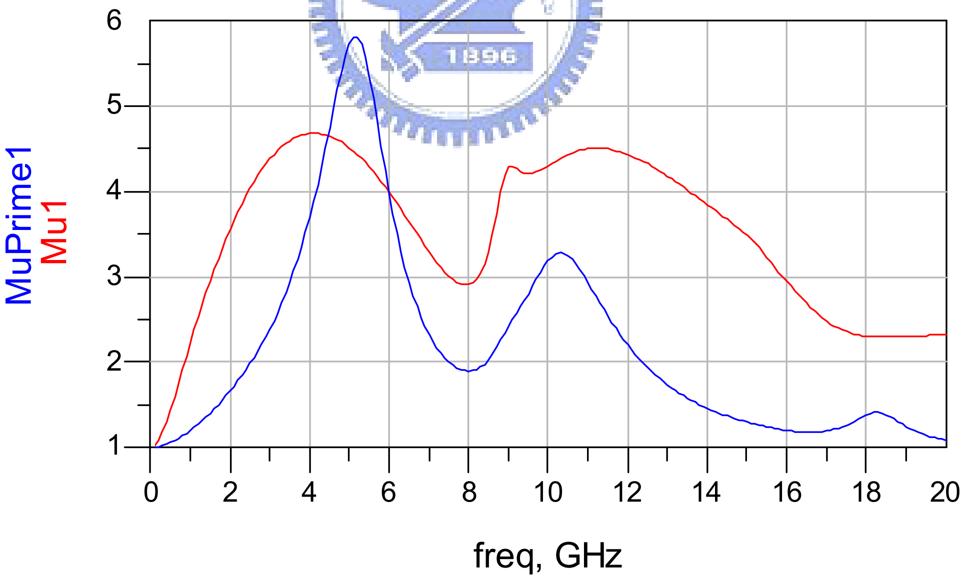
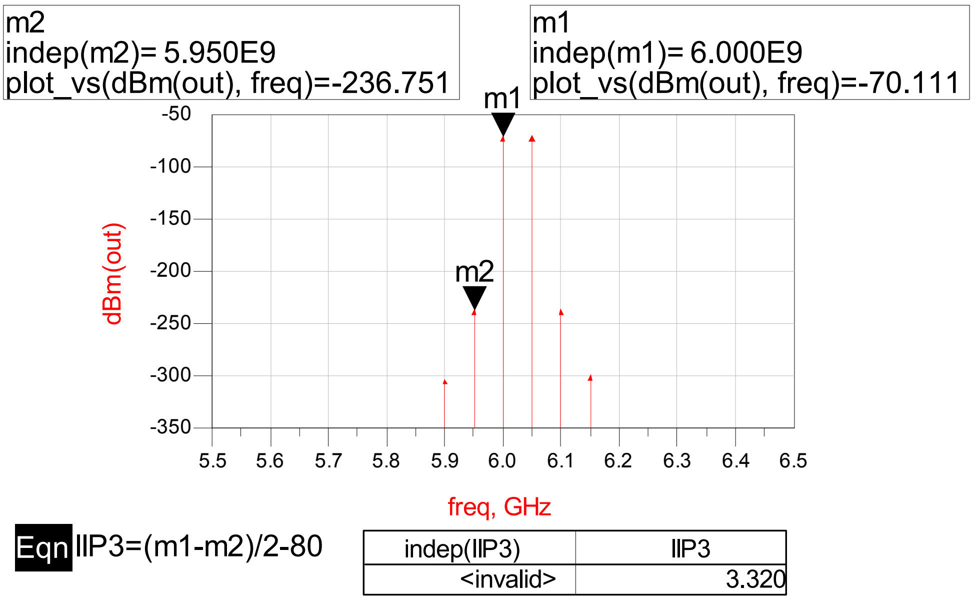


Figure 24 Simulated stability.



IIP3=(m1-m2)/2-80

indep(IIP3)	IIP3
<invalid>	3.320

Figure 25 Two tones test.

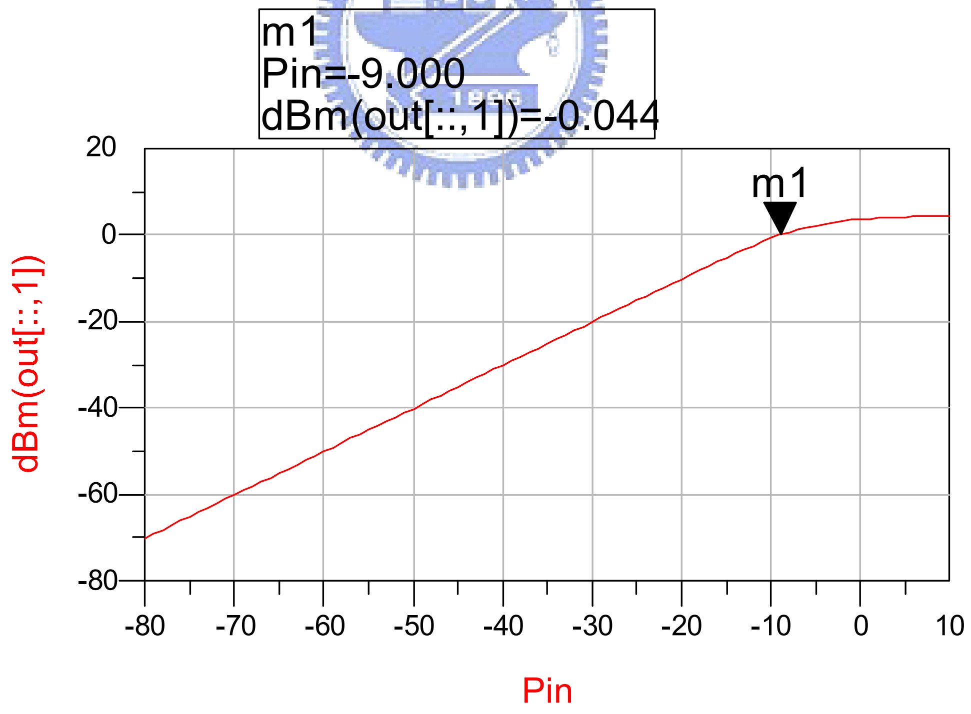


Figure 26 Power-out versus power-in.

B.W. (GHz)	Gain (dB)	NF (dB)	S11 (dB)	S22 (dB)	P_{DC} (mW)
2~10	10.4	<6	< -8	< -12	27; 15

Figure 27 Simulated circuits SPEC summary.

4.4 Measurements and Conclusions

The following figures 28~33 are the measurement results which are only slightly different form our simulation, which imply good accuracy of our simulation and good circuit design. The some of the bandwidth compression showing in figure 28 maybe due to the underestimate of the load resistor parasitic.

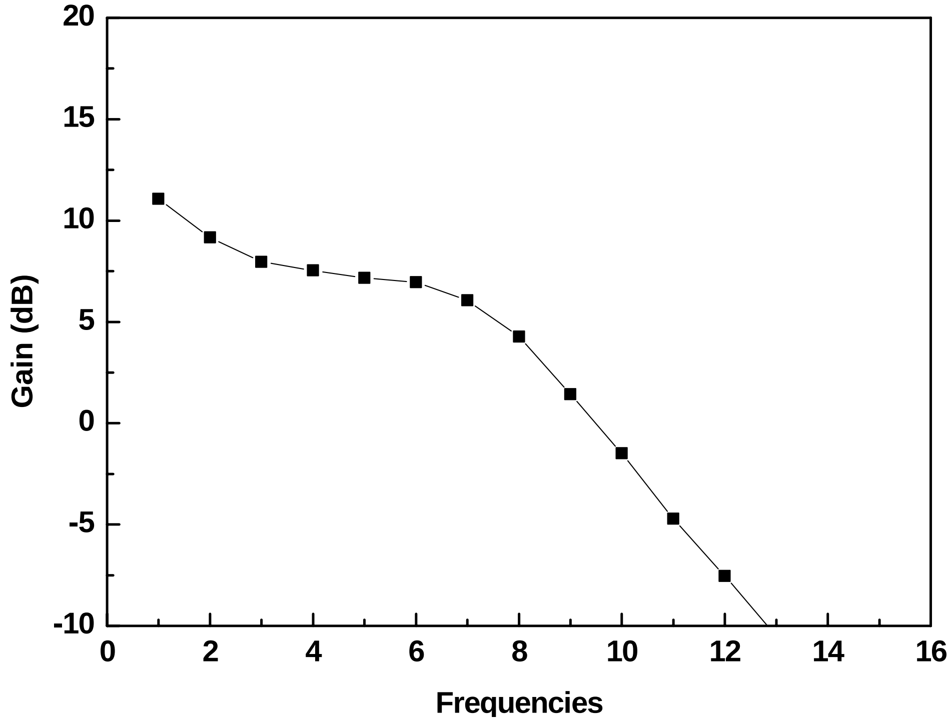


Figure 28 Measured power gain.

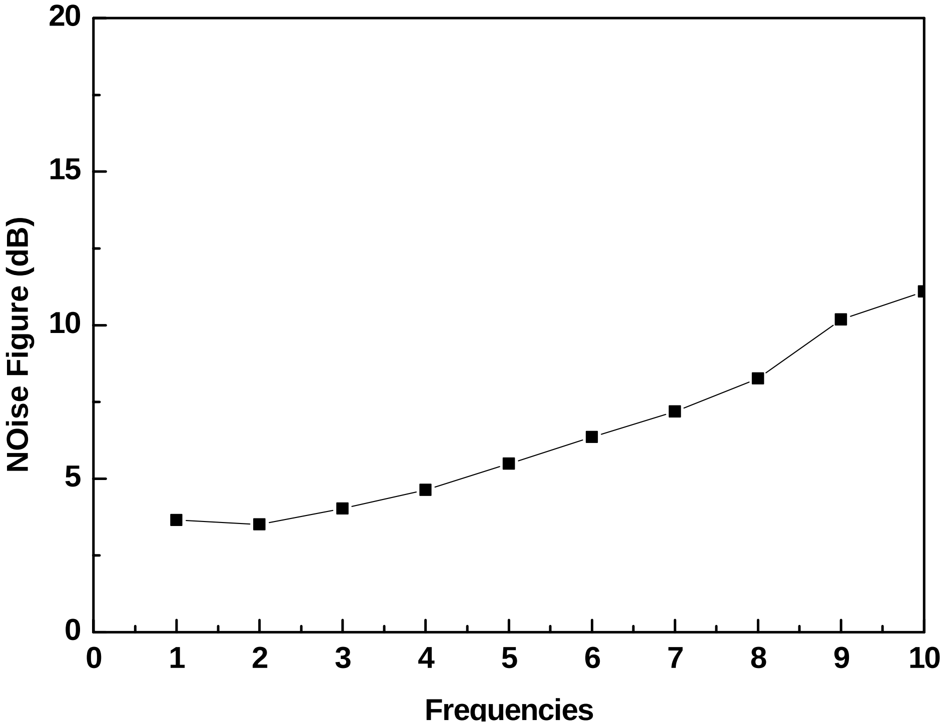


Figure 29 Measured noise figure.

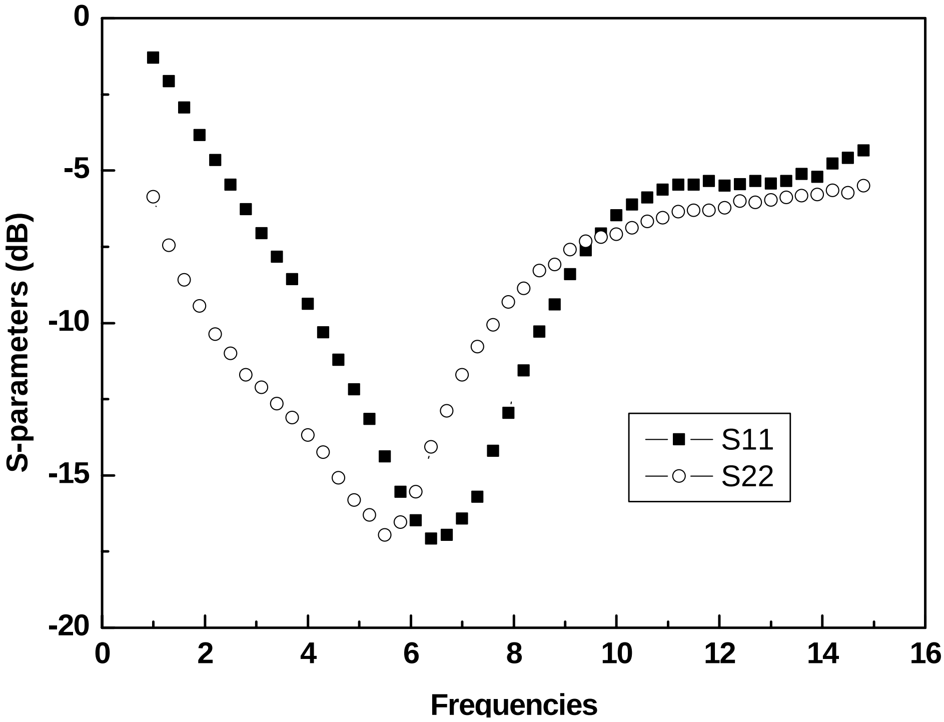


Figure 30 Measured S11 and S22.

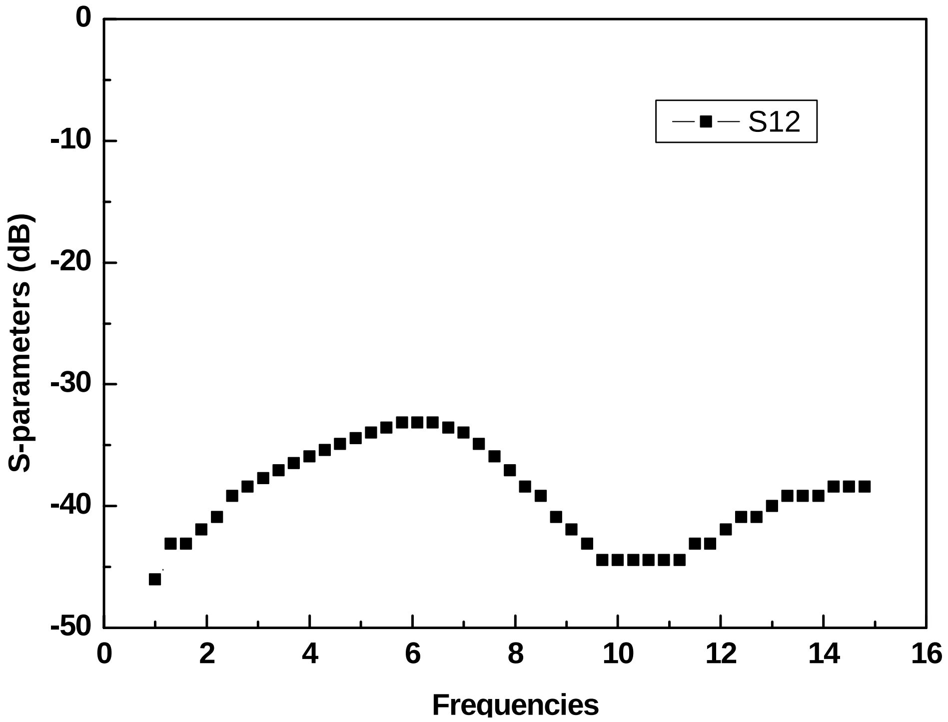


Figure 31 Measured S12.

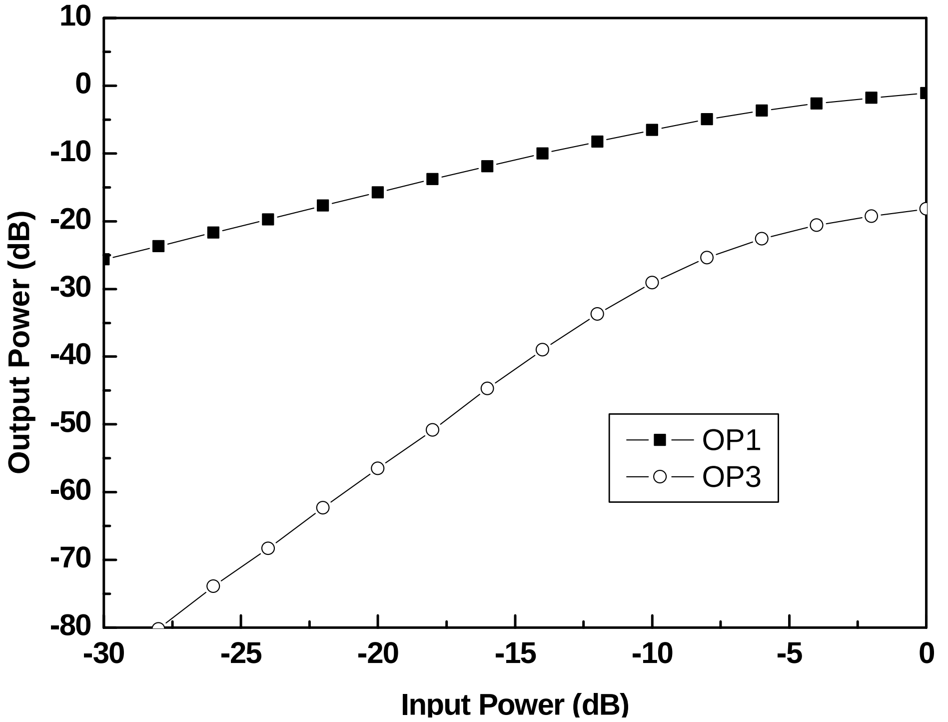


Figure 32 Measured linearity.

B.W. (GHz)	Gain (dB)	NF (dB)	S11 (dB)	S22 (dB)	IIP3 (dBm)	P_{DC} (mW)
3~8	8 (+6)	3.5~8	< -7	< -9	+2	27; 15

Figure 33 Measured results summary.

The bandwidth of this work with considering matching and power gain is from 3 to 8 GHz, while the average power gain is about 8dB which can be up to 14 dB without the current buffer in real cases. The noise performance is good and the minimum noise figure is only 3.5dB at 3~4GHz. The noise figure can be even better if we solve the bandwidth compression problem from the resistor parasitic. Input and output matching are achieved well in band and the linearity of this work is excellent. Total power consumption is 27mW, while the core LNA consumes only 15mW by 1.8V power supply. By the new input matching approach we proposed, a low noise, broadband, low power consumption and good-linearity amplifier is developed for the UWB system applications.

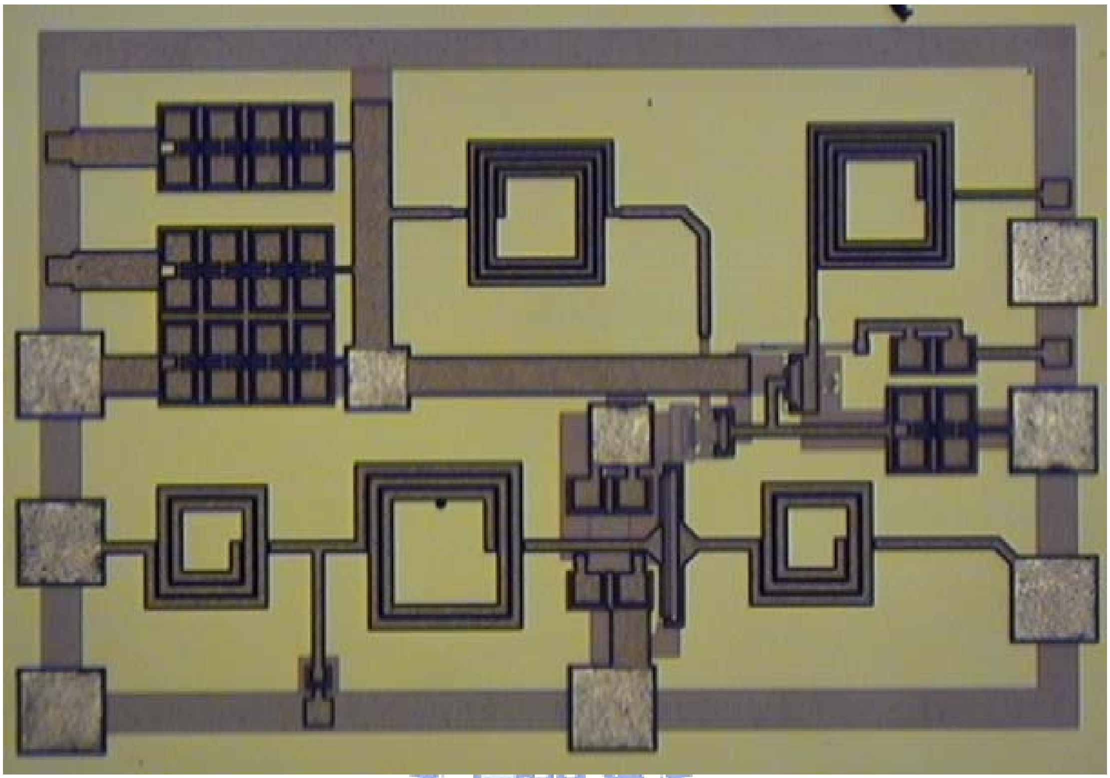


Figure 34 Die photo.

Ref.	B.W. (GHz)	Gain (dB)	NF (dB)	S11 (dB)	S22 (dB)	IIP3 (dBm)	P_{DC} (mW)	Tech.	year
[18]	2.4~9.5	9.3 (+6)	4~9	< -9.9	< -20	-6.7	9*	0.18 μm CMOS	2004
[19]	0.6~22	8.1	4.3~6	< -8	< -9	-	52	0.18 μm CMOS	2003
This work	3~8	8 (+6)	3.5~8	< -7	< -9	+2	27; 15*	0.18 μm CMOS	2005

Figure 35 Comparison of broadband LNA performance.

V. Summary

Let us summary the conclusions of this paper briefly.

Noise modeling: The low noise amplifier in a RF receiver is a significant component, since it plays an important role in the noise performance of a RF system, which affects the dynamic range and the signal to noise ratio of this system. The current noise model with BSIM3v3 core can not model the noise behavior correctly. In order to develop the accurate noise model of RF MOSFETs, we have developed a new microstrip line design to measure NFmin accurately without the need for complicated de-embedding. Based on the accurate NFmin measurement and analytical NFmin equation, close agreements to the measurements with modeling data are all obtained that is important for further circuit application.

UWB LNA: By the new input matching approach we proposed, a low noise, broadband, low power consumption and good-linearity amplifier is developed for the future UWB system applications. The advantages of this design include extending the famous source L-degenerate matching to broadband, low noise, low power consumption, reducing inductor numbers and excellent linearity. All the advantages are important for UWB system considerations.

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學經歷

姓名：賴照民

性別：男

出生年月日：民國七十年四月一日

籍貫：台北市

學歷：台北市立建國高中

（85年9月~88年6月）

國立交通大學電子工程學系

（88年9月~92年6月）

國立交通大學電子工程所

（92年9月~94年6月）

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