Chapter 1 Introduction

1.1 Introduction

Recently, the rapidly growing in communication and digital video systems creates a need for inexpensive mixed-signal circuits such as high speed and high resolution of analog-to-digital converters (ADCs) and digital-to-analog converters （DACs）. Testing mixed signal ICs is known to be a difficult and expansive task. The problem is aggravated by the recent trend of integrating mixed-signal cores in a large digital environment to achieve system-on-a-chip integration. Mixing such circuits leads to ad-hoc and nonstandard test strategies and results in complex and expensive mixed-signal automatic test equipment (ATE). Mixed-signal Built-In Self Test (BIST) approach can potentially reduce test time and cost.

Data converters are typical mixed-signal circuits that bridge the gap between analog and digital signals. Most ADCs, such as successive approximation and flash converters, still suffer from fabrication such that inaccuracy and poor linearity of the internal components, thus reducing the overall resolution of converters. For a delta-sigma ADC, it easily gets high resolution by using feedback and oversampling. Its analog part is a switched capacitor circuit, i.e. a circuit working the discrete time domain. Therefore, it is suitable to be used as the interface circuit between the analog sampling input circuit and the succeeding digital processor.

1.2 The Characteristics of Delta-Sigma Modulation

A delta-sigma ADC is presented in Fig.1.1. It consists of two sub-circuits: one is the analog part which is composed of switched capacitors, operational amplifiers and a 1-bit ADC, which is a comparator; and the other is the digital part which acts as a digital decimator, which includes the digital low-pass filter and the down-sampling circuit. The output signal of one bit ADC is a PCM code which contains the information transferred in the form of the density of codes.

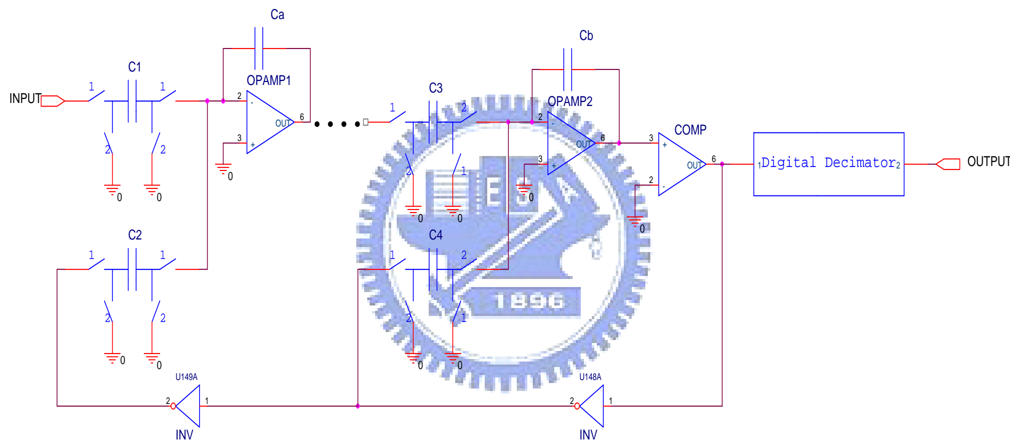


Fig.1.1 Block diagram of a delta-sigma ADC

A delta-sigma modulator is commonly known as a noise shaping modulator due to their quantization noise associated with a differential function. The order of the modulator is determined by the differential function order. A higher-order modulator has a higher differential function order, which yields more suppression on the in-band quantization noise. Not only higher-order modulator has high resolution（SNR）, but also a higher over-sampling has a high resolution（SNR）.

Fig.1.2 shows the z-transfer function of first order delta-sigma modulator including the quantization noise $E_1(z)$.

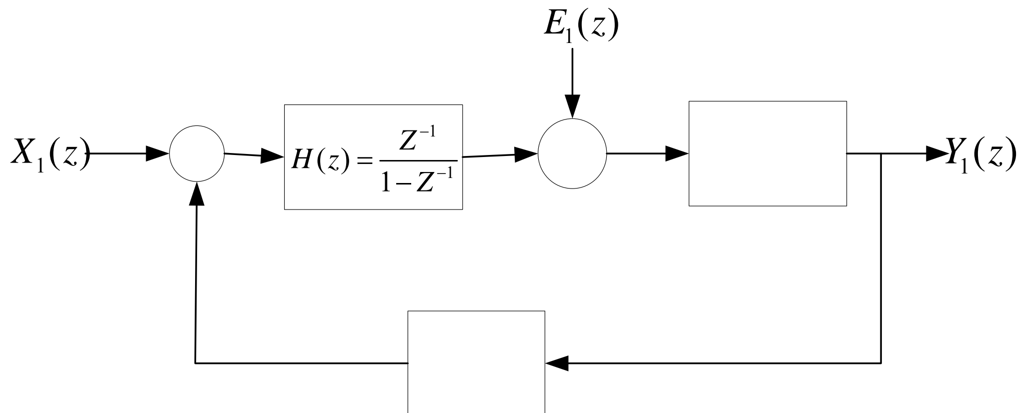
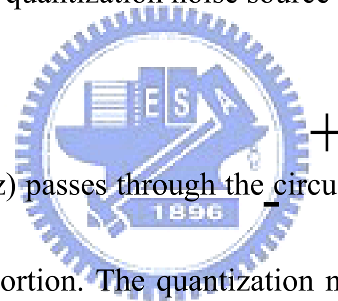


Fig.1.2 The block diagram of the first order delta-sigma modulator including the quantization noise source



In the figure, the input $X_1(z)$ passes through the circuit, after a unit delay, to be the output $Y_1(z)$ without any distortion. The quantization noise $E_1(z)$, is multiplied by a noise-shaping operation $(1\text{-}Z^{-1})$. Therefore, the quantization noise $E_1(z)$ is attenuated. Let the sampling rate be f_s, the passband be f, and the over-sampling ratio（OSR） be defined as $f_s/2$. If OSR>>1, SNR will be large, i.e., the resolution of the ADC is increased.

DAC

$$Y_1(z)=X_1(z)Z^{-1}+E_1(z)(1-Z^{-1}) \qquad (1.1)$$

$$Singal=S(z)=\frac{Y(z)}{X(z)}=Z^{-1}$$

$$Noise=N_1(z)=\frac{Y(z)}{E(z)}=(1-Z^{-1})$$

$$N_1(f) = 1 - e^{-j2\pi f / f_s} = 2j\sin(\frac{\pi f}{f_s}) \times (e^{-j\pi f / f_s})$$

$$|N_1(f)| = 2\sin(\frac{\pi f}{f_s})$$

$$P_S = \frac{\Delta^2 2^{2n}}{8} \quad , \quad OSR = \frac{f_s}{2f}$$

$$SNR_{1\max} = 10\log(\frac{P_S}{P_{N_1}}) = 6.02N + 1.76 - 5.17 + 30\log(OSR) \qquad (1.2)$$

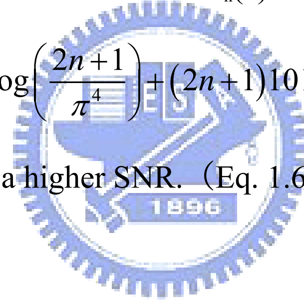
$$SNR_{2\max} = 6.02N + 1.73 - 12.9 + 50\log(OSR) \qquad (1.4)$$

In general, for a higher order (nth order) delta-sigma modulator:

$$S_n(z)X_n(z) + (1 - z^{-1})^n E_n(z) = C_n(z)Y_n(z) \qquad (1.5)$$

where $S_n(z)$ is the signal transfer function and $C_n(z)$ is the output correction function.

$$SNR_{n_\max} = 6.02N + 1.73 - 10\log\left(\frac{2n+1}{\pi^4}\right) + (2n+1)10\log(OSR) \qquad (1.6)$$



A higher-order modulator has a higher SNR.（Eq. 1.6）

1.3 Review of Delta-Sigma Modulator Diagnosis and DFT

There are many diagnosis techniques for analog and digital circuits respectively. Several BIST schemes for DAC and ADC were proposed 【1,2,3】. In【4,5,6】, these authors utilize delta-sigma modulator as signal generation to test analogy circuit. Nevertheless, there are not many papers which proposed self-test for delta-sigma modulator. In【7】, the author utilized the on-chip delta-sigma DAC for sine wave generation and digital signal processing（DSP）techniques to do data analysis. However, the technique needs both on-chip ADC and DAC, and formidable

computation, which is not always possible. In【8】, the ADC which based on oscillation-test method under test is put into an oscillator and the system oscillates between two pre-established codes by the aid of some small additional circuits in the feedback loop. However, these techniques used the characteristics of the transfer function, such as the offset error, gain error, DNL, and INL, as signatures. These parameters are not easy to be measured for a delta-sigma ADC because its output signal is PCM codes.

1.4 Outline of This Thesis

In this paper, we propose and demonstrate a very easy and fast method to diagnose a delta-sigma modulator based on the integrator output voltage. We also propose an application and demonstrate a very simple method which utilizes a delta sigma modulator to test DAC code edges. For this method, since no extra circuit is needed, the delta sigma modulator's performance is not affected. Also we only compute output numbers of logic 1 and logic 0, respectively. Then DAC code edges would be found easily.

This thesis is organized as follows: Chapter 2 presents the proposed test scheme and related analyses. Chapter 3 presents our designed method and the simulation results of process. Chapter 4 presents our proposed application of the delta-sigma

modulation for testing DAC code edges and presents the simulation results. In chapter 5, conclusions are given.

Chapter 2 Proposed Scheme for Delta-Sigma Modulator

2.1 Faults in Delta-Sigma Modulator

Fig.2.1 is the diagram of a first order delta-sigma ADC. The digital decimator which composes of a low-pass filter and a down-sampling circuit, transfers the one bit stream signal to the output. It is digital and the transformation is a pure digital operation. It's testing is relatively easy. Hence we will only discuss the faults in delta-sigma modulator.

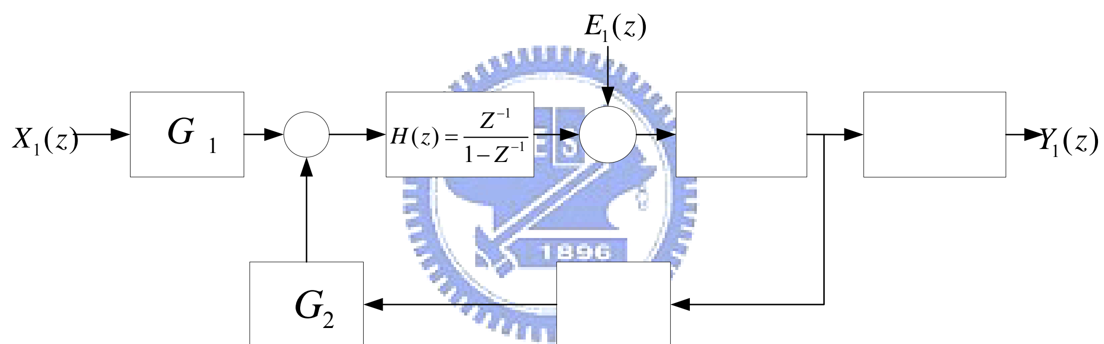


Fig.2.1 Diagram of a first order delta-sigma ADC

In Fig.2.1, the discrete time integrator is activated by two voltage sources, namely, one is the input signal and the other is the feedback signal of the digital output, where G_1 and G_2 represent the forward and feedback gain respectively. Generally, the HIGH level of the output digital signal is V_{ref} and the LOW level is $-V_{ref}$. Thus, each increment of the discrete integrator output is either the positive quantization error (Δp) (Eq. 2.1) or the negative quantization error (Δn) (Eq. 2.2), as shown Fig.2.2.

$$\Delta p = G_1 X + G_2 V_{ref} \tag{2.1}$$

+

-

$$\Delta n = G_1 X - G_2 V_{ref} \tag{2.2}$$

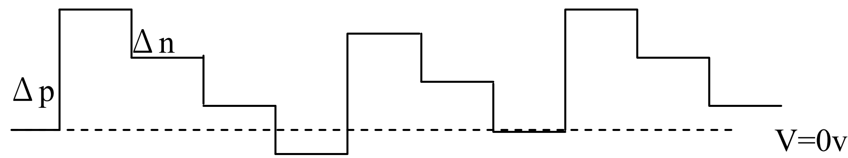


Fig.2.2 The discrete integrator output

We can apply a DC=0 test pattern to diagnose this circuit. Since the over-sampling frequency is much faster than the test pattern and the quantization error for each sampling is only one state Δ（Eq. 2.3）.

$$X = 0$$

$$\Delta = \Delta n = \Delta p = G_2 V_{ref} \tag{2.3}$$

2.1.1 Fault Case

The faults we diagnose are faults in the operational amplifiers, the forward and the feedback gains which are determined by capacitor ratios of switched-capacitor sub-circuits of the delta-sigma modulator. They are discussed as follows:

Case1 **∶** Faults in the comparator.

These faults will cause the output digital signal stuck at either the HIGH or LOW level.

Case2 **∶** Short and open in the circuit.

These faults will also cause the output digital signal stuck at either the HIGH or

LOW level.

Case3 **:** Faults in the operational amplifier.

These faults will cause an offset at the input of the amplifier. 【9】

Case4 **:** Faults in the switched capacitors.

The capacitor ratios deviate from the nominal value. That is, the forward and feedback gain, G_1 and G_2, are different from nominal values.

2.2 Added Circuits for Diagnosis for Delta-Sigma Modulator

In order to diagnose the faults mentioned above, we add extra circuits to the original modulator circuit as shown in Figure 2.3. They are discharge switches, $S_1 \ldots S_n$, in the integrating path of each stage, a test output pin, $V_{testport}$ at the output of the operational amplifier, and multiplexers, mux11 mux12 …muxn1 muxn2 which are to control forward and feedback paths respectively in test mode.

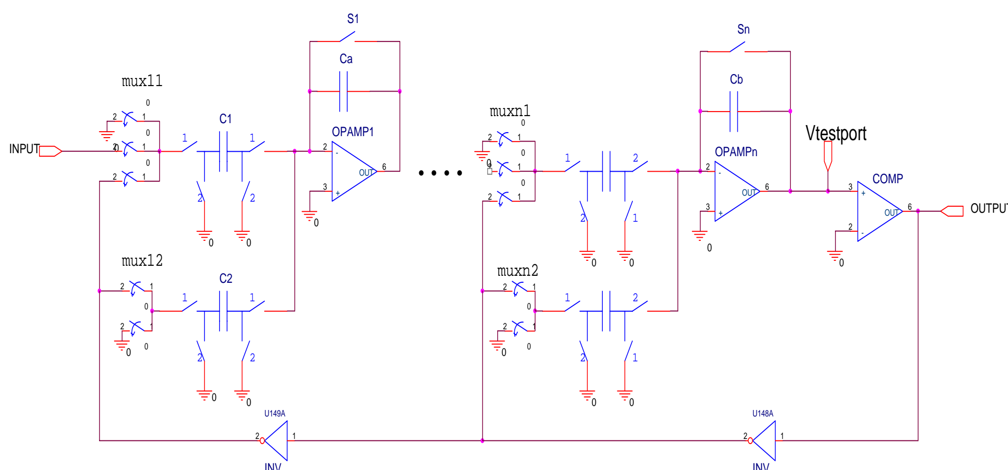


Fig. 2.3 The added extra circuits in the delta-sigma modulator

2.3 Delta-Sigma Modulator Diagnosis

The diagnosis for faults in the modulator is discussed as follows:

The faults in the operational amplifiers will cause an offset in the amplifier's input. To test this type of faults, all the input voltages of the amplifier are set to "ground". The offset voltage will be accumulated to the integrator's output and causes the output to stuck at either the HIGH or LOW which can be measured at $V_{testport}$. For the switched-capacitor faults, they will cause △ difference from the good capacitor ratio. This can be measured also at the $V_{testport}$. The operational amplifiers and switched-capacitor sub-circuits can be diagnosed stage by stage. The diagnosis steps are described in the following by taking a second stage modulator as an example in Figure 2.4.

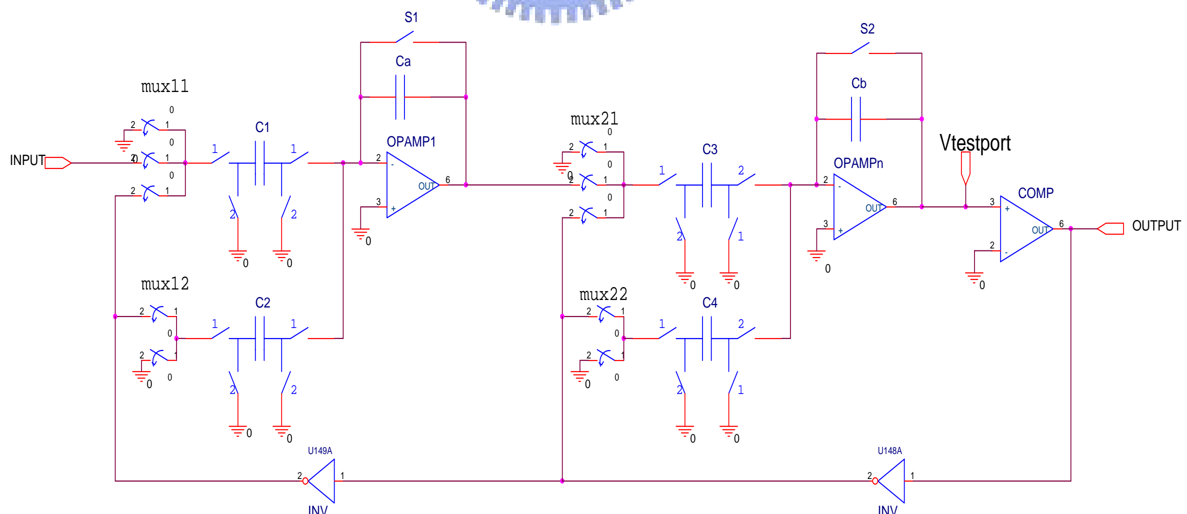


Fig. 2.4 The diagnosis of faults of a second order delta-sigma modulator

Step1：Discharge all charges stored in integrating capacitors by setting S_i=1, i=1~n.

Step2： Set $mux_2 1$ and $mux_2 2$ feedback path to ground as shown in Fig. 2.5 to

diagnose faults in the second stage and go to Step1. We can have

$$V_{testport}(t)=\sum_{k=0}^{t}\frac{C_3+C_4}{C_b}V_{offset2}\times u\left(k-\frac{1}{2}\right)+V_{offset2} \tag{2.4}$$

At t=1/2 clock：

$$V_{testport}1=\frac{C_3+C_4}{C_b}V_{offset2}+V_{offset2} \tag{2.5}$$

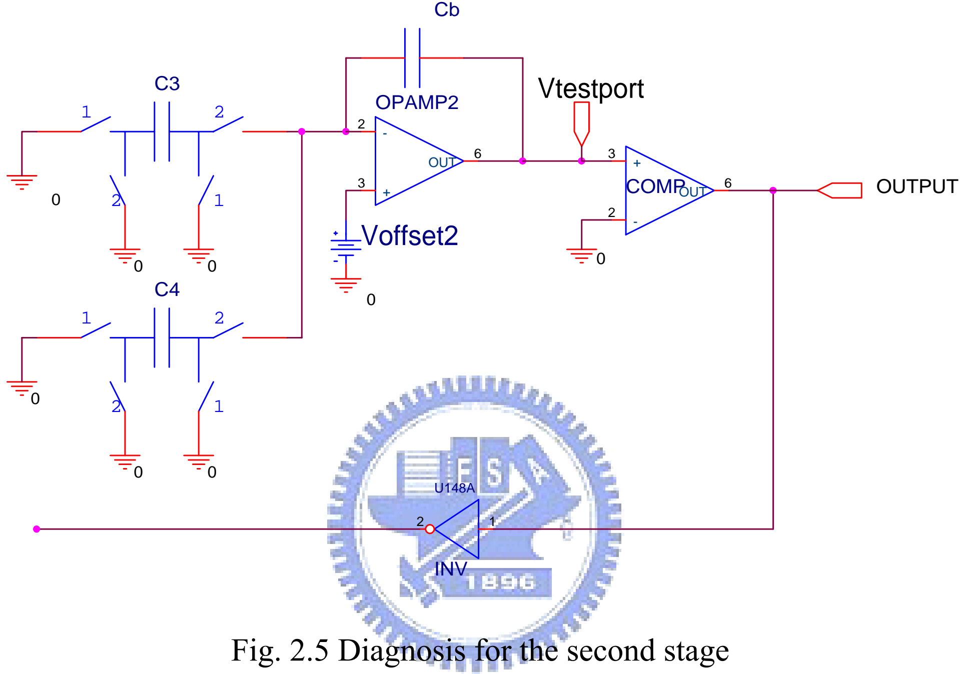


Fig. 2.5 Diagnosis for the second stage

Step3：Set $mux_2 1$ to feedback path and $mux_2 2$ to ground as shown Fig. 2.6 and go to Step1. We can have

$$V_{testport}(t)=\sum_{k=0}^{t}\left[\frac{C_3}{C_b}V_{ref}+\frac{C_3+C_4}{C_b}V_{offset2}\right]u\left(k-\frac{1}{2}\right)+V_{offset2} \tag{2.6}$$

At t=1/2 clock：

$$V_{testport}2=\frac{C_3}{C_b}V_{ref}+\frac{C_3+C_4}{C_b}V_{offset2}+V_{offset2} \tag{2.7}$$

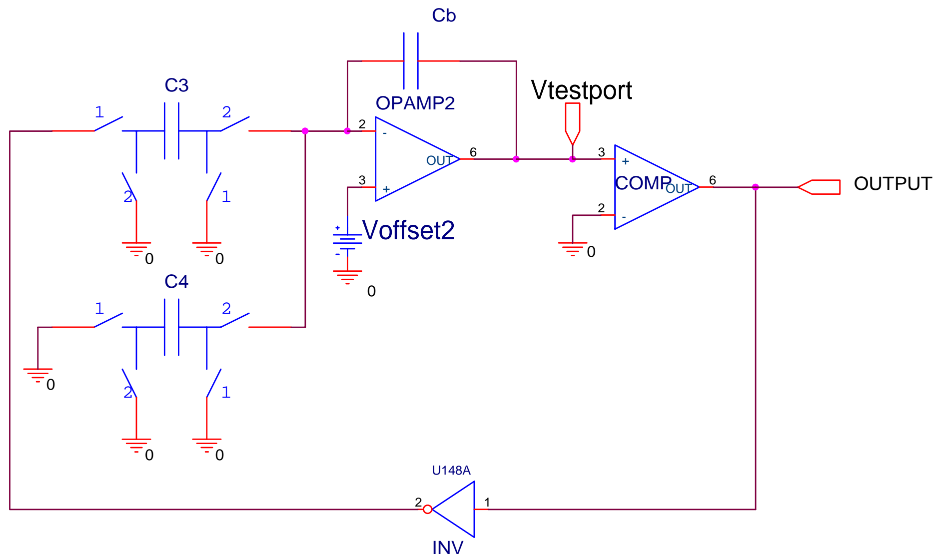


Fig. 2.6 Diagnosis for the second stage

Step4：Set $mux_2 1$ to ground and $mux_2 2$ to feedback path as shown Fig. 2.7 and go to Step1. We can have

$$V_{testport}(t)=\sum_{k=0}^{t}\left[\frac{C_4}{C_b}V_{ref}+\frac{C_3+C_4}{C_b}V_{offset2}\right]u\left(k-\frac{1}{2}\right)+V_{offset2} \tag{2.8}$$

At t=1/2 clock：

$$V_{testport}3=\frac{C_4}{C_b}V_{ref}+\frac{C_3+C_4}{C_b}V_{offset2}+V_{offset2} \tag{2.9}$$

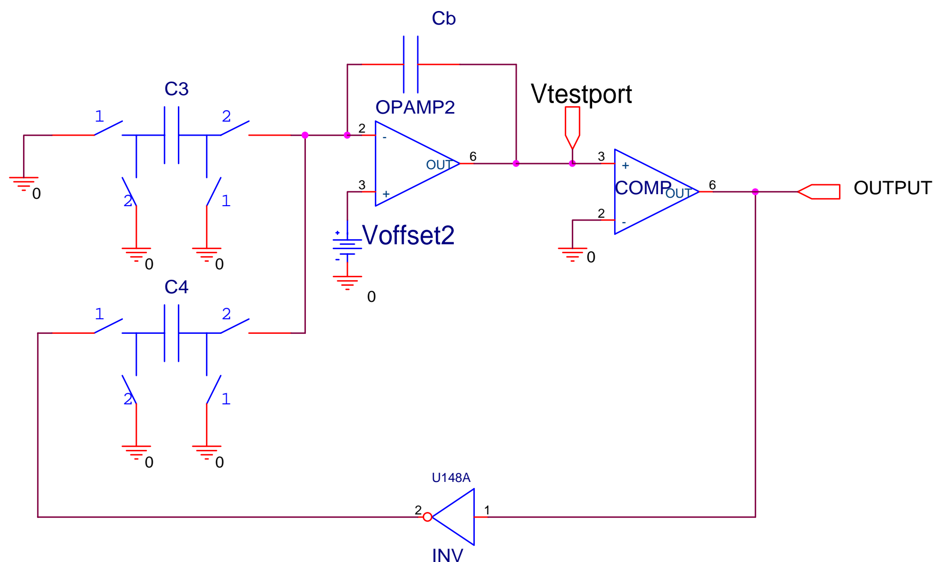


Fig. 2.7 Diagnosis the second stage

From the three equations（2.5, 2.7, 2.9）, we can obtain $V_{offset2}$, C_3/C_b and C_4/C_b of as in Eq's（2.10）(2.11) and (2.12）.

$$V_{offset2} = \frac{V_{testport}1}{1 + \frac{V_{testport}2 + V_{testport}3 - 2V_{testport}1}{V_{ref}}} \quad (2.10)$$

$$\frac{C_3}{C_b} = \frac{V_{testport}2 - V_{testport}1}{V_{ref}} \quad (2.11)$$

$$\frac{C_4}{C_b} = \frac{V_{testport}3 - V_{testport}1}{V_{ref}} \quad (2.12)$$

Then we can start to diagnose for the first stage:

Step5：Set $mux_1 1$, $mux_1 2$ and $mux_2 2$ to ground as shown Fig. 2.8 and go to Step1. We can have

$$V1(t) = \sum_{k=0}^{t} \left(\frac{C_1 + C_2}{C_a} V_{offset1} \right) u\left(k+1\right) + V_{offset1}$$

$$V_{testport}(t) = \sum_{j=0}^{t} \left[V1(j) \frac{C_3}{C_b} + \frac{C_3 + C_4}{C_b} V_{offset2} \right] u\left(j - \frac{1}{2} \right) + V_{offset2} \quad (2.13)$$

At t=1/2 clock：

$$V_{testport}4 = \left(\frac{C_1 + C_2}{C_a} V_{offset1} + V_{offset1} \right) \frac{C_3}{C_b} + \frac{C_3 + C_4}{C_b} V_{offset2} + V_{offset2} \quad (2.14)$$

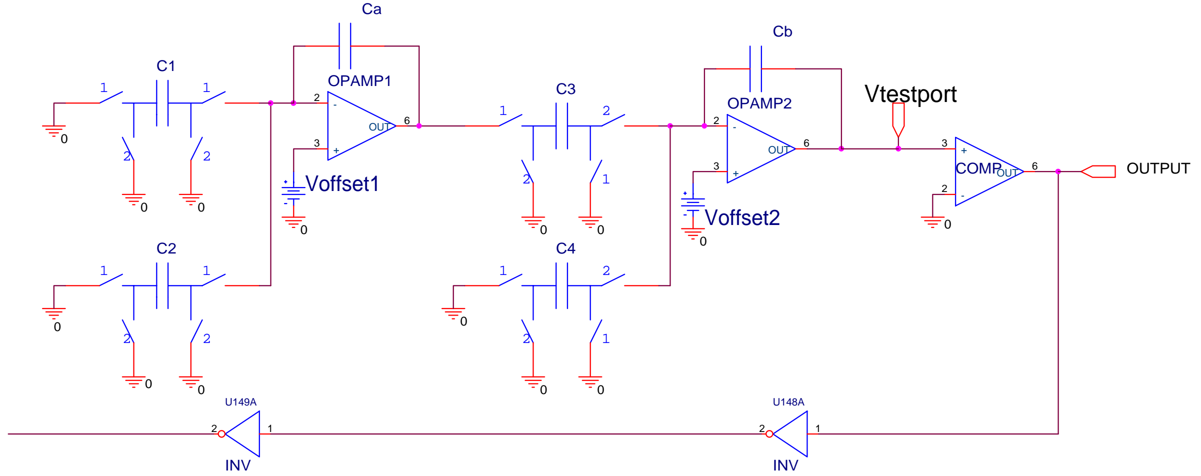


Fig. 2.8 Diagnosis for the first stage

Step6：Set $mux_1 1$ to feedback path, $mux_1 2$ and $mux_2 2$ to ground as shown in Fig. 2.9

and go to Step1. We can have

$$V1(t)=\sum_{k=0}^{t}\left(\frac{C_1}{C_a}V_{ref}+\frac{C_1+C_2}{C_a}V_{offset1}\right)u(k+1)+V_{offset1}$$

$$V_{testport}(t)=\sum_{j=0}^{t}\left[V1(j)\frac{C_3}{C_b}+\frac{C_3+C_4}{C_b}V_{offset2}\right]u\left(j-\frac{1}{2}\right)+V_{offset2} \tag{2.15}$$

At t=1/2 clock：

$$V_{testport}5=\left(\frac{C_1}{C_a}V_{ref}+\frac{C_1+C_2}{C_a}V_{offset1}+V_{offset1}\right)\frac{C_3}{C_b}+\frac{C_3+C_4}{C_b}V_{offset2}+V_{offset2} \tag{2.16}$$

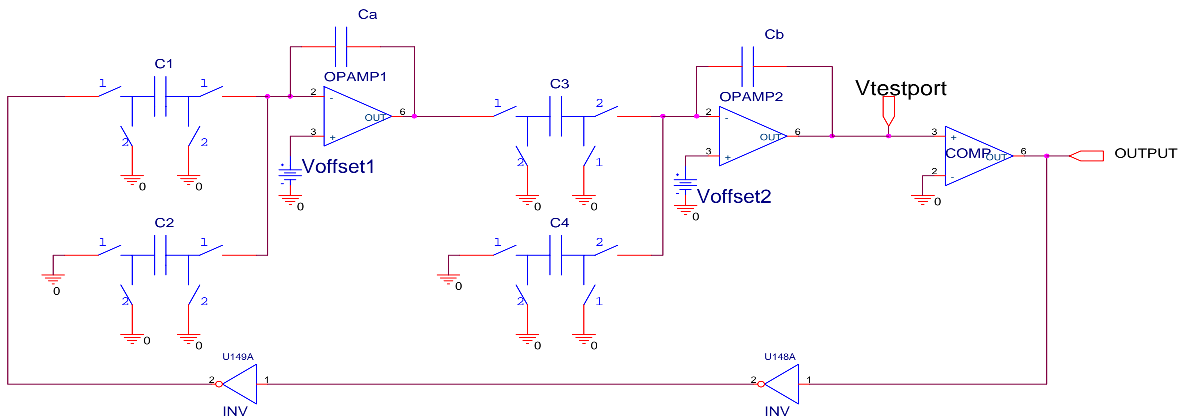


Fig. 2.9 Diagnosis for the first stage

Step7：Set $mux_1 2$ to feedback path, $mux_1 1$ and $mux_2 2$ to ground as shown Fig. 2.10 and go to step1. We have

$$V1(t) = \sum_{k=0}^{t}\left(\frac{C_2}{C_a}V_{ref} + \frac{C_1+C_2}{C_a}V_{offset1}\right)u\left(k+1\right)+V_{offset1}$$

$$V_{testport}(t) = \sum_{j=0}^{t}\left[V1(j)\frac{C_3}{C_b} + \frac{C_3+C_4}{C_b}V_{offset2}\right]u\left(j-\frac{1}{2}\right)+V_{offset2} \quad (2.17)$$

At t=1/2 clock：

$$V_{testport}6 = \left(\frac{C_2}{C_a}V_{ref} + \frac{C_1+C_2}{C_a}V_{offset1}+V_{offset1}\right)\frac{C_3}{C_b} + \frac{C_3+C_4}{C_b}V_{offset2}+V_{offset2} \quad (2.18)$$

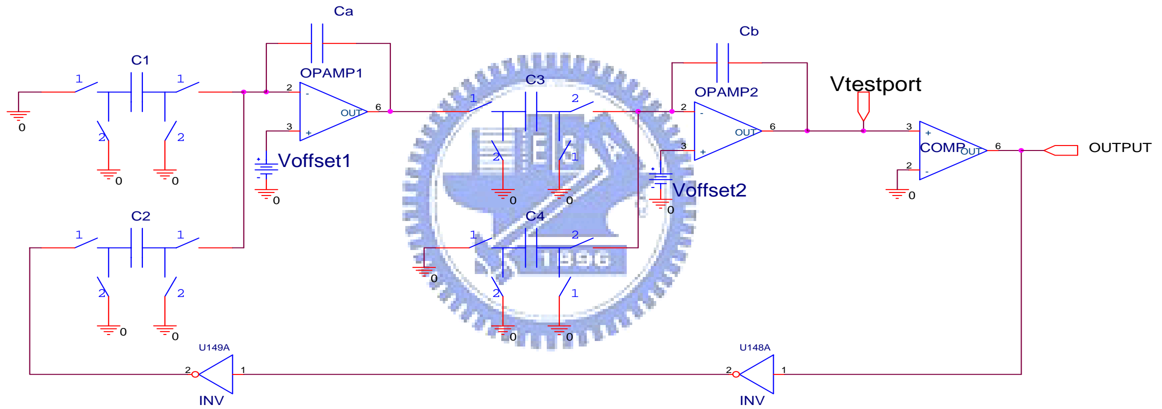


Fig. 2.10 Diagnosis for the first stage

Step8：Continue the above steps if there are more stages until all stage are diagnosed.

With Eq's（2.14） (2.16) and (2.18）, we can obtain $V_{offset1}$, C_1/C_a and C_2/Ca as shown in Eq's（2.19）(2.20) and (2.21）. Therefore we can diagnose all faults, including single fault and double faults.

$$V_{testport}4 = \left(\frac{C_1+C_2}{C_a}V_{offset1}+V_{offset1}\right)\frac{C_3}{C_b} + \frac{C_3+C_4}{C_b}V_{offset2}+V_{offset2}$$

$$V_{offset1} = \frac{\left(V_{testport}4 - \frac{C_3 + C_4}{C_b}V_{offset2} - V_{offset2}\right)\frac{C_b}{C_3}}{1 + \frac{1}{V_{ref}}\frac{C_b}{C_3}\left(V_{testport}5 + V_{testport}6 - 2V_{testport}4\right)}$$

$$V_{offset1} = \frac{\left(V_{testport}4 - \frac{C_3 + C_4}{C_b}V_{offset2} - V_{offset2}\right)V_{ref}}{V_{ref}\frac{C_3}{C_b} + \left(V_{testport}5 + V_{testport}6 - 2V_{testport}4\right)} \tag{2.19}$$

$$\frac{C_1}{C_a} = \frac{1}{V_{ref}}\frac{C_b}{C_3}\left(V_{testport}5 - V_{testport}4\right) \tag{2.20}$$

$$\frac{C_2}{C_a} = \frac{1}{V_{ref}}\frac{C_b}{C_3}\left(V_{testport}6 - V_{testport}4\right) \tag{2.21}$$

2.4 Possible Problems of the DFT Scheme

There are some problems which need to be considered for this DFT scheme. One problem is, for the switch capacitor circuit, the clock feedthrough is an important issue. Since there are added extra switches in our proposed DFT scheme, the clock feedthrough is also a problem which needs to be considered. Another problem is for the operational amplifier, the gain needs to be high in order to suppress harmonic distortion caused by the opamp nonlinearity if any. The next chapter will propose some methods to reduce error.

Chapter 3 Design of the Delta-Sigma Modulator and Simulation Results

In this chapter, a second order delta-sigma modulator is designed and simulation results are presented.

3.1 Delta-Sigma Modulator Design

3.1.1 Switches

When a MOS switch is ON（clk=1）, it operates in the triode region, while it MOS turns FF（clk=0）, the charge injection error occurs due to two mechanisms as shown Fig.3.1. The first mechanism is due to channel charges which flow out of the channel region of the MOS to the drain and to the source junction. It will cause an error voltage at the load capacitor（C_{hold}）shown as Eq.（3.1）.

$$\Delta Q_{Chold} = \frac{Q_{ch}}{2} = \frac{C_{ox}WL(V_{gs} - V_{tn})}{2} = \frac{C_{ox}WL(V_{DD} - V_{in} - V_{tn})}{2}$$
$$\Delta V_{out} = \frac{\Delta Q_{Chold}}{C_{hold}} = -\frac{C_{ox}WL(V_{DD} - V_{in} - V_{tn})}{2C_{hold}} \quad (3.1)$$

The second mechanism is due to the overlap capacitance between the gate and the junction. The charges in this overlapped capacitance will also cause an error voltage on the load capacitor（C_{hold}）shown as Eq.（3.2）.

$$\Delta V_{out} = \Delta V_{Chold} = \frac{Q_{Chold}}{C_{hold}} = \frac{\Delta V_{clk} C_{ov}}{C_{ov} + C_{hold}}$$
$$\Delta V_{out} = -\frac{C_{ov}(V_{DD} - V_{SS})}{C_{ov} + C_{hold}} = -\frac{C_{ox}WL_{ov}(V_{DD} - V_{SS})}{C_{ov} + C_{hold}} \quad (3.2)$$

Hence, the total error voltage is:

$$\Delta V_{Charge_Injection_Error} = \Delta V_{Overlap_Capacitor_Charge} + \Delta V_{Channel_Charge} \quad (3.3)$$

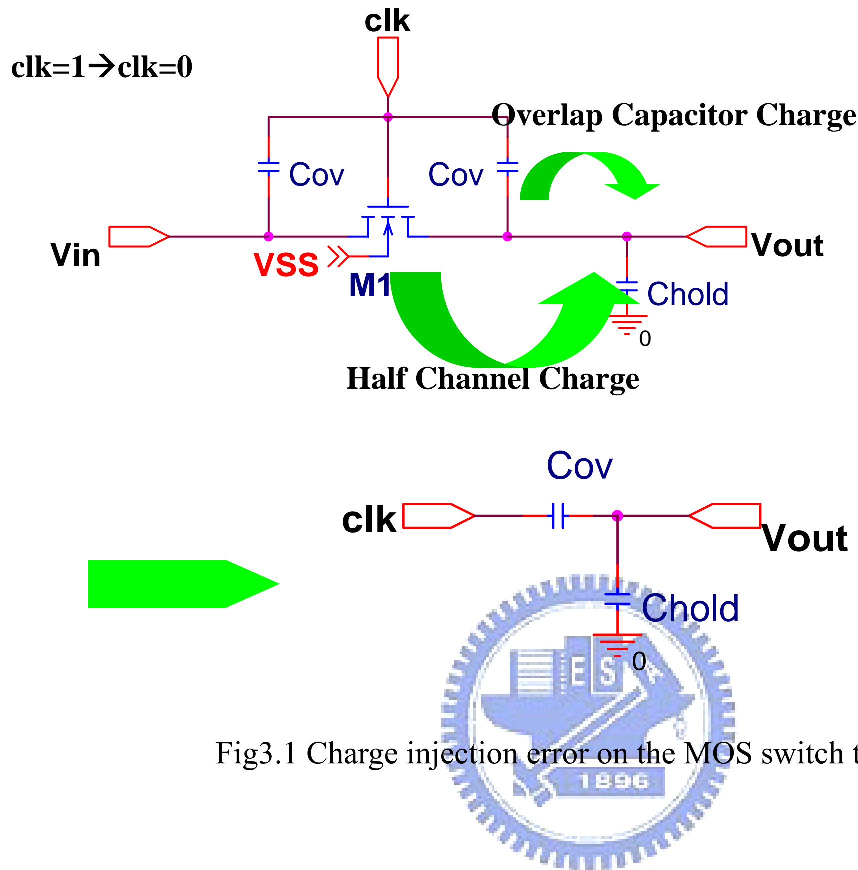


Fig3.1 Charge injection error on the MOS switch transistor

To minimize charge injection error, we add a dummy switch, as shown Fig. 3.2 【10】, where the channel widths of M3 and M4 are taken as one-half of that of M1 and M2 respectively and the clock of M1 and M2 changes slightly after that of M3 and M4 respectively. The clock arrangement guarantees that the canceling charges of M3 and M4 do not escape through M1 and M2 respectively when they are still ON.

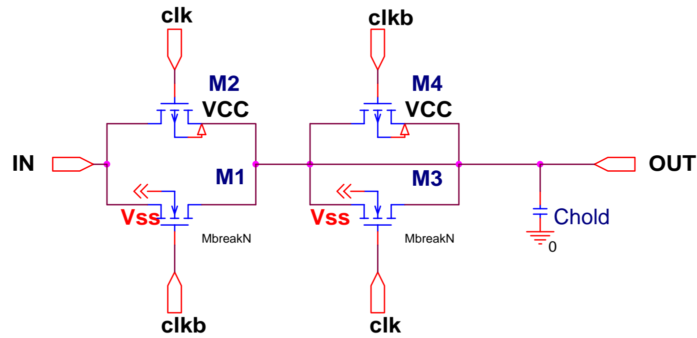


Fig. 3.2 A dummy CMOS switch for charge injection cancellation

3.1.2 Clock

The switch capacitors are controlled by two phase clocks, as shown Fig.3.3. Because Clock1 and Clock2 may cause overlap, the output will cause error. The improved method Fig.3.4 shows a simple digital circuit that is capable of generating the desired clocks【11】which avoid overlapping.

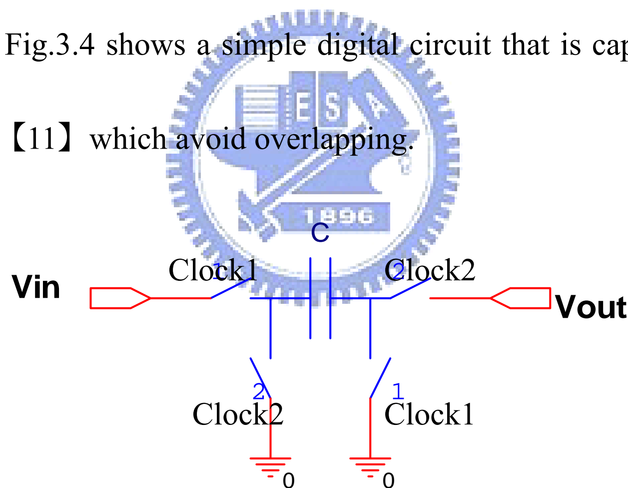


Fig.3.3 Switch capacitor

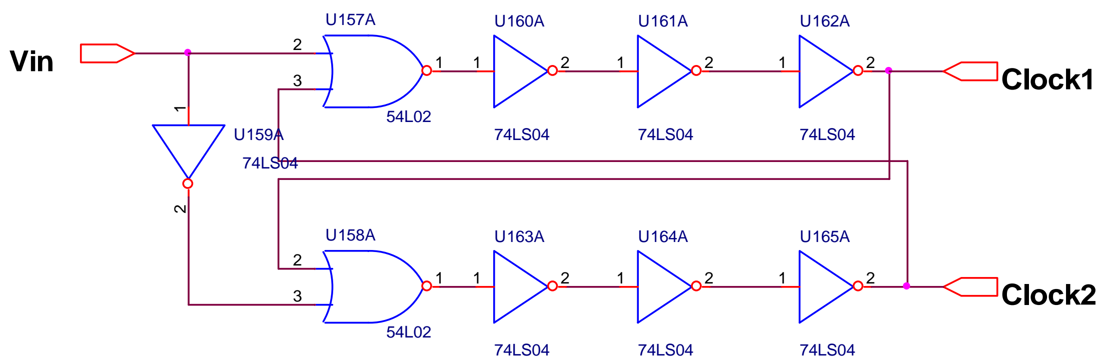


Fig.3.4 A clock generator which can generate the non-overlapped clocks

3.1.3 Operational amplifier

The operational amplifier is most important component in the design of the sigma-delta modulator. In practice, this gain needs to be high in order to suppress the harmonic distortion caused by opamp nonlinearities【11,12】. A practical CMOS version of the two-stage opamp is shown in Fig. 3.5.

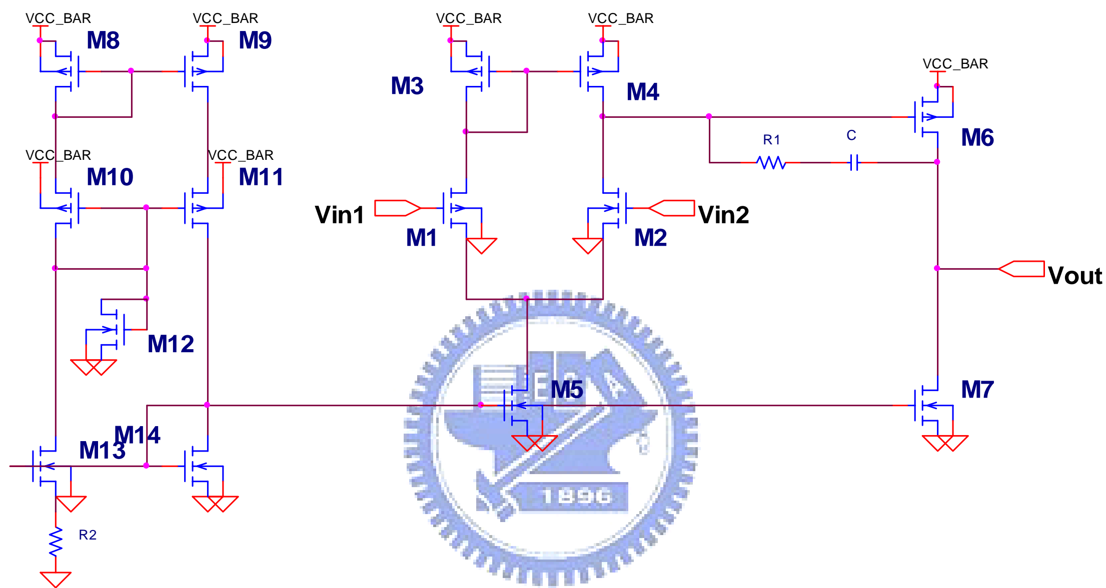


Fig. 3.5 A CMOS realization of a two-stage amplifier

3.1.4 Comparator

The purpose of the comparator is to quantize a signal and provide the output of the modulator. This output is fed to 1-bit DAC, which converts digital signal to the analog signal in the feedback modulator loop. We combine opamp with a D-type flip-flop (DFF) to realize the comparator in our design.

3.2 Simulation Results

In our design shown Fig.2.4, the capacitor sizes are C_1=0.4pF, C_2=0.8pF, C_A=4pF, C_3=1.5pF, C_4=0.3pF, C_B=3pF respectively and the sampling frequency f_{clock}= 1MHz and the comparator output reference voltage is $\pm$1.8 V. The UMC 0.18 library cells were used to implement the circuit. to simulate. The whole circuit was simulated. An error ratio is defined as:

$$Define: error_ratio \triangleq \frac{(capacitor_ratio)_{diagnosis} - (capacitor_ratio)_{ideal}}{(capacitor_ratio)_{ideal}} \times 100\% \quad (3.4)$$

The simulation results for the good circuit are presented in Table 3.1 and those for the faulty circuits, where faults were injected intentionally, are presented in Table 3.2 and Table 3.3 for each fault respectively. In Table 3.1, Ideal means that the original ideal values for capacitors, real is the values obtained through the diagnosis procedure, and Error Ratio is that obtained from Eq. (3.4).

Ratio	Ideal	Real	error_ratio
C_1/C_a	0.1	0.09978	-0.221%
C_2/C_a	0.2	0.19955	-0.226%
C_3/C_b	0.5	0.49836	-0.328%
C_4/C_b	0.1	0.09971	-0.286%
C_a=4pF C_b=3pF C_1=0.4pF C_2=0.8pF C_3=1.5pF C_4=0.3pF $\pm V_{ref} = \pm 1.8V$			

Table3.1 Simulation results for the good modulator

3.2.1 Case 1 : Single Fault

Table 3.2 shows the diagnosis results through simulation for injected single faults. For each column, it lists the injected faults; and for each row, it lists the simulated Error Ratio values for each capacitance ratio or V_{offset} under each injected fault. For example, we inject a C_1 +20% fault and the simulated Error Ratio value obtained for C_1/C_a by using the diagnosis procedure is 19.73% and for other capacitance ratios are less than 0.3%. By observing the values, we can then tell that the fault is that occurs at C_1/C_a. For operational amplifier 1, we injected an *Offset1*=10mV fault. The simulated result on $V_{offset1}$ is 9.64 mV and that for $V_{offset2}$ is 0.039 mV. We can tell that the fault occurs at operational amplifier 1 with a magnitude of 9.84mV which is approximately 10 mV. The error is equal to 1.6% and the other offset error are in the tolerance bound (±5%).

error_ratio	C_1+20%	C_2+20%	C_3+20%	C_4+20%	C_a+20%	C_b+20%	$V_{offset1}$=10mV	$V_{offset2}$=-10mV
C_1/C_a	19.73%	-0.229%	-0.204%	-0.221%	-16.84%	-0.231%	-0.222%	-0.222%
C_2/C_a	-0.23%	19.72%	-0.209%	-0.226%	-16.85%	-0.235%	-0.227%	-0.227%
C_3/C_b	-0.328%	-0.328%	19.56%	-0.332%	-0.328%	-16.92%	-0.328%	-0.326%
C_4/C_b	-0.286%	-0.286%	-0.304%	19.65%	-0.286%	-16.89%	-0.286%	0.285%
$V_{offset1}$							9.84mV	-0.227mV
$V_{offset2}$							0.039mV	-10.06mV

Table3.2 Analysis results for single fault cases

3.2.2 Case 2: *Multiple Faults (Double Faults)*

This procedure can diagnose for multiple faults. In experiments, we injected double faults to demonstrate this and the results are shown in Table 3.3A-E. In the table, for instance, we inject C_1 +20% and C_2 +20% faults and the Error Ratio obtained through simulation for this diagnosis procedure are C_1/C_a = 19.72% and C_2/C_a = 19.71% respectively and all other capacitor ratios are within a tolerance bound (±5%).

error_ratio	C_1+20% C_2+20%	C_1+20% C_3+20%	C_1+20% C_4+20%	C_2+20% C_3+20%	C_2+20% C_4+20%	C_3+20% C_4+20%
C_1/C_a	19.72%	19.56%	19.73%	-0.212%	-0.229%	-0.204%
C_2/C_a	19.71%	-0.213%	-0.229%	19.74%	19.72%	-0.209%
C_3/C_b	-0.328%	19.56%	-0332%	19.56%	-0.332%	19.56%
C_4/C_b	-0.286%	-0.304%	19.65%	-0.304%	19.65%	19.63%

Table3.3A Analysis results for multiple faults cases

error_ratio	C_a+20% C_3+20%	C_a+20% C_4+20%	C_b+20% C_1+20%	C_b+20% C_2+20%	C_a+20% C_b+20%
C_1/C_a	-16.83%	-16.84%	19.72%	-0. 239%	-16.85%
C_2/C_a	-16.83%	-16.85%	-0.239%	19.71%	-16.85%
C_3/C_b	19.56%	-0.332%	-16.92%	-16.92%	-16.92%
C_4/C_b	-0.304%	19.65%	-16.89%	-16.89%	-16.89%

Table3.3B Analysis results for multiple faults cases

error_ratio	C_1+20% $V_{offset1}$=10mV	C_2+20% $V_{offset1}$=10mV	C_3+20% $V_{offset1}$=10mV	C_4+20% $V_{offset1}$=10mV	C_a+20% $V_{offset1}$=10mV
C_1/C_a	19.73%	-0.23%	-0.205%	-0.222%	-16.84%
C_2/C_a	-0.231%	19.72%	-0.21%	-0.226%	-16.85%
C_3/C_b	-0.328%	-0.328%	19.56%	-0.332%	-0.238%
C_4/C_b	-0.286%	-0.286%	-0.304%	19.56%	-0.286%
$V_{offset1}$	9.84mV	9.84mV	9.86mV	9.84mV	9.84mV
$V_{offset2}$	-0.039mV	-0.039mV	-0.039mV	-0.038mV	-0.039mV

Table3.3C Analysis results for multiple faults cases

error_ratio	C_b+20% $V_{offset1}$=10mV	C_1+20% $V_{offset2}$= -10mV	C_2+20% $V_{offset2}$= -10mV	C_3+20% $V_{offset2}$= -10mV	C_4+20% $V_{offset2}$= -10mV
C_1/C_a	-0.232%	19.73%	-0.23%	-0.206%	-0.221%
C_2/C_a	-0.236%	-0.231%	19.72%	-0.211%	-0.227%
C_3/C_b	-16.92%	-0.326%	-0.326%	19.57%	-0.33%
C_4/C_b	-16.89	-0.285%	-0.285%	-0.303%	19.65%
$V_{offset1}$	9.84mV	-0.223mV	-0.219mV	-0.2mV	-0.226mV
$V_{offset2}$	-0.032mV	-10.06mV	-10.06mV	-10.06mV	-10.06mV

Table3.3D Analysis results for multiple faults cases

error_ratio	C_a+20% $V_{offset2}$= -10mV	C_b+20% $V_{offset2}$= -10mV	$V_{offset1}$=10mV $V_{offset2}$= -10mV
C_1/C_a	-16.84%	-0.232%	-0.224%
C_2/C_a	-16.85%	-0.236%	-0.228%
C_3/C_b	-0.326%	-16.91%	-0.326%
C_4/C_b	-0.285%	-16.89%	-0.285%
$V_{offset1}$	-0.28mV	-0.215mV	9.79mV
$V_{offset2}$	-10.06mV	-10.05mV	-10.06mV

Table3.3E Analysis results for multiple faults cases

3.2.3 Monte Carlo Simulation：

When the error component C_1 increases by 20% and the other component parameters were allowed to vary with a $3\sigma = \pm$ 5% tolerance, the results through the Monte Carlo simulation are shown in Fig.3.6, where the vertical axis is C_1/Ca error ratio and the horizontal axis is Ca deviation for 100 points. These error ratios have shown narrow band. Therefore this diagnosis method is very accurate.

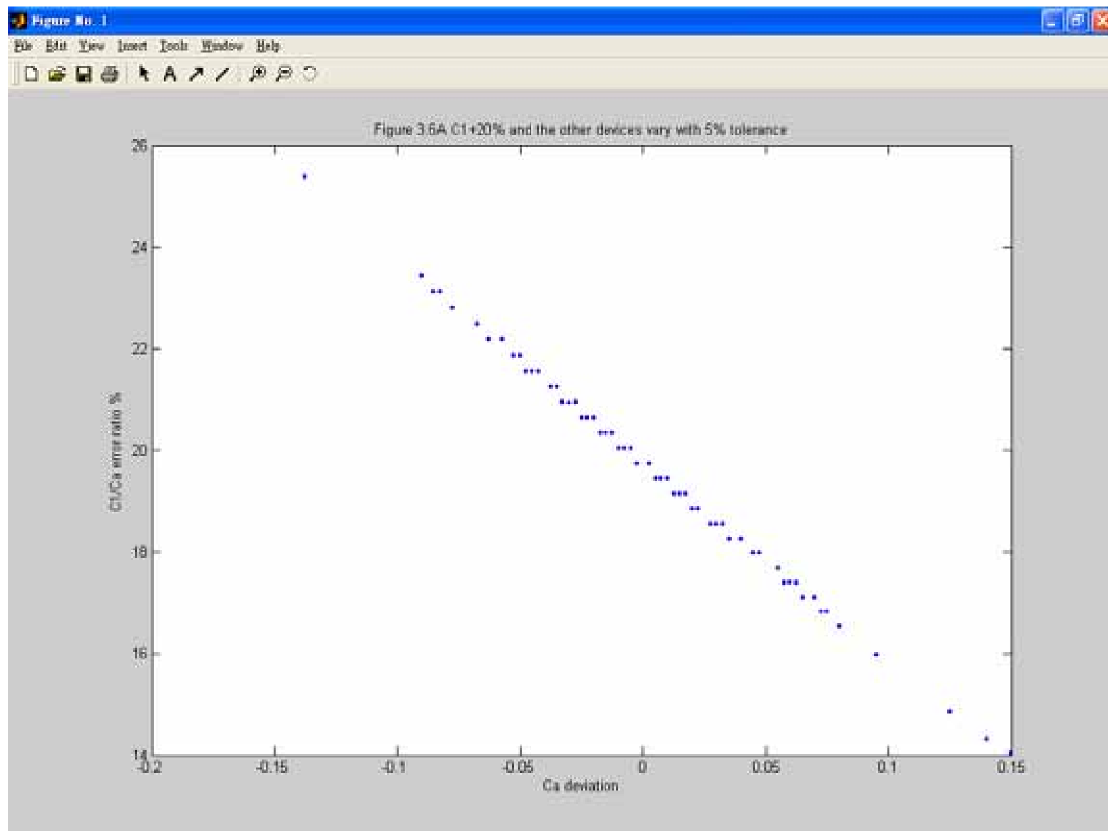


Fig. 3.6 C_1+20% and the other devices vary with a $3\sigma = \pm$ 5% tolerance

Chapter 4 Application of Delta-Sigma Modulator for DAC Code Edge Measurement

Most analog tests rely on specification based test, which requires arbitrary waveform generators (AWG) and digitizers in an ATE. During the past several years, many paper used the delta-sigma modulator as sinusoidal generation to test ADC or analog circuits【5, 6, 7, 14, 15, 16】.

In this chapter we propose a method for measurement for code edges of a DAC by using the delta-sigma modulator. The technique is composed of inserting the 2-to-1 de-multiplexer as one bit DAC with the output of the DAC-under-test connected to its input in the delta-sigma modulator oscillating loop. And during testing, the input of the delta-sigma modulator is applied a zero input. Then, the delta-sigma modulator PDM output is used as the test output. The method does not require any added extract switch or circuit in the delta-sigma modulator, so it does not affect performance of the delta-sigma modulator. We only count the numbers of logic 1 and logic 0 of the delta-sigma modulator output, respectively to derive the DAC code edges. Parameters such as INL error, DNL error, offset error and gain error the DAC can be measured.

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i) - V_{LSB}}{V_{LSB}} LSB \tag{4.1}$$

$$INL(i) = \frac{V_{out}(i) - V_{ref}(i)}{V_{LSB}} LSB \tag{4.2}$$

$$INL(i) = \sum_{k=0}^{i-1} DNL(k) + C \tag{4.3}$$

$$E_{off} = \frac{V_{out}}{V_{LSB}}\Big|_{0....0} \tag{4.4}$$

$$E_{gain} = \left(\frac{V_{out}}{V_{LSB}}\Big|_{1...1} - \frac{V_{out}}{V_{LSB}}\Big|_{0...0} \right) - \left(2^n - 1\right) \tag{4.5}$$

4.1 The Idea of the DAC Measurement

For a delta-sigma modulator, the quantization noise $E_1(z)$ dues to ADC and the integrator non-idealities can be suppressed by noise shaping（1.1）. However, delta-sigma modulation suffers from the non-ideal DAC, denoted as E_{DAC}, since it can not be suppressed neither by over-sampling nor by noise shaping of the modulator. Fig 4.1 shows a block diagram of the modulator including this effect, where a noise source, E_{DAC}, is added at the output of the DAC. The output $Y_1(z)$ is then able to be expressed as:

$$Y_1(z) = X_1(z)Z^{-1} - E_{DAC}(z)Z^{-1} + E_1(z)(1 - Z^{-1}) \tag{4.6}$$

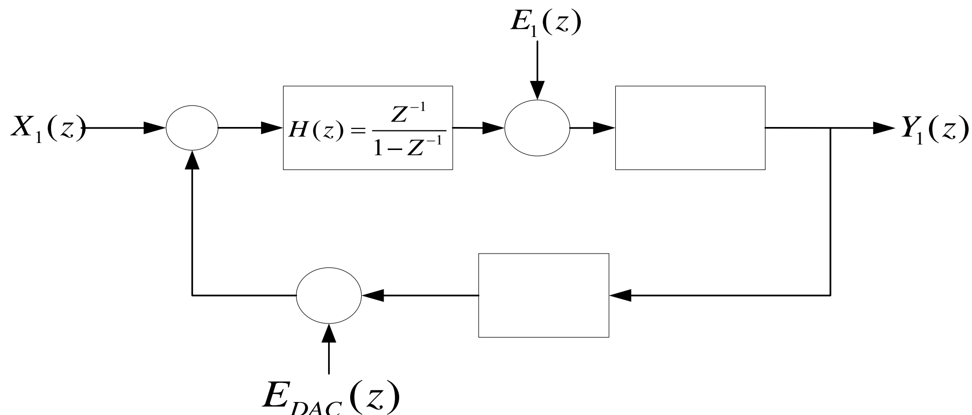


Fig. 4.1 Block diagram of a first order delta-sigma modulator with the equivalent

noise caused by DAC non-ideality included

The main idea for this measurement scheme is that a DAC-under-test is put to be the DAC in the above circuit and the input $X_1(z)$ is set to be zero. Then Eq.（4.6）becomes:

$$Y_1(z) = -E_{DAC}Z^{-1} + E_1(z)(1 - Z^{-1}) \tag{4.7}$$

It means that by quantifying the PDM output of $Y_1(z)$ over a long period (i.e. $Z \approx 1$), we can accurately measure the mean value of E_{DAC}. We can use a counter to count the bit stream of the modulator PDM output over a long period and the long averaging period results in high measurement accuracy. Then DAC code edges, offset error, DNL error, INL error and gain error can be directly measured by evaluating the output digital bit stream【16】.

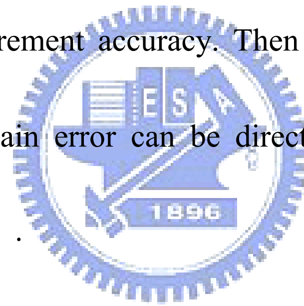


Fig.4.2 shows a first order delta-sigma modulator. The output of the DAC-under-test is connected to one of two inputs of the 2-to-1 multiplexer whose control pin is connected to the output of the modulator. In the normal mode, the input of the operational amplifier gets the value of $\pm V_{ref}$ according to the output of the modulator so that the modulator works as a normal modulator. In the test mode, the input delta-sigma modulator is zeroed and the input of the 2-to-1 multiplexer is connected to the output of the DAC-under-test as shown in Fig. 4.3 to measure the code edge voltage of the DAC-under-test. If we are to measure the DAC negative

code edges, we connect it to the negative input of the 2-to-1 multiplexer with $+V_{ref}$ connected to the other multiplexer input as shown in Fig.4.3; if we are to measure the DAC positive code edges, we connect it to the positive input of the 2-to-1 multiplexer with $-V_{ref}$ connected to the other multiplexer input as shown in Fig.4.4. The 1/0 counter evaluates numbers of “1” (N1) and “0” (N0) of the PDM bit stream over a period of time T_n. Then, we use the following Eq’s to derive the code edge voltages:

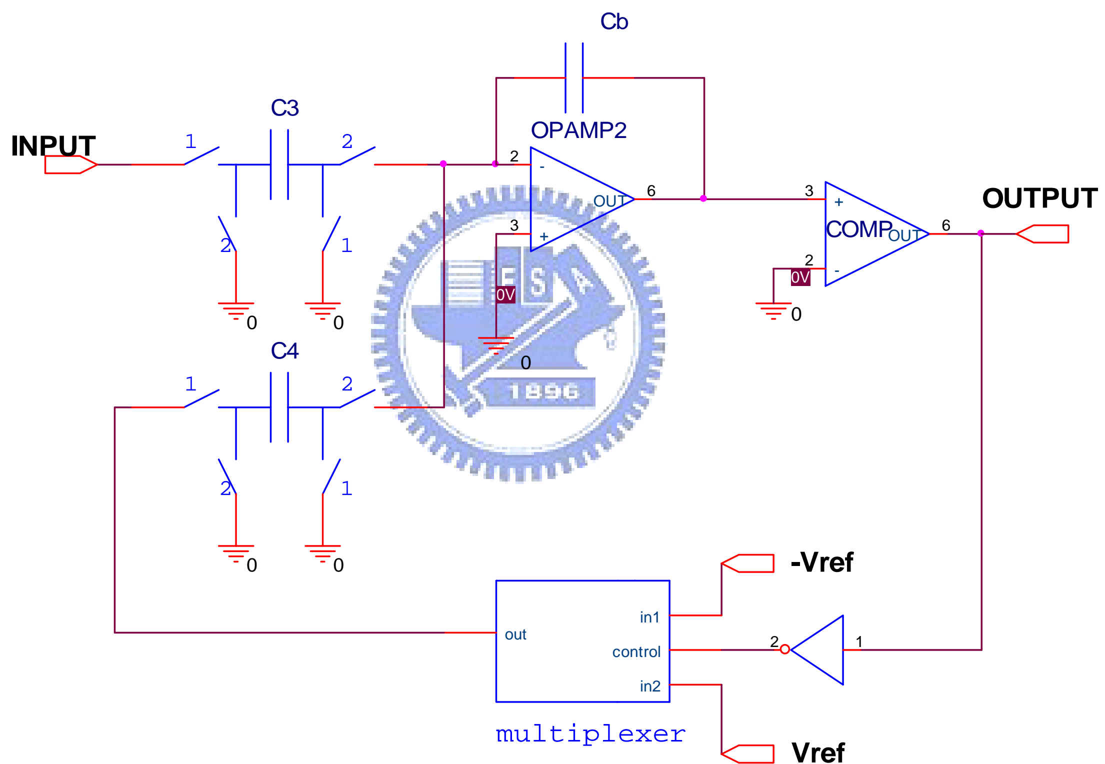


Fig.4.2 Block diagram of a first order delta-sigma modulation working in the normal mode

$$N0V_{CUT}\frac{C_4}{C_b}+N1V_{ref}\frac{C_4}{C_b}+(N0+N1)\frac{C_3+C_4}{C_b}error=0 \tag{4.8}$$

$$-N0V_{ref}\frac{C_4}{C_b}+N1V_{CUT}\frac{C_4}{C_b}+(N0+N1)\frac{C_3+C_4}{C_b}error=0 \tag{4.9}$$

$$V_{CUT}=-\frac{N1V_{ref}}{N0}-\frac{(N0+N1)error}{N0}\left(\frac{C_3+C_4}{C_4}\right) \tag{4.10}$$

$$V_{CUT}=\frac{N0V_{ref}}{N1}-\frac{(N0+N1)error}{N1}\left(\frac{C_3+C_4}{C_4}\right) \tag{4.11}$$

, where the *error* includes the operational amplifier's offset and the distortion caused by the non-ideality in circuits such as sample-and-hold.

Once code edges are obtained, the DNL error, INL error, offset error and gain error can be derived by Eq's（4.1）, (4.3), (4.4) and (4.5）, respectively.

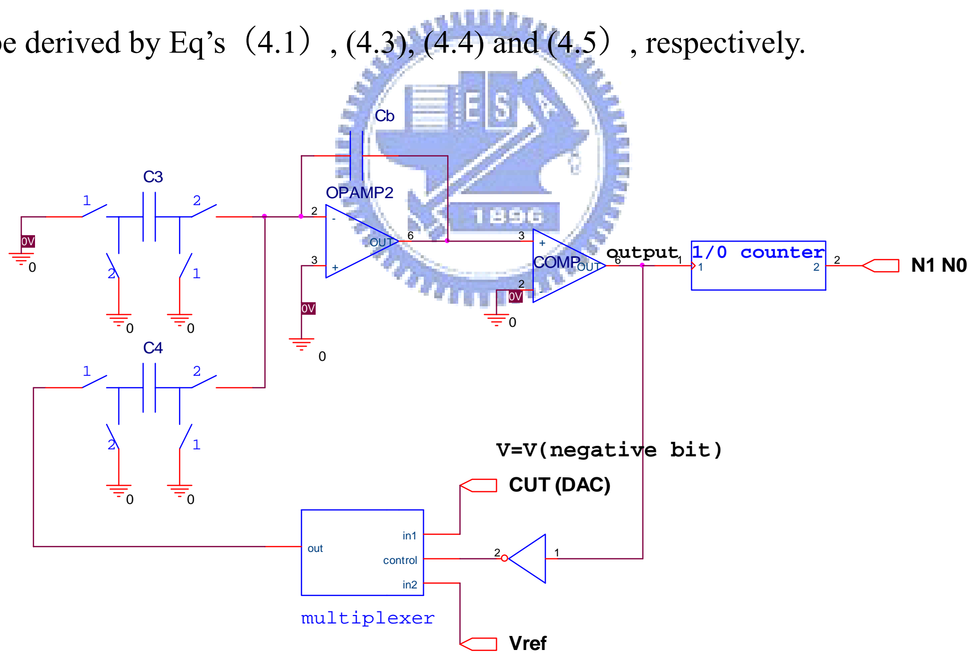


Fig. 4.3 The modulator set-up to measure the DAC negative code edges

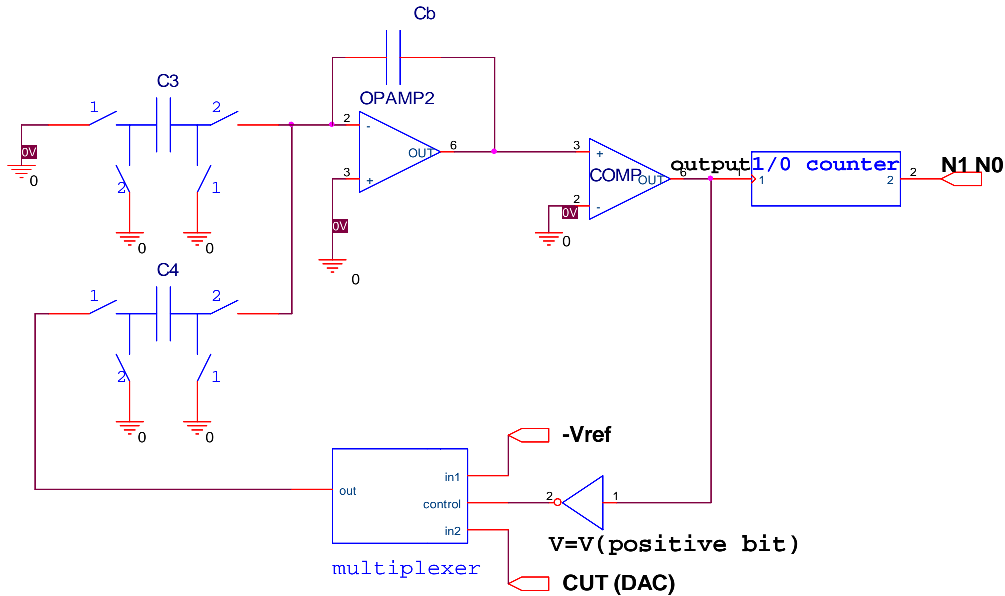


Fig. 4.4 The modulator to measure the DAC positive code edges

4. 2 Error Analysis via Simulation

In the proposed delta-sigma modulator measuring circuit of the above chapter, there are some error sources which may affect the measurement accuracy of the circuit. Those error sources include those discussed in Chapter 3 in switches, comparator, and operational amplifier. In this chapter, we do an analysis on the measurement error of the proposed circuit via SPICE simulation. The simulation is done by considering the process variation on the device parameters on switches, comparator and operational amplifiers.

A first order delta-sigma modulator measurement circuit was first designed in the same way as that described in chapter 3 with the capacitor sizes: C_3=1pF, C_4=1pF, C_B=4pF, and $\pm V_{ref} = \pm 1$ V. The sampling frequency f_{clock}= 1MHz, the comparator

output reference voltage is ±1.8 V.

First, Fig.4.5 shows the simulated output of the delta-sigma modulator over the time period T_n=6u and the output of the integrator of the circuit. In the figure, N1 = 1 and N0 = 5, the code edge measured is 200 mV by Eq（4.11）.

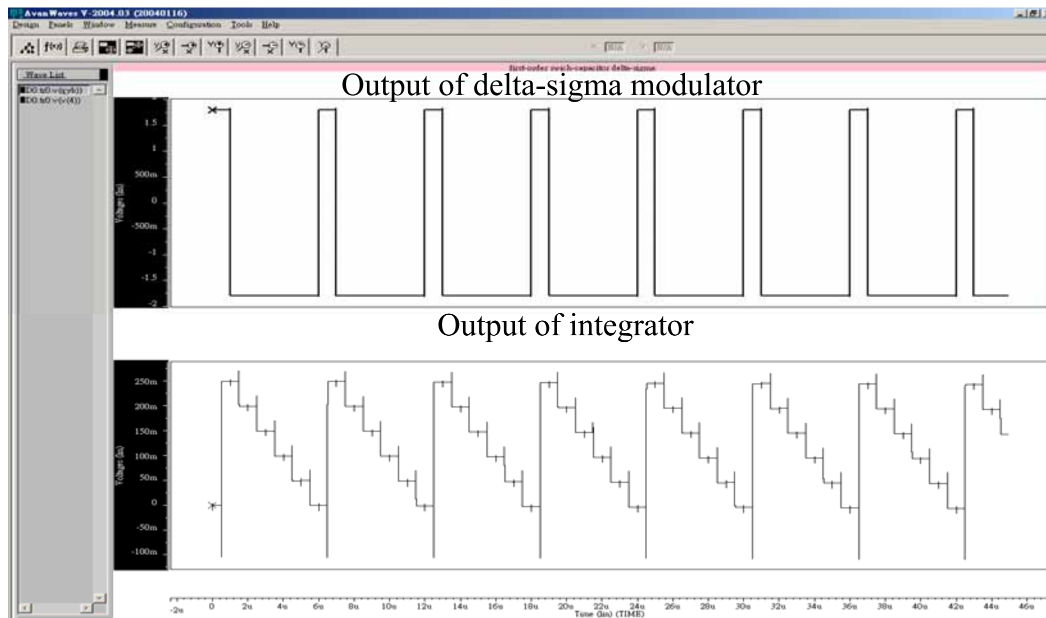


Fig.4.5 Simulated outputs of the delta-sigma modulator and the integrator

Figure 4.6 shows the simulation results of the measurement error versus the measured voltage of the DAC. The measurement error is defined in Eq.（4.12）as the difference between the simulated measured value of the circuit and the applied value of the output of the DAC-under-test. With the error obtained, we can define the maximum number of bits, which is defined in Eq. (4.13), of the DAC-under-test that this circuit can measure. In the figure, we can see as the measured input varies from -500mV to -1mV, the error increases linearly from -0.749mV to 1.14mV. The main error comes from the circuit sample-and-hold. For Fig.4.7 shows the same plot but

with the input voltage varying from 1mV to 500mV and the error decreasing also linearly from 0.709mV to -1.12mV. The derived maximum number of bits for this circuit is 8 bits for the DAC code edges between -500mV and 500mV.

$$Measurement\ Error = V_{measurement} - V_{CUT} \tag{4.12}$$

$$Define : nbits_resolution = 2^n \leq \frac{V_{DAC_Full_Swing}}{\max_measurement\left[V_{DAC}(i+1) - V_{DAC}(i)\right]} \tag{4.13}$$

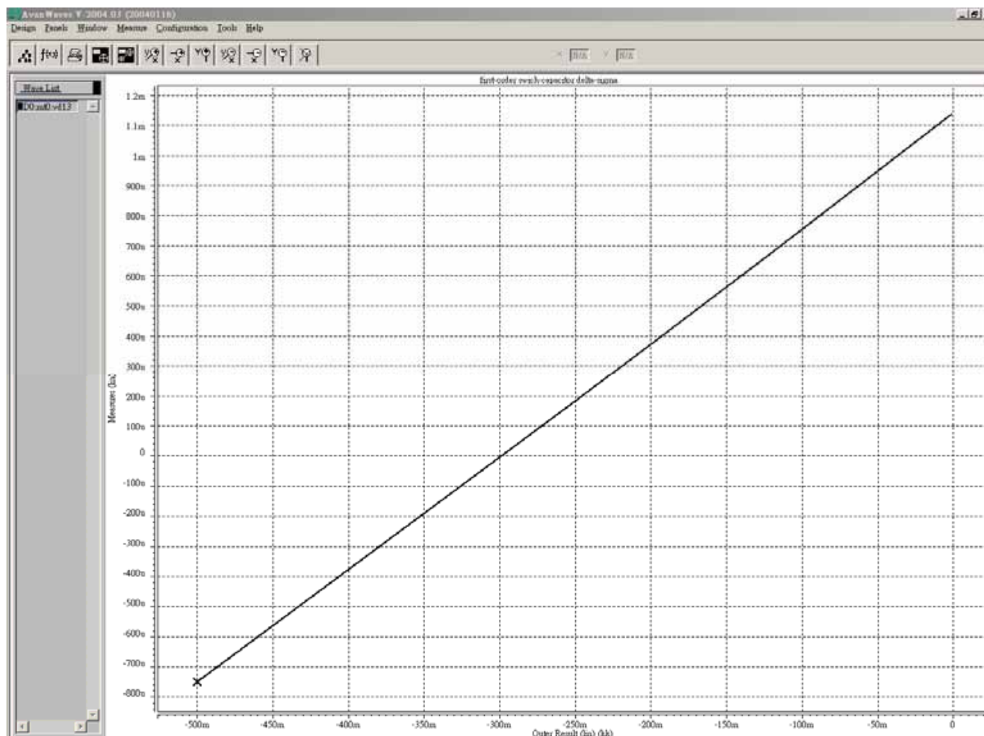


Fig.4.6 Simulated measurement error plotted with respect to the applied input from the DAC-under-test between -500mV and -1mV

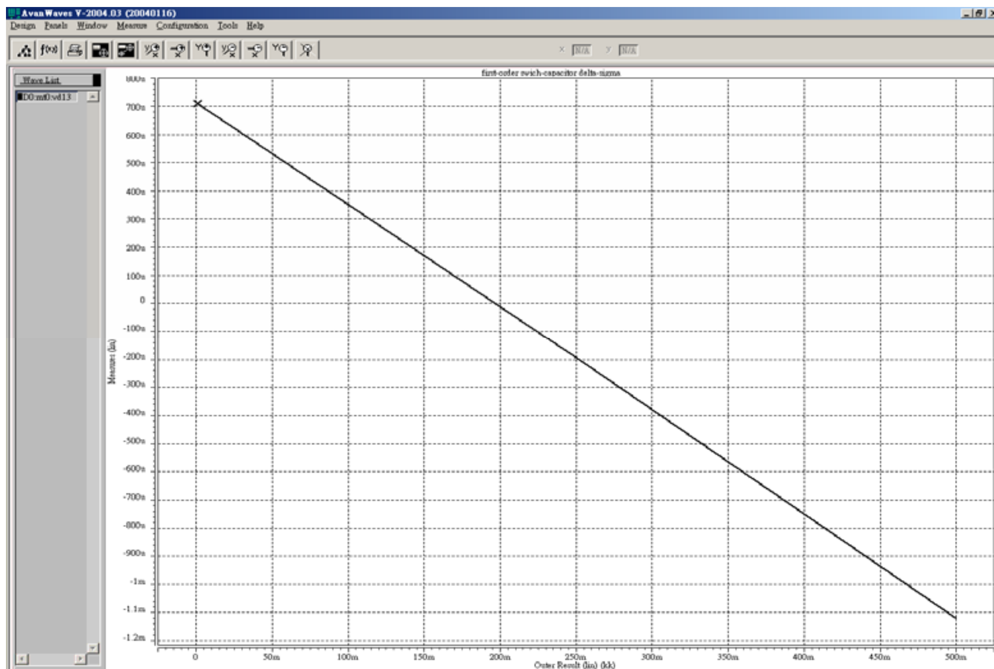


Fig.4.7 Simulated measurement error plotted with respect to the applied input from the DAC-under-test between 1mV and 500mV

When the device parameters were allowed to vary with a $3\sigma = \pm$ 10% tolerance, the results are shown in Fig.4.8A-C. These figures show that the variation on capacitor values almost does not affect resolution. The sample-and-hold error causes the difference between the variation curves and normal curve. When the capacitor value increases, the sample-and-hold error decreases; when the capacitor value decreases, the sample-and-hold error increases. In general, the error is very small. This fact can be seen from Eq's (4.10, 4.11) that the capacitor parameter does not affect the numbers of N0 and N1 when the error is zero.

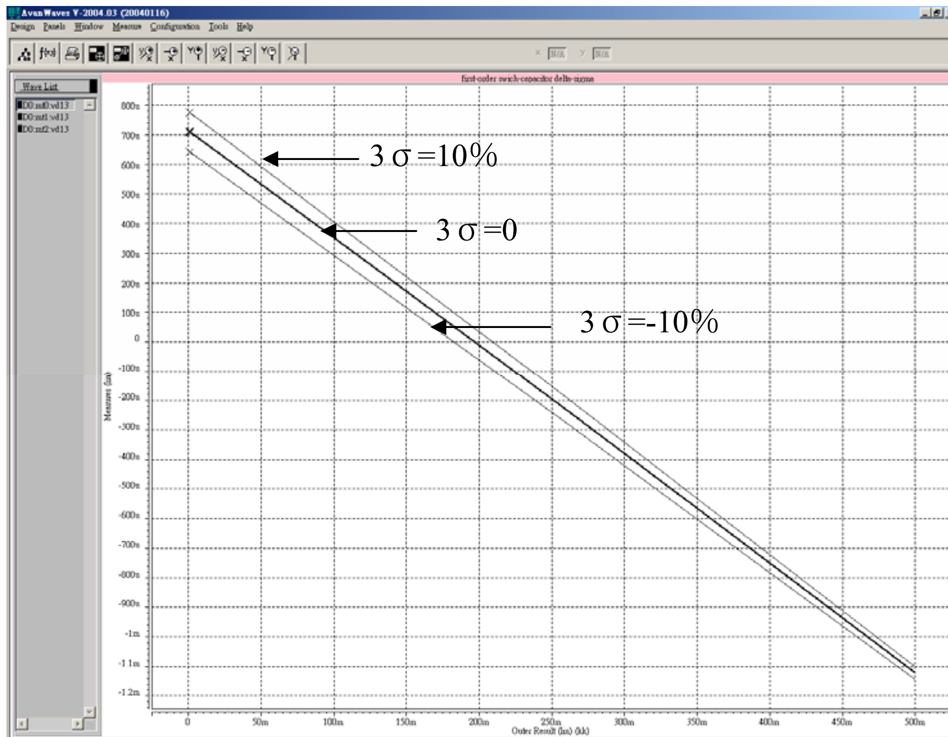


Fig.4.8A C_4 vary with a $3\sigma = \pm$ 10% tolerance

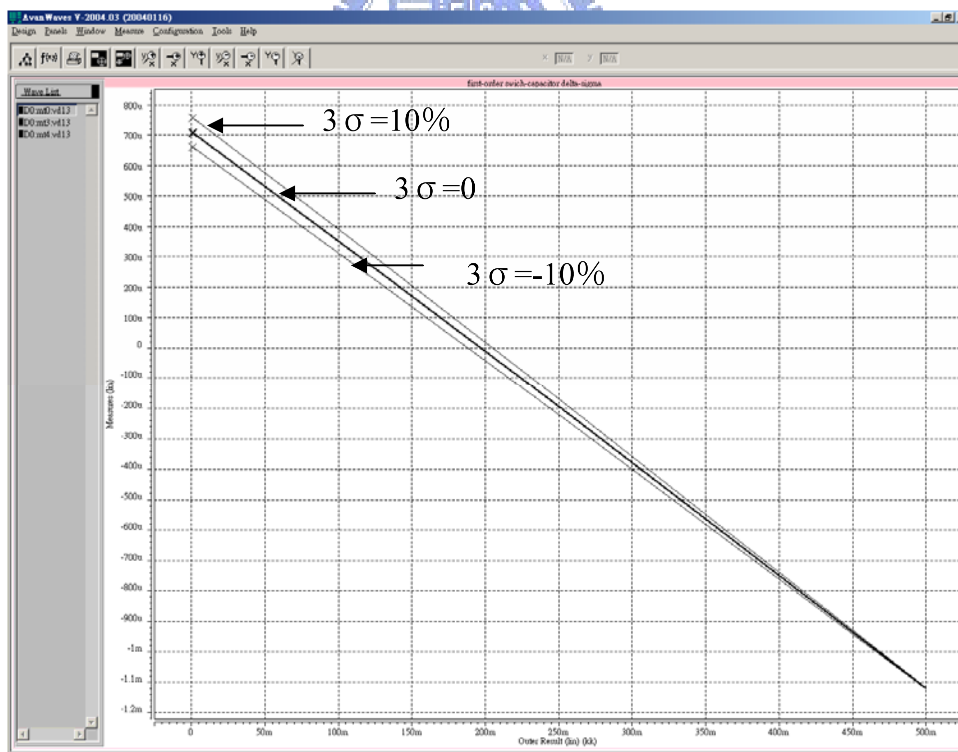


Fig.4.8B C_3 vary with a $3\sigma = \pm$ 10% tolerance

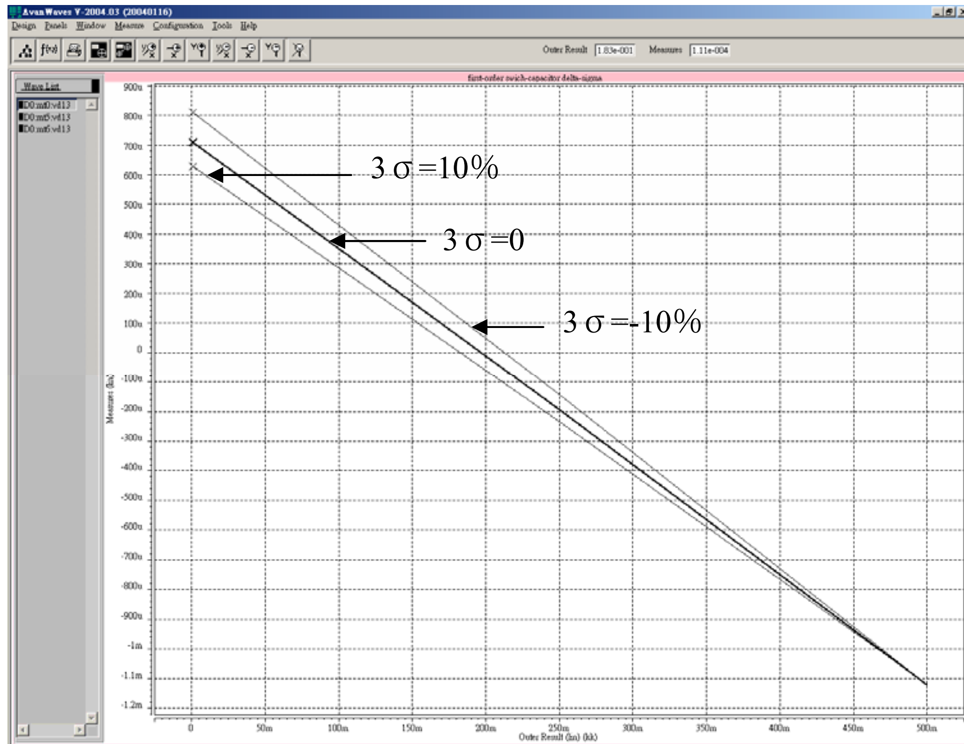


Fig.4.8C C_b vary with a $3\sigma = \pm 10\%$ tolerance

Fig.4.9 shows the result for the case that when the operational amplifier has an offset error. The offset error causes the curve shift. This shows that the operational amplifier offset obviously affects resolution. According to Eq's（4.8, 4.9）, when the circuit input is zero in the normal mode, we can obtain Eq（4.14）. We can find the offset value by observing N1 and N0 from the output of the PCM code.

$$error = \frac{N0}{N0+N1}\frac{C_4}{C_3+C_4}V_{ref} - \frac{N1}{N0+N1}\frac{C_4}{C_3+C_4}V_{ref} \tag{4.14}$$

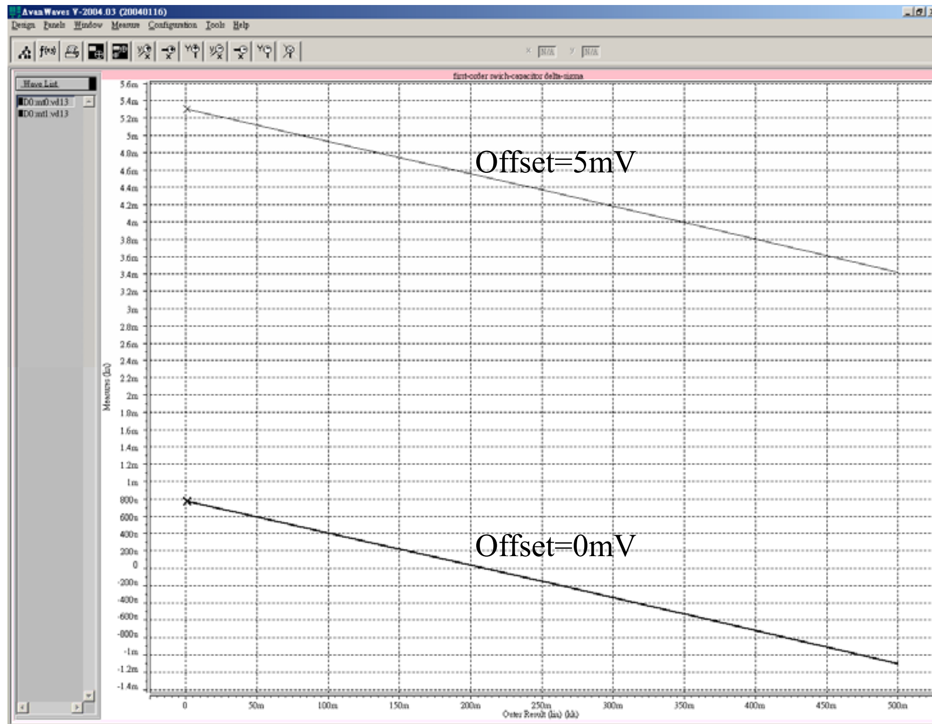


Fig.4.9 The integrator's operational amplifier has offset error

Fig.4.10 and Fig.4.11 show the same plots as those of Fig. 4.6 and Fig 4.7 respectively for the post simulation results for the implemented circuit. In Fig.4.10, the error varies from 0.264mV to -0.631mV linearly and in Fig.4.11, it varies from -0.115mV to 0.255mV. This data shows that the implemented circuit can achieve a 9 bits resolution for the DAC code edges between -500mV and 500mV.

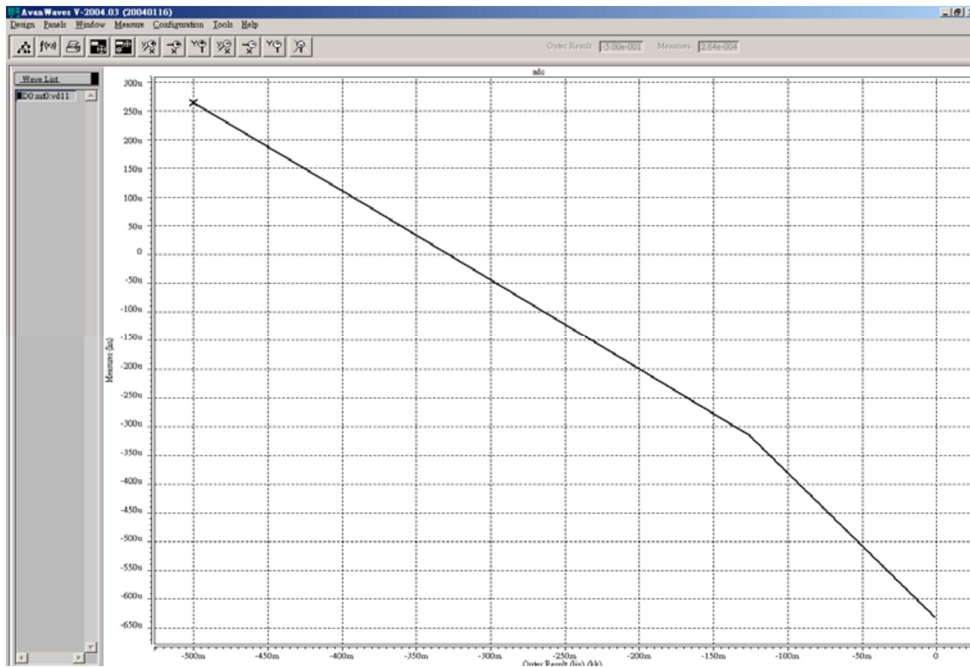


Fig.4.10 Measurement error plotted with respect to the applied input from the DAC-under-test between -500mV and -1mV for post layout simulation

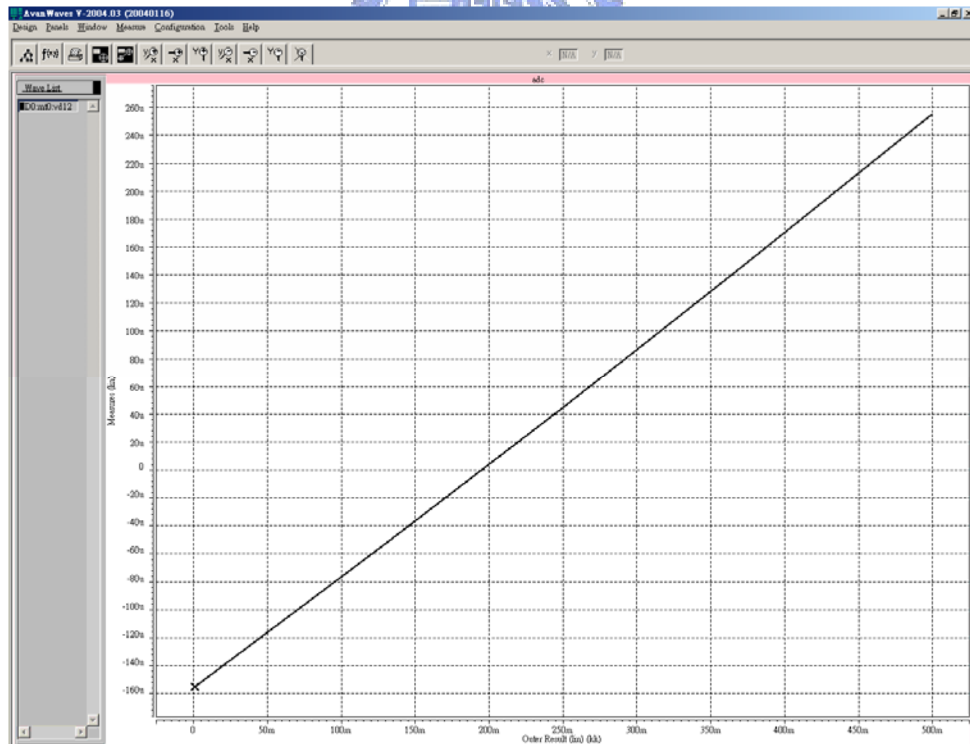


Fig.4.11 Measurement error plotted with respect to the applied input from the DAC-under-test between 1V and 500mV for post layout simulation

To apply this circuit to measure the LSB of a higher resolution DAC, we need to put an amplifier in front of the input of the inputs of the multiplexer of the circuit as shown in Fig 4.12A & B. This expand the range of the input of the test circuit, thus effectively increase the resolution of this measurement circuit.

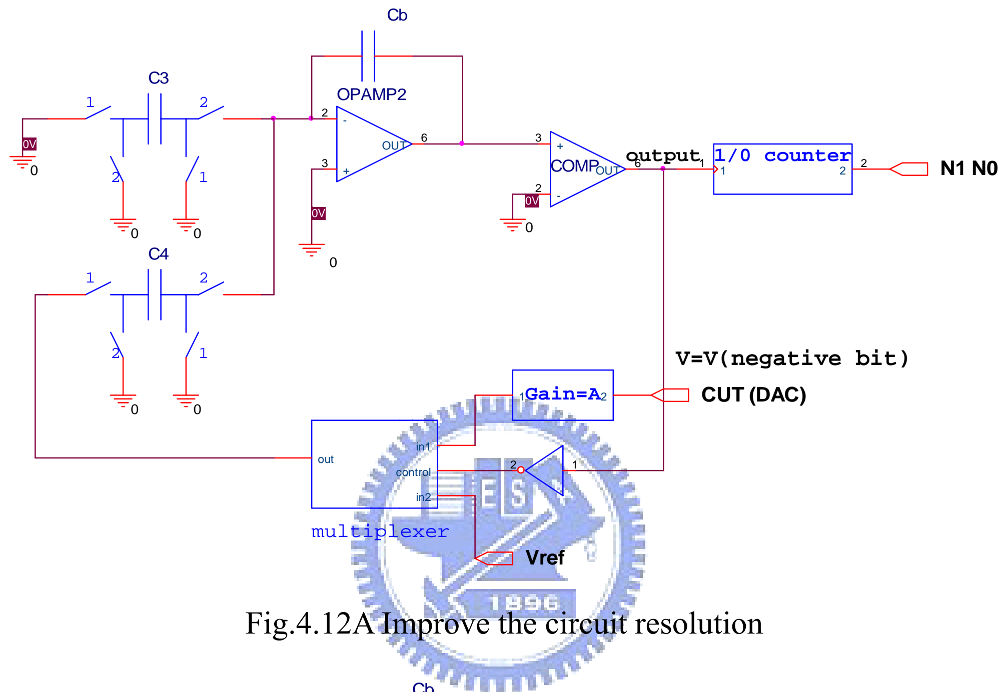


Fig.4.12A Improve the circuit resolution

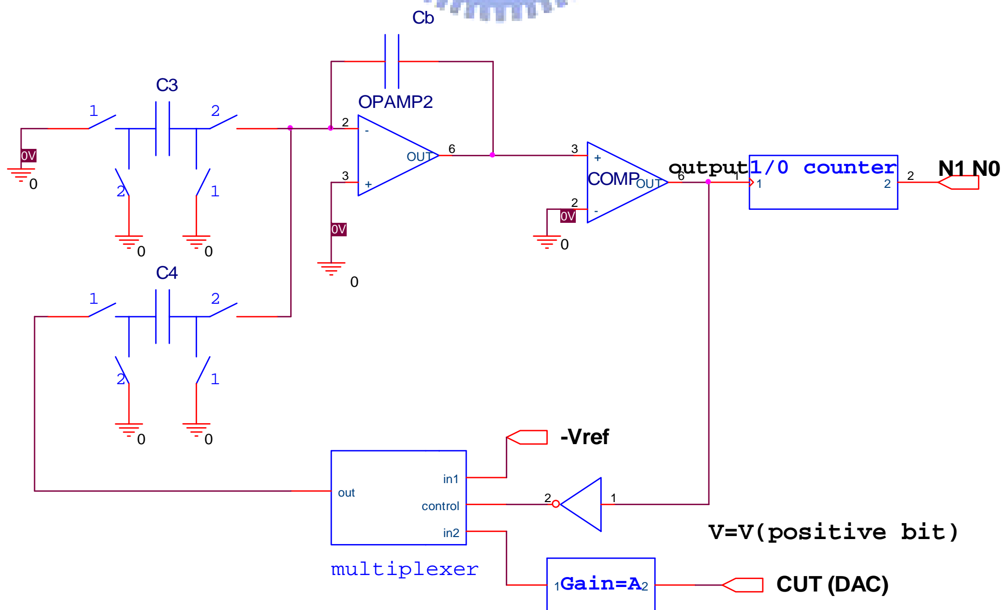


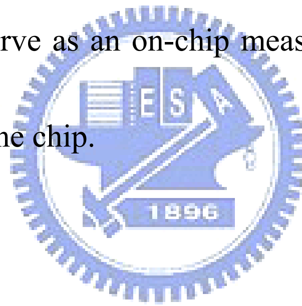
Fig.4.12B Improve the circuit resolution

Chapter 5 Conclusion

In this thesis, we present a new test method to diagnose faults in the delta-sigma modulator and present an application of the delta-sigma modulator circuit as a code edge measurement circuit for DAC. For the diagnosis method, it can diagnoses the stuck-at HIGH or LOW faults at the output of the comparator and the faults at switched-capacitors and operational amplifiers. It needs a few extra added circuits including four multiplexers and two switches. It has a very high accuracy to determine operation amplifier offsets and capacitor ratios. Also, it can not only test single fault but also test multiple faults. The case study which diagnoses a second order delta-sigma modulator for this technique has shown that it is useful and gives the high resolution to identify errors on capacitor ratio of the delta-sigma modulator circuit.

For the application of delta-sigma modulator in DAC code edge measurement, it uses delta-sigma modulation property to accurately measure a DC voltage level which could be the output of a DAC-under-test. It uses a 2-to-1 multiplexer to replace the one bit DAC in the feedback loop of the delta-sigma modulator and applies the output of the DAC-under-test to one of two inputs of the 2-to-1 multiplexer while connecting the output of the modulator circuit to the control pin of the 2-to-1 multiplexer. It does not require any extract additional switch or circuit, so the original performance of

delta-sigma modulator is preserved. Also, its circuitry is only a first order delta-sigma modulator. Therefore the area overhead is small. Since the test method is capable of measuring code edges, all other static parameters such as offset error, gain error, INL error and DNL error of the DAC-under-test can be derived. Experimental results on an implemented circuit of this measuring modulator circuit with UMC0.18 technology show that can give this measuring circuit a 9-bits resolution for the DAC code edge measurement between -500mV and 500mV. This can be improved by connecting an amplifier stage at the output of the DAC-under-test. Also, this measuring circuit can be built in an SOC chip to serve as an on-chip measuring circuit for measuring any voltage levels of modules on the chip.

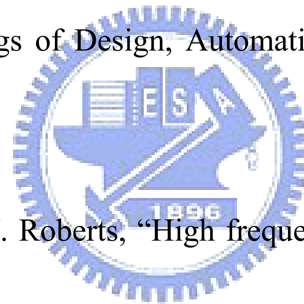


Reference

【1】K. Arabi, B. Kaminska, and J. Rzeszut. A new built-in self test approach for digital-to-analog and analog-to-digital converters. In *International Conference on Computer Aided Design*, pages 491–4, November 1994.

【2】B. Dufort and G. W. Roberts. Signal generation using periodic single and multi-bit sigma-delta modulated streams. In *International Test Conference*, pages 396–405, 1997.

【3】J.L. Huang, C.K. Ong, and K.T. (Tim) Cheng. A BIST Scheme for On-Chip ADC and DAC Testing. Proceedings of Design, Automation & Test in Europe, 216-220, March, 2000



【4】B.R. Veillette and G.W. Roberts, "High frequency sinusoidal generation using delta-sigma modulation techniques", *Proc. 1995 ISCAS*, pp. 637-640.

【5】*Kuen-Jong Lee, Soon-Jyh Chang, Ruei-Shiuan Tzeng*. A Sigma-Delta Modulation Based BIST Scheme for A/D Converters. 12th Asian Test Symposium (ATS'03) November 16 - 19, 2003

【6】*Jochen Rivoir*, Agilent Technologies Low-Cost Analog Signal Generation Using a Pulse-Density Modulated Digital ATE Channel 13th Asian Test Symposium (ATS'04) November 15 - 17, 2004

【7】M. F. Toner and G. W. Roberts. A BIST scheme for an SNR test of a sigma-delta

ADC. In *International Test Conference*, pages 805–14, 1993.

【8】K. Arabi and B. Kaminska, “Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method” IEEE Transaction on CAD, Vol. 16, No. 7, July 1997, pp.745-753.

【9】Yeong-Jar Chang, Chung Len Lee, Jwu E Chen and Chauchin Su, ”A Behavior Level Fault Model for Closed-Loop Operational Amplifier” , Journal of Information Science and Engineering 1999.

【10】McCreary and P.R. Gray, “All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques-Part1”, IEEe . of Solid-State Circuits, Vol. SC-17, pp. 1139-1143, 1982.

【11】Martin “Improved Circuits for the Realization of Switched-Capacitor Filters”, IEEE Trans. Circuits and Systems, Vol. CAS-27, no. 4, pp. 237-244, 1980.

【12】text book “ANALOG INTEGRATED CIRCUIT DESIGN”, DAVID A. JOHNS and KEN MAETIN.

【13】text book “Design of Analog CMOS Integrated Circuits”, Behzad Razavi.

【14】Jiun-Lang Huang and Kwang-Ting Cheng “A Sigma-Delta Modulation Based BIST Scheme for Mixed-Signal Circuits” CA 93106 IEEE 2000

【15】K. Arabi, B. Kaminska and J. Rzeszut, “BIST for D/A and A/D Converters,” IEEE Design & Test of Computers, 1996, pp. 40-49.

【16】Hassan, I.H.S.; Arabi, K.; Kaminska, B. “Testing digital to analog converters based on oscillation-test strategy using sigma-delta modulation“ Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conference on 5-7 Oct. 1998 Page(s):40 – 46

簡　歷

姓　　名： 陳威憲

性　　別： 男

生　　日： 民國六十八年十一月十二日

籍　　貫： 臺灣省嘉義縣

通訊地址： 嘉義縣大林鎮西結里 3 鄰 46 號

學　　歷： 民國九十二年九月至民國九十四年六月

國立交通大學電子研究所碩士班

民國八十八年九月至民國九十二年六月

國立台灣海洋大學電機工程學系

論文題目： Delta-Sigma 調變器之錯誤診斷

Fault Diagnosis for Delta-Sigma Modulator