

Chapter 3

MOCVD HfO₂ Gate Dielectric on Ge Substrate

3-1 Introduction

As mentioned in the chapter 1, we know that high-*k* materials are critical to apply in semiconductor industry. Since HfO₂ almost meets all of the criteria and requirements for the adaptability of high-*k* dielectrics, many deposition methods have been employed to form HfO₂ films, such as physical vapor deposition (PVD) [43], metal-organic chemical vapor deposition (MOCVD) [44]-[46], atomic layer deposition CVD (ALDCVD) [46]-[48], UV-photo-CVD [49] and epitaxial methods (MOMBE [50] and MBE, etc.). From the sight of industrial application, PVD and MBE are not appropriate for high-*k* film deposition, while MOCVD has the advantages of superior step coverage, high deposition rate, good controllability of composition and excellent uniformity of film thickness over large area. Therefore, the utilization of MOCVD technology serves as our tool to deposit HfO₂ thin film.

The MOCVD used in this work is equipped with a turbo-molecular pump and a liquid injection system (which has four independent-controlled injectors). The latter is consisted of a liquid pump to pump the precursors through a hot nickel frit with a proper rate, since the pump is unreliable at low pump rates. The vapors are carried with a 200 sccm flow of Ar to a gas distribution ring which is located at a proper distance from the substrate. The components of the vaporizer, the gas ring and the connecting tube are maintained at a temperature of

190°C with heating tapes and blankets, while the substrate temperature is controlled at 350°C -500°C with quartz-halogen lamps and a thermocouple. A rotating susceptor is used for uniform heating during processes. A flow of 100 sccm N₂ is maintained throughout the deposition cycle. The base pressure of the MOCVD chamber is ~10⁻⁸ Torr. The deposition pressure of the deposition is at the 5 mTorr where the gas-phase collisions are rare.

3-2 Experimental Procedures

In this section, both n-type (Sb) and p-type (Ga) doped 4-inch Ge(100) wafers with the resistivity of 8-12 and 25-29 Ω·cm, respectively, were used to study the MOS characteristics. The optimized cleaning procedure obtained in Chapter 2 was employed for Ge wafers. HfO₂ film of approximately 6 nm was deposited by atomic vapor deposition (AVDTM) in an AIXTRON Tricent[®] system at different substrate temperatures. The deposited temperatures were 350°C, 400°C, 450°C and 500°C, respectively. The N₂ PDA was performed to improve the electrical characteristics. A 5000 Å Al or 1000 Å Pt was deposited through a shadow mask to form the top gate electrode. Also, a 5000 Å Al deposited on the backside of Ge wafer was used to reduce the contact and series resistances. Noted that the high-density NH₃ plasma pre-treatment was also performed to serve as the passivation layer on Ge surface. Various plasma times of 10 s, 30 s and 60 s were tested to inspect the effect on MOS characteristics. For electrical analysis of the HfO₂ film, a precision impedance meter of HP4284 was used for C-V measurement, and a semiconductor parameter analyzer of Keithley 4200 was used for

I - V measurement. For physical analysis, the surface morphology was examined by AFM technique, while the thickness and composition were evaluated by the HRTEM images and EDS spectra, respectively.

3-3 Electrical and Material Characteristics

3-3-1 C - V and I - V characteristics

Figure 3-1(a) shows the PDA effect on the capacitor characteristics of Al/HfO₂/p-Ge gate stack. A significant amount of frequency dispersion as well as a larger hysteresis was observed before and after 500°C annealing. The higher PDA temperature, i.e., 600°C, completely damaged the MOS capacitor properties. By contrast, Pt/HfO₂/p-Ge gate stack exhibited the smaller hysteresis and no frequency dependence on inversion capacitance, as shown in Fig. 3-2. We infer that these differences depend on the quality of gate dielectric, which is closely correlated to the gate leakage performances, thus affecting the resulting C - V characteristics. Therefore, too larger gate leakage current density (J_g), i.e., 2×10^{-1} A/cm² @ $V_g = -1$ V, observed in Pt/HfO₂/p-Ge gate stack may lead to the incorrect observation of C - V curves. This speculation shows agreement with the examination of Fig. 3-3. As we have seen, without NH₃ surface treatment, the decrease of accumulation capacitance originated from severe gate leakage at the region of strong negative bias. Such a considerable leakage current was suppressed after NH₃ surface passivation, in agreement with the consequence of N. Wu et al., [45]. It was demonstrated that the directly deposited HfO₂ film on n-Ge exhibited J_g of ~ 1

$\times 10^0 \text{ A/cm}^{-2}$ @ $V_g = 1\text{V}$ and ~ 4 orders reduction of J_g provided that the surface nitridation was performed. Comparing the 100 kHz C - V curves for different NH_3 duration, the lower inversion capacitance with longer nitridation time was observed. This feature might be attributed to the reduced generation rate of minority carrier. In Fig. 3-4, the effect of N_2 PDA on the electrical properties of Pt/ HfO_2 /Ge MOS capacitor is presented. Although the higher accumulation capacitance seemed to be achieved after performing higher temperature N_2 PDA, the degradation of C - V characteristics due to the raised J_g was found as well. It may be related to the increase of trap states in dielectric film and/or the shrinkage of dielectric thickness during the N_2 thermal annealing.

Temperature-dependent C - V characteristics of Pt/ HfO_2 /Ge MOS capacitor measured at 13°C , 25°C and 50°C , respectively, are plotted in Figs. 3-6 (a)-(c). Differing from the traditional Si substrate in Fig. 3-6 (d), the inversion regime of Ge capacitor revealed significant dependence on the measured temperature. When the temperature was upon 50°C , the multi-frequency C - V curves almost merged together because that the minority carrier lifetime was obviously shortened due to the thermally enhanced carrier transition. On the other hand, we have investigated the Hf-based precursor pre-deposition and O_2 pre-purge during HfO_2 deposition at substrate temperatures of 400°C and 500°C , as shown in Fig. 3-7. The 400°C presented smaller hysteresis width than 500°C did, however, with a larger leakage current. Compared to the O_2 pre-purge, $\sim 10\text{\AA}$ Hf pre-deposition showed no difference at 400°C , while revealing somewhat EOT and hysteresis damages at 500°C . It should be noted

that for identical deposition process, the leakage current density in this work was in the order of 10^{-6} - 10^{-8} A/cm² @ $V_{FB}+1V$, which was much lower than the previously experimental results in Figs. 3-2 and 3-3. We believe that this difference originate from the deposition process.

3-3-2 High-Resolution Transmission Electron Microscopy and Electron Dispersive Spectra

Figures. 3-7 and 3-8 presents the HRTEM images of HfO₂ films deposited at 500°C before and after the PDA. Apparently, the deposited HfO₂ film was composed of two different layers. From the EDS analysis of these two layers in Fig. 3-9, the top and bottom layers were referred to as “Hf-riched HfGeO_x” and “Ge-riched HfGeO_x”, respectively. Both layers of as-deposited film exhibited locally-crystalline before the PDA and further crystallized after the 500°C PDA. The similar deposition composition for various deposition temperatures was found in Fig. 3-10, except that another amorphous layer existed between the so-called “HfGeO_x” layer and Ge substrate. It seemed to be violable as the temperature raised from 350°C to 500°C, thereby damaging the surface roughness. The composition of this layer, which was characterized from EDS in Fig. 3-11, was likely to be GeO_x. Three possible mechanisms were proposed. First, a GeO_x($x \leq 2$) layer probably formed before the deposition and continuously grew provided that the oxygen diffuses through grain boundary of the crystallized HfO₂ film. Second, considering the Gibbs free energy of formation for HfO₂ (-1172 kJ/mol at 700 K), GeO₂ (-608 kJ/mol at 700 K) and GeO (-254 kJ/mol at 700 K), it is

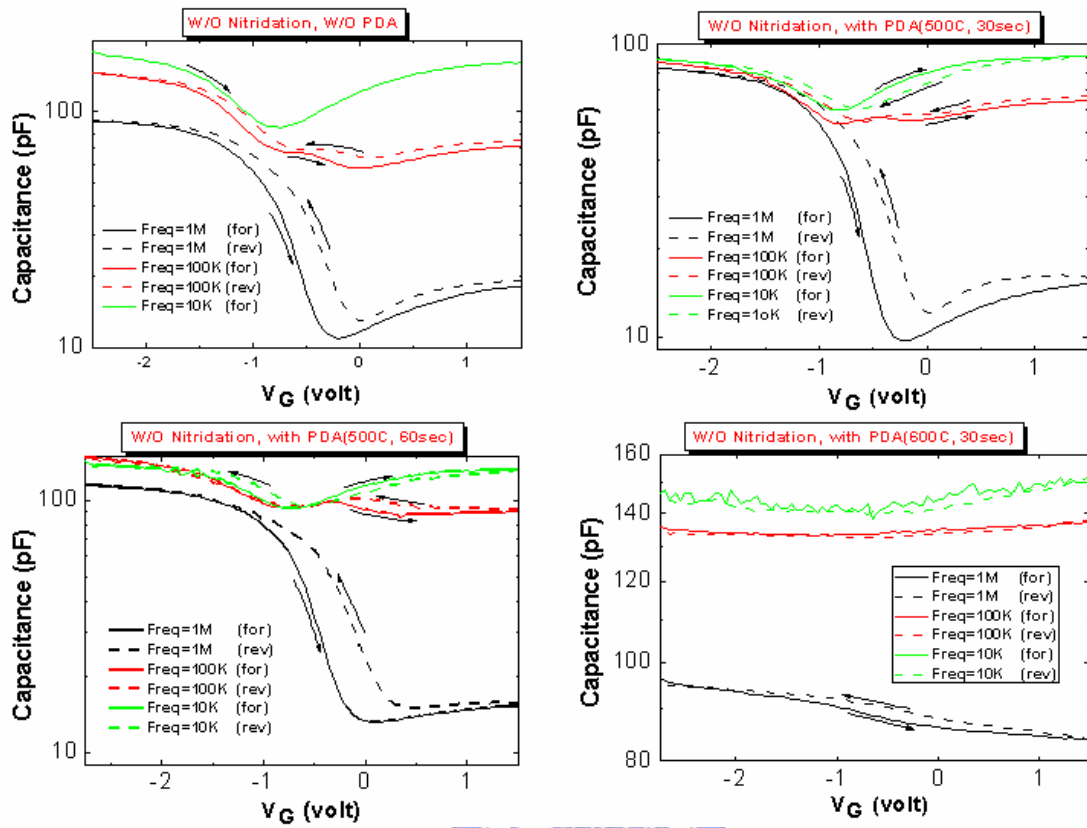
plausible that HfO_2 should be thermodynamically stable with respect to solid-state reactions with the Ge substrate [51]. However, if the GeO_x has existed on Ge surface, the formation of HfO_2 might occur by the snatch of oxygen from this GeO_x . Lastly, the Ge oxides (GeO and GeO_2) were known to be very unstable at moderately high temperatures ($>400^\circ\text{C}$) [41, 52] and this phenomenon has been verified in Chapter 2. These combined effects are believed to influence the resulting composition of HfO_2 gate dielectric. These results also demonstrate again that the MOCVD HfO_2 deposited on Ge substrate shows strong dependence on growth parameters, e.g., substrate temperature, gas flow, precursor sequence, etc.

3-3-3 Atomic Force Microscopy

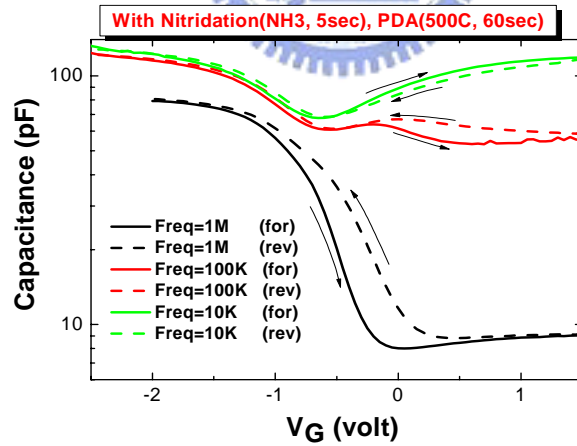
The surface morphology of deposited HfO_2 films were also studied by AFM. We discussed the effects of deposition and annealing temperature on deposition film. All scanning results with the same scale in height are depicted in Figs. 3-12 to 3-15. As can be seen, the surface roughness of as-deposited films were 0.353 nm, 0.405 nm, 0.863 nm and 1.116 nm, which corresponded to the deposition temperature of 350°C , 400°C , 450°C and 500°C , respectively. These results showed agreement with TEM examination in Fig. 3-10. We deduce that the upper roughness of gate dielectric shall come from the uneven bottom interface, not determine from the deposition uniformity itself. Additionally, even though the N_2 PDA played a minor role on the roughness variation for all temperatures, the electrical characteristics have seriously damaged.

3-4 Summary

In this chapter, we have studied the electrical and physical properties of MOCVD HfO₂ film deposited on Ge substrate. For as-deposited HfO₂ film, the manifest frequency dispersion with a larger hysteresis was observed in multi-frequency *C-V* characteristics. Rapid thermal annealing of as-deposited film in an N₂ ambient also showed the unfavorable effect on the capacitor characteristics, especially for the *C-V* distortion and gate leakage increment. Through the EDS analysis, the resultant composition of deposited film by MOCVD was found to be hafnium-germanium mixed oxide. In addition, the low deposition temperature of 400°C facilitated to obtain smoother deposition film but resulted in a larger leakage current, while the high deposition temperature of 500°C entirely exhibited the opposite tendency. Finally, from our experimental findings, the surface passivation, e.g., NH₃ pre-treatment, was essential to further improve the quality of HfO₂ films on Ge surface. We suggest that NH₃ plasma process, including the time, power, pressure, gas flow, etc., shall be optimized in order to obtain the high-quality HfO₂/Ge gate stack.

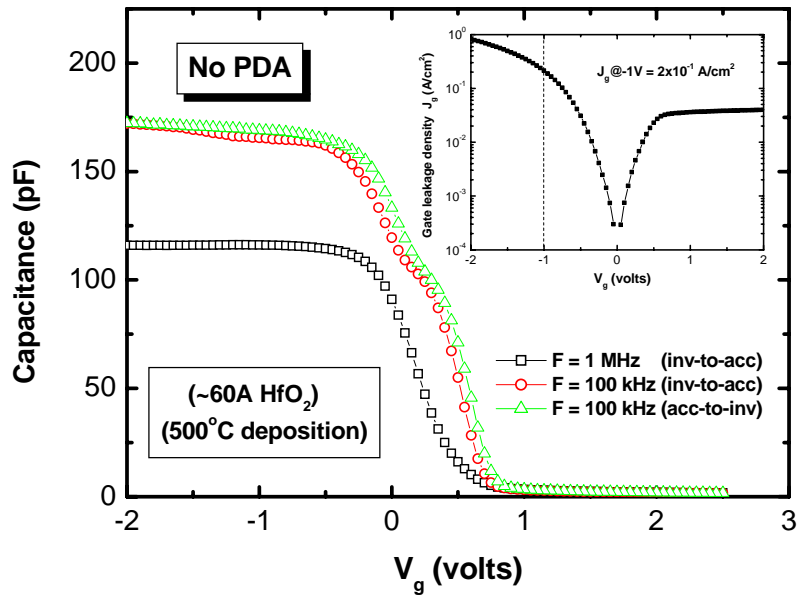


(a)

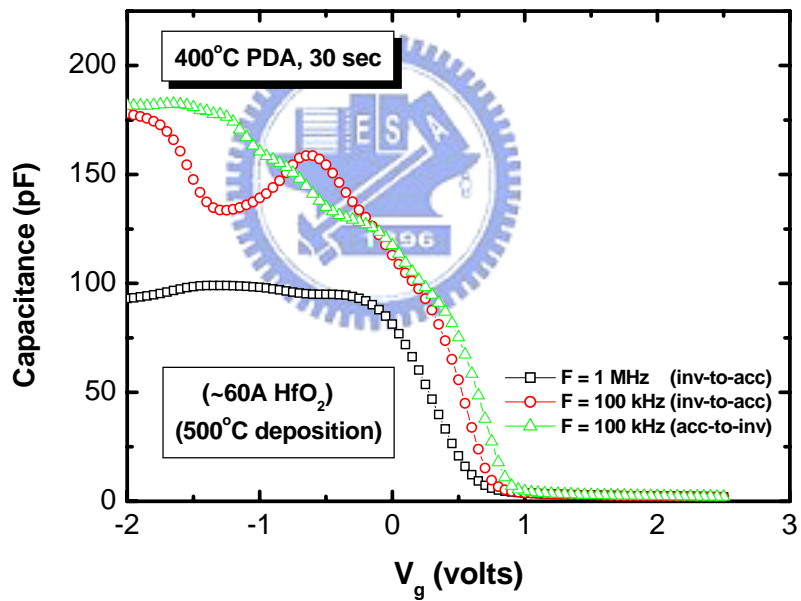


(b)

Fig. 3-1 (a) The PDA effect on C - V characteristics of Al/HfO₂/Ge MOS capacitor w/o surface nitridation. (b) The C - V characteristics of Al/HfO₂/Ge MOS capacitor with surface nitridation.



(a)



(b)

Fig. 3-2 (a) The C - V characteristics of Pt/HfO₂/Ge MOS capacitor without N₂ PDA. The MOCVD HfO₂ deposited at 500°C. (b) The C - V characteristics of Pt/HfO₂/Ge MOS capacitor with 400°C N₂ PDA.

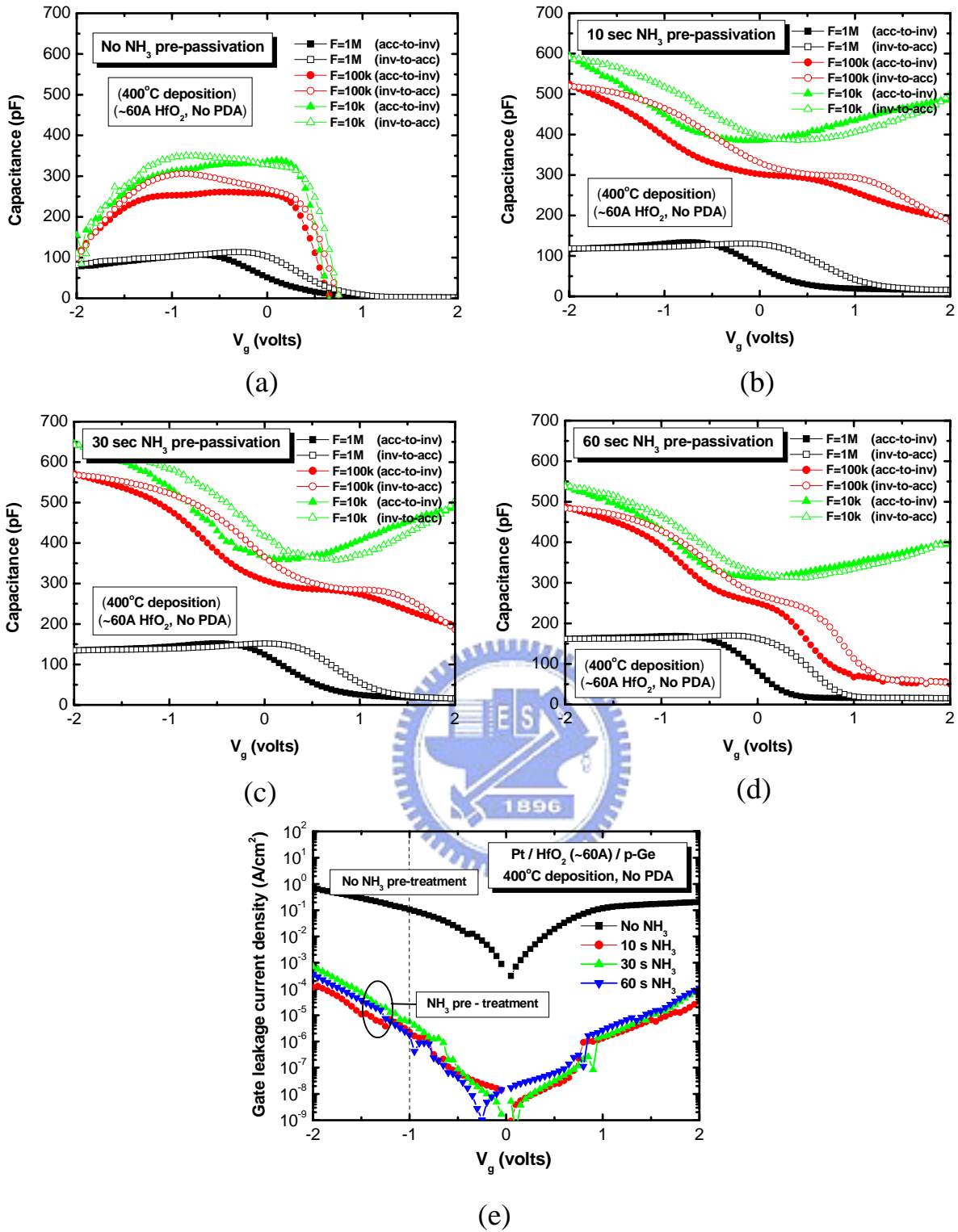


Fig. 3-3 The C-V characteristics of Pt/HfO₂/Ge MOS capacitor with NH₃ pre-passivation. (a) No NH₃. (b) 10sec NH₃. (c) 30sec NH₃. (d) 60sec NH₃. The MOCVD HfO₂ deposited at 400 °C. (e) The effect of NH₃ pre-passivation on I-V characteristics of Pt/HfO₂/Ge MOS capacitor.

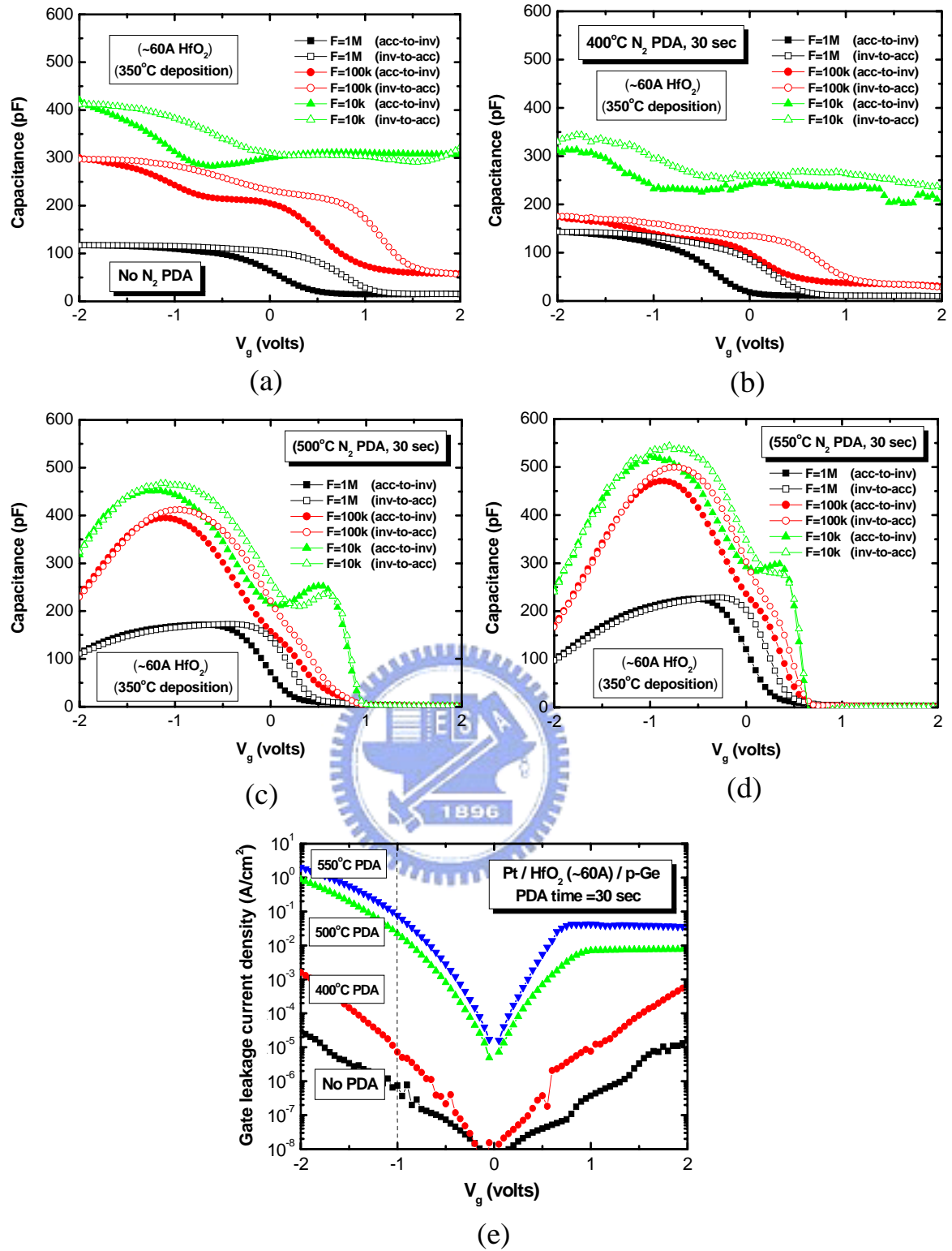


Fig. 3-4 The C-V characteristics of Pt/HfO₂/Ge MOS capacitor with and w/o N₂ PDA. The MOCVD HfO₂ deposited at 350°C. (a) No PDA. (b) 400°C PDA. (c) 500°C PDA. (d) 550°C PDA. (e) The PDA effect on the I-V characteristics of Pt/HfO₂/Ge MOS capacitor.

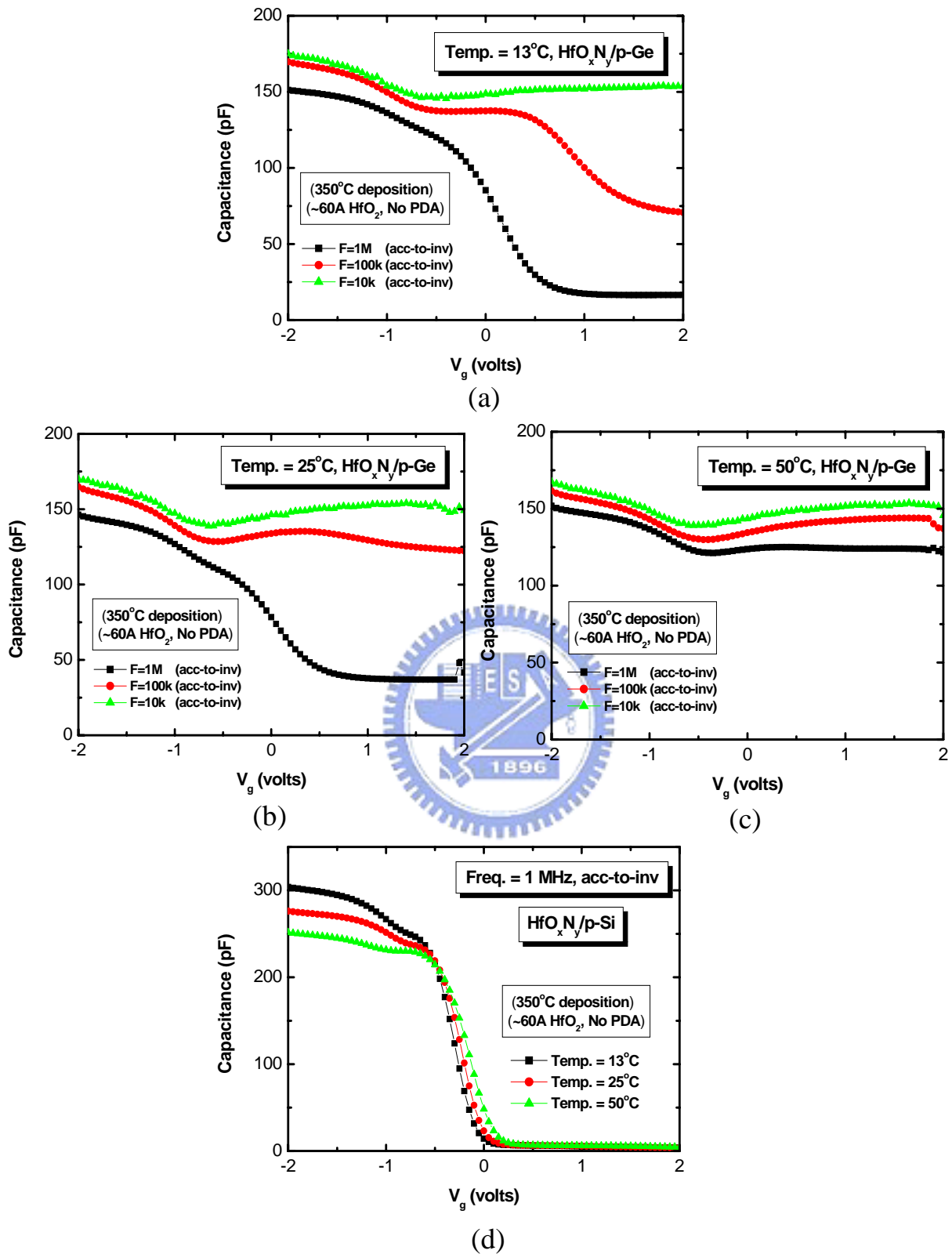


Fig. 3-5 (a)-(c) Temperature-dependent C - V characteristics of Pt/ HfO_2 /Ge MOS capacitor. (d)

Temperature-dependent C - V characteristics of Pt/ HfO_2 /Si MOS capacitor.

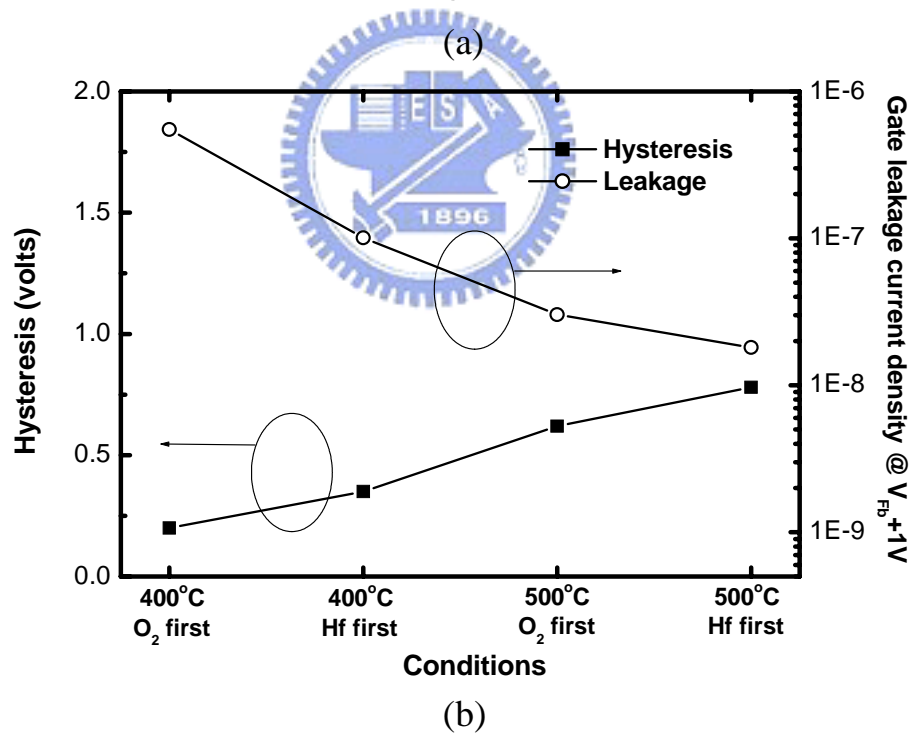
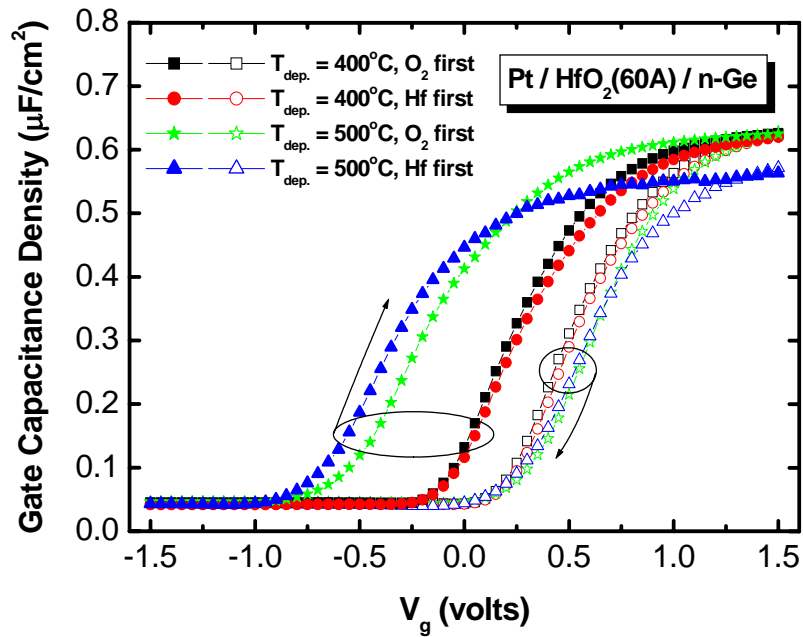
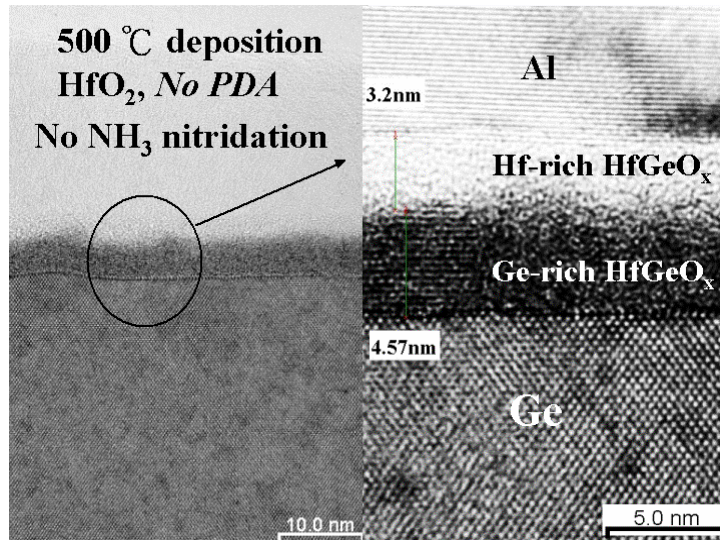
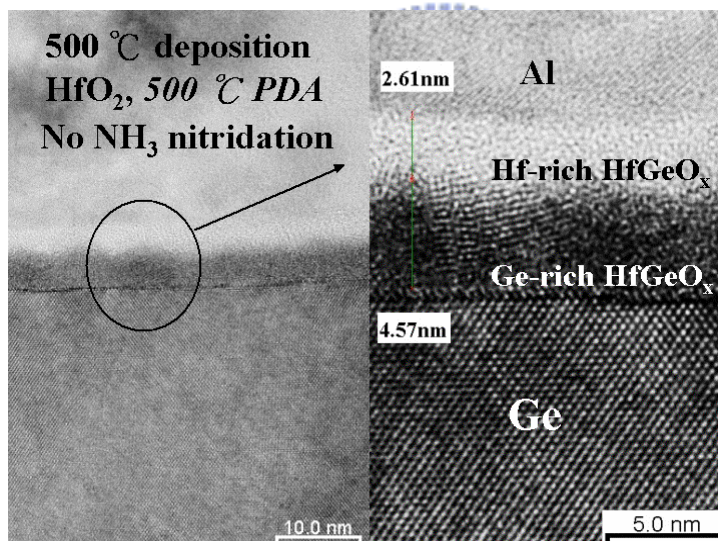


Fig. 3-6 (a) The C - V characteristics of Pt/HfO₂/Ge MOS capacitors under different deposition conditions. (b) The hysteresis width and gate leakage current for different deposition conditions.

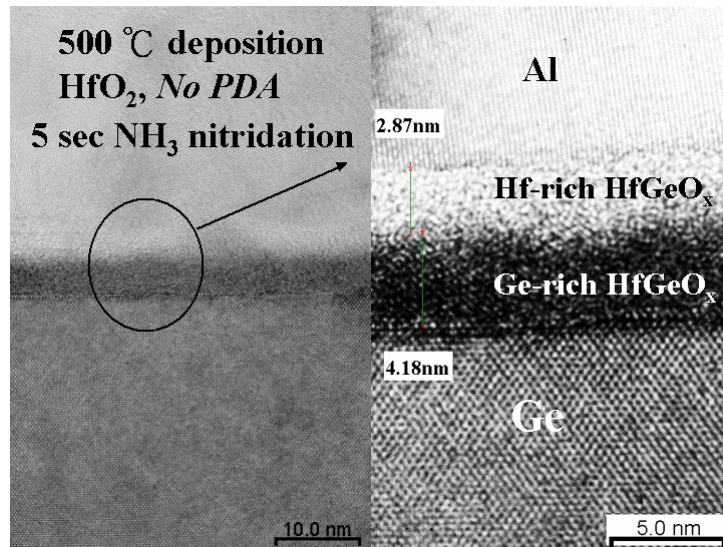


(a)

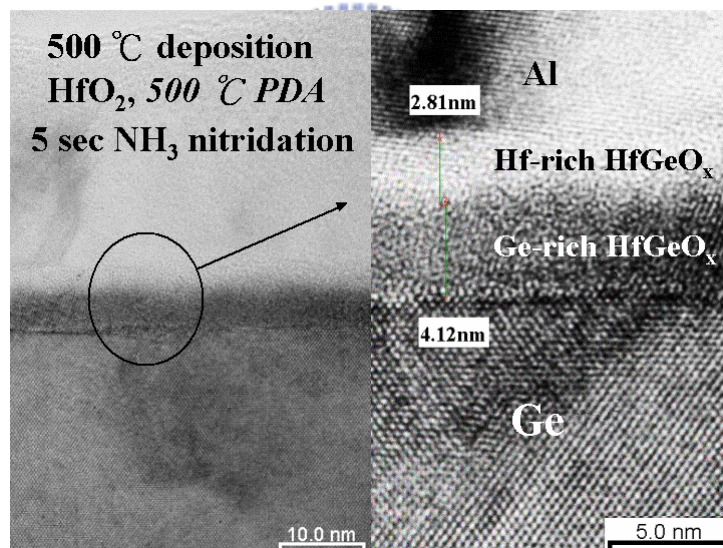


(b)

Fig. 3-7 The HRTEM images of HfO₂ thin film deposited on cleaning Ge substrate (a) No PDA. (b) 500 °C PDA. No surface nitridation was done before HfO₂ deposition. The deposition temperature for HfO₂ dielectric is 500 °C.



(a)



(b)

Fig. 3-8 The HRTEM images of HfO₂ thin film deposited on nitrated Ge substrate. (a) No PDA. (b) 500°C PDA. Surface NH₃ pre-passivation for 5 sec was done before HfO₂ deposition. The deposition temperature for HfO₂ dielectric is 500°C.

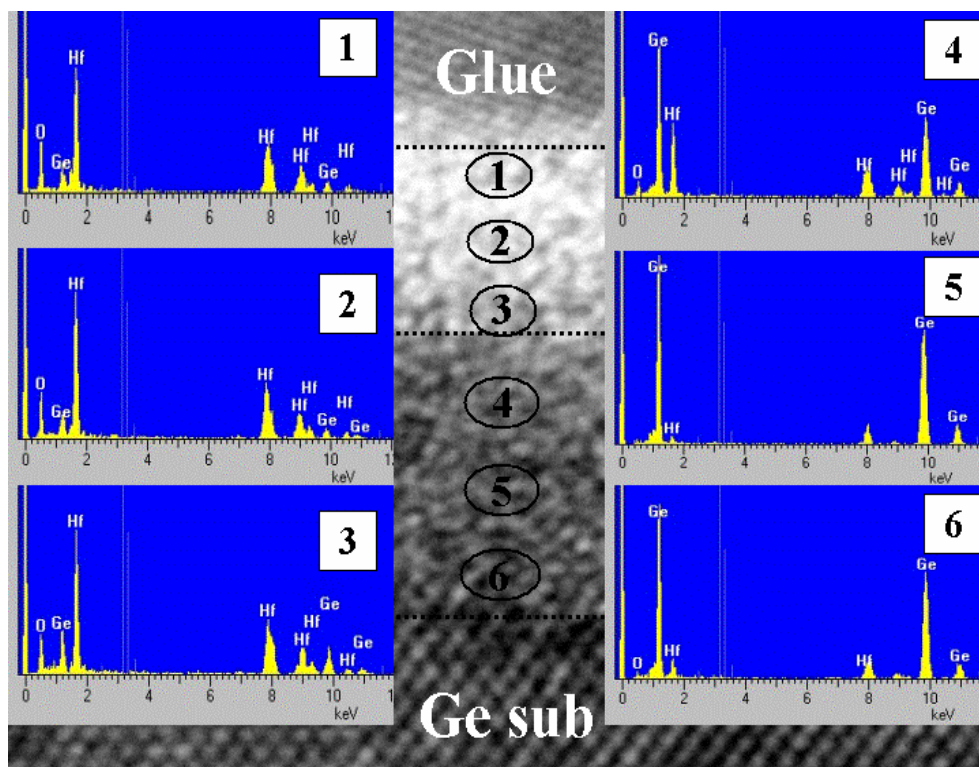


Fig. 3-9 The EDS analysis of the compositions of the HfO₂ thin film deposited on Ge substrate. The deposition temperature for HfO₂ dielectric is 500°C.

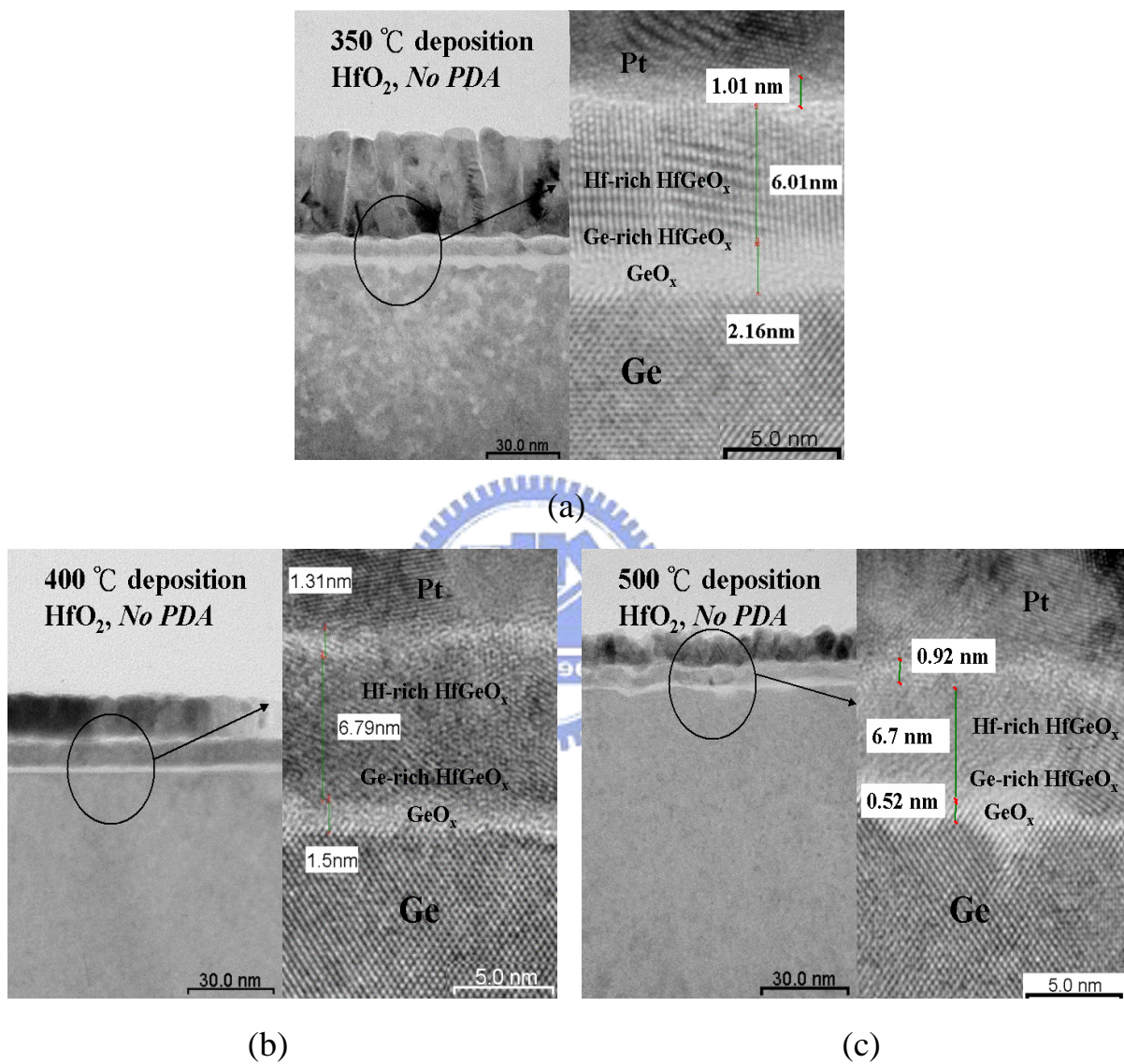
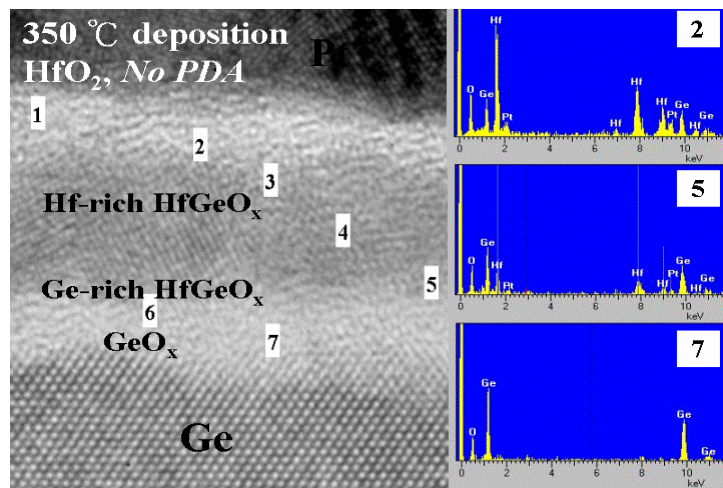
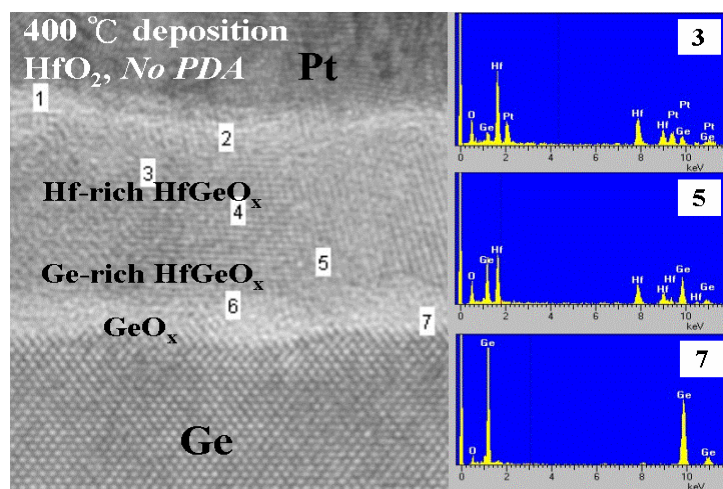


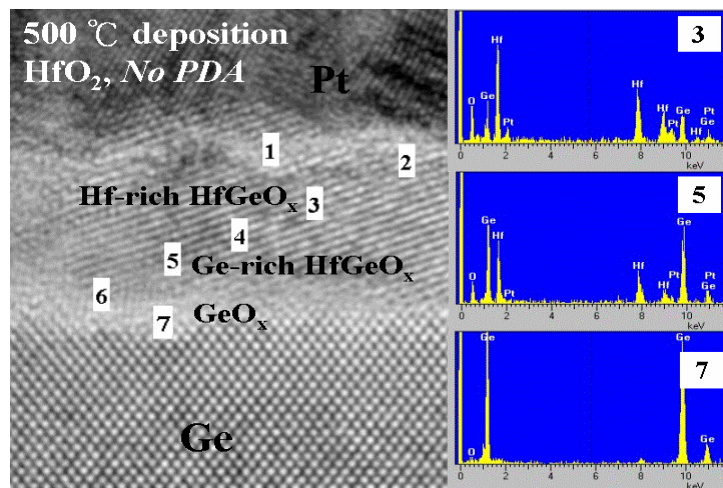
Fig. 3-10 The HRTEM images of HfO₂ thin film deposited on cleaning Ge substrate at different deposition temperatures. (a) 350°C. (b) 400°C. (c) 500°C.



(a)



(b)



(c)

Fig. 3-11 The EDS analysis of the compositions of the HfO_2 thin film deposited on Ge substrate at different deposition temperatures. (a) 350°C . (b) 400°C . (c) 500°C .

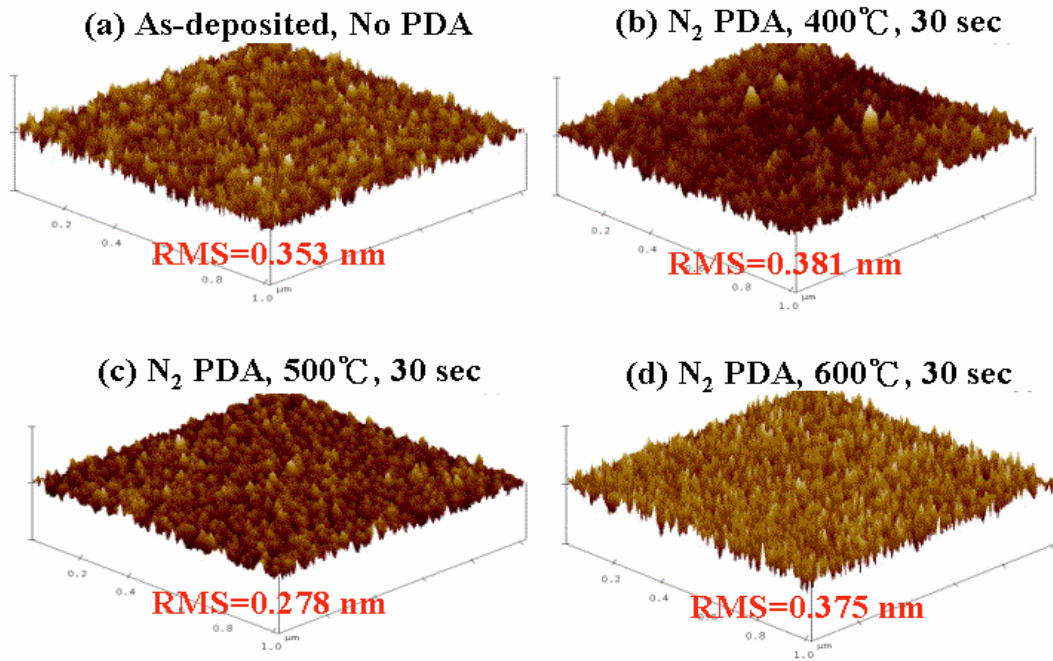


Fig. 3-12 AFM characterization of HfO₂ thin film on Ge substrate after different PDA temperature annealing. The deposition temperature for HfO₂ dielectric is 350°C.

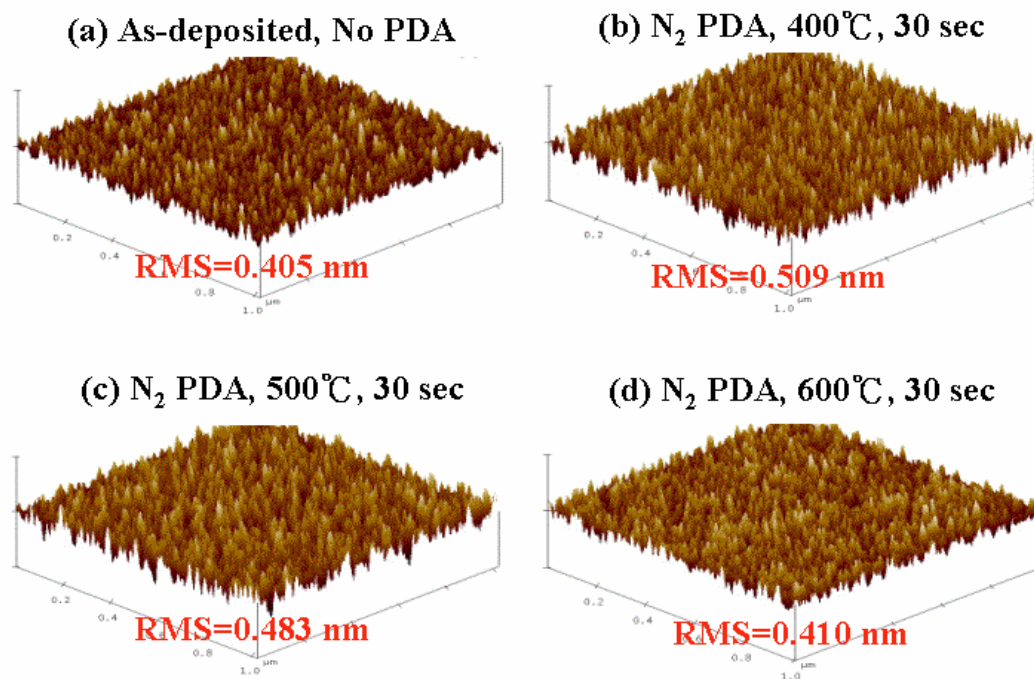


Fig. 3-13 AFM characterization of HfO₂ thin film on Ge substrate after different PDA temperature annealing. The deposition temperature for HfO₂ dielectric is 400°C.

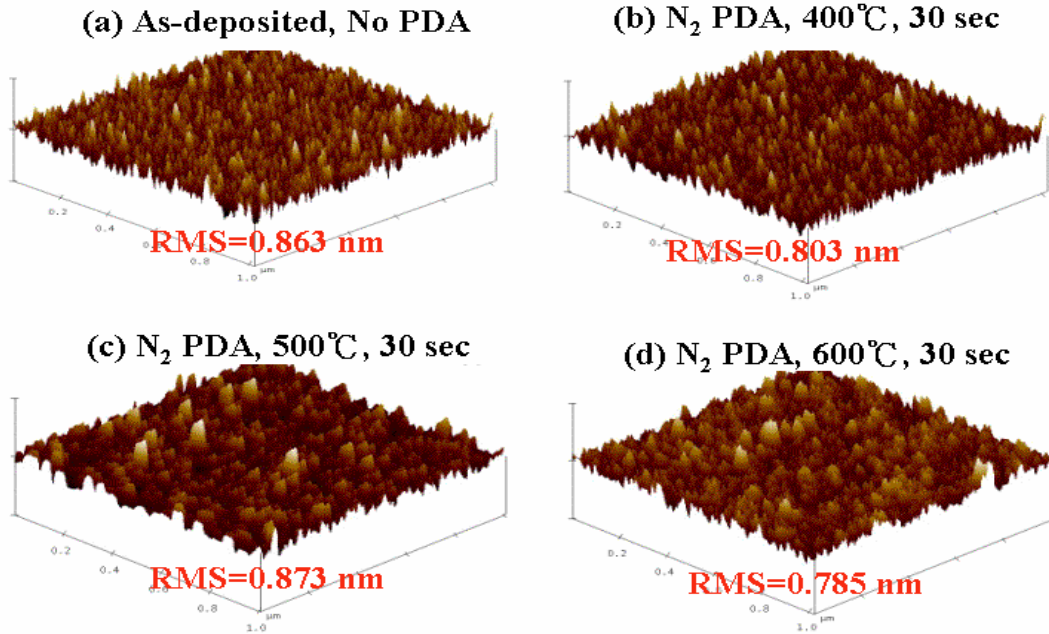


Fig. 3-14 AFM characterization of HfO_2 thin film on Ge substrate after different PDA temperature annealing. The deposition temperature for HfO_2 dielectric is 450°C .

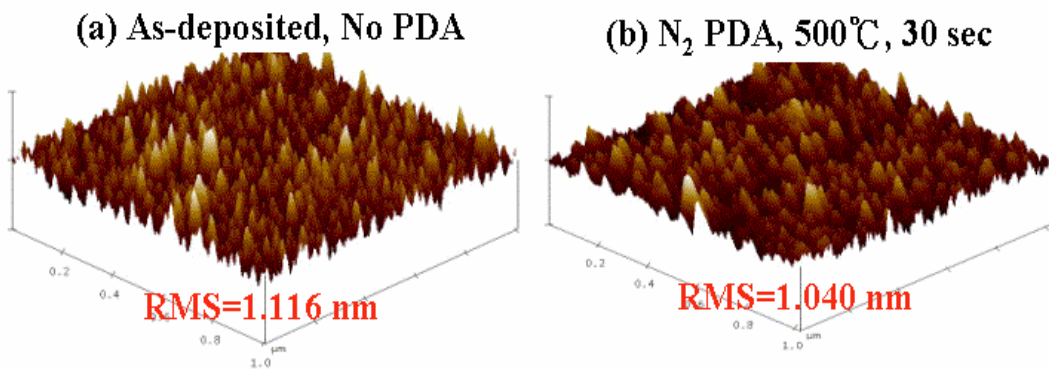


Fig. 3-15 AFM characterization of HfO_2 thin film on Ge substrate after different PDA temperature annealing. The deposition temperature for HfO_2 dielectric is 500°C .

Chapter 4

Sputtered HfO_xN_y and HfSiO_xN_y Gate Dielectric on Ge Substrate

4-1 Introduction

In recent years, high- k gate dielectrics on Si substrate have been proved being able to significantly reduce the leakage currents as compared to the traditional SiO_2/Si system, while still maintain excellent reliability and high-level of transistor performance. In order to further enhance device driving capability, Ge is a great potential semiconductor material due to its higher intrinsic electron and hole mobilities for carrier transport. Interestingly, the lack of sufficiently stable native Ge oxide makes the integration of high- k gate dielectric on top of Ge substrate receive more and more attentions. Up to now, several metal oxides, e.g., ZrO_2 [53], HfO_2 [45, 48] and Al_2O_3 [54] showing promising electrical properties have been demonstrated to be suitable for Ge. Those previous works suggested that the surface passivation prior to the deposition of the metal oxides using SiH_4 [44] or NH_3 [47] annealing was needed for pursuing high-quality gate dielectrics. However, this procedure increases the process complexity as well as the electron-trapping rate due to hydrogen incorporation [55]. Comparatively, since the hafnium oxynitride (HfO_xN_y) has a higher crystallization temperature (800°C) than pure HfO_2 (400°C) and the nitrogen incorporation can strengthen the immunity against oxygen diffusion for suppressing the interfacial layer (IL) formation during processing. In our work,

we systematically investigated the impact of PDA on the electrical properties of HfO_xN_y dielectric on the Ge substrates.

4-2 Experimental Procedures

The Ge substrate used was (100) Ga-doped p-type wafers with a resistivity of 25-29 Ω cm. The wafers were subject to the cleaning process of DI water rinse, followed by diluted HF (1:50) dipping for several cycles. After drying, the HfN thin-films were deposited with reactive sputtering with a pure Hf target, followed by a PDA with rapid thermal system for oxidation and densification. The HfN sputtering was performed in an Ar+N₂ ambient [$\text{N}_2/\text{Ar}+\text{N}_2=0.33$] with a power of 150 W and a chamber pressure of 7.6 mTorr. To avoid excess oxidation and minimize the IL, the PDA was carried out in an N₂ ambient instead of O₂ ambient for converting HfN into HfO_xN_y . The effects of PDA temperature and time on electrical performance of the HfO_xN_y gate dielectric on Ge substrate were investigated. The temperatures chosen were 400°C, 500°C and 600°C with the duration times of 1 min, 3 min and 5 min, respectively. After that, a 1000 Å Pt was deposited by e-beam evaporation through a shadow mask to define the capacitor gate electrode, subsequently, the post metallization anneal (PMA) was performed at the temperature of 400°C for 30 sec. Finally, Al was deposited on the backside of Ge wafer to reduce the contact and series resistances, followed by the forming gas annealing (10% H₂/N₂, 300°C, 30 min). For the preparation of HfSiON thin film, the fabrication process was identical to the steps described above except that HfSi₂

target was used. The HRTEM technique was taken to characterize the crystallinity and interfacial structure of HfO_xN_y film. The chemical composition and the state of elements was evaluated by EDS and further analyzed by angle-resolved XPS (AR-XPS) and AES, respectively. A 1486.6 eV Al $K\alpha$ radiation source, whose spot size was about 250 μm in diameter, was used for excitation. Photoelectrons were collected at an emission angle of 30° , 45° and 60° , respectively, with respect to the surface horizontal. The binding energy was calibrated from the Pt $4f_{7/2}$ peak at 71.2 eV. The AES depth profiles were achieved through Ar^+ ion sputtering.

4-3 Electrical and Material Characteristics

4-3-1 C-V and I-V characteristics



Figure. 4-1(a)-(d) shows multi-frequency C - V characteristics of Pt/ HfO_xN_y /Ge MOS capacitor before and after the PDA. Their corresponding frequency dispersion is estimated by the equation below, as shown in Fig. 4-1(e).

$$dispersion = \frac{C(@100kHz) - C(@1MHz)}{C(@100kHz)} \quad (4.1)$$

The PDA apparently improved the dispersion effect with increasing temperature and time, especially after 600°C annealing. As far as frequency dispersion is concerned, the series resistance effect is the dominated mechanism for the difference of frequency dispersion at accumulation region. Certainly, the PDA effect on the resulting electron polarization and ionic polarization of high- k dielectric also may be another factor. Here, the polarization effect

is out of consideration, and we still attribute this feature to the reduction of series resistance in the entire MOS structure.

Figure 4-2 displays the typical high frequency (100 kHz) C - V and leakage characteristics of $\text{HfO}_x\text{N}_y/\text{p-Ge}$ capacitors before and after PDA. The $\text{HfO}_x\text{N}_y/\text{p-Si}$ capacitor without PDA is also included for comparison. It was observed that the accumulation capacitance of the as-deposited HfO_xN_y dielectric on Ge was apparently higher than that on Si regardless of the completely identical fabrication processing. The resultant difference in EOT value, evaluated at $V_g = -2\text{V}$, between these two samples was about 0.5 nm. Meanwhile, the inversion capacitance not only lowered upon increasing annealing temperature, but also revealed the weaker frequency dependence (shown in Fig. 4-1). It indicates that the high temperature PDA step is helpful to diminish the process-induced and/or in-situ defects in the Ge substrate. Also, the activation of substrate dopant may be another possible origin because of the need of lower activation temperature in Ge [58, 59]. Meanwhile, a small bump was appeared after the PDA in the depletion region, indicating that some slow states were generated near the interface by this high temperature step. Plotted in Fig. 4-3 is the variation of EOT and hysteresis as functions of the PDA temperature and time. In general, both the EOTs of HfO_xN_y films on Si and Ge substrates decreased with raising the PDA temperature, however, the opposite trends of the EOT dependence on PDA time were found for these two different capacitors. The EOT of $\text{HfO}_x\text{N}_y/\text{Ge}$ gate stack showed shrinkage with increasing the PDA time, differing from the increased EOT for $\text{HfO}_x\text{N}_y/\text{Si}$ gate stack. In contrast, higher PDA temperatures and longer

times led to the smaller hysteresis width for the $\text{HfO}_x\text{N}_y/\text{Si}$ gate stacks, whereas resulted in the larger hysteresis width for $\text{HfO}_x\text{N}_y/\text{Ge}$ gate stacks, especially for the case of 600°C . These differences will be discussed in depth later in combination with the material analysis.

On the other hand, in order to correctly observe the PDA effect on the shift of flatband voltage (V_{FB}), the maximum/minimum biases in the two-way C-V sweep was carefully chosen for avoiding the significant charge trapping. The extracted procedures and results are presented in Fig. 4-4. The V_{FB} of as-deposited HfO_xN_y on Ge was (0.72 ± 0.3) V, which was close to the work-function difference between Pt gate of (5.4 ± 0.3) eV [60] and p-Ge substrate of 4.55 eV. A noticeable feature was that the negative V_{FB} shift, independent of the PDA time, was found with raising the PDA temperature, implying that more fixed positive charges were introduced in the gate dielectric/IL, especially for 600°C annealing. The lowered V_{FB} after the PDA may be involved with the concentration of nitrogen in the gate dielectric/IL. Similar V_{FB} shift due to nitrogen addition was reported in the HfO_xN_y [61], ZrO_xN_y [62] and SiO_xN_y [63] dielectrics, etc. In Fig. 4-5, we studied the variation of hysteresis width as a function of sweep voltage according to V_{FB} . The hysteresis width showed the increase with raising the annealing temperature and the independence with the annealing time. Higher increasing rate of hysteresis with sweep voltage observed after 600°C gave evidence of more charge trapping states existed in bulk gate dielectric. Fig. 4-6 shows the shift of V_{FB} extracted from the different scan direction. When the sweep voltage range was extended, a larger hysteresis width was expected. Interestingly, the V_{FB} extracted from the scan direction (accumulation to

inversion) as a function of voltage range monotonically revealed positive-shift for all samples. However, the V_{FB} extracted from the scan direction (inversion to accumulation) as a function of voltage range hindered positive-shift with increasing the PDA temperature. The entirely negative shift of V_{FB} was seen upon 600°C. This observation is closely related to the efficiency of charge trapping/detrapping, even the change of trapping mechanism.

Traditionally, the forming gas annealing (FGA) is demonstrated to assist the elimination of interface states between gate dielectric and Si substrate. Thus, we also investigated the FGA effect on the MOS characteristics of Pt/HfO_xN_y/Ge capacitor, as shown in Fig. 4-7. In our work, a significant stretch-out in $C-V$ curves was observed with FGA temperature going up. It differed from the result by other group that the stretch-out of as-deposited HfO_xN_y/Ge gate stack was relieved by FGA step [57, 64]. Two possible origins were presumed to explain the observed difference. First, it may be understood from the correlation between interface degradation and desorption of Hf-Ge mixed oxynitride from the interface, considering the volatility of Ge oxides in an N₂ ambient [42]. It should be noted that in Chapter 2, although the Ge oxide was seen to be stable in an N₂ ambient at 400°C, the long-time 400°C annealing, e.g., FGA (400°C, 30 min), might somewhat damage the oxide. Second, the residual oxygen exists during our FGA processing, leading to the $C-V$ stretch-out and EOT increase in Ge MIS capacitor due to oxidation-induced damages [64]. Consequentially, the resulting damaged IL after the higher FGA led to the lower equivalent breakdown field (E_{BD}) as well.

On the other hand, the electrical properties of Pt/HfSiON/p-Ge MOS capacitor are

demonstrated in Fig. 4-8. Compared to the sputtered HfO_xN_y film on Ge, the similar EOT behavior after thermal annealing was found, however, with the presence of an obvious bump. Fig. 4-9 plots gate leakage current (J_g) versus the EOT for the deposited HfO_xN_y and HfSiON films on Ge substrate, together with other's published data. The surface passivation of Ge substrate is needed before HfO_2 deposition to obtain the lower gate leakage, as shown in the figure. Remarkably, the $\text{HfO}_x\text{N}_y/\text{p-Ge}$ without surface passivation revealed extremely low J_g with near 4 orders of magnitude reduction as compared to the standard SiO_2/Si with the similar EOT. Even though the $\text{HfSiON}/\text{p-Ge}$ gate stack in our work was out of expectation, the $\text{HfO}_x\text{N}_y/\text{p-Ge}$ gate stack showed comparable insulating properties with respect to other Hf-based gate dielectrics on n-Ge.



4-3-2 Reliability Issues

Reliability is one of the most important issues of high- k material for practical application in electronic product. We first discussed the E_{BD} variation due to the PDA processing. As can be seen in Fig. 4-10, the Weibull plot indicated that the endurance of gate dielectric entirely depended on the PDA temperature, regardless of the PDA time, i.e., the higher the annealing temperature was, the more serious the degradation was. Next, from the test of constant-current-stress (CCS) on the $C-V$ characteristics in Fig. 4-11, we observed that the generation of interface state was a major degradation mechanism after dielectric stress. Simultaneously, the hysteresis increase due to interface damages also showed a linear dependence on stress time.

Figure 4-12 shows the Q_{BD} distribution for as-deposited and annealed HfO_xN_y films under CCS tests. At the same charge injection per second, i.e., $J_g = -2 \times 10^{-4} \text{ A/cm}^2$, it was found that the as-deposited HfO_xN_y film had the lowest Q_{BD} , and more charges were required to achieve the breakdown for the HfO_xN_y film after higher PDA. In addition, these four samples are subjected to constant-voltage-stress (CVS), and the results are plotted in Fig. 4-13. From the (time-dependent dielectric breakdown) TDDB reliability data, the operating voltage through 10-year lifetime projection for as-deposited, 400°C PDA, 500°C PDA and 600°C PDA films, were -2.4V, -2.3V, -1.7V and -1.6V, respectively. The continuously dropping operation voltage shows agreement with the severe charge trapping in bulk gate dielectrics after the higher PDA. Noted that the CVS is suitable for gate dielectrics in ultra-thin EOT regimes ($<20\text{\AA}$) because of severe leakage concern. Thus, the CCS result exhibited the opposite tendency to the CVS and the need of higher Q_{BD} for PDA samples was due to the reduced capacity for charge storage.

4-3-3 HRTEM and EDS

To further investigate the thickness variation of Hf-oxynitride and their ILs after the PDA, the cross-sectional HRTEM pictures are shown from Fig. 4-14 to Fig. 4-16. Unusually, We found that the deposited thickness of bulk dielectric and IL on Ge substrate was thicker than those on Si substrate. After the 600°C annealing for 5 min, the total IL thickness of HfO_xN_y/Ge was found to shrink from 21 Å to 11 Å, while that of HfO_xN_y/Si was found to increase from 12 Å to 27 Å. On the contrary, the retarded growth of sputtered HfO_2 film on

Ge was reported. Not only the HfO₂ film but the IL was thinner on Ge substrate compared with that on Si substrate [65]. K. Kita et al. assigned an ultra-thin metallic Hf layer being a crucial role to the thickness differences. Here, from our experimental findings, we firstly presume that such a thickness difference comes from different deposition mechanism, e.g., various surface states and/or dangling bonds on the deposition surface. The different compositions of resultant ILs may influence the final thickness of HfO_xN_y dielectric during the deposition process. As far as the HfO_xN_y/Ge gate stack was concerned, the thickness of HfO_xN_y bulk dielectric was almost the same, while total IL thickness shrank with increasing the PDA temperature and PDA time. This examination partly explained the EOT shrinkage of HfO_xN_y/Ge gate stack after the PDA and further experimental results were still required to analyze these phenomena. We speculate that the unlikeness of electrical characteristics between two capacitor systems after annealing may be closely related to the varied compositions and thicknesses of the resultant ILs.

Fig. 4-17 and Fig. 4-18 shows the EDS spectra of HfO_xN_y/Ge and HfO_xN_y/Si before and after the PDA. For HfO_xN_y/Ge gate stack, the composition of bulk dielectric and the IL was mainly HfO_xN_y with a certain Ge mixture. The Ge atom may transport through the grain boundary in crystallinity film. Such an inter-diffusion behavior seemed to be negligible in HfO_xN_y/Si gate stack.

4-3-4 XRD · FTIR · AES and XPS

Thin film XRD with a glancing angle of 2° was used to investigate crystallinity of

HfO_xN_y on Ge and Si substrate. Fig. 4-19(a) depicts XRD spectra of HfO_xN_y film, which was annealed under N₂ for 1 min at 600°C and 700°C, respectively. The crystallinity was unobvious for as-deposited HfO_xN_y films on both substrates. Unexpectedly, the annealed film had crystallized at the temperature of 600°C, lower than other reported values of ~900°C for HfO_xN_y [61]. We attempt to explain this result in terms of three facts. First, the local crystallinity in as-deposited films on both substrates has been observed in the HRTEM images, but was undetected in the XRD examination. Second, the crystallinity temperature for HfO₂ thin film is known to range from 400°C to 600°C. Third, the Hf atoms prefer to be oxidized rather than nitrified. These facts indicate that substantial Hf-O bonds, which may result from either the sputtering process or the PMA/FGA process, have already existed in the as-deposited HfN film. Accordingly, such a oxygen incorporation is possible to decrease the endurance of crystallinity temperature, and this speculation can be confirmed through the AR-XPS analysis. As shown in Fig. 4-19(b) is the FTIR spectra of these films, a broader band with a peak around 845 cm⁻¹ on Ge substrate was close to the asymmetric stretching mode of Ge-O, and the additional shoulder of GeO₂ at ~970 cm⁻¹ was also ambiguous in our film. Together with EDS spectra, these results suppose that the ultra-thin IL at HfO_xN_y/Ge to be possibly Hf-Ge mixed oxynitride through these elementary results [42, 65].

The comparison of AES profiles for both HfO_xN_y/Ge and HfO_xN_y/Si stacks before annealing is showed in Fig. 4-20. Further, the HfO_xN_y/Ge stack before and after the annealing is also compared in Fig. 4-21. In the element detection, the *LM2* and *MN2* transitions were

used for germanium and hafnium, respectively, and the *KLI* transition was used for the nitrogen, oxygen and silicon, respectively. Two worthy features have been observed in as-deposited $\text{HfO}_x\text{N}_y/\text{Ge}$ as compared to as-deposited $\text{HfO}_x\text{N}_y/\text{Si}$. One was that the Hf and Ge seemed to seriously diffuse into each other, another was that both oxygen and nitrogen profiles are closer to surface. After the PDA, not only the push of nitrogen peak inside the gate dielectric but also the lower nitrogen signal and nitrogen/oxygen ratio was found. We consider that the nitrogen is likely to pile up near the bottom $\text{HfO}_x\text{N}_y/\text{Ge}$ interface, and similar tendency have been found in $\text{GeO}_x\text{N}_y/\text{Ge}$ [66]. Besides, the accumulation of more Ge atoms toward the top surface was seen after higher temperature annealing. According to the previous reports and our experimental results, the Ge substrate and their oxides are unstable at higher temperatures [27, 45]. Thus, the gather phenomenon can be attributed to Ge out-diffusion from either the IL or Ge substrate through the increased grain boundary of bulk dielectric.

Before examining the AR-XPS results, the “university curve” of electron IMFP versus kinetic energy is illustrated in Fig. 4-22. The inset shows the schematic of XPS incident and emission procedures. The mean free path λ estimated in our work is $\sim 17 \text{ \AA}$ according to the employed energy of 1486.6 eV. If assuming the normal take-off angle ($\theta = 90^\circ$ in the inset), 95% of photoelectrons will come from within 3λ of surface. Considered that the highest θ used in our study is 60° , basically, the maximum sampling depth d is less than $\sim 51 \text{ \AA}$ in the following XPS examination. Fig. 4-23 shows the XPS survey from 1200 to 1300 eV for as-deposited and annealed HfO_xN_y films. As can be seen, no Ge element and related bonds

detected in no-PDA and 400°C films, and Ge-O bonding was subsequently appeared upon the 500°C annealing. This finding clearly verifies that the detection depth is limited to 50-60 Å, which is consistent with our supposition. Another noticeable result is the presence of GeO₂ in the bulk dielectric. Together with Ge incorporation explored in Ge_{LM2} AES profile, all detailed examinations were analyzed within the following results and discussions.

Next, we have indeed investigated the Hf 4*f*, N 1*s* and O 1*s* core-level spectra with various take-off angles for these samples. It should be stated first that a higher take-off angle corresponds to have a deeper detection depth. In other words, a higher surface sensitivity is for the lower angle ($\theta=30^\circ$) used in the study. All experimental results are plotted in Fig. 4-24 to Fig. 4-28 and further compared in Fig. 4-29 to Fig. 4-31. Broadly speaking, it was observed in as-deposited HfO_xN_y film that the Hf 4*f* peaks shifted to higher binding energies as the take-off angle increased. A remarkable peak shift also was found in corresponding N 1*s* and O 1*s* spectra. However, these displacement phenomena were vanished after raising the PDA temperature higher than 500°C. The origins of the binding energy shift are suggested as a number of factors, such as charge transfer effect, environmental charge density, presence of electric field, substituent electronegativity and hybridization [67, 68]. Among these, although charge transfer is regarded as a dominant mechanism to cause binding energy shift [67], it seems to be unreasonable for explaining our results. As far as the as-deposited HfO_xN_y film is concerned, the Hf 4*f*_{7/2} and Hf 4*f*_{5/2} peaks at $\theta=30^\circ$, which have binding energies of 16.35 and 17.75 eV, respectively, shifted to 17.44 and 18.84 eV, respectively, as the take-off angle

increased to 60°. Compared with the reported binding energies of (15.55±0.25) and (17.70±0.20) eV for Hf-N 4f_{7/2} peak and Hf-O 4f_{7/2} peak [45, 57, 69, 70], respectively, the occurrence of the inhomogeneous oxidation of HfN was concluded. A number of Hf atoms may be already oxidized during the sputtering process and/or the PMA and/or FGA processes. Since the electronegativity of oxygen (3.4) is higher than that of nitrogen (3.0), the oxygen atom will cause the more electron density to shift from Hf to oxygen. In other words, the amount of chemical shift depends on the number of oxygen and nitrogen atoms which are nearest neighbors of the Hf atom. Thus, more oxygen atoms replaced nitrogen atoms and bonded to one Hf atom at the bottom of HfO_xN_y dielectrics. Consequently, the whole Hf 4f spectra shift to higher binding energy due to the increased electron density. However, more Hf-N bonds existed at the top of HfO_xN_y film gave rise to our attention. This interest feature is still in analysis by studying the bond transfer mechanism.

Fortunately, since no Ge-related peak was detected in Ge 2p core level for as-deposited film (not shown), the N 1s core level showing two distinct broad peaks thus was denoted as the Hf-N and N-N/N-O bonds, respectively. The O 1s asymmetric spectra through Voigt fitting can split into two sub-peaks which represent the Hf-O bonding at ~530.9 eV and C-O bonding at ~532.5 eV [70]. On the other hand, while raising the PDA temperature higher than 500°C, the Hf 4f_{7/2} and Hf 4f_{5/2} peaks have constant binding energies of 17.12 and 18.66 eV, respectively. Each Hf 4f peak still shows a noticeable negative shift, i.e., ~0.6 eV lower than the ideal HfO₂ peaks. It implied that the residual Hf-N bonds in the film. In the N 1s spectra, a

certain presence of Hf-N and/or Ge-N at ~ 398 eV was found, however, N-N and/or N-O bonding at ~ 403 eV was almost disappeared. Besides, it is difficult to decompose O 1s signal after the PDA because it overlaps with Ge *LMN* Auger signal. Finally, since no Ge-Hf bonding at ~ 15 eV is observed in all samples, the dielectrics are of good electrical insulating property in terms of chemical states. Two kinds of possible structures may exist for the HfO_xN_y film. The first is that the dielectric film could be a mixture of HfON and GeON. Another is that the film is nitrogen-incorporated hafnium germinate and the Hf 4*f* bonding is not affected by the vicinity of the Ge atom.

4-4 Summary



We systematically investigated the PDA effect of post-deposition-annealing on the electrical and material characteristics of Ge MOS capacitors with hafnium-oxynitride gate dielectric. The different capacitor properties of HfO_xN_y film deposited on Ge and Si substrates may be closely correlated with the deposition mechanism as well as the compositions and thicknesses of the resultant ILs. The higher PDA temperature and longer PDA time was found to obtain the lower EOT of $\text{HfO}_x\text{N}_y/\text{Ge}$ gate stack, however, with a larger hysteresis width. A lower EOT of 19.5\AA with a low leakage current of $1.8 \times 10^{-5} \text{ A/cm}^2$ @ $V_g = -1\text{V}$, which is ~ 4 orders of magnitude reduction as compared to the standard SiO_2/Si , has been achieved after 600°C annealing for 5 min. Unfortunately, through the TDDB reliability test, the 10-year lifetime extrapolated operating voltage was lowered after the higher annealing temperature,

implying that the dielectric film have been degraded perhaps due to the severe charge trapping. On the other hand, the physical characterization of these films demonstrated that the inhomogeneous oxidation of as-deposited HfN film was observed and transferred into the homogeneous HfO_xN_y film after post thermal annealing. Meanwhile, a significant Ge incorporation and the presence of GeO_x oxide into the bulk dielectric were found upon 500°C . We believed that the continuous optimization of the interface structure through process modification is expected to further improve the electrical performance of the $\text{HfO}_x\text{N}_y/\text{Ge}$ gate stack, which thus be considered as a promising gate dielectric of Ge device.

