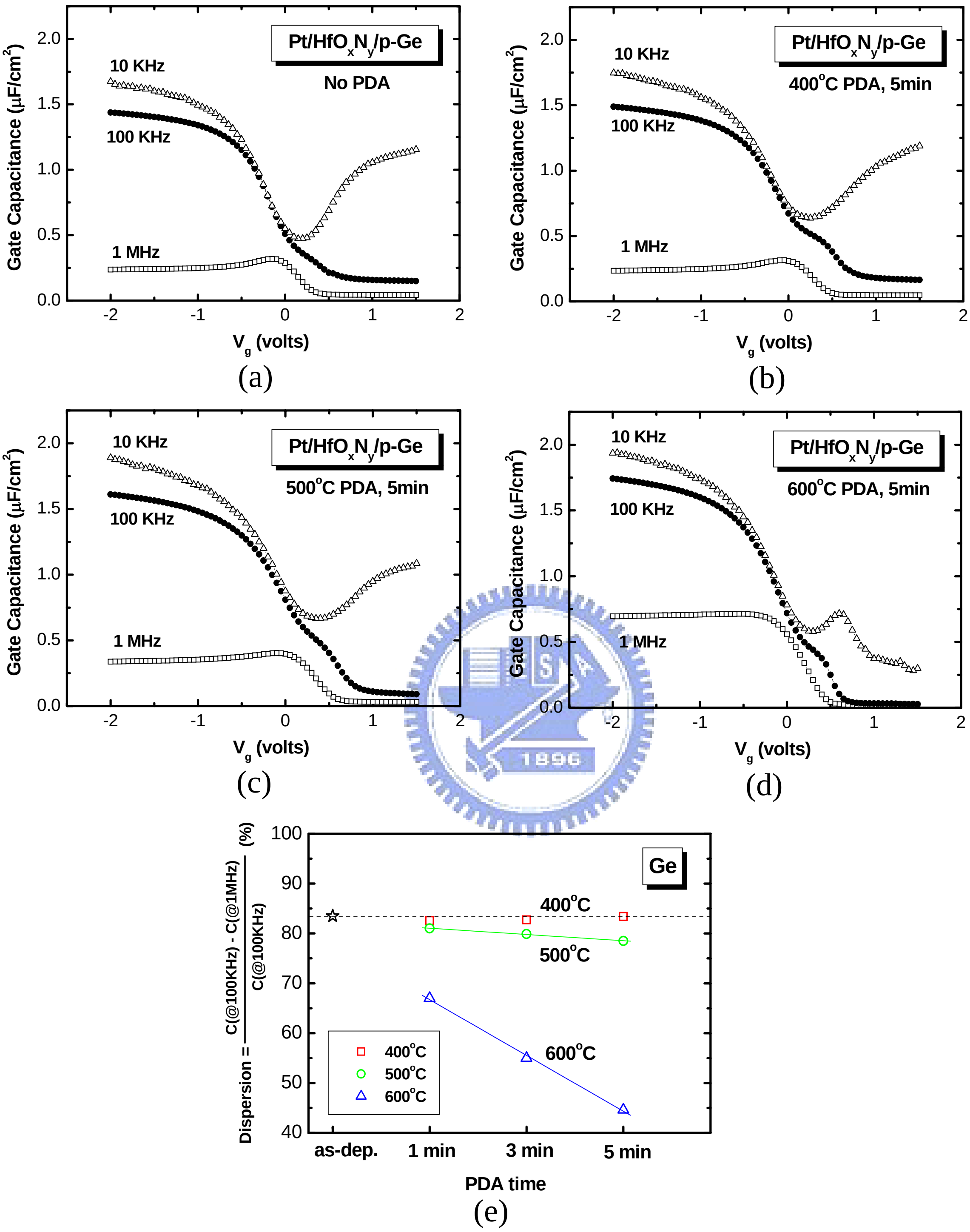
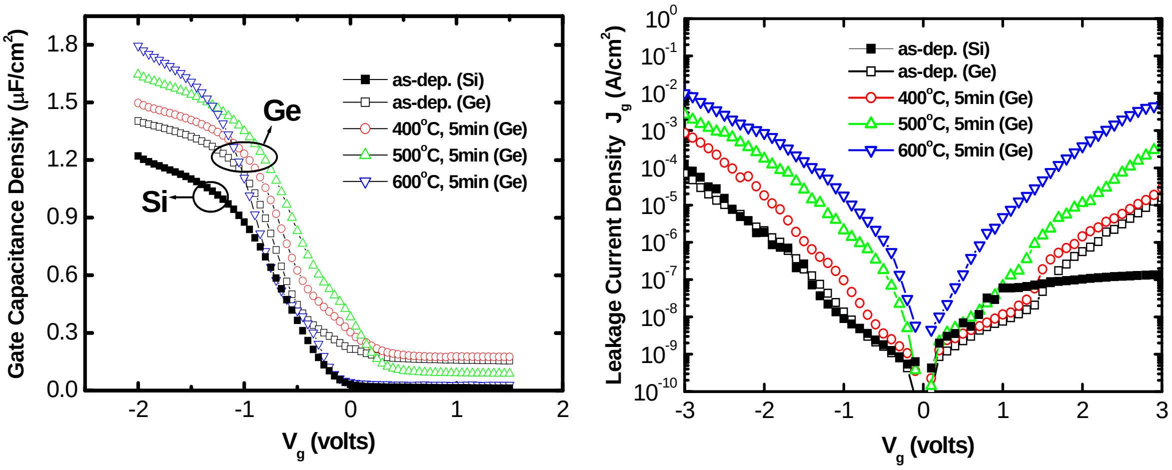


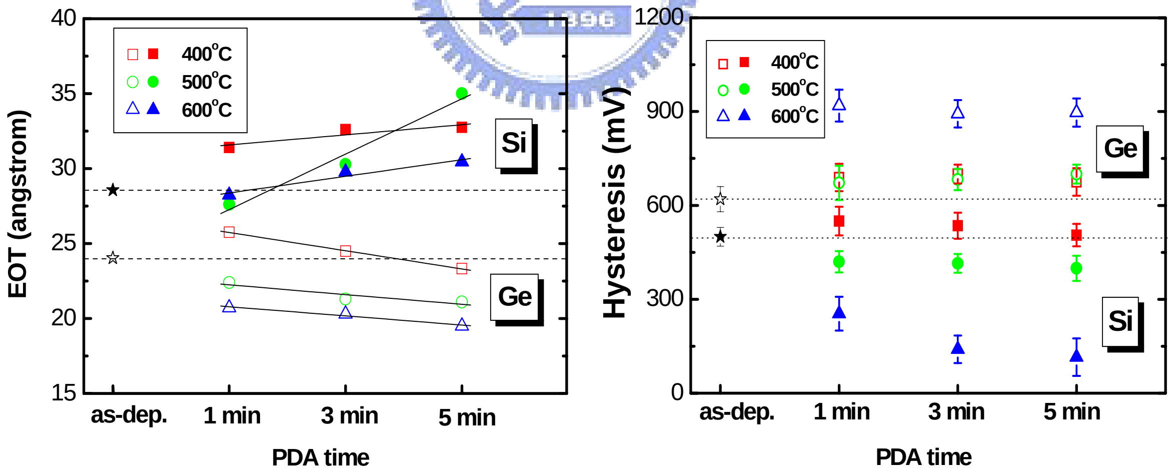
(a) (b) (c) (d) (e)

Fig. 4-1 (a)-(d) Multi-frequency *C*-*V* characteristics of Pt/HfO$_x$N$_y$/Ge MOS capacitor before and after the PDA. The sweep direction is from inversion to accumulation. (e) The PDA dependence of frequency dispersion observed in *C*-*V* characteristics.



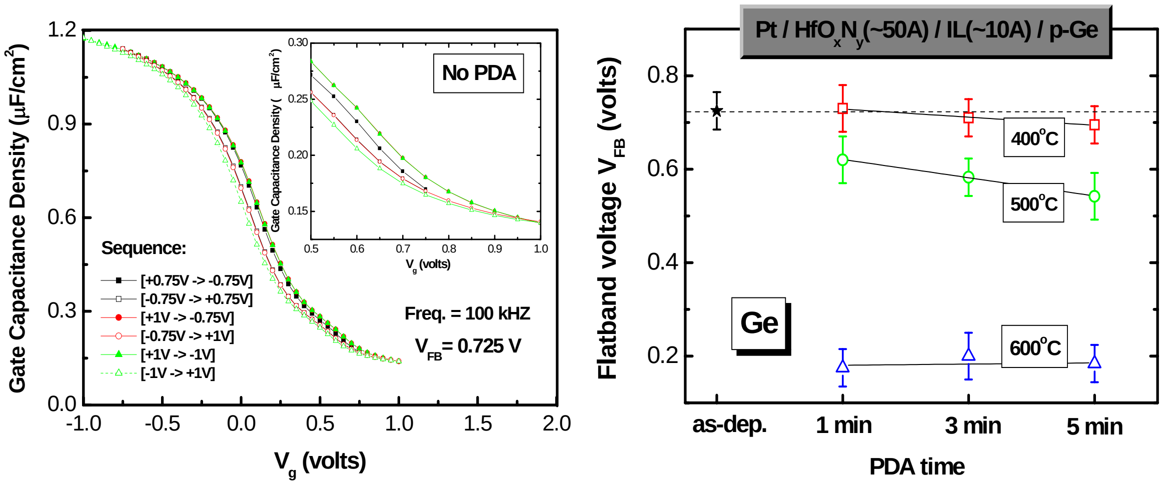
(a) (b)

Fig. 4-2 (a) The 100 kHz *C*-*V* and (b) *I*-*V* characteristics of Pt/HfO_xN_y/Ge (open symbols) MOS capacitors before and after the PDA. For comparison, as-deposited HfO_xN_y on Si (solid symbols) was also shown.



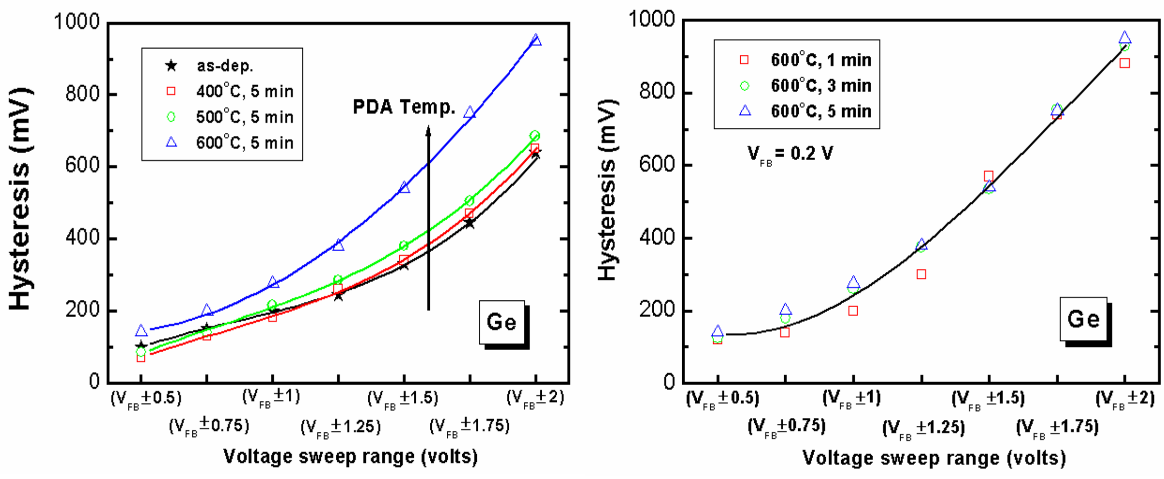
(a) (b)

Fig. 4-3 Comparison of (a) the EOT and (b) hysteresis width of the HfO_xN_y film on Si (solid symbols) and Ge (open symbols) substrates for different PDA temperatures and times.



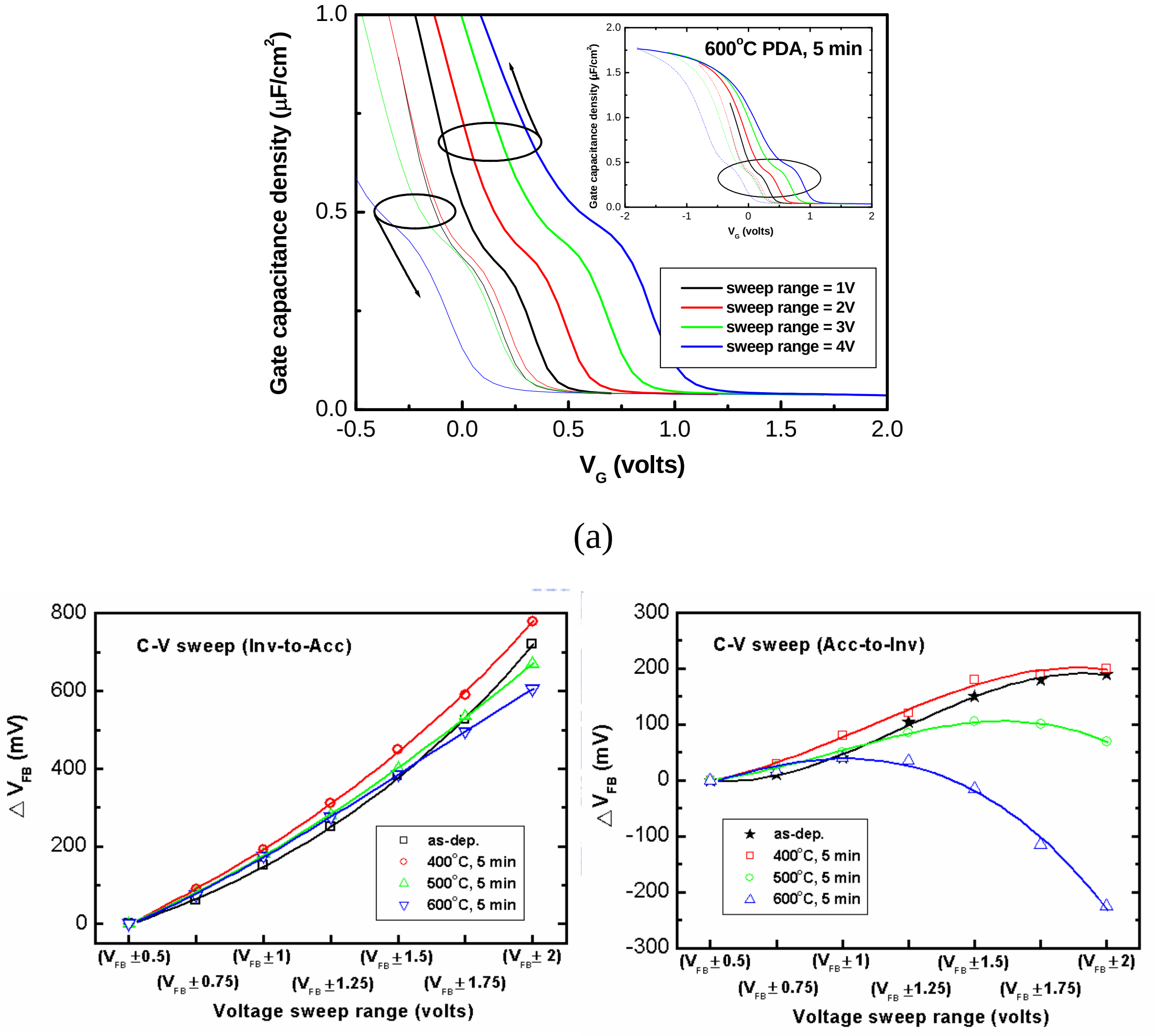
(a) (b)

Fig. 4-4 (a) A sequence of 100 kHz *C-V* curves with various sweep voltage ranges. The inset shows the zoom-in figure. (b) The flatband voltage before and after the PDA extracted from the C-V measurement for Pt/HfO_xN_y/Ge MOS capacitors.



(a) (b)

Fig. 4-5 (a) The hysteresis width as a function of sweep voltage range based on V_{FB} for different PDA temperatures. (b) The hysteresis width as a function of sweep voltage range based on V_{FB} for different PDA times.

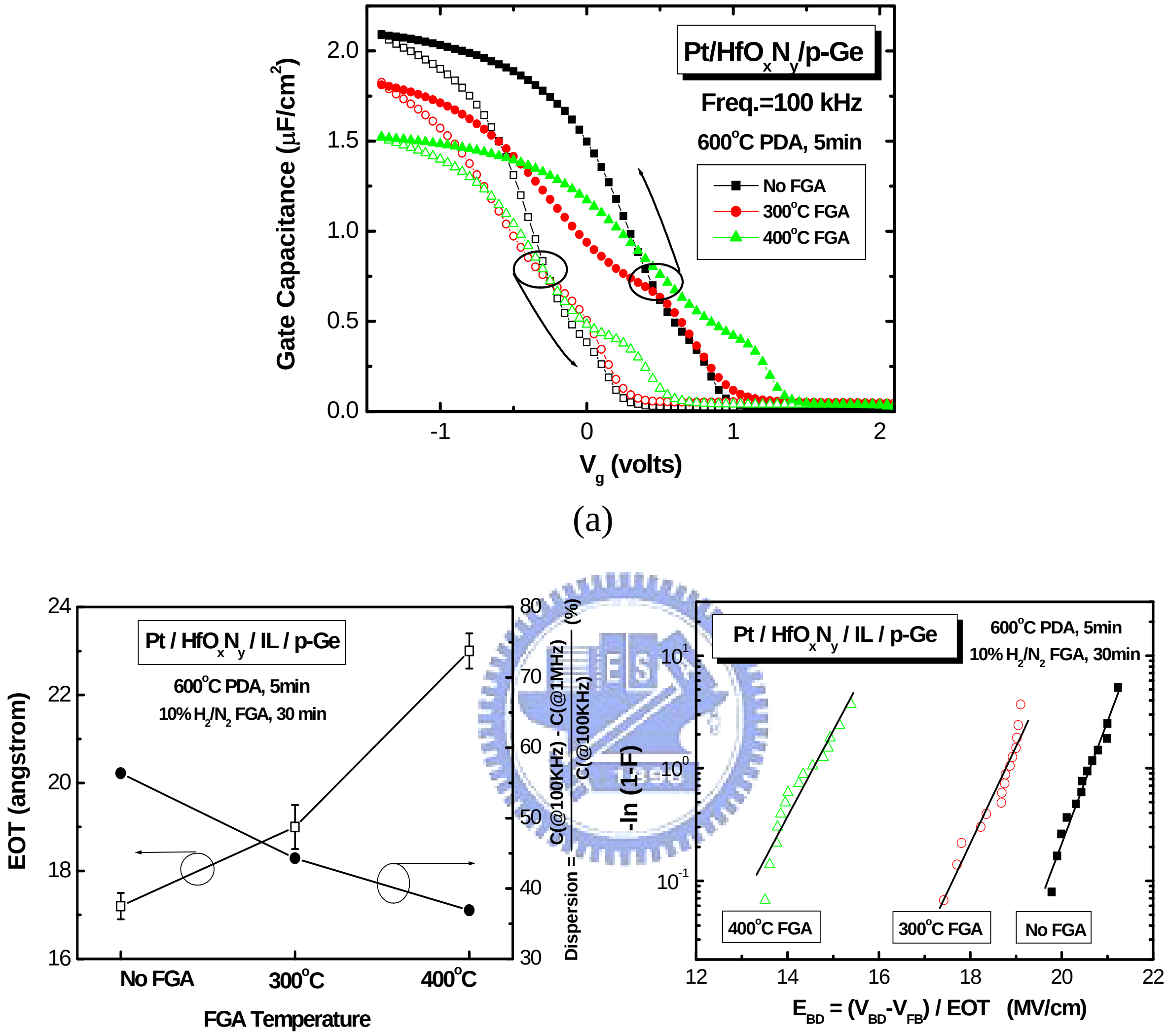


(a)

(b)

(c)

Fig. 4-6 (a) The *C-V* characteristics of Pt/HfO_xN_y/Ge MOS capacitor with four sweep voltage ranges. Noted that 600°C annealing was performed for 5 min. The shift of V_{FB} extracted from the sweep direction (b) from inversion to accumulation. (c) from accumulation to inversion.

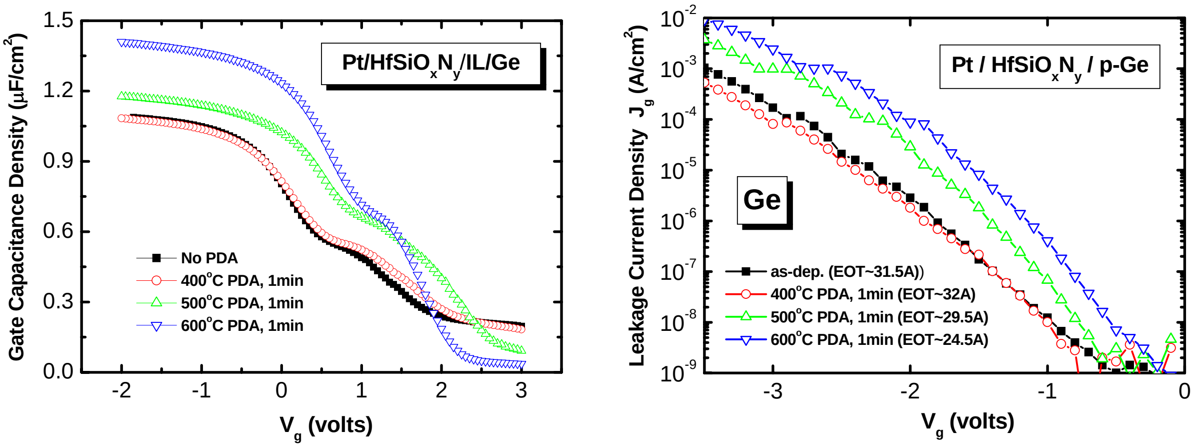


(a)

(b)

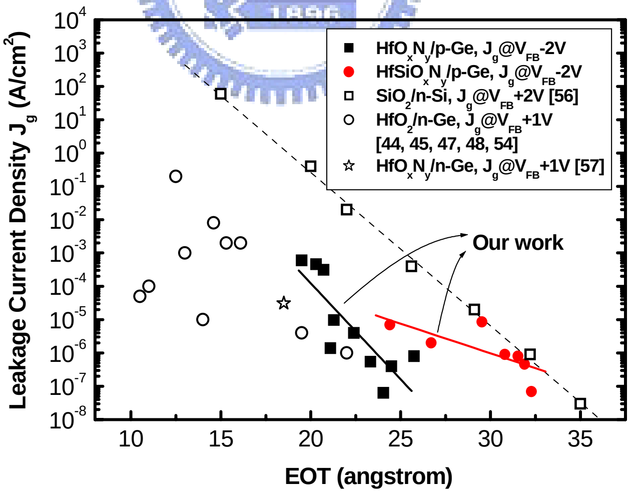
(c)

Fig. 4-7 (a) The *C-V* characteristics of Pt/HfO$_x$N$_y$/Ge MOS capacitor with and w/o FGA. (b) The estimated EOT and frequency dispersion as a function of FGA temperature. (c) The Weibull plot shows the FGA effect on E$_{BD}$.



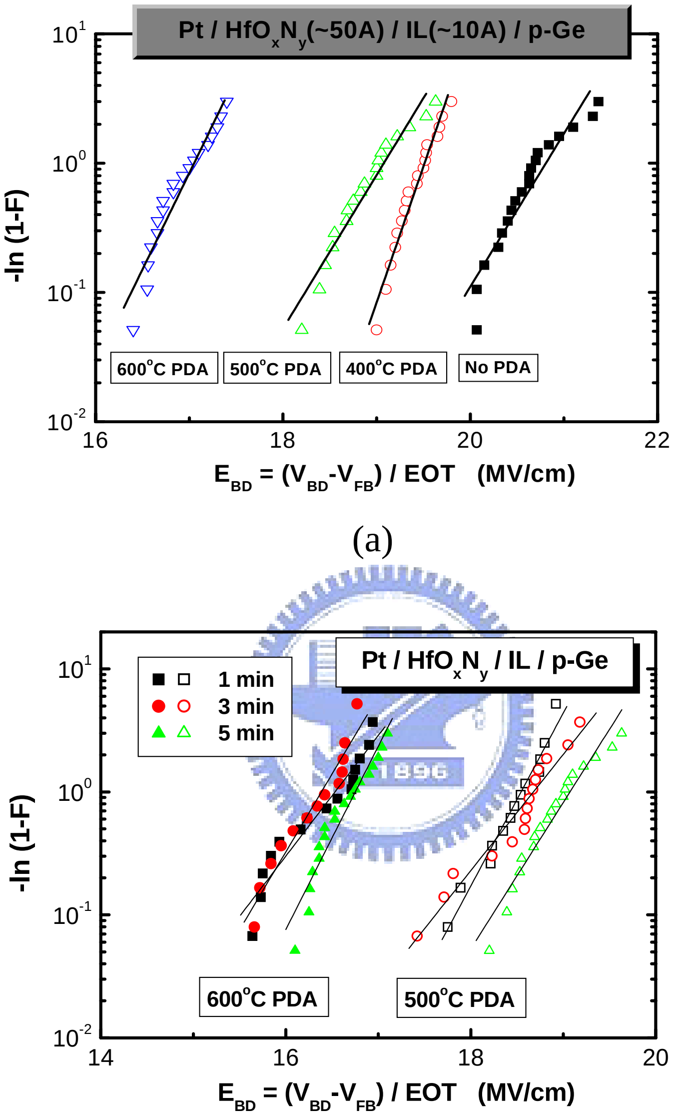
(a) (b)

Fig. 4-8 The (a) *C-V* and (b) *I-V* characteristics of Pt/HfSiON/p-Ge MOS capacitor before and after the PDA.



(c)

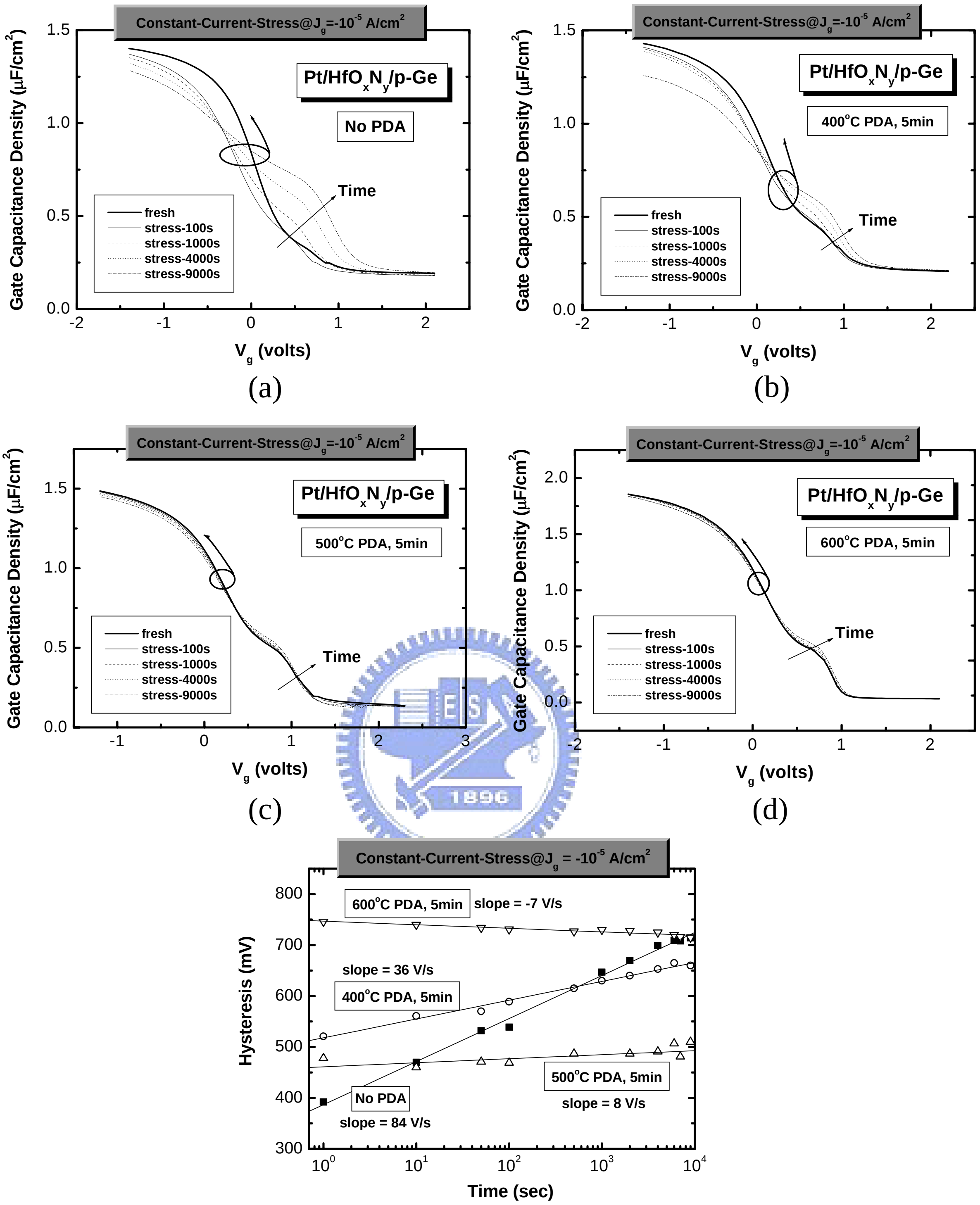
Fig. 4-9 Gate leakage currents versus the EOT for the deposited HfO_xN_y and HfSiON films on Ge substrate (solid symbols) were plotted together with other's published data (open symbols).



(a)

(b)

Fig. 4-10 (a) The Weibull plot shows the effect of PDA temperature on the variation of E_{BD}. (b) The Weibull plot shows the effect of PDA time on the variation of E_{BD}.

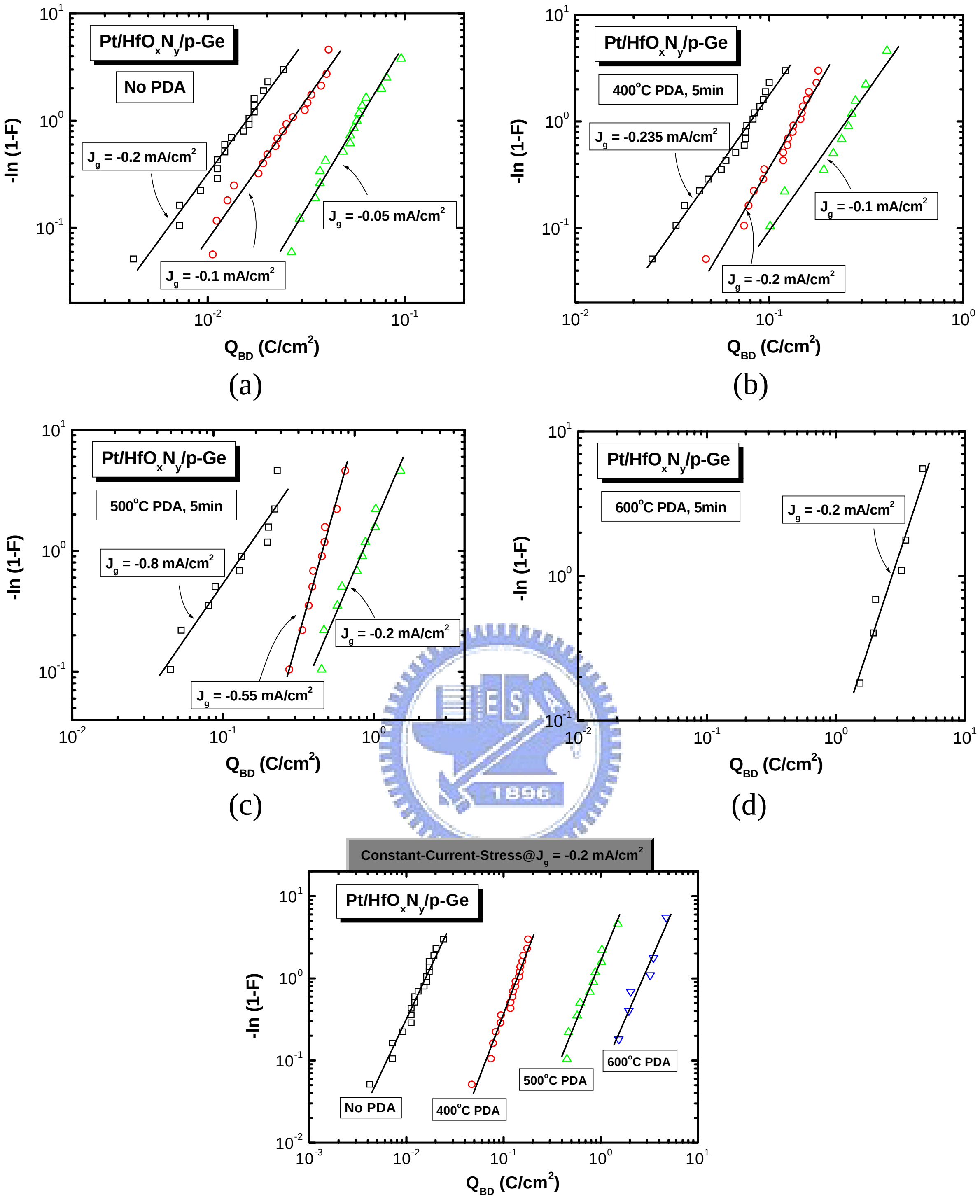


(a) (b)

(c) (d)

(e)

Fig. 4-11 (a)-(d) The *C*-*V* characteristics measured under the CCS of -10^{-5} A/cm^2 for as-deposited and annealed HfO$_x$N$_y$ films. (e) The variation of hysteresis width as a function of CCS time for as-deposited and annealed HfO$_x$N$_y$ films.

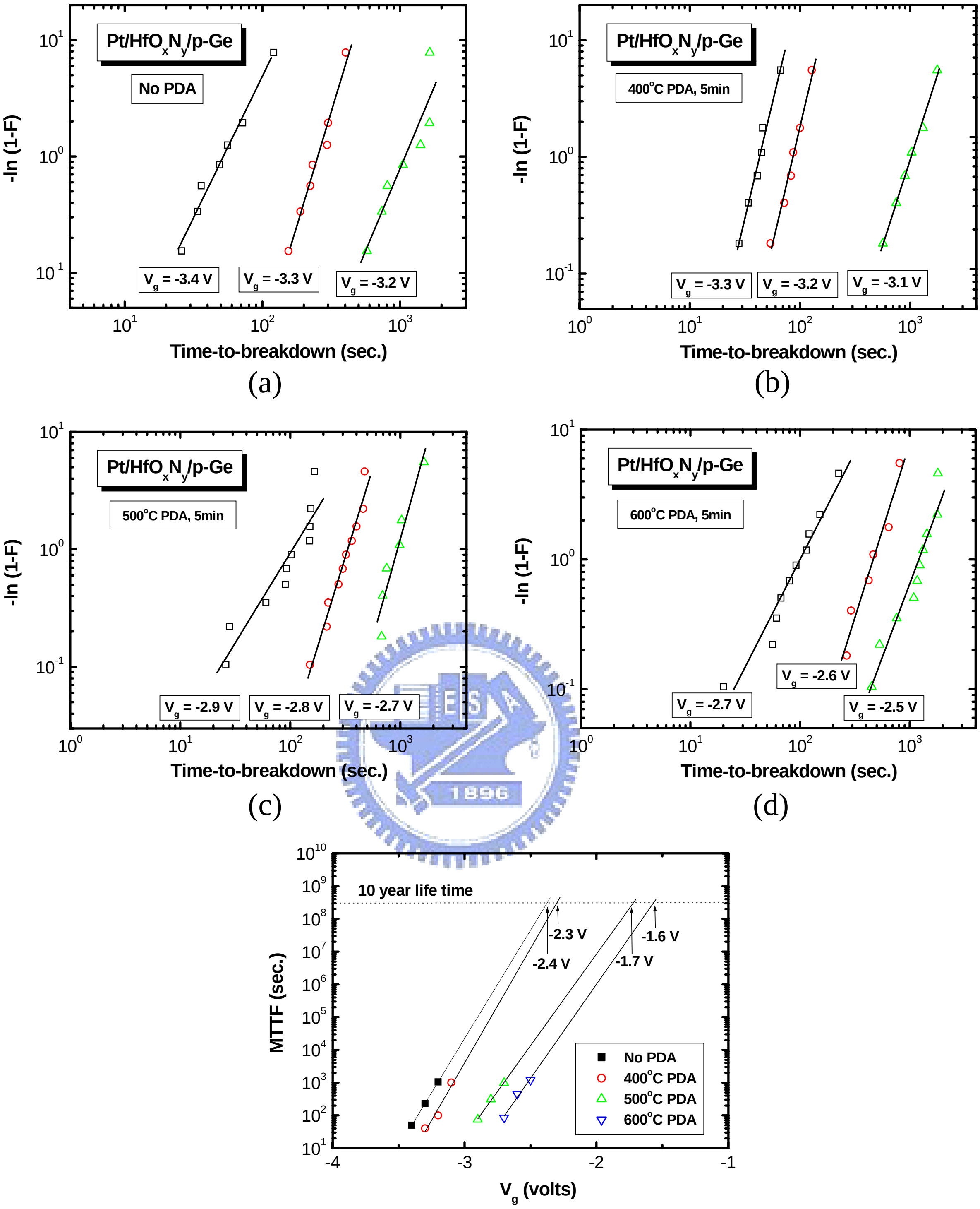


(a) (b)

(c) (d)

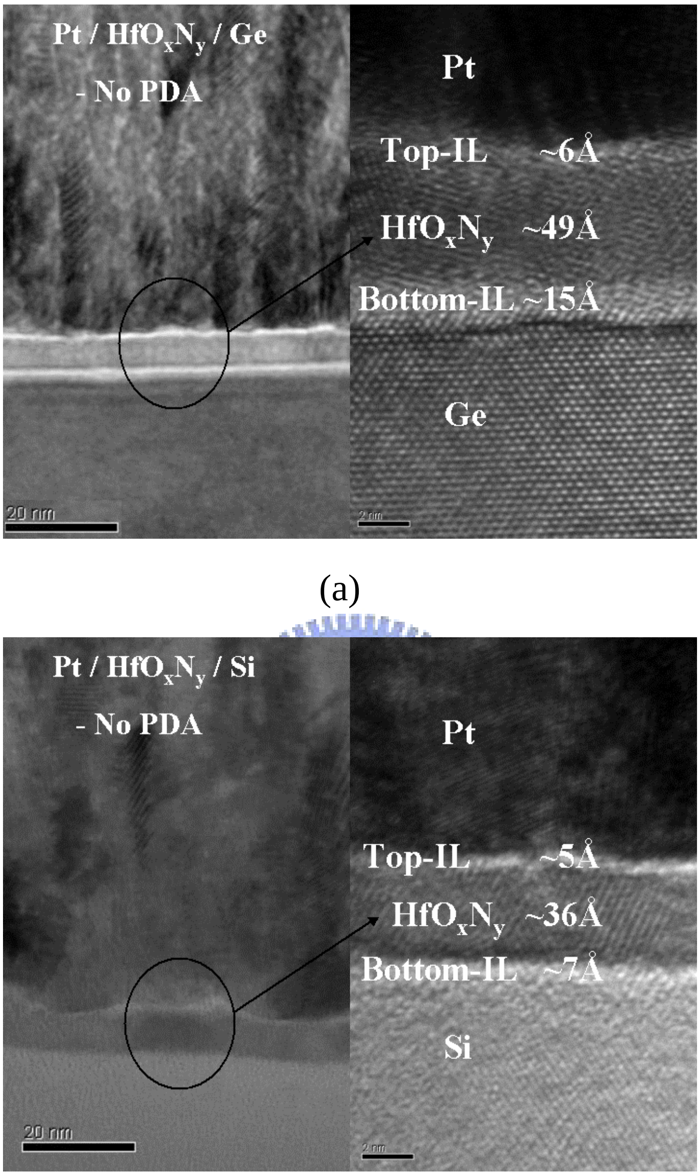
(e)

Fig. 4-12 (a)-(d) The Weibull plot shows the Q_{BD} under three CCS tests for as-deposited and annealed HfO_xN_y films. (e) The Weibull plot shows the Q_{BD} under the CCS of -2x10^{-4} A/cm^2 for the as-deposited and annealed HfO_xN_y films.



(a) (b) (c) (d) (e)

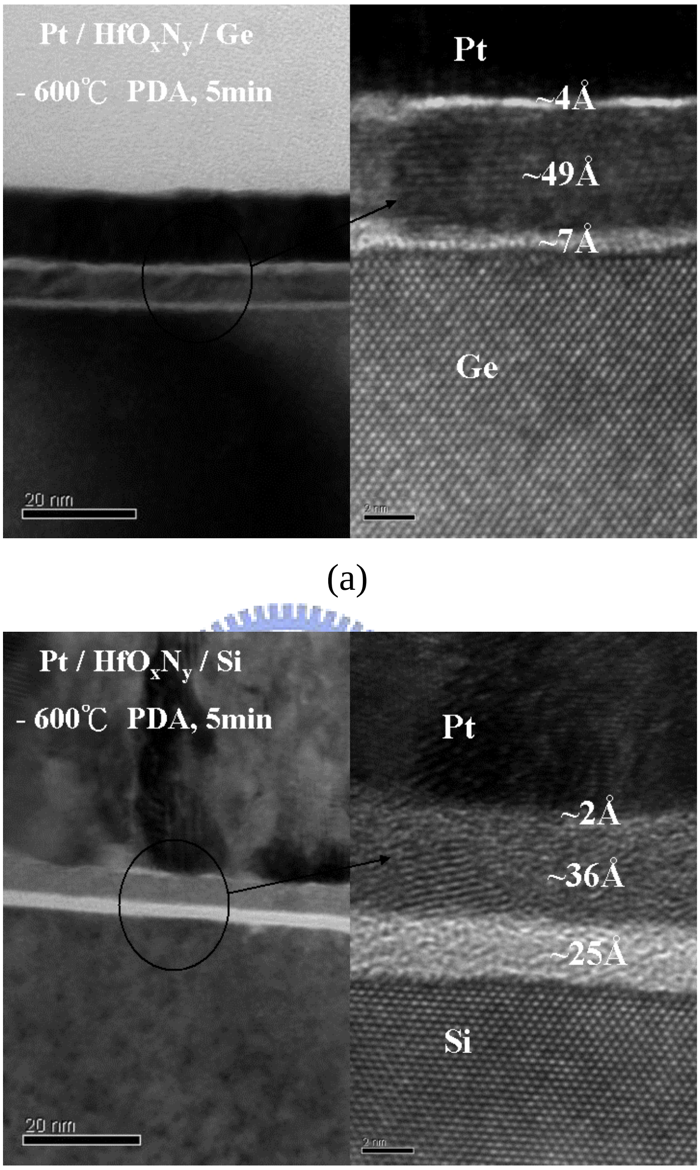
Fig. 4-13 (a)-(d) The Weibull plot shows the T_{BD} under three CVS tests for as-deposited and annealed HfO_xN_y films. (e) TDDB data reveal the 10-year lifetime extrapolated operating voltage is decreased with PDA temperature.



(a)

(b)

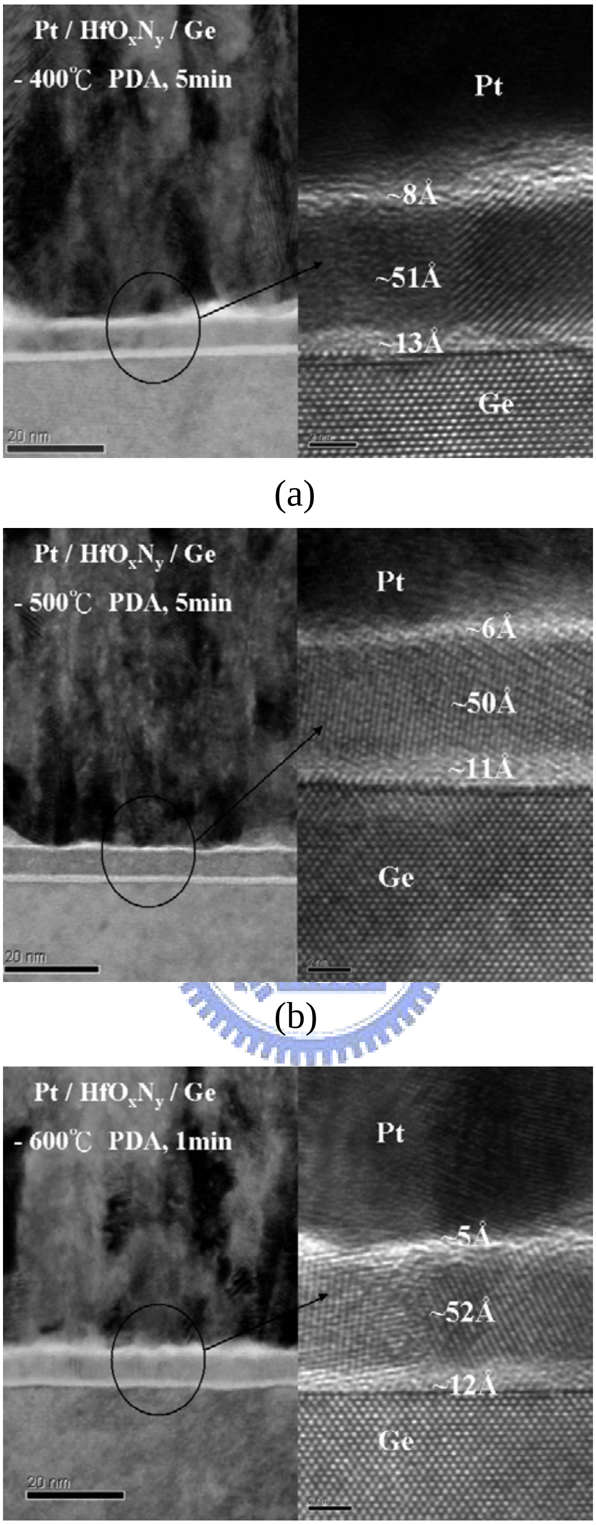
Fig. 4-14 (a) The HRTEM images of as-deposited HfO$_x$N$_y$ film on Ge and Si substrate.



(a)

(b)

Fig. 4-15 (a) The HRTEM images of as-deposited HfO$_x$N$_y$ film on Ge and Si substrate after thermal annealing at 600°C.

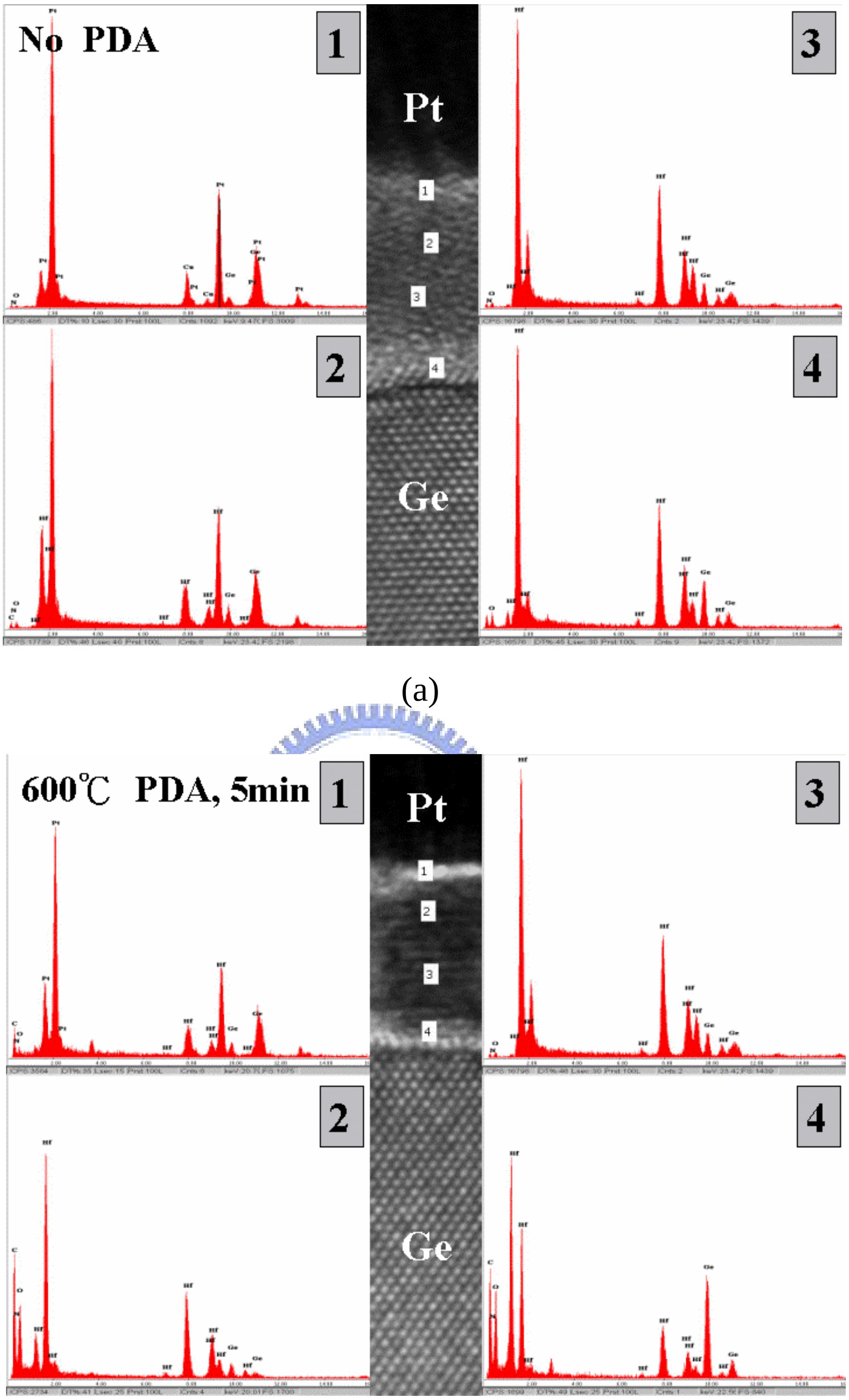


(a)

(b)

(c)

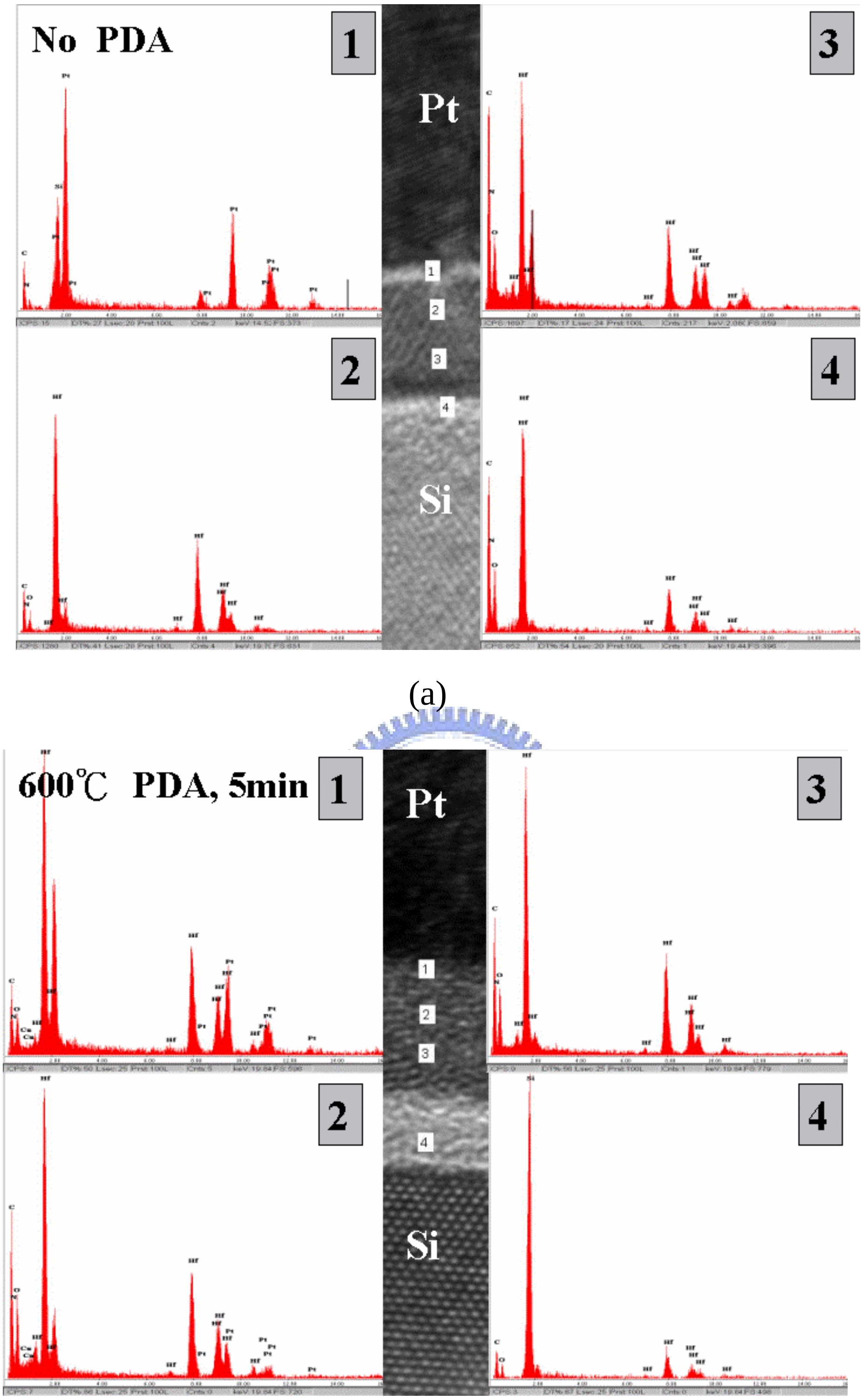
Fig. 4-16 (a) The HRTEM images of as-deposited HfO$_x$N$_y$ film on Ge substrate after post thermal annealing.



(a)

(b)

Fig. 4-17 (a) The EDS spectra of as-deposited HfO_xN_y film on Ge substrate before and after thermal annealing at 600°C.



(a)

(b)

Fig. 4-18 (a) The EDS spectra of as-deposited HfO_xN_y film on Si substrate before and after thermal annealing at 600°C.

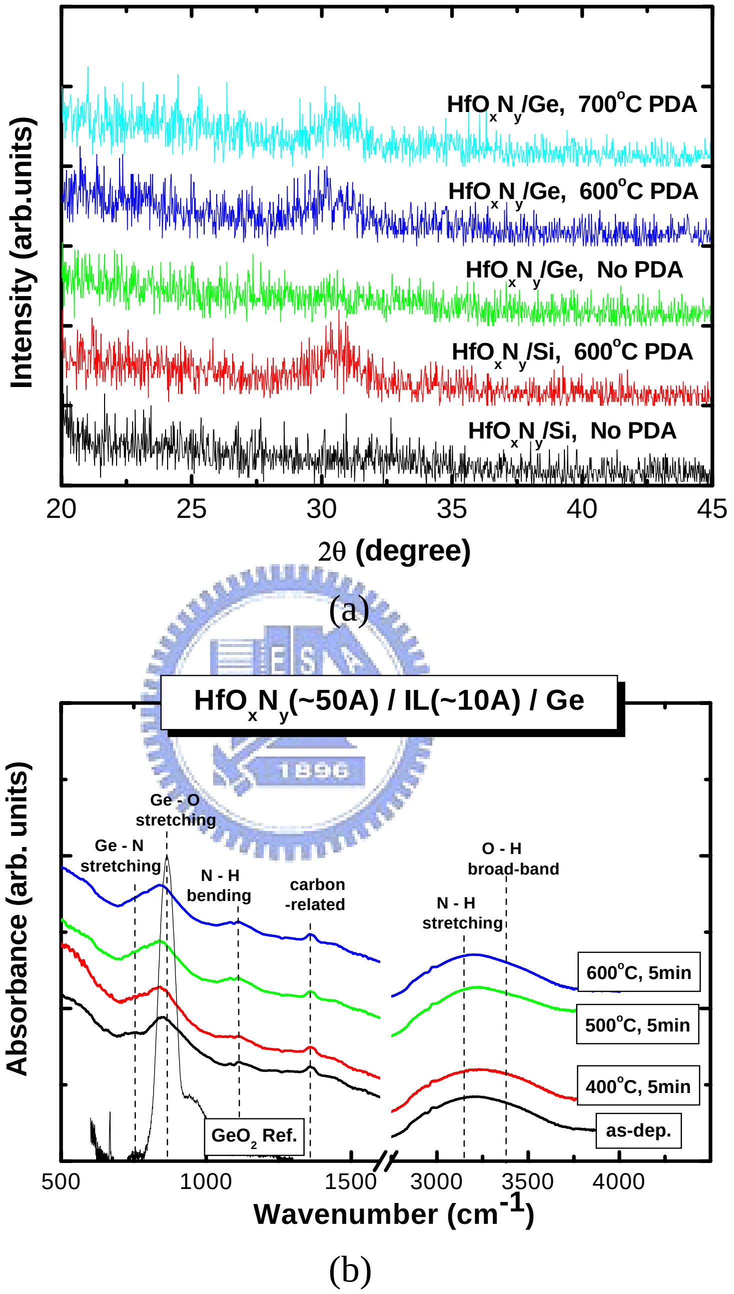
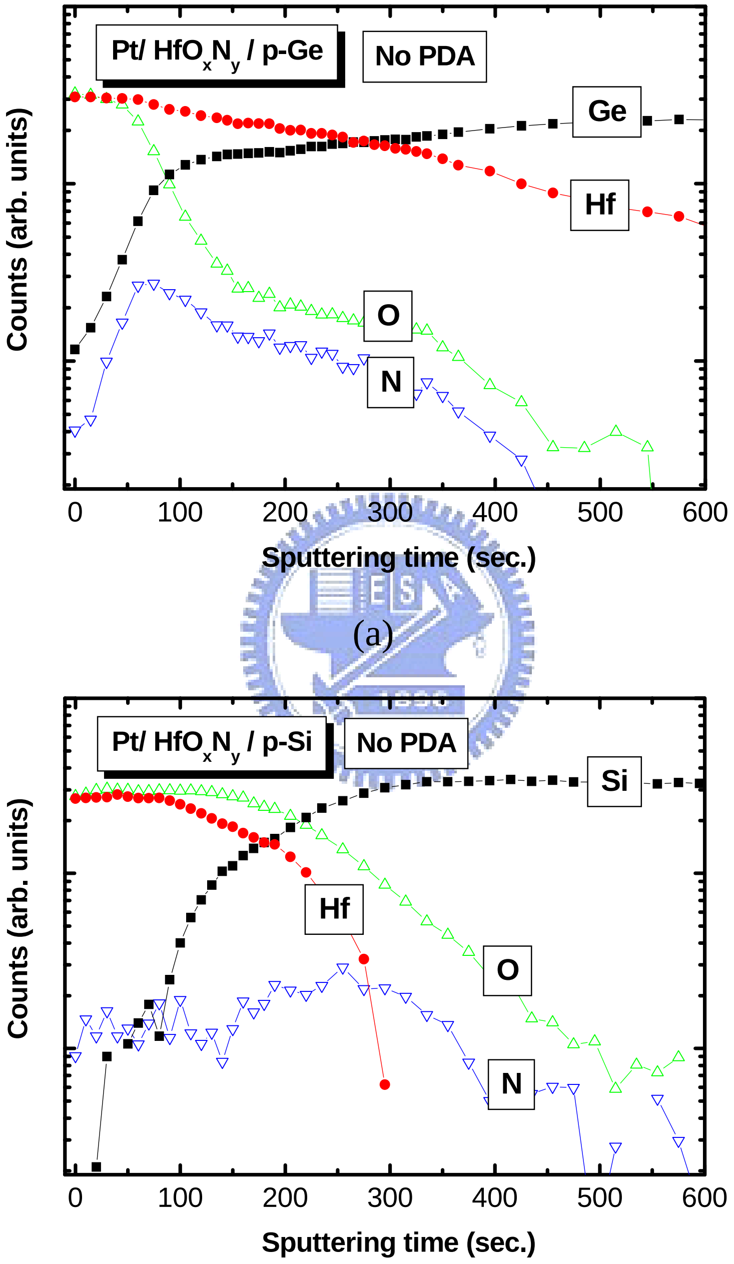


Fig. 4-19 (a) Glancing-angle XRD spectra of HfO_xN_y deposited film on Ge and Si substrate before and after thermal annealing. (b) The FTIR spectra of HfO_xN_y deposited film on Ge substrate before and after thermal annealing.



(a)

(b)

Fig. 4-20 (a) The AES depth profiles of as-deposited HfO$_x$N$_y$ film on Ge and Si substrate.

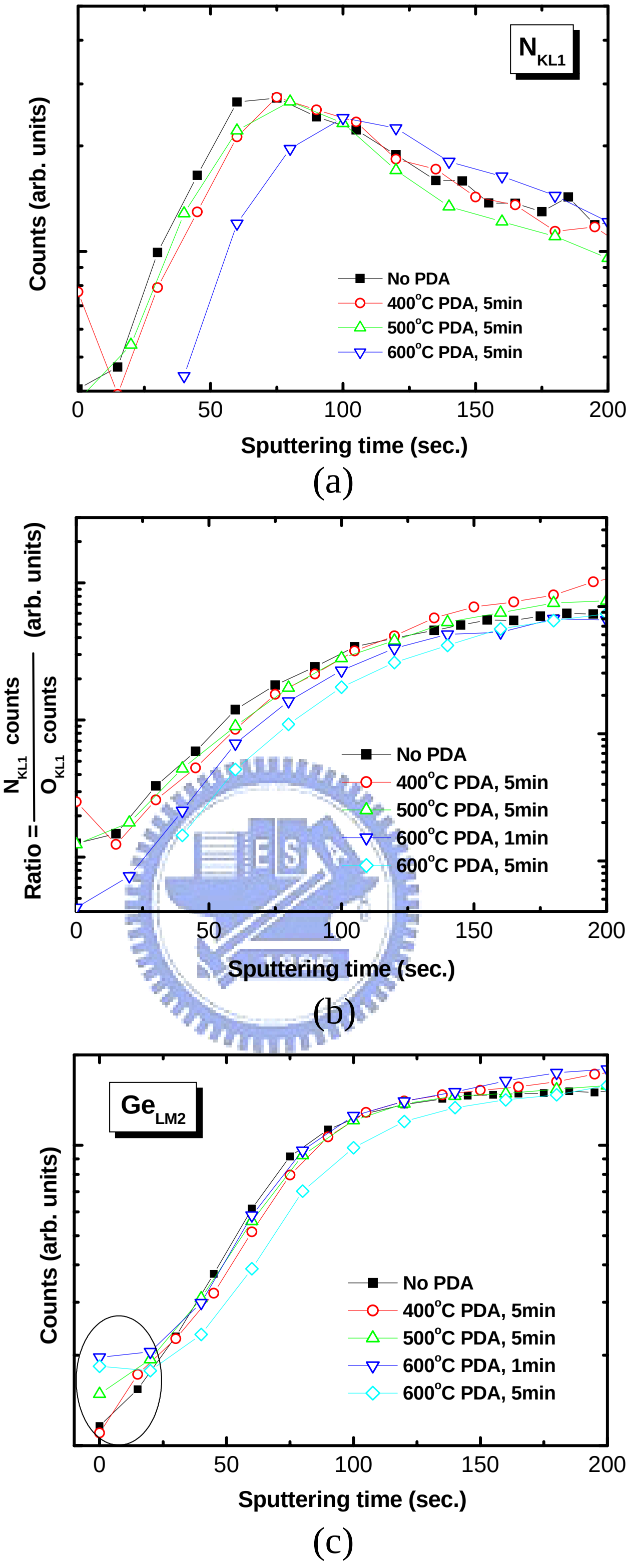


Fig. 4-21 The AES depth profiles of as-deposited HfO_xN_y film on Ge substrate before and after the PDA. (a) N_{KL1}. (b) Ratio of N_{KL1} to O_{KL1}. (c) Ge_{LM2}.

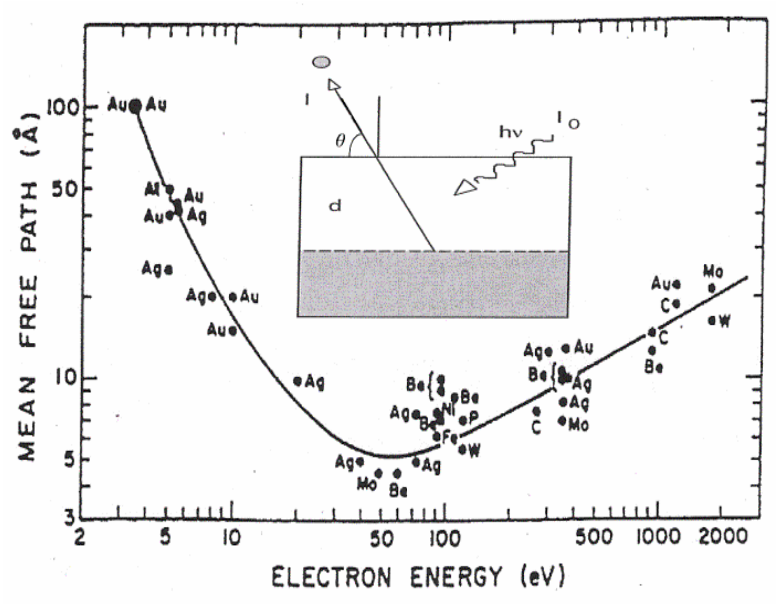
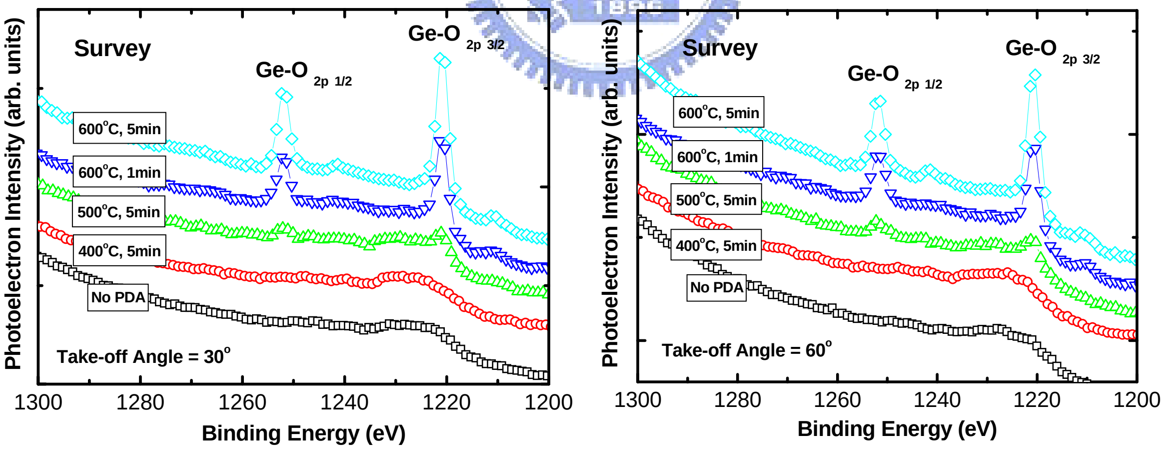
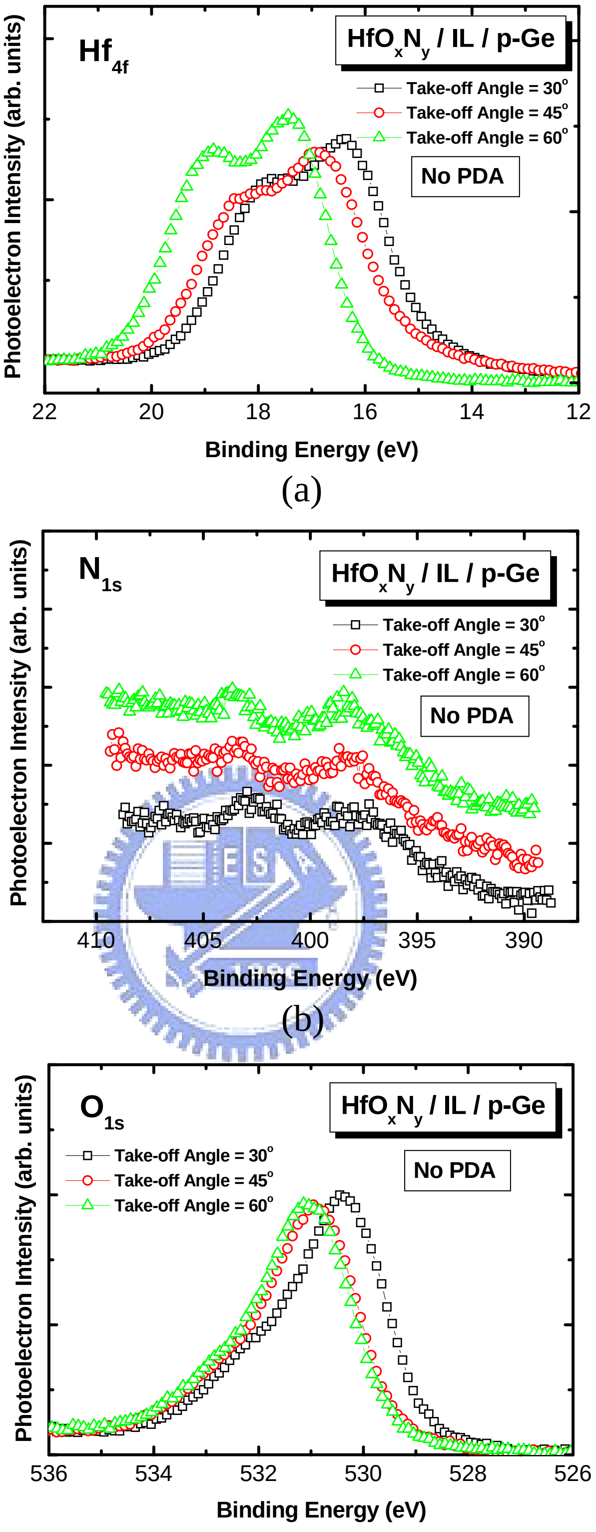


Fig. 4-22 The universal curve of electron IMFP versus kinetic energy. The inset shows the schematic of XPS incident and emission procedures.



(a)　　　　(b)

Fig. 4-23 Angle-resolved XPS survey from 1200 to 1300 eV for as-deposited and annealed HfO_xN_y films. (a) Take-off angle = 30°. (b) Take-off angle = 60°.



(a)

(b)

(c)

Fig. 4-24 Angle-resolved XPS spectra of as-deposited HfO$_x$N$_y$ films w/o PDA. (a) the Hf 4*f* core level; (b) the N 1*s* core level; (c) the O 1*s* core level.

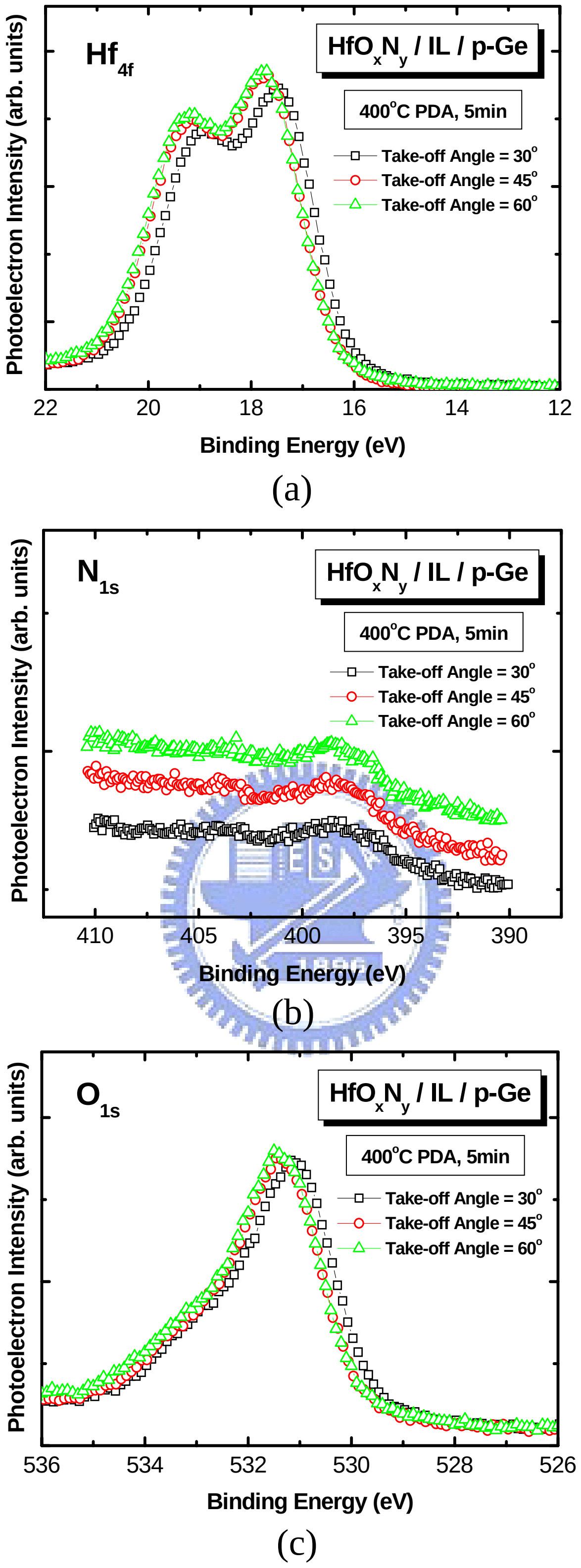
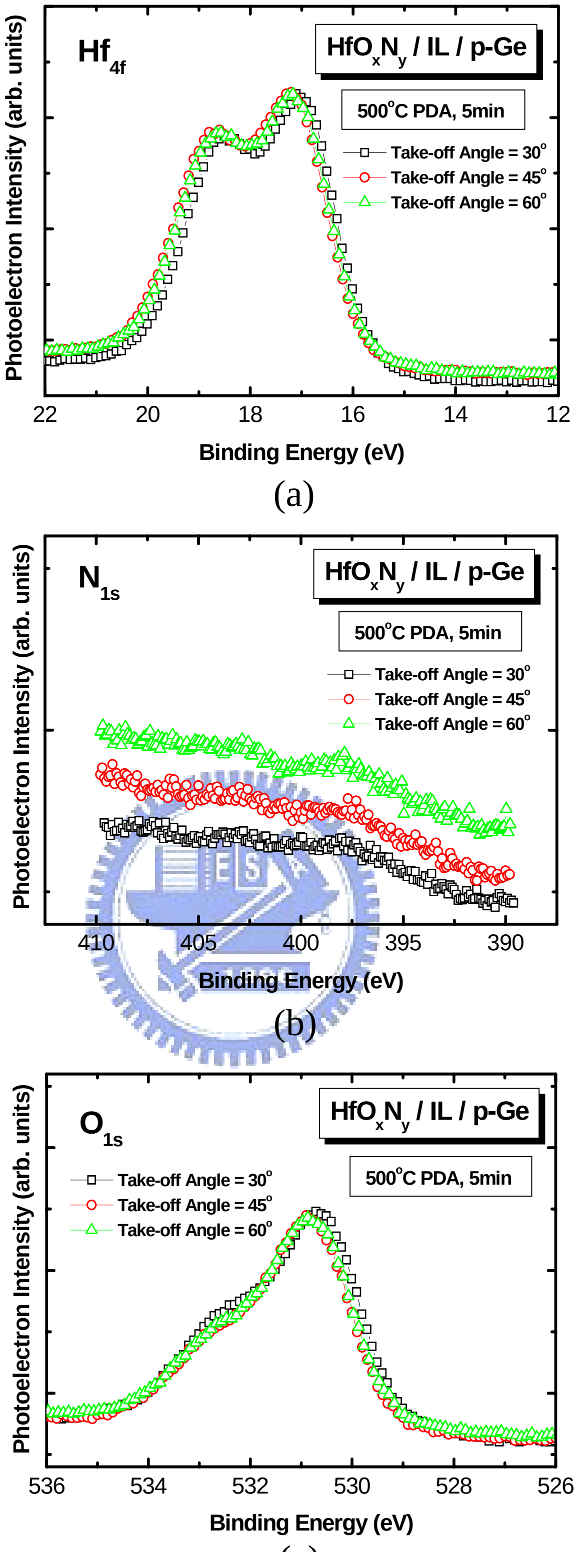


Fig. 4-25 Angle-resolved XPS spectra of the annealed HfO_xN_y film at 400°C for 5 min. (a) the Hf 4*f* core level; (b) the N 1*s* core level; (c) the O 1*s* core level.

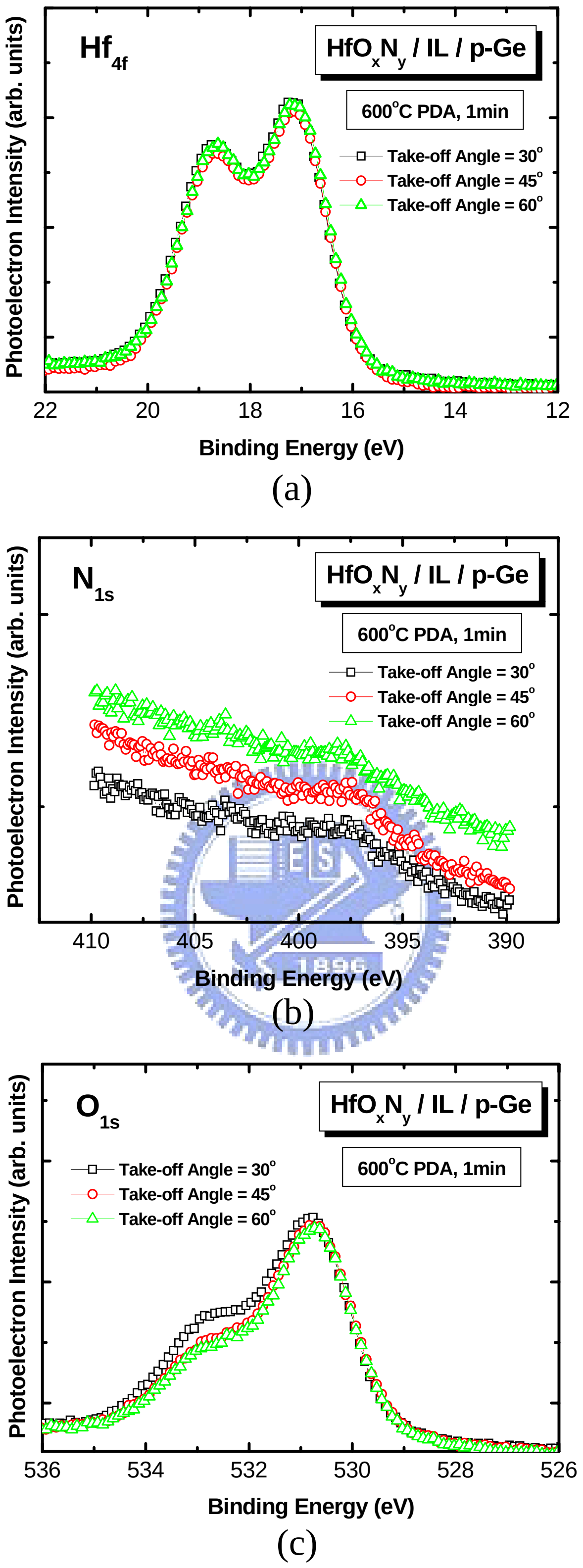


(a)

(b)

(c)

Fig. 4-26 Angle-resolved XPS spectra of the annealed HfO_xN_y film at 500°C for 5 min. (a) the Hf 4*f* core level; (b) the N 1*s* core level; (c) the O 1*s* core level.



(a)

(b)

(c)

Fig. 4-27 Angle-resolved XPS spectra of the annealed HfO_xN_y film at 600°C for 1 min. (a) the Hf 4*f* core level; (b) the N 1*s* core level; (c) the O 1*s* core level.

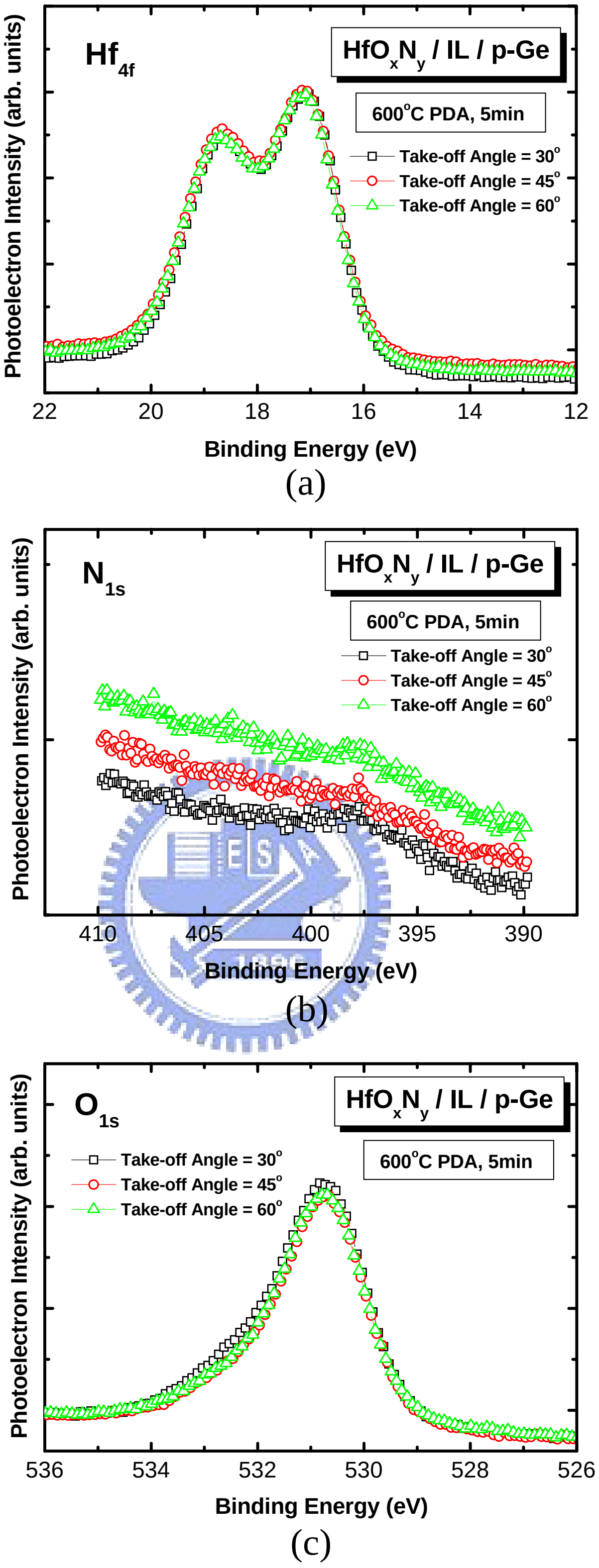
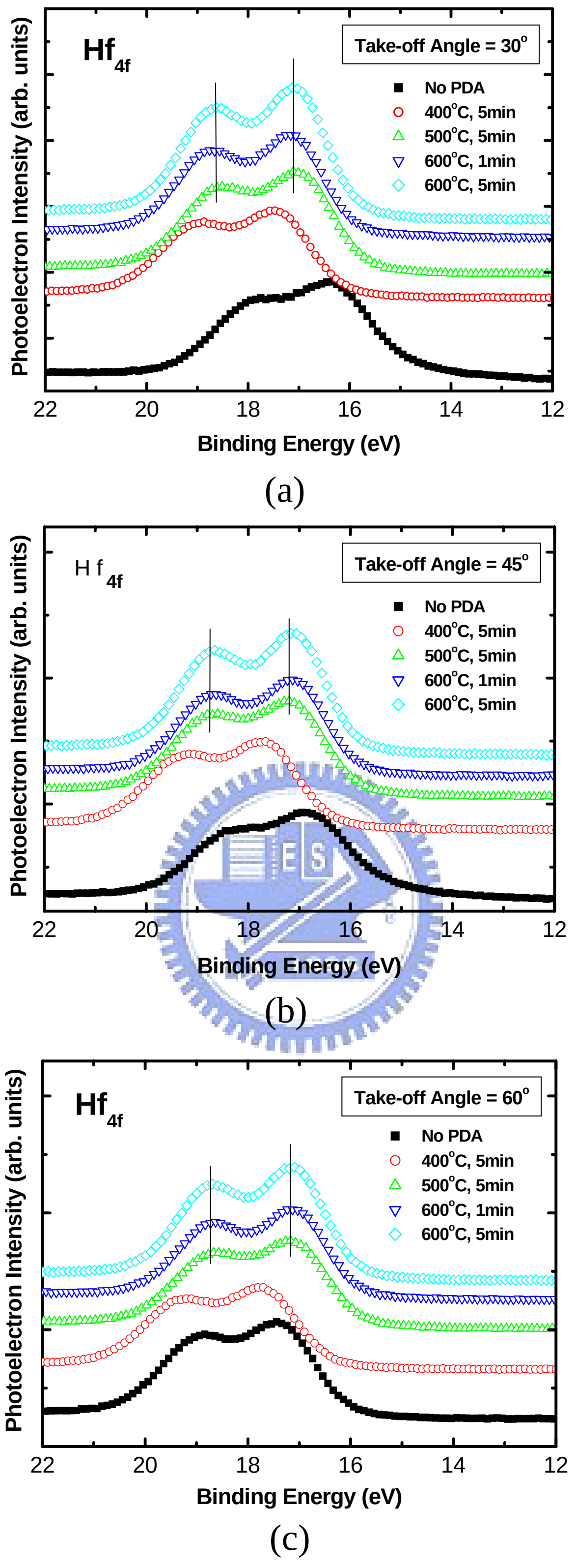


Fig. 4-28 Angle-resolved XPS spectra of the annealed HfO_xN_y film at 600°C for 5 min. (a) the Hf 4*f* core level; (b) the N 1*s* core level; (c) the O 1*s* core level.

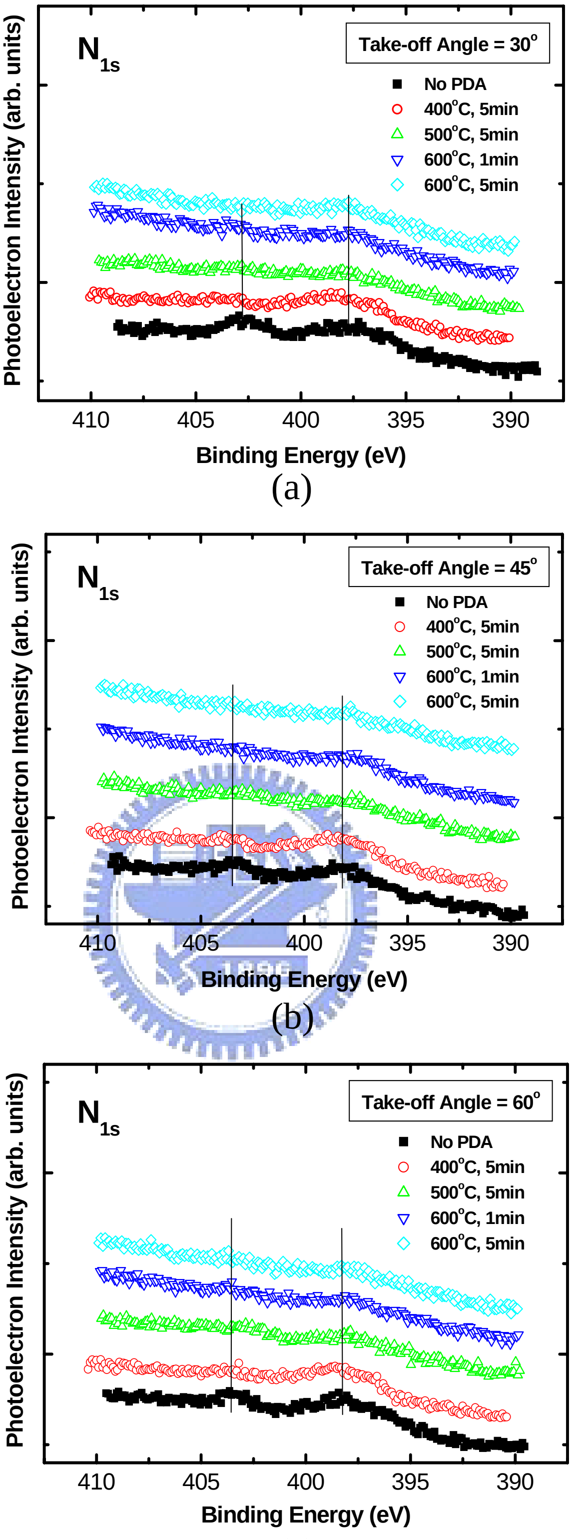


(a)

(b)

(c)

Fig. 4-29 Angle-resolved XPS spectra of the Hf 4*f* core level for the as-deposited and annealed HfO_xN_y films. (a) Angle = 30°; (b) Angle = 45°; (c) Angle = 60°.



(a)

(b)

(c)

Fig. 4-30 Angle-resolved XPS spectra of the N 1*s* core level for the as-deposited and annealed HfO$_x$N$_y$ films. (a) Angle = 30°; (b) Angle = 45°; (c) Angle = 60°.

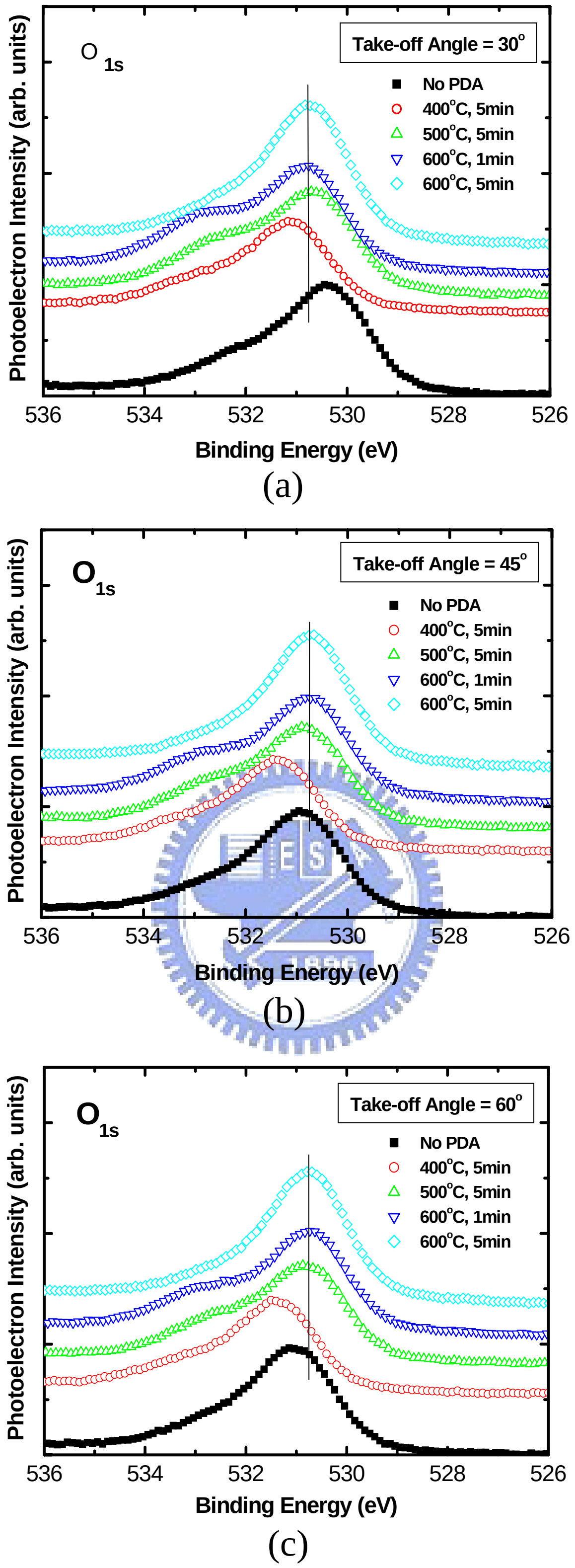


Fig. 4-31 Angle-resolved XPS spectra of the O 1*s* core level for the as-deposited and annealed HfO_xN_y films. (a) Angle = 30°; (b) Angle = 45°; (c) Angle = 60°.

Chapter 5

Conclusions and Suggestions for Future Work

5-1 Conclusions

Firstly, the flatness of the Ge surface was promoted with decreasing the acid etching concentration, whereas the hydrophobic phenomenon was also vanished. The optimized surface roughness was ~0.113 nm after the cyclical rinse of HF/DIW (1:30) and DIW. From the ellipsometry measurement and XPS examination, it showed that the growth of native oxide and carbon contamination on Ge surface as the exposure time increased. On the other hand, the oxidation behavior of Ge substrate showed two regimes, i,e., the linear oxidation rate was at initial stages, and the saturated oxidation rate was at prolonged stages. Nearly two monolayers of GeO_x layer were formed at lower temperature of 350°C for 30 sec in an O_2 ambient. Besides, thermal desorption of GeO_2 film was observed after 500°C annealing in an Ar and N_2 ambient. Considering the easily oxidized properties of Ge, these experimental findings suggest that the processing temperature is limited below 500°C and the interface damage may be occurred during the deposition of high-*k* material.

Next, the electrical and physical properties of MOCVD HfO_2 film deposited on Ge substrate were studied. For as-deposited HfO_2 film, the manifest frequency dispersion with a larger hysteresis was observed in multi-frequency *C-V* characteristics. Rapid thermal annealing of as-deposited film in an N_2 ambient also resulted in the degradation of the electrical performances, especially for the *C-V* distortion and gate leakage increment. For MOCVD HfO_2 deposition process, the lower deposition temperature of 400°C facilitated to obtain smoother deposition film, however, with a larger leakage current, while the higher deposition temperature of 500°C revealed the opposite tendency. Through the EDS analysis, the resultant composition of deposited HfO_2 film was found to be hafnium-germanium mixed oxide. Furthermore, it was found that the surface passivation, e.g., NH_3 pre-treatment, was essential to improve the quality of HfO_2 films on Ge surface. We suggested that the optimization of NH_3 plasma process, including the time, power, pressure, and gas flow, etc., might obtain the high-quality HfO_2 thin film on Ge substrate.

Subsequently, we also in-depth investigated the MOS capacitor characteristics of sputtered hafnium-oxynitride dielectric film on both Ge and Si substrates. The difference of electrical and material properties between two capacitor stacks may be closely related with the compositions and thicknesses of the resultant IL and bulk dielectric. The higher PDA temperature and longer PDA time were found to obtain the lower EOT of HfO_xN_y/Ge gate stack, however, with a larger hysteresis width. A lower EOT of 19.5 Å with a low leakage current of 1.8×10^{-5} A/cm^2 at $V_g = -1$ V, which is ~4 orders of magnitude reduction as compared to the standard SiO_2/Si, have been achieved after 600°C annealing for 5 min. Unfortunately, the 10-year lifetime obtained from the TDDB test was gradually degraded after the higher annealing temperature perhaps because of the severe charge trapping effect. From the physical characterization of these films, the inhomogeneous oxidation of as-deposited

HfN film was concluded and transferred into the homogeneous HfO_xN_y film after post thermal annealing. Meanwhile, a significant Ge incorporation and the presence of GeO_x oxide were examined upon 500°C.

Finally, we believe that the continuous optimization of the interface structure through process modification is expected to further improve the electrical performance of the HfO_xN_y/Ge gate stack, which thus be considered as a promising gate dielectric of Ge device.

5-2 Future Work

For the Ge cleaning, the absence of the hydrophobic phenomenon gives rise to our attention, differing from the traditional hydrogen-terminated Si. We suppose that this phenomenon is closely related to the required formation energy and the strength of Ge-H/Ge-F bonding. Because of such an interest difference between Si and Ge substrate, how to obtain the suitable cleaning procedures for Ge wafer and clarify the discrepancy of surface bonding mechanism between these two substrates is an attractive issue.

In the Chapter 3, we have demonstrated that the surface nitridation through NH_3 plasma is required to improve the HfO_2 dielectric film on Ge, especially the leakage performance. Several investigators also reported the need of surface passivation to obtain the high quality of HfO_2 thin film. On the other hand, the easily oxidized properties of Ge and the thermal instability of the GeO_2 have been noticed in our experiments. Therefore, the attempt of different surface pre-treatments, such as the NH_3, SiH_4 and CF_4, in order to change the surface bonding states may be a essential procedure to improve the electrical characteristics of HfO_2 film and other oxide-based high-*k* materials.

In the Chapter 4, a considerable hysteresis width observed in sputtered HfO_xN_y film on Ge is the most serious problem, which in turn lead to threshold instability of Ge MOSFET. The PDA resulting in the reliability degradation of dielectric film may be owing to the Ge incorporation and the formation of GeO_x bonding, since these events may serve as the trapping states and/or dielectric defects. One solution is the attempt of surface passivation has mentioned above, another is the enhanced nitrogen incorporation into the HfO_xN_y film to suppress the crystallinity. In addition, the post CF_4-plasma treatment of the HfO_xN_y film before the PDA is performed. The aims of fluorine incorporation are expected to diminish the defects inside the gate dielectric and increase the resistance to Ge inter-diffusion. For the physical characterization, i.e., XPS and AES, the change of composition bonding and their mechanism for bulk dielectric and interface layer before and after the PDA can be characterized in depth.

On the other hand, although the electrical performance of sputtered HfSiON thin film on Ge substrate is out of expectation, it is believed that the HfSiON film can be considered as the suitable insulator on Ge through the modification of fabrication process. For example, the co-sputtering of Hf and Si target replaces the $HfSi_2$ target to form the HfSiON film. We also suggest that other nitrided high-*k* gate dielectrics with closer lattice match to Ge may be good candidates for epitaxial in high-*k*/Ge MOS devices.

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