Chapter 5

Conclusions

LTPS TFTs are widely applied in the fields of active-matrix displays, system-on-panel, and 3D ICs. Unfortunately, conventional LTPS TFTs suffer from both poor device characteristics and reliability, which are caused by large leakage current, kink effect, and hot-carrier effect, as well as limit the development in those application fields. Therefore, there is great interest in improving the performance of LTPS TFTs.

Although many drain relief structures to improve those undesired effect has been reported, they often require additional implantation for lightly doped drain, and/or complicated process (such as, spacer formation), and/or more process mask numbers. In this thesis, we have demonstrated three improved structures with the novel process to suppress the unfavorable effects pertaining to electrical field near drain junction. And, those structures are required no additional mask and ion-implantation process to fabricate. They are self-aligned field induced drain, gate overlapped graded with a bottom gate structure, and gate overlapped graded with a double gate structure, respectively.

In this work, device simulation is carried out to compare the maximum electric field of TFTs with different drain junction structures, which is followed by the experimental details of fabricating LTPS TFTs. The proposed FID TFTs with the Vacuum cavities near the drain side both can reduce the maximum vertical and lateral electric field. And gate overlapped graded LDD LTPS TFTs with a bottom gate structure and a double gate also can effectively reduce the lateral electric field. The graded LDD is *in-situ* formed during the source/drain laser activation and without any additional ion-implantation. As the maximum drain electric field is

reduced, the leakage current and kink current can be reduced and the hot-carrier reliability also can be improved.