以新穎降電場結構改善低溫多晶矽薄膜電晶體特性之研究

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摘要

低溫多晶矽薄膜電晶體已被廣泛運用於主動式陣列顯示器(active matrix display)的開關元件以及在其同一基板上的周邊控制電路。相信在更進一步發展後，多功能的電路與系統也可完全整合在同一面板上，指即為所謂的System-on-Panel (SOP)。而多晶矽薄膜電晶體也可用於垂直整合(vertical integration)的超大型積體電路上，如此一來除了可使整體的集成密度提升更可藉由減少信號傳輸的延遲而增加積體電路的效能。不幸的是，傳統低溫多晶矽薄膜電晶體由於有較大的漏電流、扭結效應(kink effcet)、熱載子效應(hot-carrier effect)，使得元件特性不佳、可靠度低。這嚴重的限制了它在前面敘述的發展。也因此，如何提升低溫多晶矽薄膜電晶體的效能是非常重要的。

造成大漏電流、扭結效應(kink effcet)、熱載子效應等不好的效應主要是靠近汲極接面的大電場造成。也就是說，降低其大電場即可有效抑制那些不好的效應。已經很多文獻報導很多結構皆可有效降低汲極電場。但是，那些結構往往需要額外的離子植入去形成低參雜汲極結構；或是需要較複雜的製程，如側間隔(spacer)的製作；或是製程上需要較多到光罩數目。

在本論文中，我們提出了三種利用新穎製程以降低汲極端電場的結構，來抑制那些由汲極端大電場造成的效應。且這三種結構皆簡單製作而不需額外的光罩數和額外的離

子植入。首先，一個對稱性自對準 self-aligned field induce drain (FID)被我們提出，它只需要一次選擇性的磷酸側吃製程去形成 FID 的 sub-gate 和 main-gate。接下來，下閘極和雙閘極的 gate overlapped graded LDD 的結構分別也被我們提出。其 LDD 區域為線性分布且可藉由活化源極/汲極時自然形成而不要需要任何的離子植入製程。藉由模擬分析，這些結構也皆可有效降低汲極端電場。

Study on the Novel Drain-Relief Structures in Low-Temperature Polycrystalline Silicon Thin Film Transistors to Improve the Device Characteristics

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ABSTRACT

Low-temperature poly-Si thin film transistors (LTPS TFTs) have been used as pixel switches in active matrix displays and as devices in driver integration onto display substrate as well. High-performance poly-Si TFTs. With more future development, high versatile circuits and systems can be fully integrated on the display panel substrate, which is so-called system-on-panel (SOP). Moreover, poly-Si may allow the vertical integration of devices for VLSI that can increase packing density and improve performance through reduced interconnect delay. Unfortunately, conventional LTPS TFTs suffer from both poor device characteristics and reliability, which result from the undesired effects, including large leakage current, kink effect, and hot-carrier effect and limit the development in those fields. Therefore, there is great interest in improving the performance of LTPS TFTs.

All the undesired effects are mainly caused by the high electric field near the drain junction. That is, "how to reduce the electric field" is an important topic in LTPS TFTs. It has been widely reported that many structures can effectively relax the maximum drain electric field in the channel. However, those structures often require additional implantation for lightly doped drain, and/or complicated process (such as, spacer formation), and/or more process

mask numbers. In this thesis, we demonstrate three drain-relief structures with the novel process to suppress the unfavorable effects pertaining to electrical field near drain junction. And, those structures are simple to fabricate without any additional mask and implantation process. First, a symmetric self-aligned field induce drain (FID) LTPS TFTs is proposed and it only require one selective H_3PO_4 side-etch process to form sub-gate and main-gate. Then, two gate overlapped graded LDD structures with bottom gate and double gate, respectively, are also proposed. The LDD is graded distribution and is *in-situ* formed during the source/drain laser activation and without any additional ion-implantation. And, those structures we proposed all can effectively alleviate the maximum electric field near the drain junction.