

Figure Captions

Chapter 2

Fig. 2-1. Schematic illustration of drain engineering. Drain engineering can effectively to suppress the undesired effect, including high leakage current, kink effects, and hot carrier effects.

Fig. 2-2. Schematic illustration of the leakage current model in poly-Si TFTs.

Fig. 2-3. (a) Parasitic bipolar elements in a thin film transistor device. Hole are stored in a floating body, and injected into the source region. The bipolar action is accelerated and the resulting positive-feedback effect enhances the generation of hot carriers. (b) Schematic illustration of the related energy band diagram.

Fig. 2-4. The simulation data of the electric field vector distribution at $V_g=3V$, $V_d=10V$.

Fig. 2-5. The different drain junction structures. (a) Conventional self-aligned, (b) offset gate, (c) LDD, (d) GOLDD.

Fig. 2-6. The maximum electric field distribution of the offset gate, LDD, and GOLDD near the drain side.

Chapter 3

Fig. 3-1. Schematic diagrams of different field induced drain structures.

Fig. 3-2. Schematic diagram of the poly-Si TFT with vacuum cavity and its equivalent structure.

Fig. 3-3. The fabrication process of self-aligned field induced drain LTPS TFT.

Fig. 3-4. (a) and (b) show the simulation result of the conventional structure and FID structure with a vacuum gap, respectively.

Fig. 3-5. Simulated electric field distribution along the channel (8 μ m) direction near the drain, (a) lateral electric field, and (b) vertical electric field.

Fig. 3-6. SEM image of the T-shape gate before PECVD oxide deposition.

Fig. 3-7. SEM image of the T-shape gate with a vacuum cavity after PECVD oxide deposition.

Chapter 4

Fig. 4-1. The fabrication process of bottom-gate overlapped graded LDD LTPS TFT.

Fig. 4-2. SEM image of the side-etch of the patterned Al film under the photo-resist.

Fig. 4-3. SEM image of the poly-Si film on the patterned bottom gate and bottom gate oxide after 440 mJ/cm² XeCl ELA process.

Fig. 4-4. Schematic diagrams of the conventional bottom gate (a), the bottom gate overlapped graded LDD.

Fig. 4-5. The simulated surface electric field comparison between the conventional bottom gate and the proposed bottom-gate overlapped graded LDD.

Fig. 4-6. The transfer characteristics of LTPS TFTs with different laser shots.

Fig. 4-7. (a) Schematic graph of the proposed gate-overlapped graded LDD structure with a double gate structure, (b) The corresponding equivalent circuit of Fig.4-5 (a).

Fig. 4-8. The fabrication process of gate overlapped graded LDD LTPS TFT with a double gate structure.

Fig. 4-9. The 3-D sketch map of the double-gate structure. Contact hole of gate should be perforated through passivation layer, top-gate (Al) and two TEOS-oxide layers

(i.e., top-gate oxide and bottom oxides) to the bottom-gate (*in-situ* doped poly-Si).

Fig. 4-10. The SEM image of gate contact hole after metallization. Al (top gate) does not jut out the oxide layers and can not contact to bottom gate.

Fig. 4-11. The SEM image of gate contact hole before stripping photo-resist. A RIE process is used to etch both passivation oxide layer and Al layer and then BOE is used to etch TEOS oxide and passivation oxide without harming Al. So, naturely, Al can jut out the oxide layers.

Fig. 4-12. The electric field distribution with different structures along (a) top-surface channel, and (b) bottom-surface channel.

Fig. 4-13. The simulated I_D - V_D results with different structures.

