# Chapter 1

# Introduction

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## 1.1 An overview of Polycrystalline Silicon Thin-Film Transistors (Poly-Si TFTs) Technology

### 1.1.1 Applications to Active-Matrix (AM) Display and System-on-Pannel (SOP)

In recent years, thin-film transistors (TFTs) fabricated on polycrystalline silicon (Poly-Si) or amorphous silicon (a-Si) are commonly used in display applications, including flat panel liquid crystal displays (LCDs) [1.1], liquid crystal light valves for projectors [1.2], and organic electro-luminescent displays [1.3]. Those displays are extensively applied to mobile phones, PDAs, camcorders, PCs, notebooks, and TV.

With increasing the display area and pixel density of TFT-LCD, TFTs with high mobility are required for pixel driver of TFT-LCD in order to shorten the charging time of pixel electrodes. However, it is very difficult for the devices made on a-Si film to possess high mobility (typically below 1 $cm^2V^{-1}s^{-1}$). The problem of low carrier mobility of a-Si TFTs can be to settle by introducing poly-Si film as its active region. Poly-Si, consequently, is the most promising material for obtaining such higher mobility and higher drive current. The higher drive current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display

performance [1.4]. In addition, the capability can realize complementary metal-oxide-semiconductor (CMOS) circuits to allow low-power driver circuitry to be integrated with the active matrix on the same substrate, for reduced display-module cost and improved reliability [1.5].

Moreover, with more future developments on LTPS TFT technology, high versatile circuits and systems can be fully integrated on the display panel substrate (i.e., so-called system on panel, SOP) [1.6], [1.7].

### 1.1.2 Applications to Three-Dimensional Integrated Circuits (3D ICs)

With the increasing demand for portable systems, it is desirable to have high performance integrated circuits with high integration density, low power consumption, and low voltage operation. Traditionally, this has been achieved by device scaling. However, with the current state-of-the-art technology, the achievable integration density using a conventional approach has almost reached its saturation point. In order to provide a revolutionary breakthrough in circuit compactness, three-dimensional (3-D) VLSI technology has become an important topic in research. Poly-Si Thin-film-transistor technology is a promising means of achieving 3-D integration, which has been utilized in various 3-D circuits such as static random access memories (SRAMs), dynamic random access memories (DRAMs), and electrically erasable programmable read only memories (EEPROMs) [1.8]–[1.15]. Therefore, poly-Si TFTs have high potential to be vertically stackable components for 3-D structures.

As a result, LTPS TFTs are widely applied in the fields of active-matrix displays,

system-on-panel, and 3D ICs. Unfortunately, conventional LTPS TFTs suffer from both poor device characteristics and reliability, which limit the development in those fields. Therefore, there is great interest in improving the performance of LTPS TFTs. The goal of this work is to study the basic physics of various processes utilized in the fabrication of LTPS TFTs, and to exploit these phenomena to develop elegant means of improving the performance of LTPS TFTs.

### 1.1.3 Development in LTPS TFTs

Recently, dozens of researches have been made to develop various technologies for improving the performance and reliability of LTPS TFTs. Crystallization of a-Si thin films has been considered the most important process for fabricating high-performance LTPS TFTs. Among various crystallization technologies, excimer laser crystallization has become the mainstream technology for mass production of flat panel displays (FPDs) because of high throughput, low temperature process compatible with glass substrates, and formation of high-quality poly-Si [1.16]. However, other low-temperature process technologies in the procedure of fabricating LTPS TFTs, such as gate dielectric formation, ion doping/dopant activation, defect passivation, thin film deposition, lithography, and etching, are also indispensable for producing high-performance LTPS TFTs [1.17].

Modification of process procedure for reducing fabrication cost and enhancing TFT performance is another issue in the fabrication of LTPS TFTs on large-area glass substrates. Self-aligned processes are very attractive for advanced circuit systems on large-area glass substrates, while reducing masks and process steps can effectively promote production yield and reduce fabrication cost.

In addition, various device architectures, which are different from the conventional self-aligned source/drain structure, have also been adopted to enhance TFT performance and reliability, such as offset gate [1.18], [1.19], lightly doped drain (LDD) [1.20], [1.21], field induced drain (FID) [1.22], gate-overlapped LDD [1.23]-[1.25], and so on. Most of these structures effectively reduce the electric field near the drain junction. Consequently, the anomalous leakage current and kink current of poly-Si TFTs can be effectively reduced, accompanying with a promotion of reliability in poly-Si TFTs. In the following chapters, more detailed information about drain engineering, electrical characteristics, device architectures of LTPS TFTs is introduced to give an overall concept.

## 1.2 Motivation

As described in last session, the maximum drain electric field at the drain junction is a serious problem in LTPS TFT technology. It causes many undesired effects, such as leakage current, kink current and hot carrier effect, which degrade the characteristics and reliability in LTPS TFTs. It has been widely reported that many structures can effectively reduce the maximum drain electric field in the channel. However, those structures often require additional implantation for lightly doped drain, and/or complicated process (such as, spacer formation), and/or more process mask numbers. In this thesis, we demonstrate three improved structures with the novel process to suppress the unfavorable effects pertaining to electrical field near drain junction. And, those structures are simple to fabricate without any additional mask and implantation process.

## 1.3 Thesis Outline

In order to make LTPS TFTs suitable for advanced circuits implementing on SOP or 3-D ICs, both of the improvement of performance and reliability of the LTPS TFTs are greatly important. That is, understanding of the undesirable mechanisms and drain-relief structures become increasingly necessary. Thus, in chapter 2, in LTPS TFTs, we review the undesirable effects and analysis the maximum electric field near the drain with different structures by using the two-dimensional simulators “ISE”, “SUPPREM-4”, and “MEDICI”. In chapter 3, we exhibit the symmetric self-aligned field induce drain (FID) LTPS TFTs with selective side etch. In chapter 4, we demonstrate two novel gate overlapped graded lightly-doped-drain LTPS TFTs with the bottom-gate and double-gate Structures, respectively. Those devices we proposed are also discussed by material analysis and simulation results. At last, in chapter 5, we draw the conclusions of these researches.