Chapter 2

Drain Engineering in Low-Temperature Polycrystalline Silicon Thin-Film Transistors

2.1 Introduction

Drain engineering is an important topic in single-crystalline Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs), especially when the device dimension is scaling down. All the unwelcome effect, such as short channel effect, hot carrier effect, and so on, will appear. However, drain engineering is also imperative to poly-Si TFTs, not only in small dimension device. Concerning the electrical characteristics, most of the undesired effects, including *leakage current*, *kink-effect*, and *hot-carrier effect*, are related to the presence of high electric fields at the drain junction, mainly determined by the abruptness of the lateral doping profile in the drain. The schematic graph is shown in Fig. 2-1. Those effects degrade the performance and reliability of the poly-Si TFTs seriously and limit the applications to the AM-display, SOP, and 3-D ICs. That is, conventional self-aligned poly-Si TFTs structures should be modified in the drain region to reduce the maximum electric field in the channel.

In the following session, those undesired effects will be reviewed in detail, and poly-Si TFTs with drain-relief structures will be discussed by two-dimensional simulators.
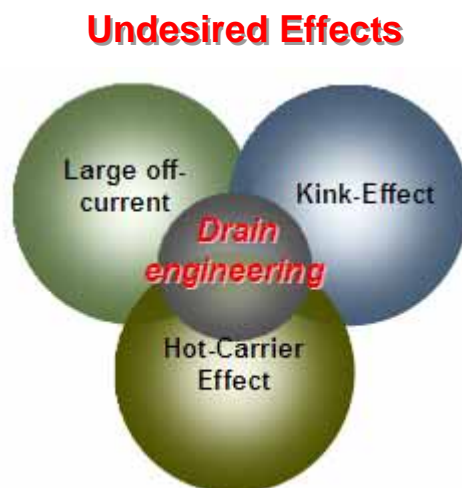
Undesired Effects

Fig. 2-1. Schematic illustration of drain engineering. Drain engineering can effectively to suppress the undesired effect, including high leakage current, kink effects, and hot carrier effects.

2.1.1 Leakage Current

The leakage current of a poly-Si TFT is generally higher than that of an a-Si TFT. In order to apply the poly-Si TFTs into active matrix circuit, the anomalous leakage current must be reduced. This is because the pixel should maintain the charge when the line is not selected, i.e., the TFTs are at off-state. The reduction of the leakage current is also important for SRAM application of poly-Si TFTs in terms of the low power consumption during the waiting time.

The leakage current is explained to be field emission via grain boundary traps in the drain depletion region, as shown in Fig. 2-2 [2.1]-[2.4]. Grain boundary between grains creates trap energy level inside the energy gap of the crystalline Si, and generate leakage current when it is reverse biased and depleted, i.e., at off-state. The leakage current, thus, strongly depends on the local electric field in the drain depletion region and the amount of

trap states. That is, there are two means to reduce the leakage current, the one is reducing the defect traps, such as by hydrogenation; the other is reducing the electric field near the drain junction by improved poly-Si TFTs structures with drain relief structures. The trap states can be decreased by hydrogenation [2.5]. However, the hydrogenation method does not completely remove the states. Besides, the hydrogenation process also creates a large amount of weak Si-H bonds in poly-Si. These weak bonds can easily be broken during device operation, which will result in the variation of device characteristics [2.6], [2.7]. On the other hand, decrease in the electric field in the drain depletion region is very effective in suppressing the high leakage current.
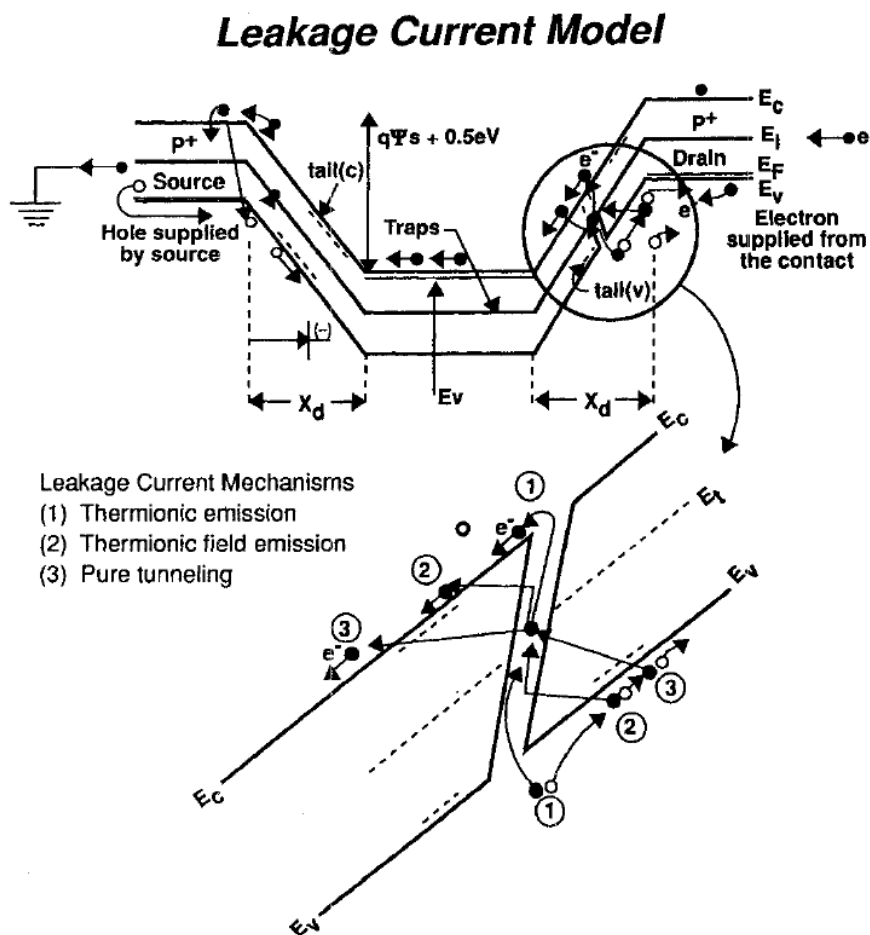

Fig. 2-2.   Schematic illustration of the leakage current model in poly-Si TFTs. [2.2]

2.1.2 Kink effect

Kink effect is the saturation current increase due to generation of electron-hole pairs induced by the high electric field at the channel/drain contact region [2.8]. The high electric field accelerates electrons and raises their kinetic energy until impact ionization occurs. It can even raise parasitic bipolar action (PBA) [2.9]. The impact ionization generated holes are injected into the floating body (base) forcing further electron injection from the source (emitter) and collected by the drain (collector), as shown in Fig. 2-3. This added drain current enhances the impact ionization and causes a premature breakdown. That is so-called channel avalanche multiplication occurred in the high-field near the drain combined with the floating body effect, which is similar to the kink effect of SOI MOSFET's. Furthermore, for poly-Si TFTs, there is an additional mechanism related to the high trap state density that enhances the effect of avalanche multiplication [2.8]. Kink effect increases the current, which increases the output conductance, and hence, power dissipation in digital circuits. It also reduces gain in analogue circuit.
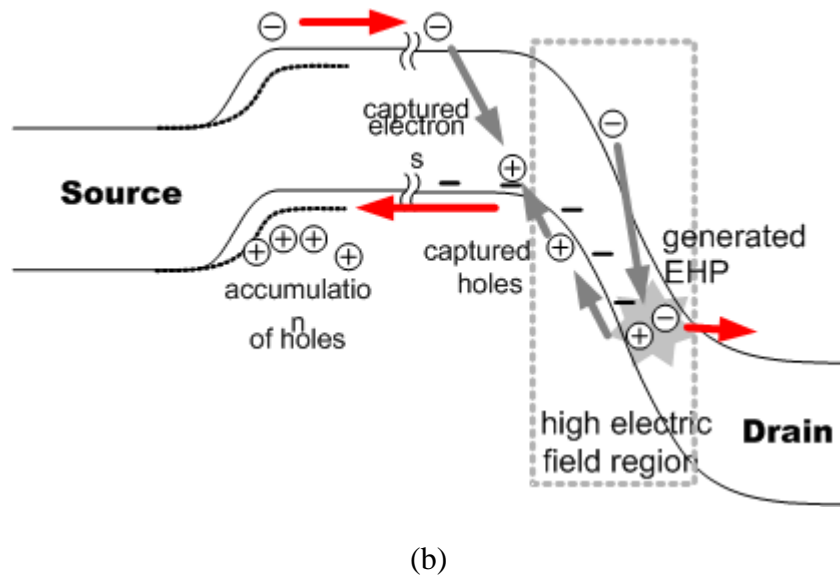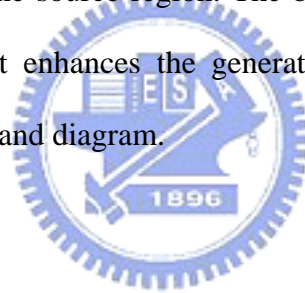

(a)

(b)
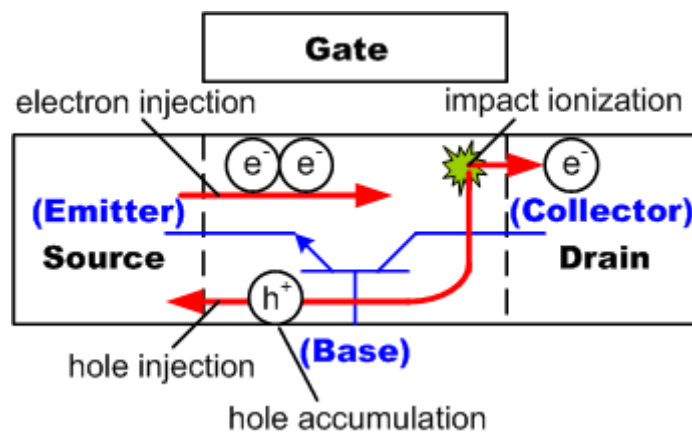
Fig. 2-3. (a) Parasitic bipolar elements in a thin film transistor device. Hole are stored in a floating body, and injected into the source region. The bipolar action is accelerated and the resulting positive-feedback effect enhances the generation of hot carriers. (b) Schematic illustration of the related energy band diagram.

2.1.3 Hot-carrier effect

As shown in Fig. 2-4, the simulation distribution data of the electric field vector at Vg=3V, Vd=10V. It can be found that the maximum electric field in the channel is near the drain side. Conduction carriers can obtain energy from the high electric field and become "hot". And then these impact ionization generated hot carriers can easily break weak bond in poly-Si and the interface between gate oxide and poly-Si, creating lots of defect states and injecting into the gate oxide. This phenomenon produces the device degradation, and the degree of degradation depends on the strength of electric field. The predominant mechanism for device degradation induced by the hot carrier injection is formation of interface states

near the drain [2.10]. The formation of the interface traps is related to sequential trapping of holes followed by electron captures. Prolonged drain bias stress degrades the transfer characteristics. The electrical instability is a serious issue for long-term reliability of the circuit.

That is, there are two methods to suppress the hot-carrier effect, the one is strengthening the gate oxide and Si-SiO$_2$ interface against hot-carrier damage. The other is to reduce the maximum electric field near the drain side. However, the gate insulator of poly-Si TFTs often growth by low temperature deposition for implementing on the glass substrate, so the strong gate oxide and interface, such as thermal oxide, is difficult to be obtained. Consequently, the most effective method is still to reduce the maximum electric field.
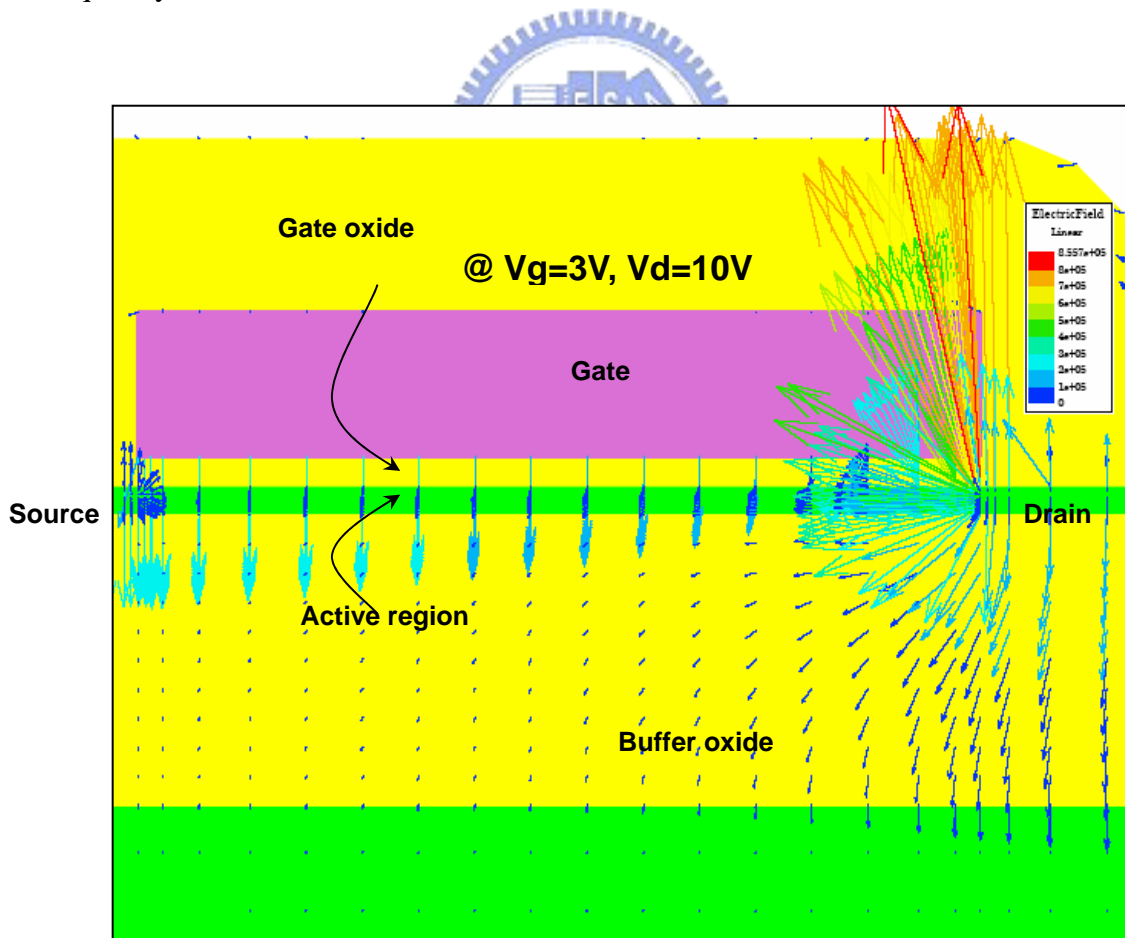

Fig. 2-4 The simulation data of the electric field vector distribution at Vg=3V, Vd=10V.

2.2 Device architectures for drain-relief

It has been necessary to develop techniques to combat those undesired effects. Since these effects are induced the presence of the intense electric field at channel/drain region, many structures engineered at the drain electric field have been reported, such as offset gate, lightly doped drain (LDD), gate-overlapped (GO) LDD, shown in Fig. 2-4 (b), (c), and (d), respectively. They are discussed in this section in detail.
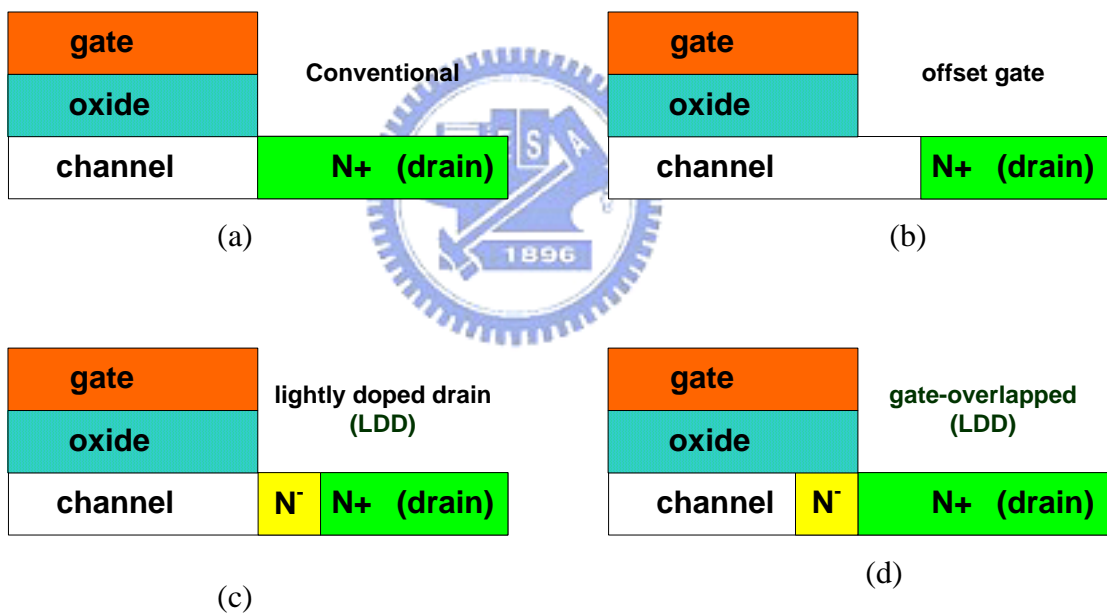

Fig. 2-5.   The different drain junction structures.

2.2.1 Offset gate

The drain electric field can be reduced if the distance between the two edges of the channel and the drain increases, as shown in Fig. 2-5 (b). It has been reported that, with an offset length of 5 um, the leakage current could be reduced by about one decade in magnitude compare to that of conventional TFT structure. However, the on-current was also reduced by the same order due to the high parasitic resistance, i.e., current pinching phenomenon. This results in almost the same value of the on/off current ratio. The ratio can be improved by shortening the offset length; however, this would lead to a severe alignment requirement. An additional lithography step is required to define the offset region. This raises two major drawbacks. One is the increased process complexity, and the other is the variation in the channel length due to the difficulty in precise control of the offset length.

2.2.2 Lightly doped drain (LDD)
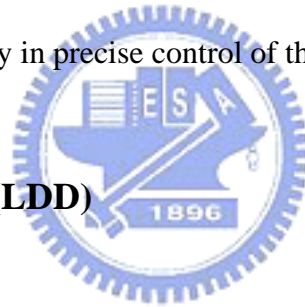
The current pinching phenomenon in the offset gate structure can be improved by employing an n$^-$ region between the channel and drain, i.e., lightly doping the offset region as shown in Fig. 2-5 (c). The LDD region can be formed by, for example, an additional implantation or ion-doping of impurity atoms with a low dosage. Since the parasitic resistance effect is inversely proportional to the LDD doping concentration while the drain field decreases for decreasing the the LDD doping concentration, the choice of the LDD doping concentration is determined on the actual application requirement of the TFT. the LDD doping concentration with a concentration of about 1×10^{14}cm^{-2}, the TFT's on/off current ratio is improved by one order of magnitude compared with that of the conventional offset-gated TFTs. The LDD structure also lowers the lateral field in the saturation regime, and consequently, decreases the impact ionization rate.

2.2.3 Gate overlapped LDD (GO-LDD)

In this GO-LDD structure, the gate overlaps with the LDD region, as shown in 2-5 (d). The gate modulates the conductance of the LDD region; it lowers the conductance only when the gate is positively biased. Owing to the gate modulation of the LDD region, the series resistance problems of LDD are substantially suppressed.

2.3   The electric field comparison of different structures by the 2-D simulators

As the undesirable effects, anomalous leakage current, kink effect, and hot-carrier effect, are related to the lateral electric field in the channel. In order to study the electric field effects of the various LTPS TFT structures, the two-dimensional (2D) numerical device simulator "MEDICI" was utilized. For the sake of simplicity, the single crystalline silicon model available in MEDICI was employed to estimate the electric field. In particular, the conventional drift-diffusion model, generation-recombination (SRH) model, and the parameters reflecting the nature of LTPS material were used.

The schematic cross-sections of devices used in the simulations are shown in the Fig. 2-5 (a)-(d). The device drain junction structures used in the simulations include fully self-aligned source/drain, offset gate, lightly doped drain (LDD), gate overlapped LDD, and the source and drain junction structures are symmetrical in all cases.

As shown the electric field simulation results in Fig. 2-5, the offset gate, LDD, and

GOLDD all can reduce the maximum electric field in the channel. Among them, the offset gate can reduce it most effectively. However, it decays a great deal of on current, as above session description. LDD structure and GOLDD structure have almost the same maximum electric field, while GOLDD structure can has more on current than LDD structure due to its LDD region is fully overlapped by gate. That is to say, GOLDD structure is most effective method to reduce drain electric field while maintaining the on current.
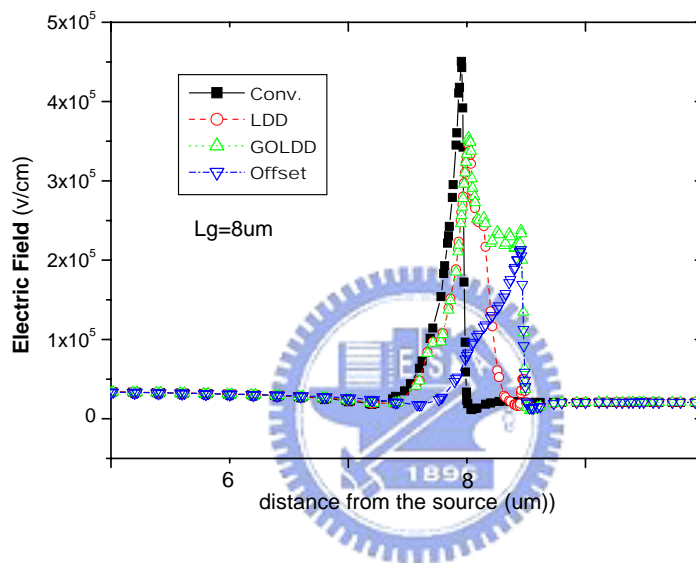

Fig. 2-6 The maximum electric field distribution of the offset gate, LDD, and GOLDD near the drain side.