

Chapter 3

A Novel Low Temperature Self-Aligned Field Induced Drain Polycrystalline Silicon Thin Film Transistor by Using Selective Side-Etching Process

3.1 Introduction

Low-temperature poly-Si (LTPS) TFTs have attractive advantages over amorphous Si (a-Si) counterparts in portable applications; such as high resolution, low turn-on voltage and low power consumption [3.1]. LTPS TFTs with CMOS process are widely used for system-on-panel (SOP) display, where all the electronic components related to the display can be integrated inside the panel. It is the future trend to produce SOP displays and active-matrix organic lightemitting diodes (AMOLEDs) by using LTPS processes.

However, the realization of a SOP display requires the high-performance and high-reliability poly-Si TFTs to fabricate on the large glass substrate. Many techniques have been proposed to improve the electrical characteristics of poly-Si TFTs, such as enlarging the channel grains by laser-induced lateral crystallization, and improved structures with reducing the electric field near the drain. In this work, the improved structures are focused to study.

It is widely known that the high electric field induced near the drain causes a large leakage current, saturation current and device instability. Poly-Si TFTs with an offset gate, a

lightly doped drain (LDD) structure have been suggested to reduce the electric field near the drain, as described in session 2-3. As the offset region between gate and source/drain suppresses the drain electric field, the offset gated poly-Si TFT has a low OFF-state leakage current. However, the ON-state current lowering by the high series resistance of the offset region is a serious problem. In order to reduce the parasitic series resistance of the offset gated TFT, an additional LDD implantation is employed [3.2], [3.3]. Although a poly-Si TFT with LDD has better turn-on characteristics than an offset-gated TFT, device degradation due to additional n⁻ implant damage and difficulty in doping control at the grain boundaries are important issues. And, it is difficult to fully active the implant damage under the low temperature (<600 °C).

A poly-Si TFT with a field-induced-drain (FID) structure shows a low OFF-state leakage current, while maintaining good turn-on characteristics. And, a FID poly-Si TFT can suppress both the vertical and lateral electric fields near the drain effectively. It is distinct from a LDD poly-Si TFT that only can reduce the lateral electric field. Several FID structures have been reported by different processes. The transcriptions of those device architectures are shown in Fig.3-1 [3.4]-[3-8]. Those will be discussed in next session. However, those are often required more complicated process flow and more photo lithographic steps which may raise the mis-alignment problem. The polarity between source and drain in poly-Si TFT for AMLCD display application must be altered to reduce the DC stress of liquid crystal so that symmetric characteristic characteristics are required in AMLCD pixel [3-9]. In this chapter, a self-aligned FID Poly-Si TFT is proposed by using the selective side etch process.

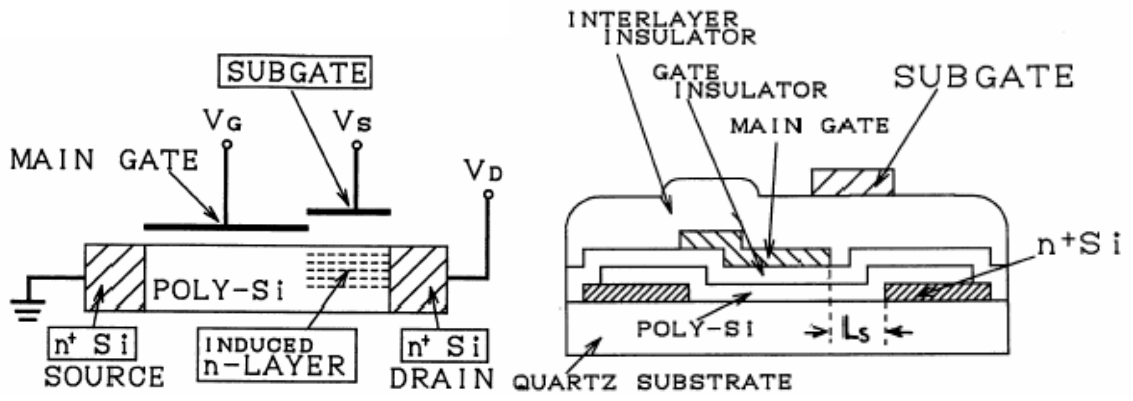
Recently, Low-k materials, such as vacuum and air, have been used to reduce capacitance and propagation delays within the interconnect layers of a device more effectively than mainstream silicon dioxide insulators and attracted considerable attention in

VLSI technology [3.10], [3.11]. However, there is scarce report in using low-k materials to reduce the electric field near the drain. In this chapter, a simple method to fabricate a FID poly-Si TFT with a vacuum cavity near the drain is proposed. Using this new structure, both the vertical and lateral maximum electric fields are simultaneously decreased.

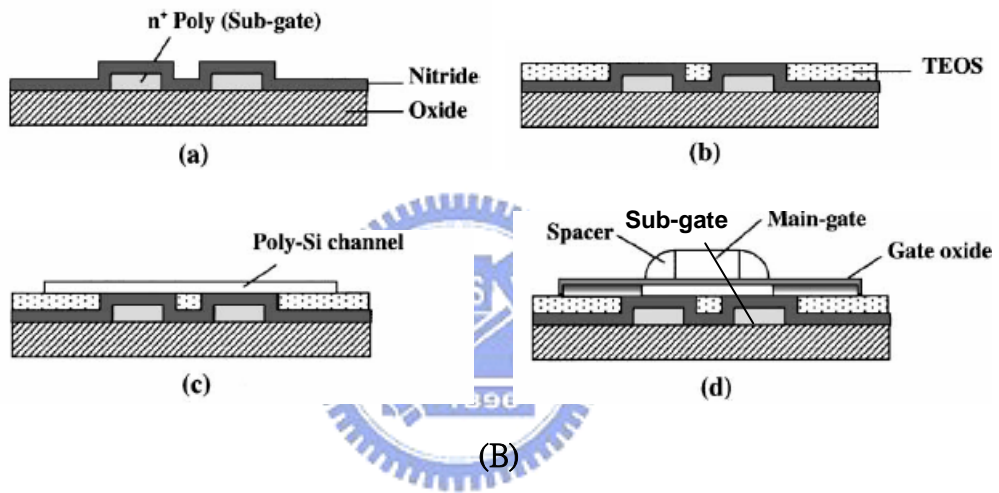
3.2 Field-Induced-Drain Structures

3.2.1 An overview of the field-induced-drain poly-Si TFTs

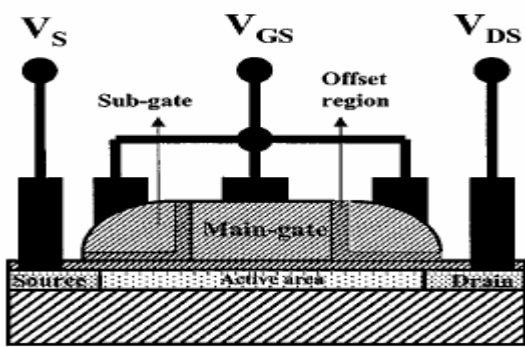
The key feature of the Field-Induced-Drain (FID) is addition of the metal field plate (sub-gate) covering the entire offset region to the offset gate structure. The FID structures can be divided into two forms. The one form is that the sub-gate has additional bias electrode, as shown in Fig. 3-1 (A) and (B) [3.4]-[3.5]. When a positive voltage is applied to the sub-gate, an n^+ -inversion layer will be formed at the offset region. This will lower the problematic high parasitic resistance in the offset structure. When the TFT is at the off-state, the applied field-plate voltage also equally distributes the drain field on both ends of the offset regions, thereby minimizing the peak electric field. However, drawbacks of the FID include the increased complexity in manufacturing and the additional supply of a high voltage to the sub-gate, which requires a complicated biasing scheme, and it is difficult to be integrated into the pixel circuit.



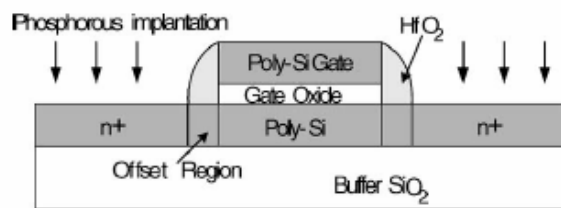
(A)



(B)



(C)



(D)

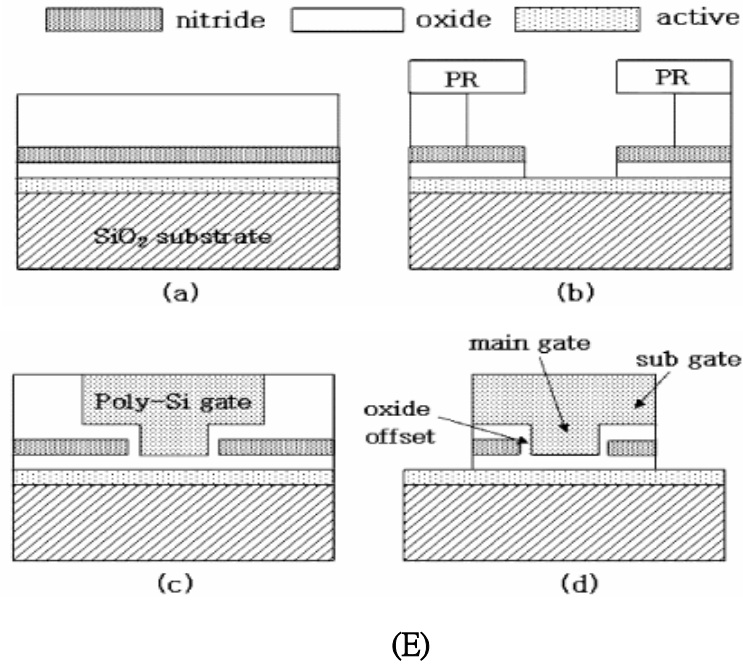


Fig.3-1 Schematic diagrams of different field induced drain structures. [3.4]-[3.8]

The other FID form is that the sub-gate is applied to the same electrode with the main gate, as shown in Fig.3-1 (C), and (D) [3.6]-[3.8]. The feature of this structure all has a thick insulator below the sub-gate. Due to the thicker insulator than main gate insulator, the maximum electric field near the drain can be reduced effectively. And, it also has larger on current than offset gate structure because it has a gate electrode overlapped above the offset region. And this structure does not require additional electrode and can applied into circuit easily. However, those structures often require complicated process, such as spacer process [3.6], [3.7] and damascene process [3.8]. In this work, we propose a novel FID structure with simple selective side-etch method.

3.2.2 The proposed field-induced-drain structure

The schematic diagram of the proposed FID TFT is shown in Fig.3-2 (a). Vacuum

cavities reduce the vertical electric field near the drain due to the low dielectric constant of vacuum ($\epsilon = 1$). And, the dielectric constant of oxide material is 3.9. That is, the vacuum material serves like an about 4-time-thick oxide film, as shown the schematic diagram in Fig.3-2 (b). The poly-Si region under vacuum cavity can be considered as an offset region and the gate edge (Mo) over the vacuum cavity serves as a field plate (sub-gate) connected with the main gate (Al).

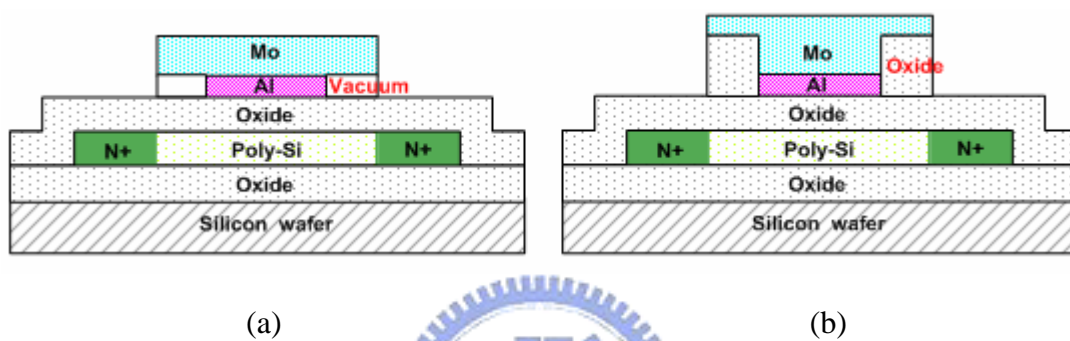
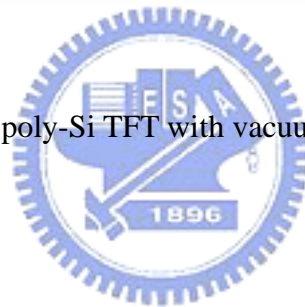


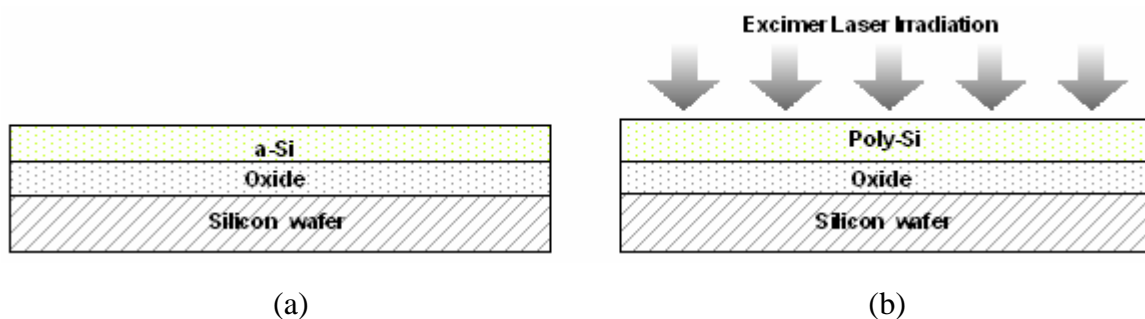
Fig.3-2 Schematic diagram of the poly-Si TFT with vacuum cavity and its equivalent structure.



3.3 Experimental Procedure

The proposed FID TFTs were fabricated by the following sequence of processes, and the key processes are illustrated in Fig.3-3. First, A 500Å- a-Si thin film was deposited on oxidized silicon wafer by decomposition of SiH_4 with LPCVD at 550°C, shown in Fig.3-3 (a). Then, the a-Si thin film was crystallized into polycrystalline type by XeCl excimer laser annealing with 440 mJ/cm^2 and without substrate heating, shown in Fig.3-3 (b). After defining the active layer, a 1000Å-thick TEOS gate oxide was deposited by low-pressure chemical vapor deposition (LPCVD) at 600°C. 1000Å-thick Al and 2000Å-thick Mo films were

deposited at room temperature by sputter system, respectively. Then, the stacked Mo/Al films were simultaneously etched by reactive ion etch (RIE) to form gate electrodes, shown in Fig.3-3 (c). A self-aligned phosphorous implantation with dose of $5 \times 10^{15} \text{ cm}^{-2}$ and 70keV was carried out to form source and drain regions, shown in Fig.3-3 (d), and then KrF excimer laser irradiation with 280 mJ/cm^2 was employed at room temperature to activate dopants. Mo material can reflect the laser light, so only source/drain regions absorb the laser energy and activate dopants, shown in Fig.3-3 (e). H_3PO_4 solution is well selective etching between Al and Mo materials, so the side-etch of Al films without harming Mo films was performed easily, shown in Fig.3-3 (f). That is, the side-end of Mo layer is the field-plate (sub-gate) and Al layer is the main gate for the field-induced drain structure. Next, a 3000Å-thick SiH_4/O_2 oxide was deposited at 400 mtorr by PECVD as passivation layer, and the vacuum cavities were *in-situ* formed near the source/drain, shown in Fig.3-3 (g). Contact opening formation and metallization were carried out, shown in Fig.3-3 (h). For comparison, conventional self-aligned (SA) LTPS TFTs without Al-side-etch structure were also fabricated.



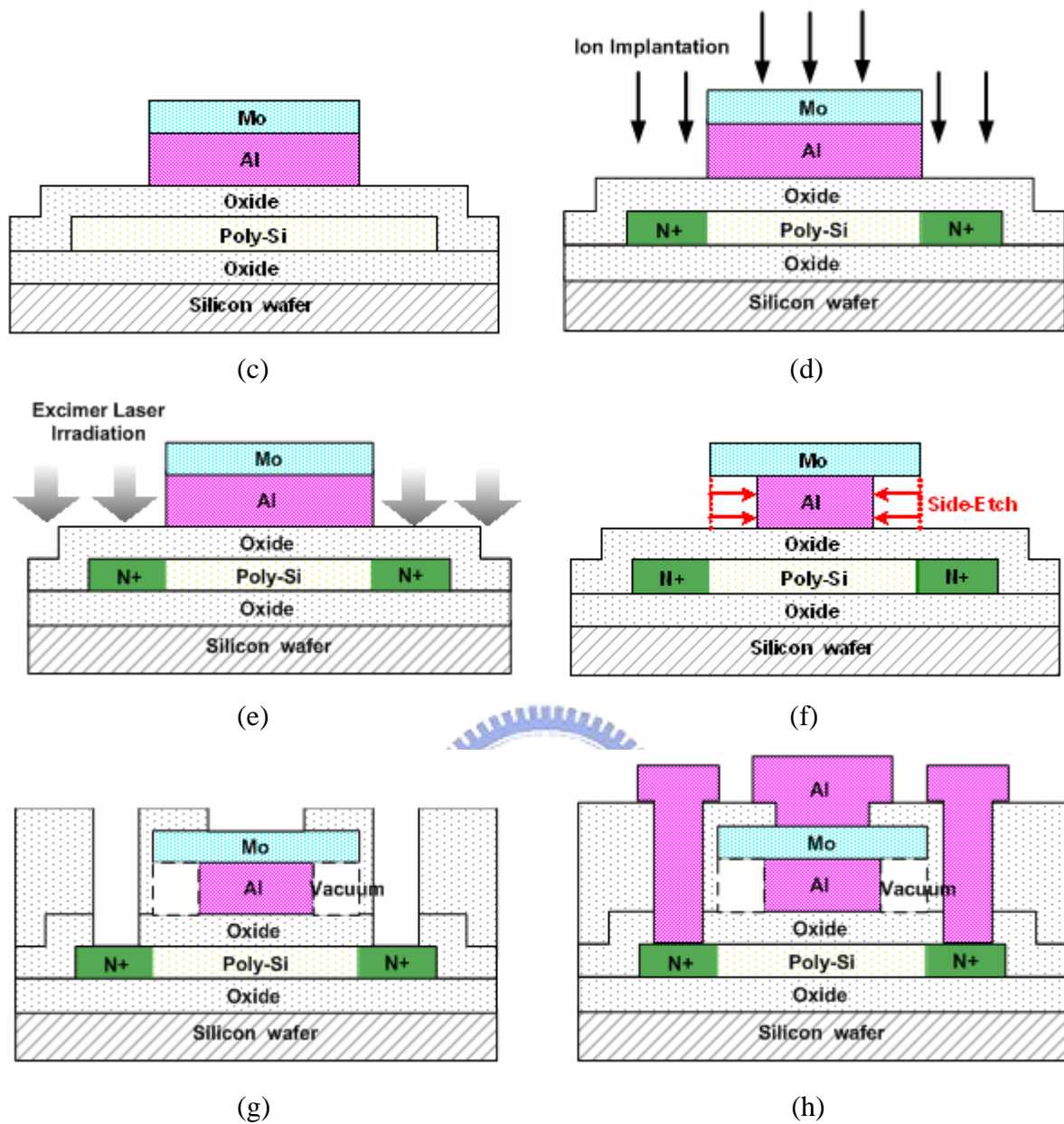


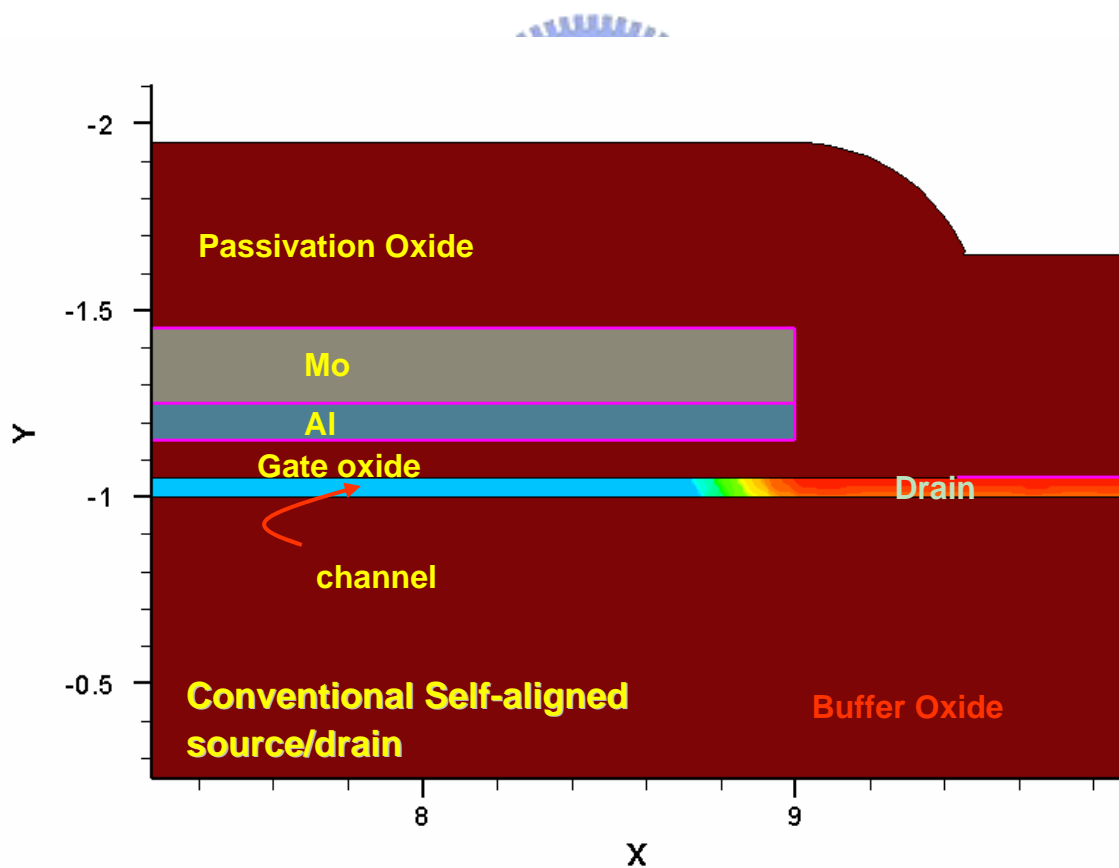
Fig. 3-3 The fabrication process flow of self-aligned field induced drain LTPS TFT.

3.4 Electrical Simulations

As the undesirable effects, anomalous leakage current, kink effect, and hot-carrier effect, are related to the maximum electric field in the channel. In order to study the electric field

effects, the two-dimensional (2D) numerical device simulator “Integrated Systems Engineering (ISE)” was utilized [3-12]. For the sake of simplicity, the single crystalline silicon model available in ISE was employed to estimate the electric field. In particular, the conventional drift-diffusion model, generation-recombination (SRH) model, and the parameters reflecting the nature of LTPS material were used.

Fig.3-4 (a) and (b) show the simulation (Ligament process simulator of ISE) results of the conventional structure and FID structure with a vacuum gap, respectively. The process steps and materials are the same as the fabricated one.



(a)

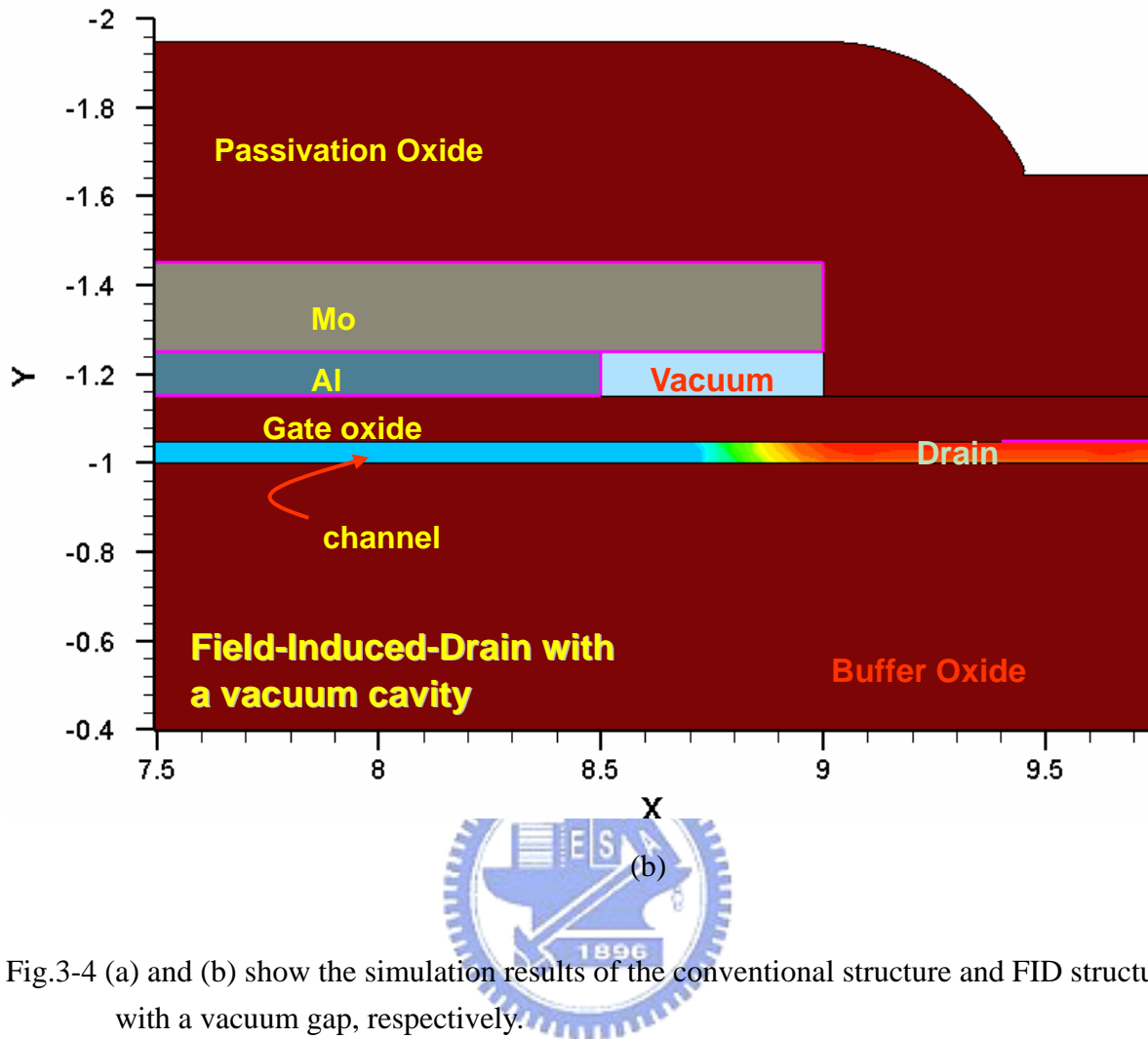
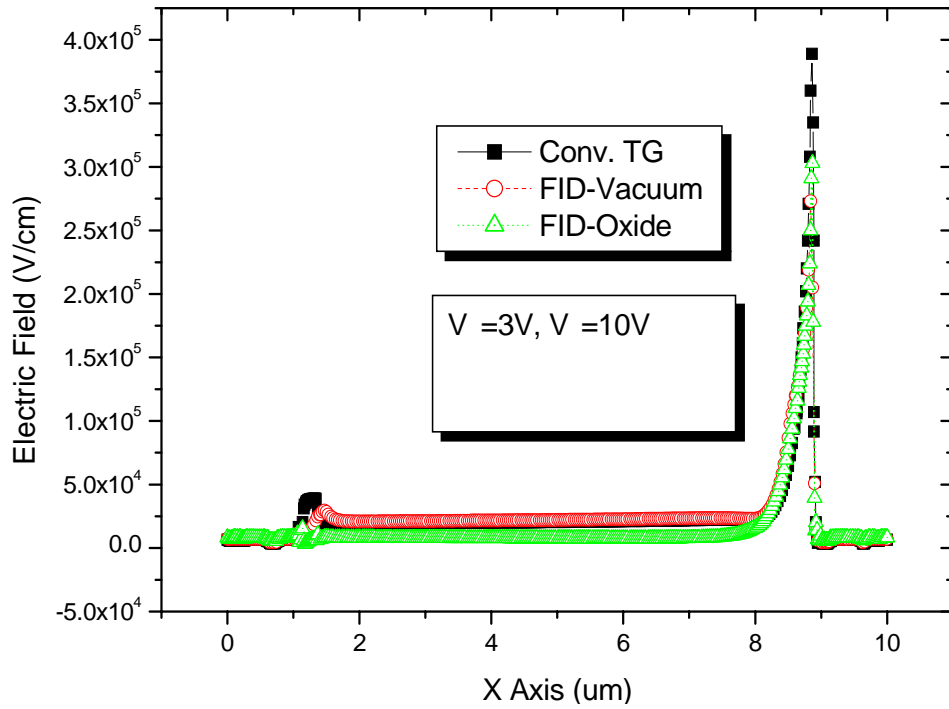
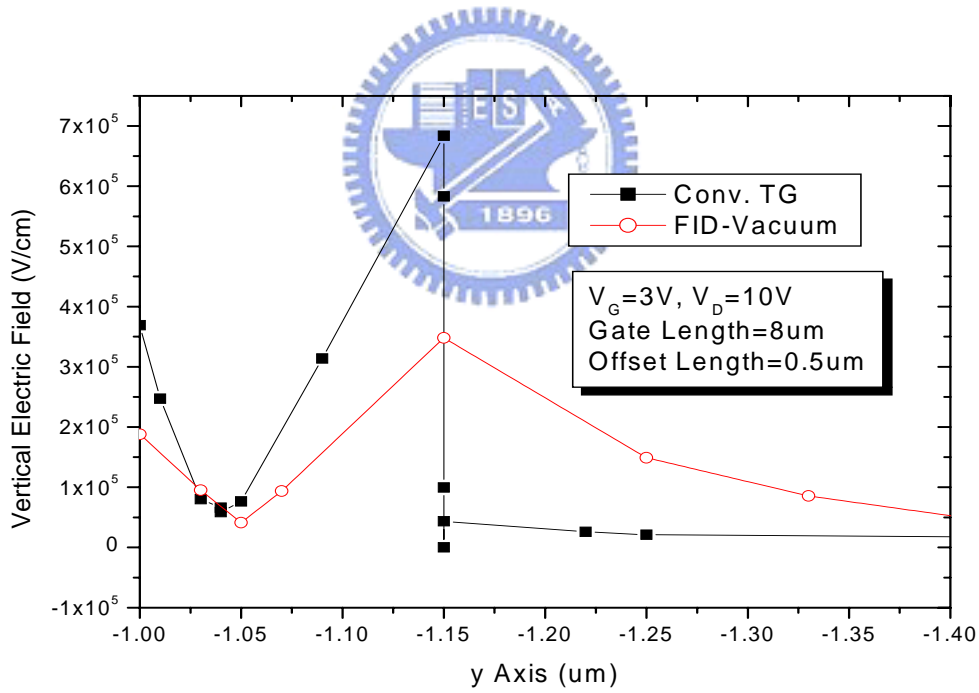


Fig.3-4 (a) and (b) show the simulation results of the conventional structure and FID structure with a vacuum gap, respectively.

Due to the vacuum gap, the best low k material, beside the drain, the maximum may be reduced. In order to verify the effect of the vacuum cavity on the vertical and lateral electric field near the drain, the electric field in the TFT is simulated by “MDraw” and “Dessis” simulators followed by Ligament simulator. Fig. 3-5 shows the electric field distribution along the channel/ gate oxide interface for $V_{GS} = 3$ V, and $V_{DS} = 10$ V. At the active layer surface under the vacuum gap, the lateral electric field and the vertical electric field, as shown in Fig. 3-5 (a) and Fig. 3-5 (b), respectively, are reduce considerably compared with conventional structure without vacuum gap.



(a)



(b)

Fig.3-5 Simulated electric field distribution along the channel (8um) direction near the drain, (a) lateral electric field, and (b) vertical electric field.

3.5 Result and Discussion

Al side etching can be formed after the H_3PO_4 solution treatment 20 sec at $45^\circ C$ and observed by SEM. Fig.3-6. shows an image of the T-shape gate structure before Plasma Enhanced Chemical Vapor Deposition (PECVD) passivation oxide deposition. That is, with a simple wet-etching and without any complicated process, a FID structure with a T-shape gate can be formed.

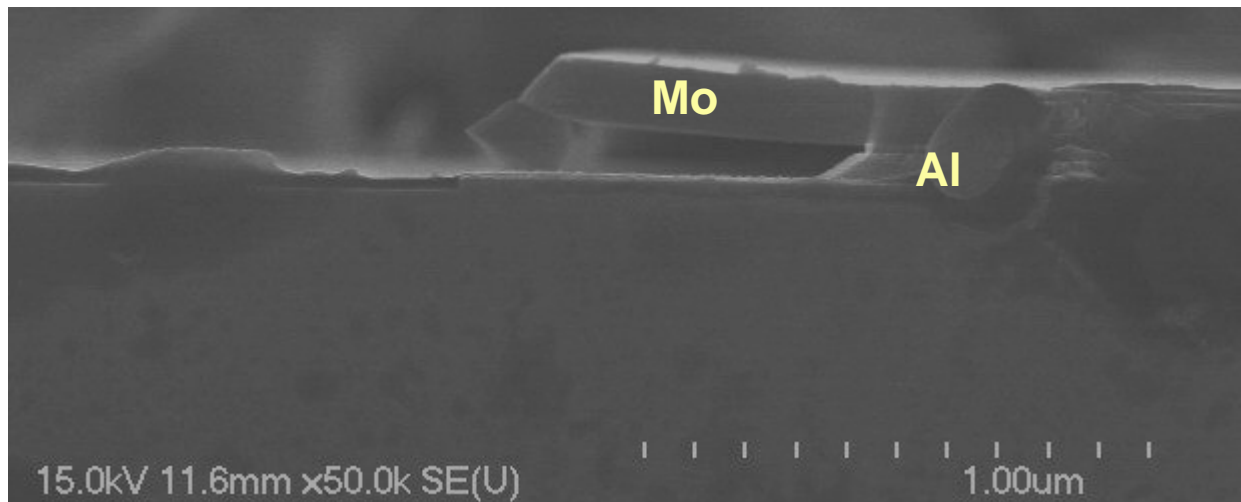


Fig.3-6. SEM image of the T-shape gate before PECVD oxide deposition.

A vacuum cavity can be formed after the SiH_4/N_2O (5sccm/90sccm) PECVD deposition 3000 \AA under substrate temperature $350^\circ C$, chamber pressure 400 mtorr. Fig.3-7. shows the SEM image of the T-shape gate after PECVD deposition. Due to the source of PECVD is SiH_4/N_2O , the mean free path of SiH_4 precursor is so short that it can not diffuse into the cavity. The side-etching region of Al film cannot be filled during PECVD deposition, that is, the *in-situ* vacuum cavities can be formed.

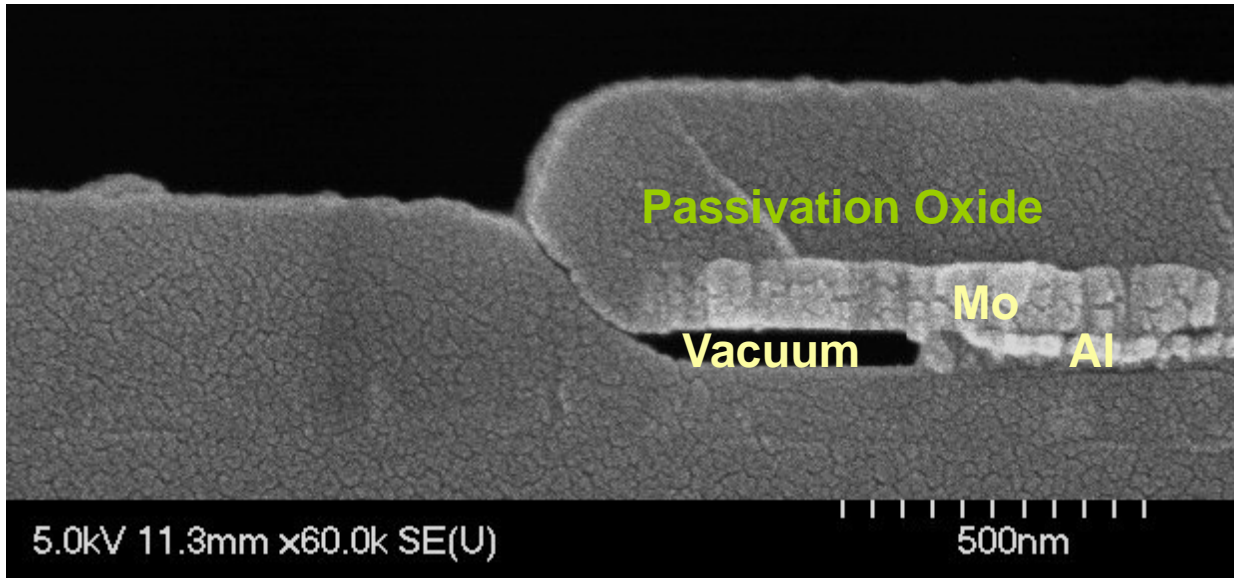
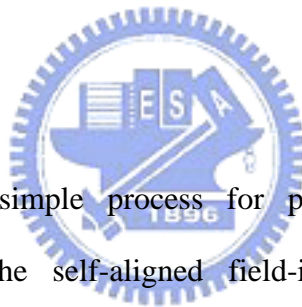


Fig.3-7. SEM image of the T-shape gate with a vacuum cavity after PECVD oxide deposition.

3.6 Summary



We have developed a simple process for poly-Si TFTs with a self-aligned field-induced-drain structure. The self-aligned field-induced-drain structure has been achieved without any additional lithograph step. The total masks of our fabrication process are four masks which are equal to those of conventional process in top gate poly-Si TFT. The process is based on the excellently selective wet etching between Mo and Al materials. From the simulation data, the proposed FID structure can effectively reduce both the vertical and lateral electric field compared with the conventional structure. It should be noted that, as the maximum drain electric field is reduced, the leakage current, kink effect, and hot carrier effect can effectively suppressed as the previous chapter described.