Chapter 4

Two Novel Low Temperature Gate Overlapped Graded Lightly-Doped-Drain Polycrystalline Silicon Thin Film Transistors with the Bottom-Gate Structure and Double-Gate Structure

4.1 Introduction

In recent, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) become attractive due to their applications in active-matrix displays, such as LCDs and OLEDs. Active matrix displays with integrated circuits on a single panel substrate can be implemented by high-performance LTPS TFTs. The requirements for high-performance devices are high current-driving capacity and low leakage-current characteristics.

In the previous chapters, we have introduced that to reduce the drain electric field is an important issue to reduce those undesired effects in low-temperature poly-Si TFTs. The objective of fabricating the modified device structure is to eschew lightly doped drain (LDD) structure, which requires additional lithography, process for spacer [4-1][4-2], or ion implantation to form a junction containing two different concentrations. Furthermore, the general LDD structure has a drawback of increasing the series resistance that lowers the

driving capability of devices. In order to use LDD structure without an additional ion implantation and lithography, we devised a new method to achieve the purpose by accompanying with excimer laser irradiation. The concept of the method is to build up source/drain offset spaces beside the gate electrode, and then use excimer laser irradiation to activate and diffuse dopants at the same time. Finally, graded doping concentration between gate and source/drain will be formed naturally. The graded doping profile will have similar effect with the LDD structure. Besides, the process is not only uncomplicated but also has the capability of alleviating the lateral electric field near the drain junction without increasing series resistance seriously.

As description in session 2.3, we have a summary that gate-overlapped LDD device is more suitable to possess high on/off current ratio because LDD can lead to low leakage current and gate-overlapped structure can maintain the on current. It is imperative for devices aiming at AMLCD/AMOLED drivers and matrices over a glass substrate. So, in this chapter, we demonstrate two gate-overlapped LDD structures with a bottom gate structure and a double gate structure, respectively. And, those LDD is graded distribution and formed by using excimer laser irradiation to activate and diffuse dopants.

4.2 Gate Overlapped Graded Lightly-Doped-Drain Polycrystalline Silicon Thin Film Transistor with a Bottom-Gate Structure

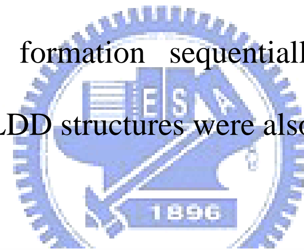
The bottom-gate structure can also be used for poly-Si TFTs, and offers some advantages over the top-gate structure for AMLCD applications. For example, good interface

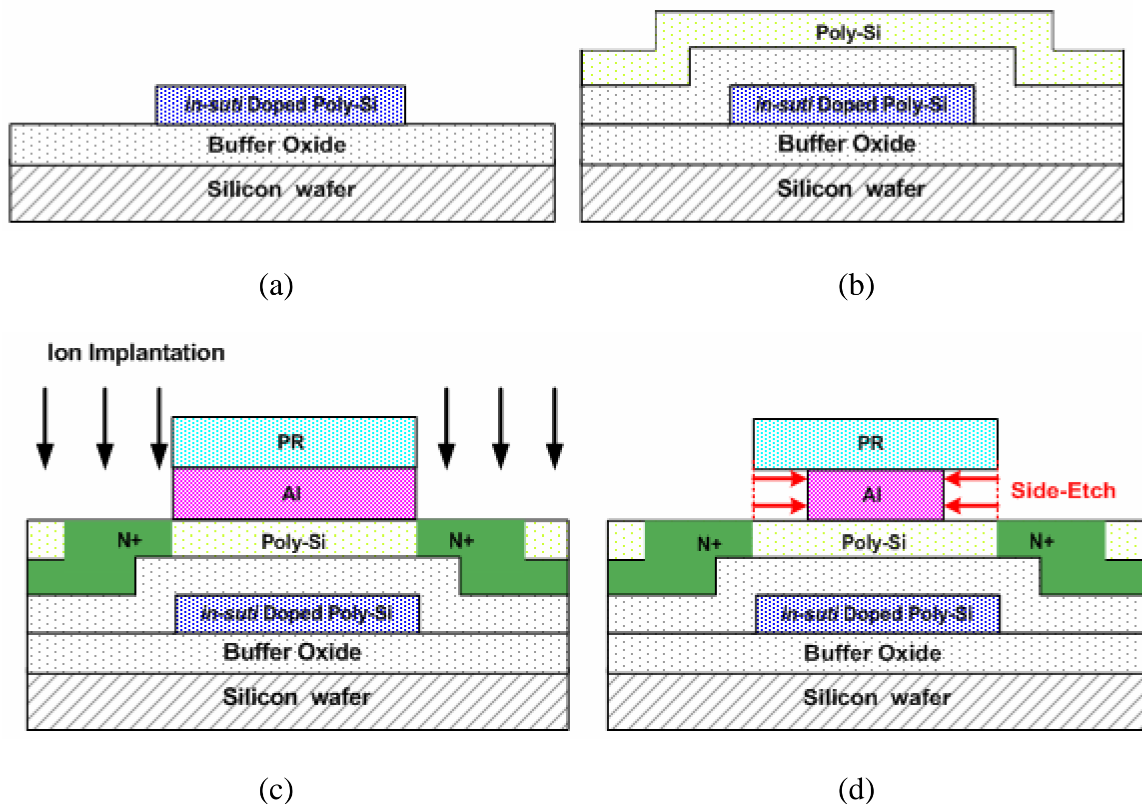
control can be achieved due to the ability to deposit the gate dielectric and precursor silicon sequentially in a single system without exposing to atmosphere ambient. For instance, the plasma hydrogenation rate for the bottom-gate TFT structure is significantly higher than for top-gate TFT structure, because the channel thin film is not blocked by the gate-dielectric and gate-electrode thin films during hydrogenation process. In this session, we propose a novel gate-overlapped graded LDD poly-Si TFT with a bottom gate structure.

4.2.1 Experimental Details

Fig.4.1 shows the process flows of fabricating a double-gate gate-overlapped graded LDD poly-Si TFT (BG-GO-GLDD) have laterally graded doping concentration at source/drain junctions. Firstly, a 1000Å *in-suti* doped poly-Si film was deposited on the oxided wafer by low-pressure chemical vaper deposition (LPCVD) at 550°C. After defining the bottom-gate pattern, as shown in Fig.4.1 (a), 1000Å bottom-gate oxide and 500Å a-Si films are deposited sequentially on the patterned doped poly-Si bottom gate by LPCVD using TEOS source at 600°C and SiH_4 source at 550°C, respectively, and subsequently transformed a-Si into polycrystalline phase by a solid-phase recrystallization (SPC) treatment at 600°C for 24 hours, as shown in Fig.4.1 (b). The crystallization of this work is SPC instead of excimer laser annealing (ELA), it is because a-Si film on the patterned bottom gate and TEOS oxide layer will be shrinked during the ELA crystallization. The total thickness of patterned bottom gate and TEOS oxide layer is 2000 Å, however, the a-Si film is only 500Å. Especially, the a-Si on the corner region has larger stress than somewhere else. So, as ELA process performing, a-Si is melting in a blink and solidifying into poly-Si type, and the larger stress region at the corner become not continuous, as shown in Fig.4.3. After SPC recrystallization,

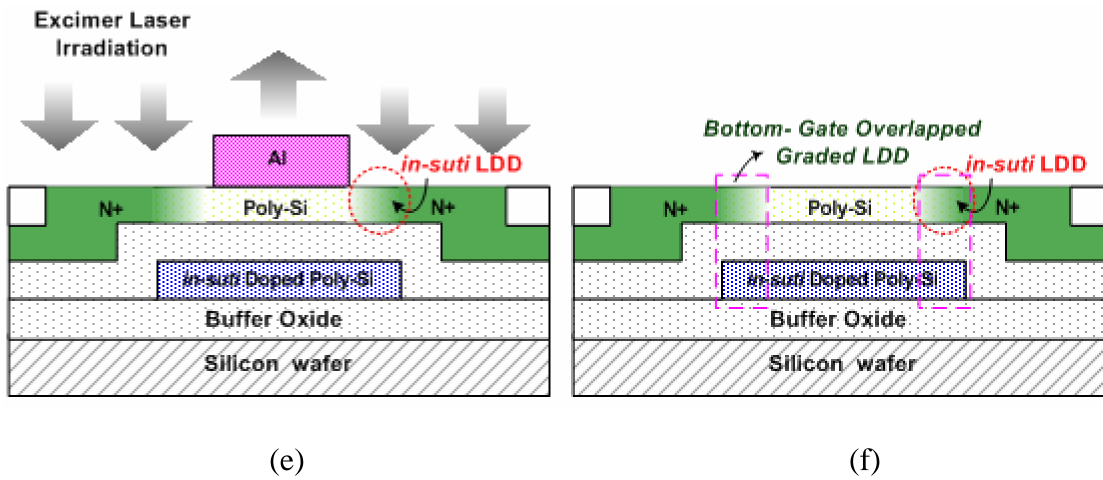
the SPC poly-Si film was tailored into the active island. Next, 3000Å Al films was deposited using sputter system, respectively. Then, the Al film was patterned to form dummy-gate for ion implantation. It is noted the formation of dummy-gate and bottom-gate electrodes were patterned by the same mask. Without removing the photo-resist above the dummy-gate, a phosphorous implantation with doe of 5E15 cm^{-2}, 70 kev was carried to form source and drain regions, shown in Fig.4-1(c). Then, the side-etch of dummy-gate was performed under the photo-resist, as shown in Fig.4-1(d) and Fig.4.2. After removing photo-resist, the excimer laser irradiation with different energy density and different shot numbers was performed at room temperature to activate dopants and diffuse dopants laterally, as shown in Fig.4-1(e). Then, the dummy patterned Al film was removed by H_3PO_4, as shown in Fig.4-1(f). Next, a 3000Å-thick PECVD oxide was deposited as passivation layer, following contact opening formation and metallization is formation sequentially. For comparison, conventional bottom-gate LTPS TFTs without LDD structures were also fabricated.





(a) (b)

(c) (d)



(e) (f)

Fig.4.1 The fabrication process of bottom-gate overlapped graded LDD LTPS TFT.

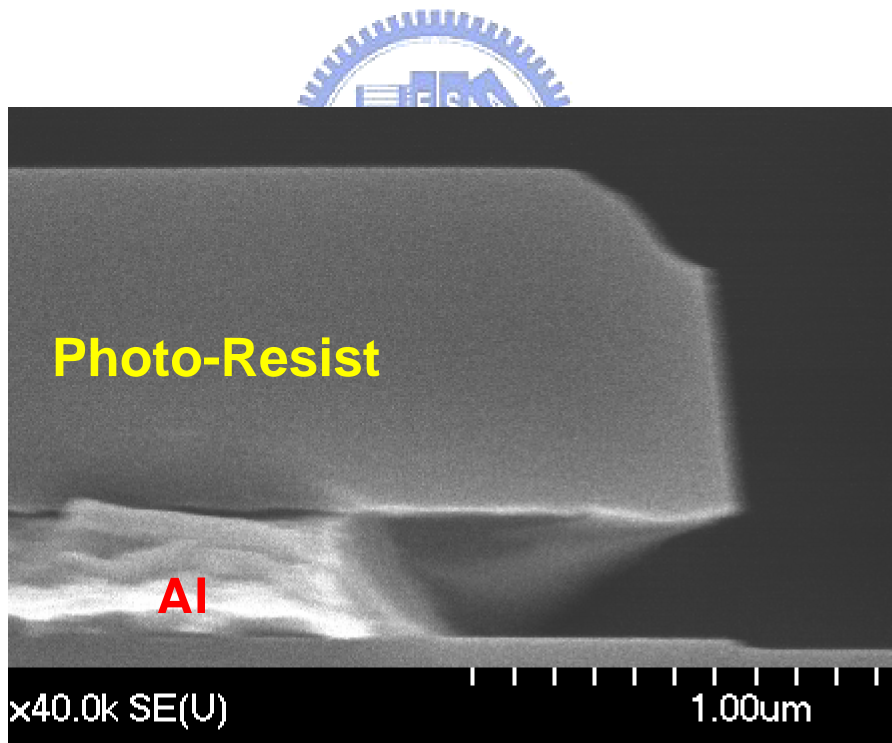
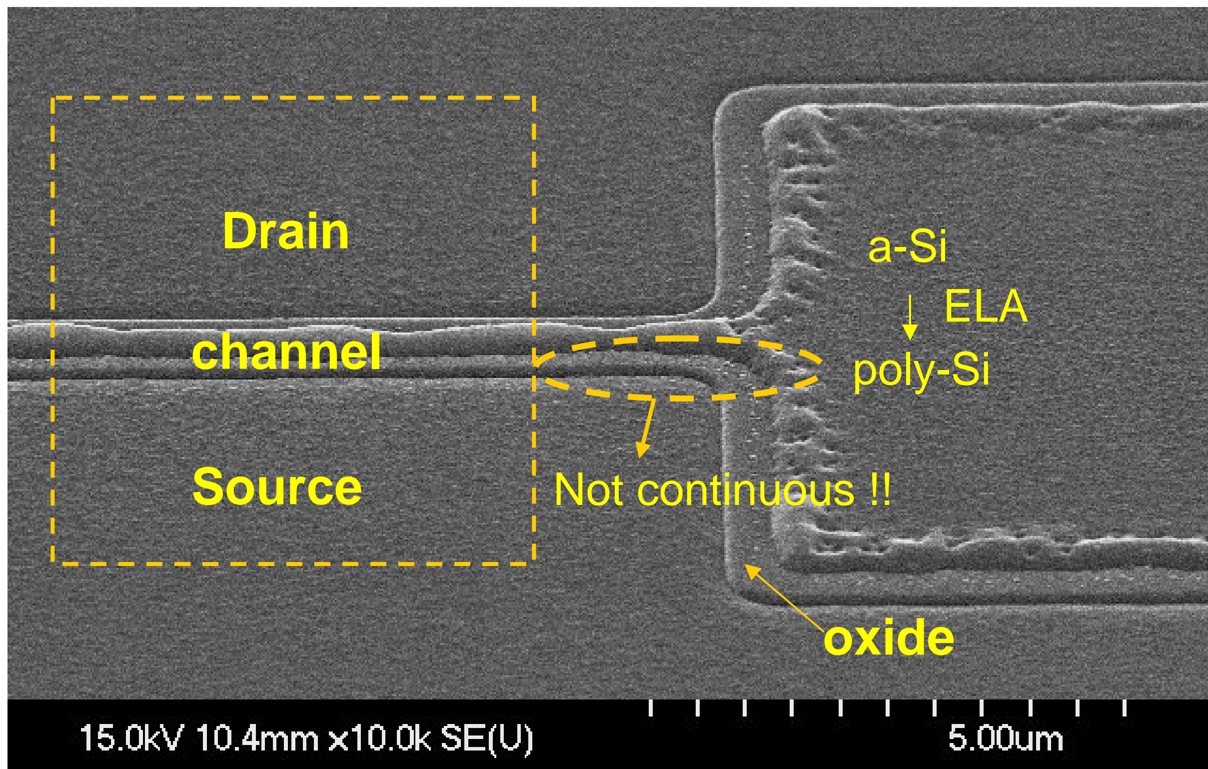


Fig.4.2 SEM image of the side-etch of the patterned Al film under the photo-resist.



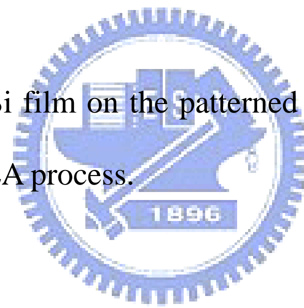
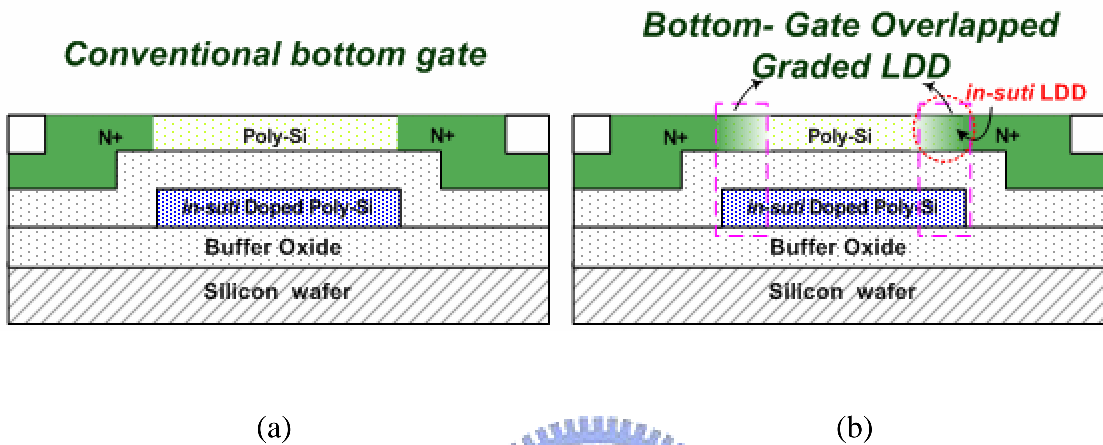


Fig.4.3 SEM image of the poly-Si film on the patterned bottom gate and bottom gate oxide after 440 mJ/cm^2 XeCl ELA process.

4.2.2 Simulation results

As the undesired effects, anomalous leakage current, kink effect, and hot-carrier effect, are related to the maximum electric field in the channel. In order to study the electric field effects, the two-dimensional (2D) numerical device simulator "Integrated Systems Engineering (ISE)" was utilized. For the sake of simplicity, the single crystalline silicon model available in ISE was employed to estimate the electric field. In particular, the conventional drift-diffusion model, generation-recombination (SRH) model, and the parameters reflecting the nature of LTPS material were used.

The schematic cross-sections of devices used in the simulations are shown in the Fig. 4-4(a)-(b). The device drain junction structures used in the simulations include fully self-aligned source/drain, offset gate, lightly doped drain (LDD), gate overlapped LDD, and the source and drain junction structures are symmetrical in all cases.



(a) (b)

Fig.4.4 Schematic diagrams of the conventional bottom gate (a), the bottom gate overlapped graded LDD

Fig. 4-5 shows the electric field distribution along the channel/ gate oxide interface for V_{GS} = 3 V, and V_{DS} = 10 V. It can be found clearly that the bottom gate overlapped graded LDD can effectively reduce the maximum electric field near the drain.

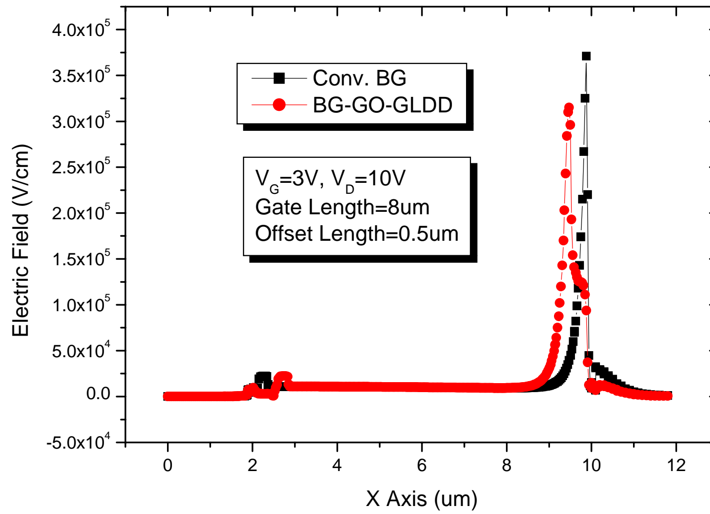
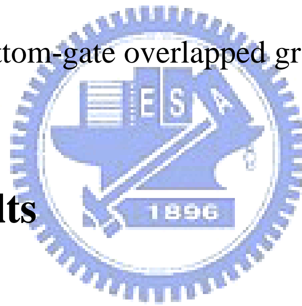


Fig. 4-5 The simulated surface electric field comparison between the conventional bottom gate and the proposed bottom-gate overlapped graded LDD.



4.2.3 Experimental results

Fig. 4-6 shows the transfer characteristics of LTPS TFTs with different laser shots. It is shown that the leakage current of LTPS TFTs with graded LDD structure could be suppressed effectively. It is attributed to the drain field relief and low series resistance. The leakage current of LTPS TFTs could also be further reduced by increasing the graded LDD length with increasing the laser shot numbers. This is because the degree of drain field relief increases with stretching the graded LDD length. The on current could raise a little with increasing laser shot numbers, it is because the effective length is shorter as the length of dopnats diffusion is longer as well as more laser shot is performed.

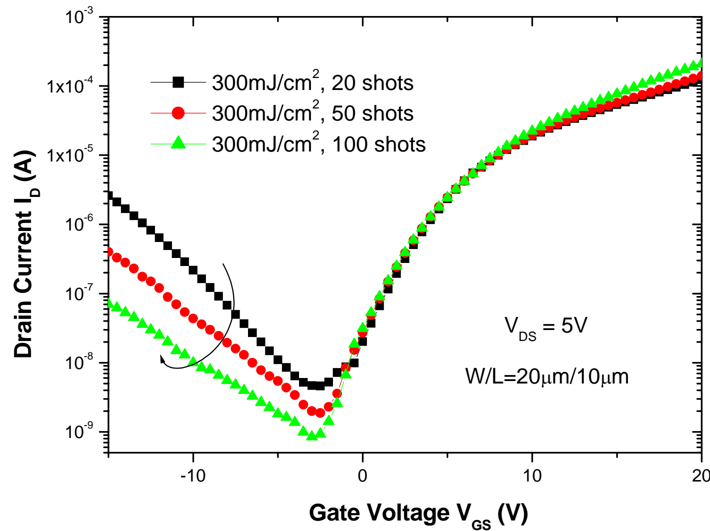
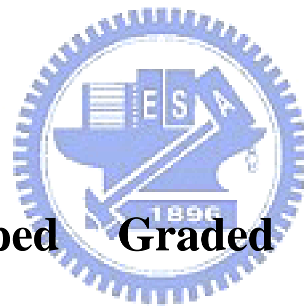


Fig. 4-6 The transfer characteristics of LTPS TFTs with different laser shots.

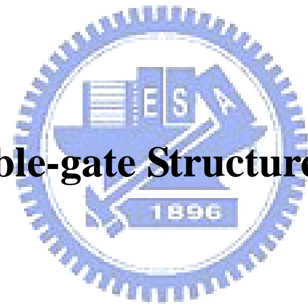


4.3 Gate Overlapped Graded Lightly-Doped-Drain Polycrystalline Silicon Thin Film Transistor with a Double-Gate Structure

Low temperature poly-Si TFT appears to be one of the most promising technologies for the ultimate goal of building large area microelectronic systems on glass [4.1],[4.2]. With more future developments, this technology will enable high functionality small or medium size display systems to be integrated on the panel substrate. The major components of the enabling technology should include an efficient pixel device, a high current driver device, a high current digital device, a kink-free analog device, a large storage capacitor, and an

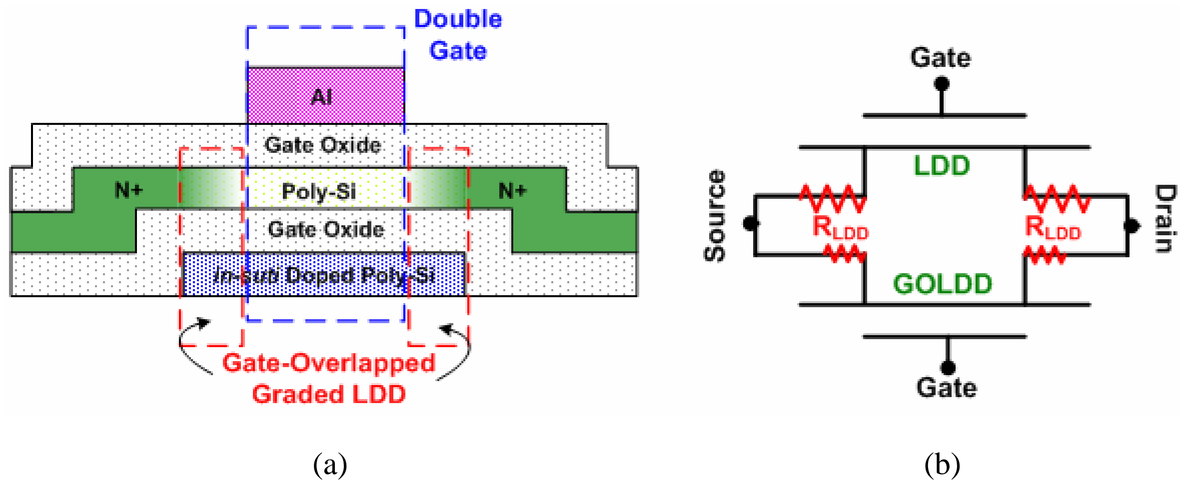
efficient memory device. Currently, researchers in this area are managed to put a few of these components together using a particular poly-Si TFT technology.

Poly-Si thin-film transistor (poly-Si TFT) technology is the most promising candidate for building a fully integrated flat panel display (FPD) system on glass (SOG). However, the performance of conventional poly-Si TFT is far from satisfactory to meet the speed and current drive requirements for the SOG application [4.3]. It has been demonstrated that double-gate structure is capable to provide a significant improvement in current drive, a reduced susceptibility to short channel effect and a steeper subthreshold slope [4.4]-[4.7]. However, the kink effect under the DG mode operation is more noticeable. It is due to the higher drain electrical field under the DG operation [4.8].



4.3.1 The proposed double-gate Structure

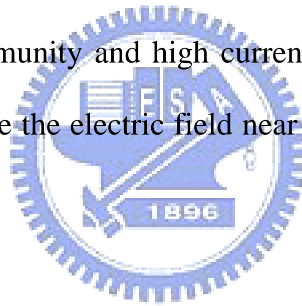
The schematic diagram of the proposed double-gate gate-overlapped graded LDD TFT is shown in Fig.4-7. It is a sandwich structure that two gates (i.e., Al top gate and *in-suti* doped-poly-Si bottom gate) wrap the two gate oxide layers (i.e., top-gate oxide and bottom-gate oxide) and the active poly-Si layer, as shown in Fig.4-6(a). And, the top gate-length is shorter than the bottom one just for the graded-LDD formation. Thus, the double-gate structure is composed of the top transistor with a graded-LDD structure and the bottom counterpart with a gate-overlapped graded-LDD structure. The corresponding equivalent circuit is shown in Fig.4-6(b).



(a) (b)

Fig.4-7 (a) Schematic graph of the proposed gate-overlapped graded LDD structure with a double gate structure, (b) The corresponding equivalent circuit of Fig.4-5 (a).

Thus, the proposed structure not only can provide fundamental advantage such as excellent short-channel effect immunity and high current drivability due to the double gate coupling [4.9], but also can reduce the electric field near the drain junction due to the *in-suti* graded-LDD.

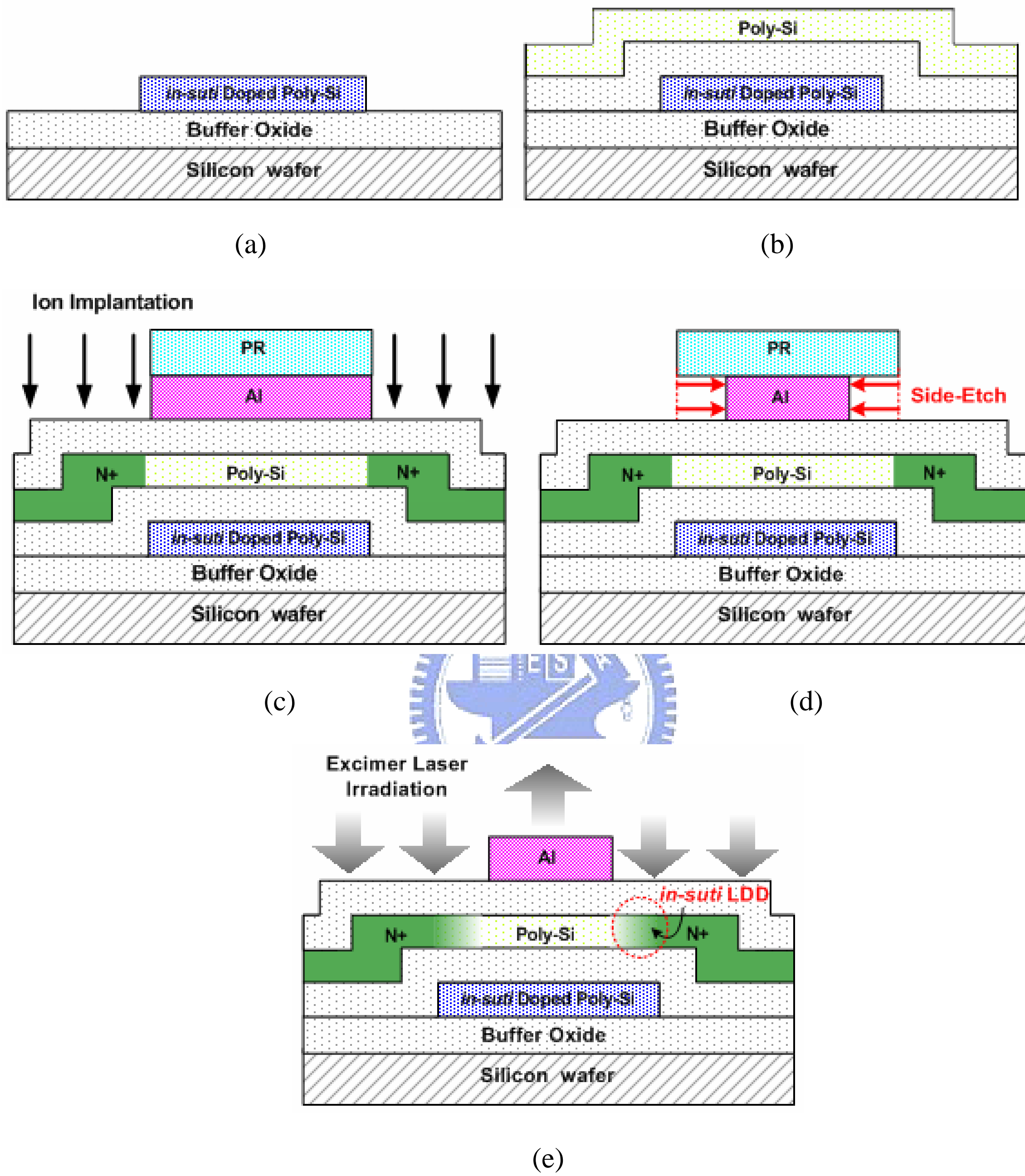


4.3.2 Experimental Details

Fig.4-8 shows the process flows of fabricating a double-gate gate-overlapped graded LDD poly-Si TFT (DG-GO-graded LDD) have laterally graded doping concentration at source/drain junctions. Firstly, a 1000Å *in-situ* doped poly-Si film was deposited on the oxided wafer by low-pressure chemical vaper deposition (LPCVD) at 550°C. After defining the bottom-gate pattern, 1000Å bottom-gate oxide and 500Å a-Si films are deposited sequentially on the patterned doped poly-Si bottom gate by LPCVD using TEOS source at

600°C and SiH_4 source at 550°C, respectively, and subsequently transformed a-Si into polycrystalline phase by a solid-phase recrystallization (SPC) treatment at 600°C for 24 hours. After recrystallization, the SPC poly-Si film was tailored into the active island. Next, 1000Å TEOS top-gate oxide and 3000Å Al films were deposited using LPCVD and sputter system, respectively. Then, the Al film was etched to form top-gate electrode. It is noted the formation of top-gate and bottom-gate electrodes were by the same mask. Without removing the photo-resist above the gate electrodes, a self-aligned phosphorous implantation with dose of 5E15 cm^{-2}, 70 kev was carried to form source and drain regions. Then, the side-etch of gate-electrodes was performed under the photo-resist, as shown in Fig.4-8 (d). Different lengths of side-etch were used in this experiment to form different LDD lengths. After removing photo-resist, the excimer laser irradiation with different energy density and different shot numbers was performed at room temperature to activate dopants and diffuse dopants laterally. Next, a 3000Å-thick PECVD oxide was deposited as passivation layer, following contact opening formation and metallization is formation sequentially. For comparison, conventional double gate and bottom gate LTPS TFTs without LDD structures were also fabricated.

It should be noted that the top gate and bottom gate were patterned by the same mask, so the contact hole of gate should be perforated through passivation layer, top-gate (Al) and two TEOS-oxide layers (i.e., top-gate oxide and bottom-gate oxides) to the bottom-gate (*in-situ* doped poly-Si), as shown in Fig.4-9. We did this step carefully to ensure that top gate can contact to bottom gate. And, the Al (top gate) should jut out the oxide layers to let the following metallization can contact to it, Fig.4-10 shows that Al does not jut out and can not contact to bottom gate after metallization. A RIE process is used to etch both passivation oxide layer and Al layer and then BOE is used to etch TEOS oxide and passivation oxide without harming Al. So, naturely, Al can jut out the oxide layers, shown in Fig.4-11.



(e)

Fig.4-8 The fabrication process of gate overlapped graded LDD LTPS TFT with a double gate structure.

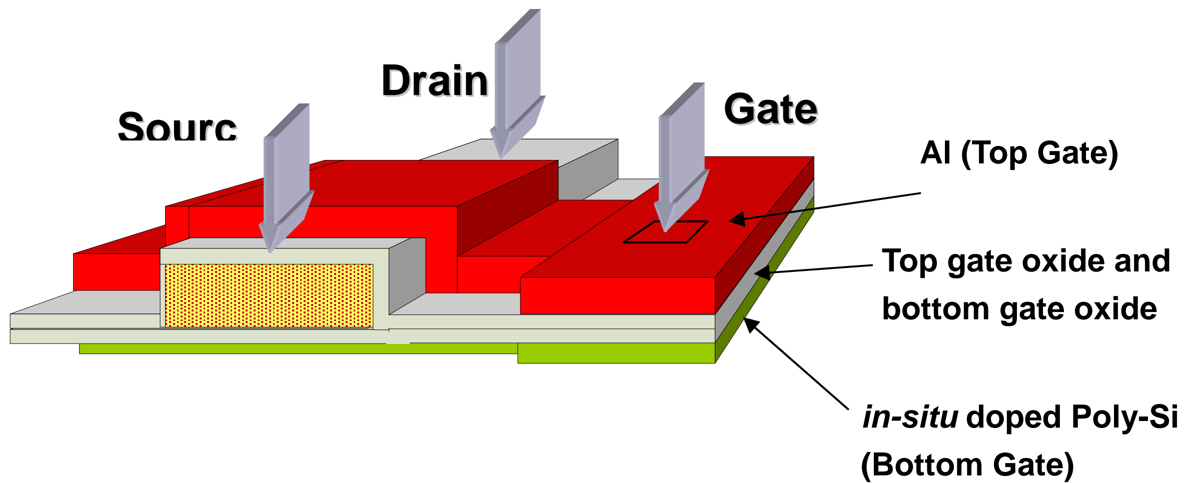


Fig.4-9 The 3-D sketch map of the double-gate structure. Contact hole of gate should be perforated through passivation layer, top-gate (Al) and two TEOS-oxide layers (i.e., top-gate oxide and bottom oxides) to the bottom-gate (*in-situ* doped poly-Si).

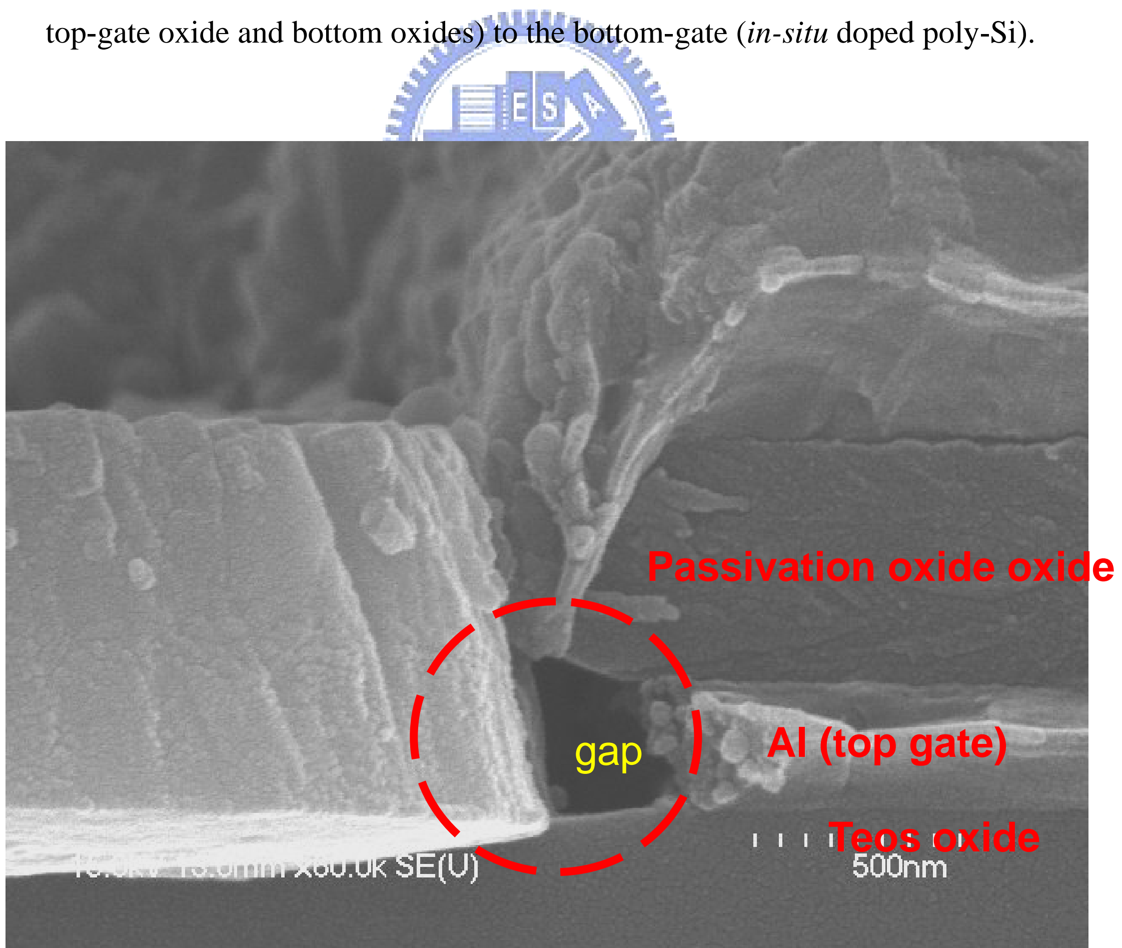


Fig.4-10 The SEM image of gate contact hole after metallization. Al (top gate) does not jut out the oxide layers and can not contact to bottom gate.

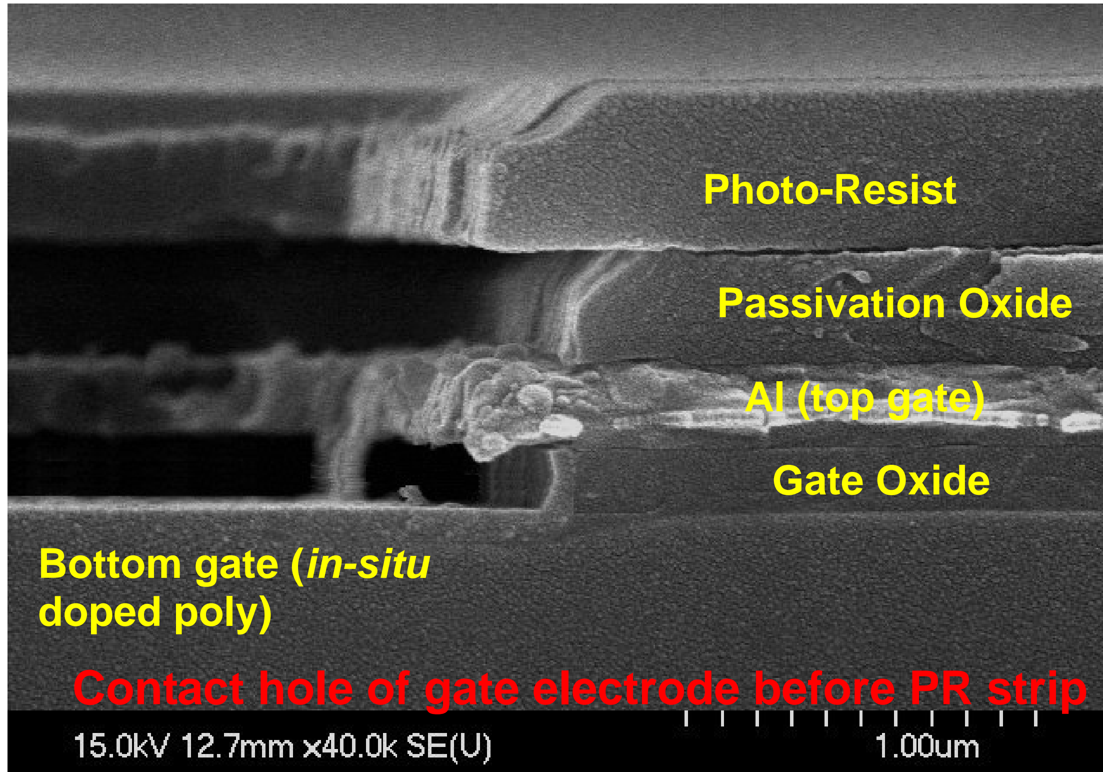
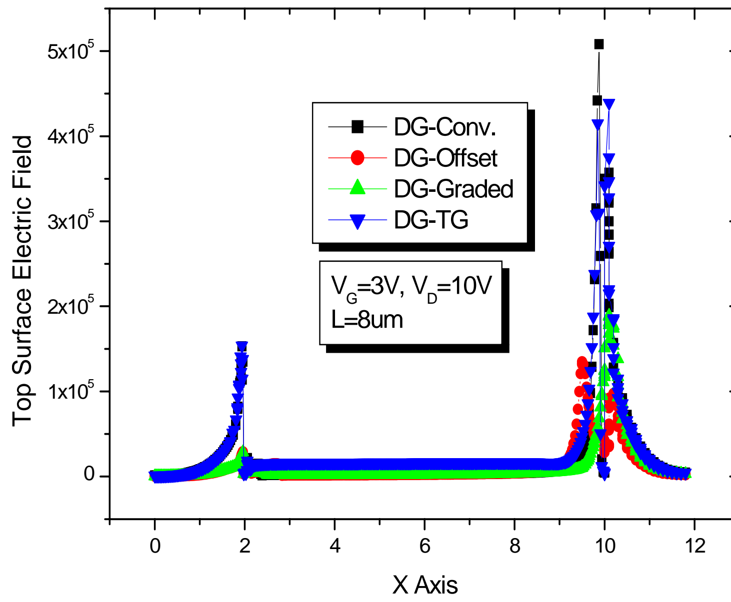


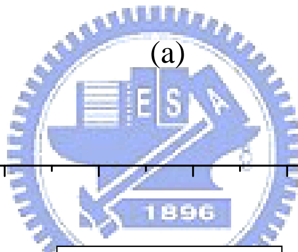
Fig.4-11 The SEM image of gate contact hole before stripping photo-resist. A RIE process is used to etch both passivation oxide layer and Al layer and then BOE is used to etch TEOS oxide and passivation oxide without harming Al. So, naturely, Al can jut out the oxide layers.

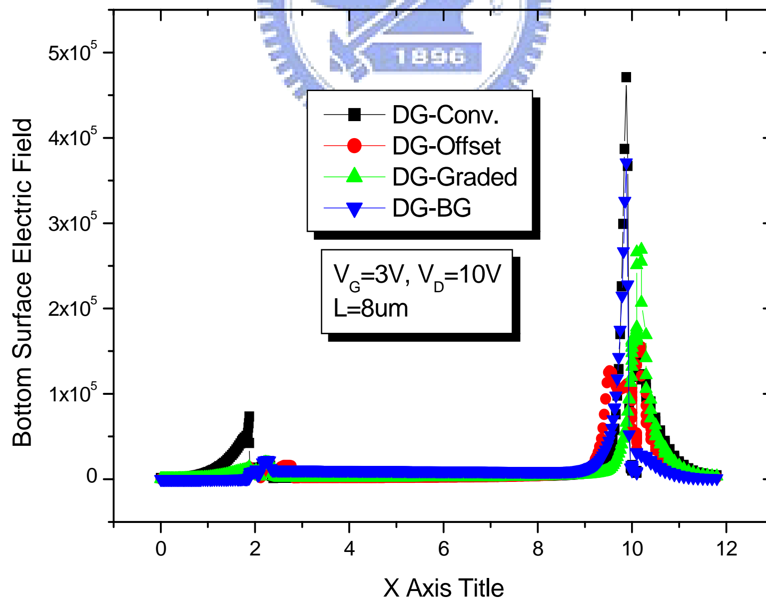
4.3.3 Electrical Simulations

In the simulations, the simulation models are the same as the previous section's. Fig. 4-12 (a) and (b) show the electric field of top-surface channel and bottom-surface channel,.respectively. It can be seen clearly that the proposed structure can reduce effectively the electric field comparison to other structures. Fig.4-13 shows the simulated I_D-V_D result, it can be found that the on current of DG GLDD almost the same as the conventional DG, and two-time lager than conventional TG and BG.



(a)





(b)

Fig.4-12 The electric field distribution with different structures along (a) top-surface channel, and (b) bottom-surface channel.

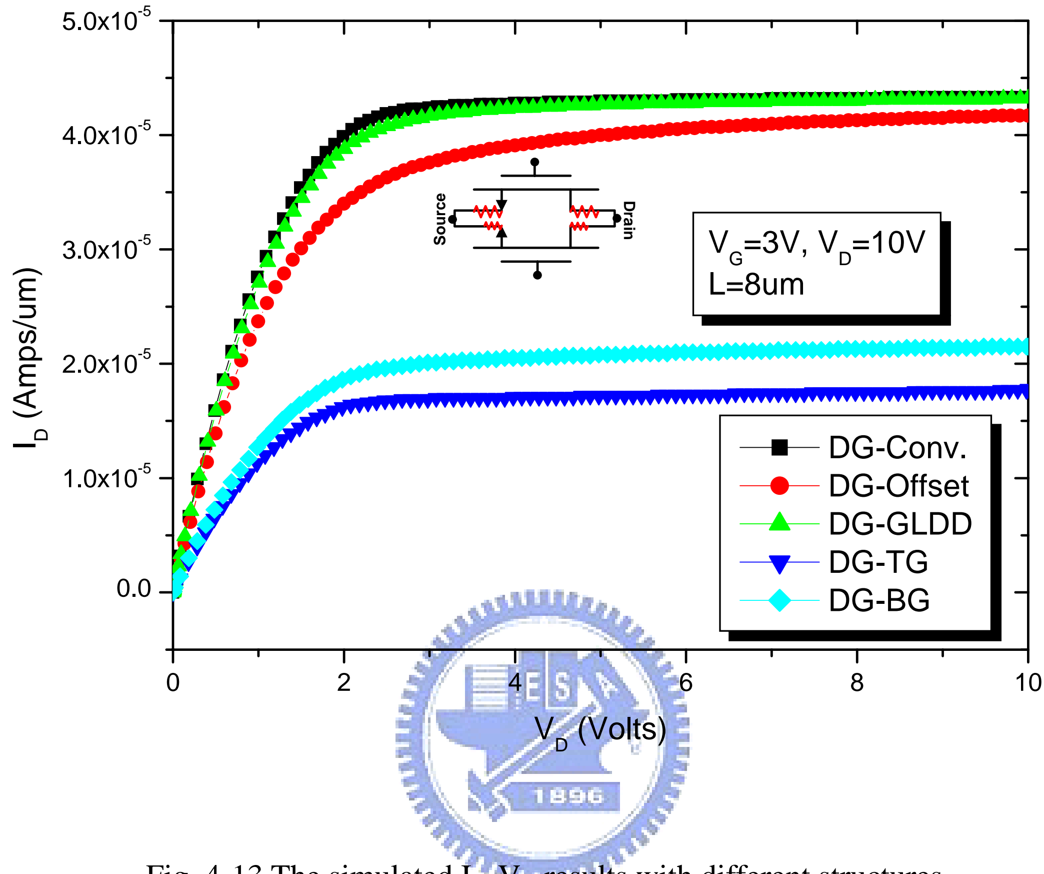


Fig. 4-13 The simulated I_D-V_D results with different structures.

4.4 Summary

Two types of high-performance gate overlapped graded LTPS TFTs with bottom gate and double gate structures were demonstrated in this chapter. The graded LDD are formed by controlling laser shot during source/drain activation without additional n^- ion-implantation. From the simulation results, the lateral electrical field near the drain junction could be effectively reduced by using graded LDD structure. And, the on current can be maintained by using the gate-overlapped structure.