A Single-Chip 2.5-Gb/s CMOS Burst-Mode Optical Receiver

Wei-Zen Chen, *Member, IEEE*, Ruei-Ming Gan, and Shih-Hao Huang

***Abstract*—This paper describes the design of a 2.5-Gb/s burst-mode optical receiver in a 0.18-μm CMOS process. A dual-gain-mode transimpedance amplifier (TIA) with constant damping factor control is proposed to tolerate a wide dynamic range input signal. By incorporating an automatic threshold tracking circuit (ATC), the TIA and limiting amplifier (LA) are dc coupled with feedforward offset cancellation. Dual-band filters are adopted in the ATC for a rapid response time while keeping the tracking error small. By integrating both a TIA and a post-LA in a single chip, the burst-mode receiver provides a conversion gain of 106 dB $\cdot$ Ω in the high gain mode, 97 dB $\cdot$ Ω in the low gain mode, and a $-$3-dB bandwidth of 1.85 GHz. The measured input sensitivity, overload level, and dynamic range of the optical receiver are $-$19 dBm, $-$2 dBm, and 17 dB, respectively. The response time is less than 50 ns. Operating under a single 1.8-V supply, this chip dissipates only 122 mW.**

***Index Terms*—Automatic threshold tracking circuit (ATC), burst-mode receiver, limiting amplifier (LA), transimpedance amplifier (TIA).**

I. Introduction

In a passive optical network, an expensive optical line terminal (OLT) is shared by multiple optical network units (ONUs) through a passive optical splitter, as shown in Fig. 1. It provides point-to-multipoint data communication and is considered as a cost-effective subscriber system to make a broadband access network like "fiber to the home" feasible. In such a shared access system, the data are continuously transmitted in the downstream traffic. On the contrary, the upstream data from the ONUs are transmitted in a burst mode. Due to the different path loss between the ONUs and the OLT, the received signal power at the OLT side may vary drastically.

In addition, for burst-mode data receiving, the optical receiver must track the input power level for properly recovering the input data, as shown in Fig. 2. In order to improve the transmission efficiency, a quick response to the input power level is necessary to reduce the guard time between data packets. Conventionally, the signal power level is captured through a feedback loop with a level detection circuit. The level detector composes a low-pass loop filter with a narrow loop bandwidth for precise power-level detection while tolerating long consecutive identical (CID) bit periods. It turns out that the settling time for threshold tracking would become quite long, and it would be difficult to meet the speed requirement for passive optical network (PON) systems. In summary, major issues for the burst-mode optical receiver design are focused on high sensitivity, wide dynamic range, and rapid response speed to the burst-mode input data.

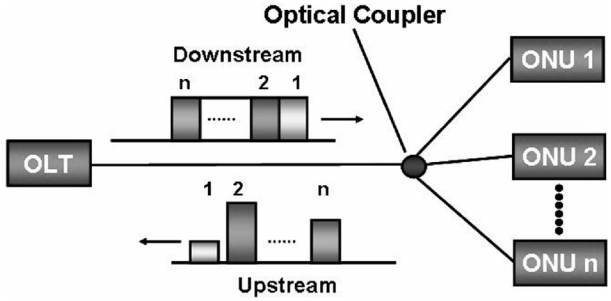

Fig. 1. Passive optical network system architecture.

This paper proposes circuit techniques for a single-chip burst-mode optical receiver to be applied in PON systems [1]. A dual-gain-mode transimpedance amplifier (TIA) with a constant damping factor is proposed for loud/soft burst receiving while avoiding jitter degradation caused by excess group-delay variations. The receiver front-end circuitries, comprising of a TIA and a limiting amplifier (LA), are dc coupled with feedforward offset cancellation by incorporating an automatic threshold tracking circuit (ATC) [2]–[4]. Fig. 3 shows an example of a two-stage cascaded amplifier with feedforward offset cancellation. Here, the ac input signal is grounded for the simplicity of analysis. Let the input offset voltages and voltage gains of the two-stage amplifier be denoted as $V_{\rm os1}$ and $V_{\rm os2}$ and A_1 and A_2, respectively. The threshold level at the positive and negative output terminals of the first stage amplifier will deviate by $A_1 V_{\rm os1}$, which is then captured by ATC1 and ATC2 and subtracted from the input of the succeeding gain stage. Since the offset voltage $(V_{\rm os2})$ at the last stage will leak to the output V_o without any compensation, it turns out that the input-referred offset voltage $(V_{\rm os})$ of the cascaded amplifier becomes

$$V_{\rm os} = \frac{V_{\rm os2}}{A_1}. \tag{1}$$

For an n-stage cascaded amplifier, the input-referred offset voltage is then suppressed by the multiple of the previous $n-1$ stages $(A_1 A_{2...} A_{n-1})$ by employing feedforward offset

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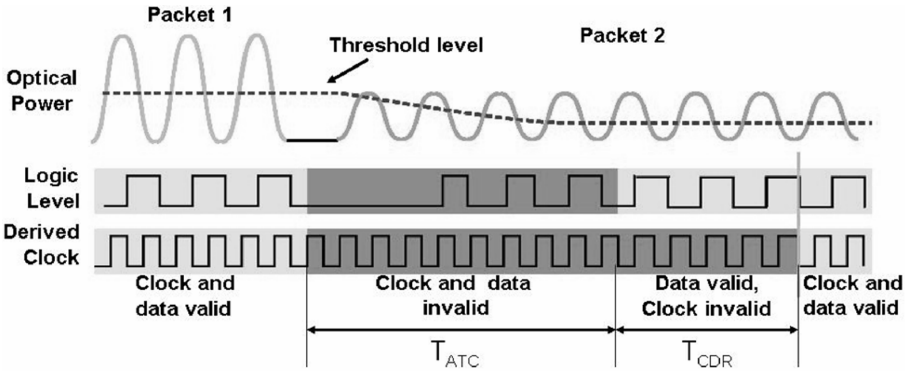


Fig. 2. Burst-mode receiver timing diagram.

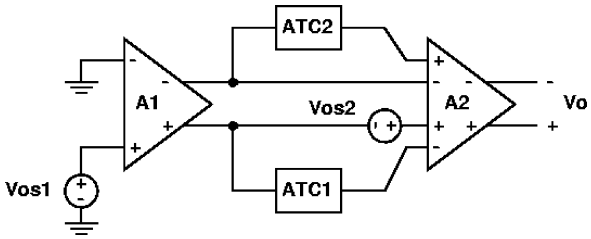


Fig. 3. Two-stage cascaded amplifier with feedforward offset cancellation.

cancellation. To accelerate the response speed of the ATC while keeping the tracking error small, in this design, a dual-band ATC is proposed. It circumvents the severe tradeoff between CID tolerance and the settling time.

Conventional burst-mode optical receivers are based on multichip solutions [2], [5] and are fabricated in more expensive InP/InGaAs HBT or SiGe BiCMOS technologies [2], [6], [7]. In contrast to the prior arts, this 2.5-Gb/s burst-mode optical receiver integrates both TIA and LA in a single chip and is fabricated in a relatively low cost 0.18-μm CMOS process. It has another advantage that no broadband matching networks are needed at the output stage of the TIA and the input stage of the postamplifiers [8], [9]. Thus, lower power dissipation can be benefited. It doubles the operating speed while dissipating much less power compared with the prior art in [2], [4], [6], [10], and [11].

This paper is organized as follows. Section II introduces the receiver architecture. Section III describes the circuit techniques for the receiver design. The experimental results are shown in Section IV. Finally, the conclusion is drawn in Section V.

II. Receiver Architecture

Fig. 4 shows the system architecture of the optical receiver. It integrates a TIA, a three-stage LA, a gain control circuit for the TIA, a timing control unit (timer), and automatic threshold tracking circuits (ATC1–ATC3) on a single chip. According to IEEE 802.3ah recommendations, the OLT should adapt an amplitude variation of 20 dB for less than 400 ns (500 bit time) at 1.25-Gb/s operation. In this design, the targeted tracking time for the burst-mode optical receiver analog front end is less than 50 ns (125 bit time) at 2.5-Gb/s operation. To achieve an input sensitivity level of -20 dBm and an input dynamic range of 20 dB, the conversion gain of the TIA is switchable between dual gain modes according to the detected input signal level. In this design, the TIA provides 66 dB$\cdot\Omega$ in the high gain mode and 57 dB$\cdot\Omega$ in the low gain mode, so as to avoid data jitter induced by signal overload. Moreover, the postamplifier provides additional 40 dB to generate fully switch logic signals ($> 300\ \mathrm{mV_{pp}}$). The TIA and the LA are dc coupled with feedforward offset cancellation utilizing the proposed ATCs. Here, ATC1 performs as a power-level detector of the TIA for gain mode switching and also provides the input common-mode level for differential to single-ended signal conversion. ATC2 and ATC3 capture the threshold deviation of the preceding gain stage by averaging the peak and bottom voltage levels. The offset voltage is then subtracted in the succeeding gain stage. One thing noteworthy is that the ATCs are applied only at the input of the second gain stage and the output buffer, so as to provide sufficient offset suppression without too much hardware overhead. All the ATCs incorporate dual-band low-pass filters to accelerate automatic gain mode setting and offset cancellation in the gain chains while maintaining a small tracking error.

The procedure for the receiver parameter setting is as follows. Before the data burst in, a global reset signal is provided between the data packet to initialize the receiver parameter. The front-end TIA is then set in the high gain mode, and ATC1–ATC3 are set in the wide band mode for a quicker threshold tracking. After about 30 ns, the gain control circuit then adjusts the gain mode of the TIA according to its output swing, and ATC1 to ATC3 are switched to a narrow band mode one by one. All the steps are moderated by the open-loop timing control unit (timer). In this way, the tracking error of the ATC can be suppressed when the data are valid.

III. Circuit Design

A. Transimpedance Amplifier (TIA)

The circuit schematic of the TIA is shown in Fig. 5, which is based on a cascode voltage amplifier (comprised of M_1, M_2, R_1, M_3, and M_4) with shunt feedback resistors R_{f1} and R_{f2}. The buffer stage (M_5, M_6) performs as a level shifter to drive the succeeding stage. For the voltage amplifier to achieve a sufficiently high gain under a 1.8-V supply, a current-injection technique is utilized. Here, M_{10} enhances the transconductance of M_1 without sacrificing the open-loop

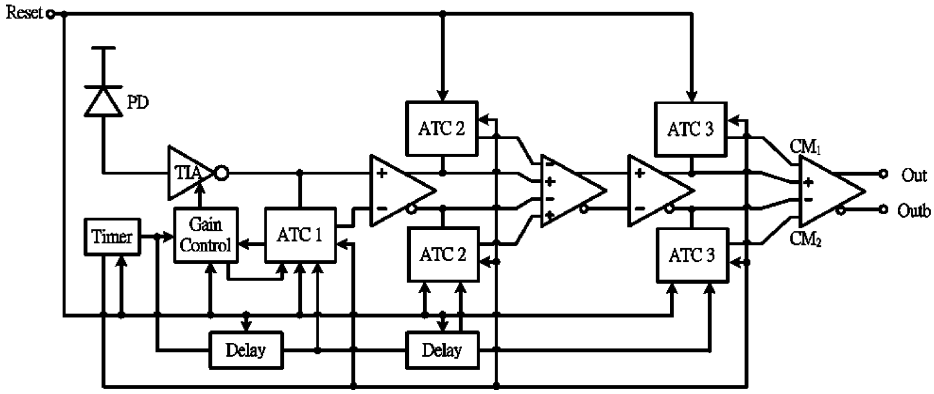


Fig. 4. Burst-mode receiver architecture.

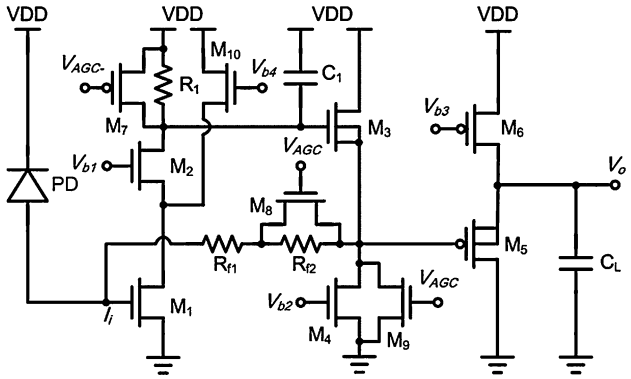


Fig. 5. TIA circuit schematic.

bandwidth of the voltage amplifier, which is dominated by the parasitic capacitor C_1.

Assuming that ω_0 and A_0 represent the -3-dB bandwidth and conversion gain of the cascode voltage amplifier, $C_{\rm in}$ denotes the parasitic capacitance at the input node of the TIA, and R_f is the feedback resistor, the damping factor (ζ), natural frequency (ω_n), and conversion gain (T_z) of the TIA can be derived as [12]

$$\zeta \approx \frac{1}{2}\sqrt{\frac{C_{\rm in}R_f\omega_0}{1+A_0}} \tag{2}$$

$$\omega_n = \sqrt{\frac{(1+A_0)\omega_0}{C_{\rm in}R_f}} \tag{3}$$

$$T_Z \approx R_f. \tag{4}$$

As the natural frequency and damping factor of the TIA are related to its conversion gain (R_f), to maintain a relatively constant damping factor and -3-dB bandwidth, the open-loop gain of the voltage amplifier A_0 should be adjusted along with the feedback resistor R_f. The frequency response of the TIA is designed to behave as a Bessel-type filter response in both gain modes so as to have a smaller group-delay variation. In this case, the corresponding -3-dB bandwidth of the cascode amplifier ω_0 can be derived as

$$\omega_o \approx \frac{3A_0}{R_f C_{\rm in}}. \tag{5}$$

The dual-gain mode is controlled by $V_{\rm AGC}$. In the high gain mode, M_7, M_8, and M_9 are turned off. The feedback resistor

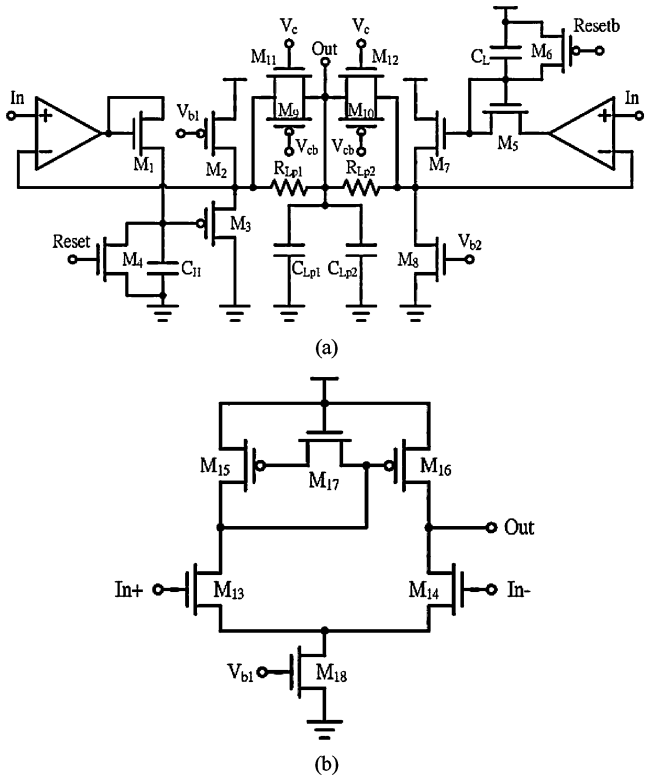


Fig. 6. (a) ATC circuit. (b) OP in the ATC.

becomes $R_{f1} + R_{f2}$, such that the conversion gain T_Z is increased. On the contrary, for a low gain mode operation, M_8 is turned on to reduce the feedback resistor. Meanwhile, M_7 is turned on to reduce the voltage amplifier gain A_0, so as to compensate damping factor variation. At the same time, M_9 is turned on to maintain a relatively constant dc output voltage to avoid disturbing the threshold level in the gain chain.

B. Automatic Threshold Tracking Circuit (ATC)

To circumvent the severe compromise between the tolerable CID, offset cancellation, and response time, optical receivers with feedforward offset cancellation are widely applied in PON systems [2]–[4], [10]. In the receiver front end, [2], [4], and [10] employ a peak hold circuit to capture output threshold voltage deviations caused by input offset voltage. However, it becomes inaccurate when the signal is overloaded. Seo *et al.* [3] employ both peak/bottom hold circuits and voltage divider to cope with

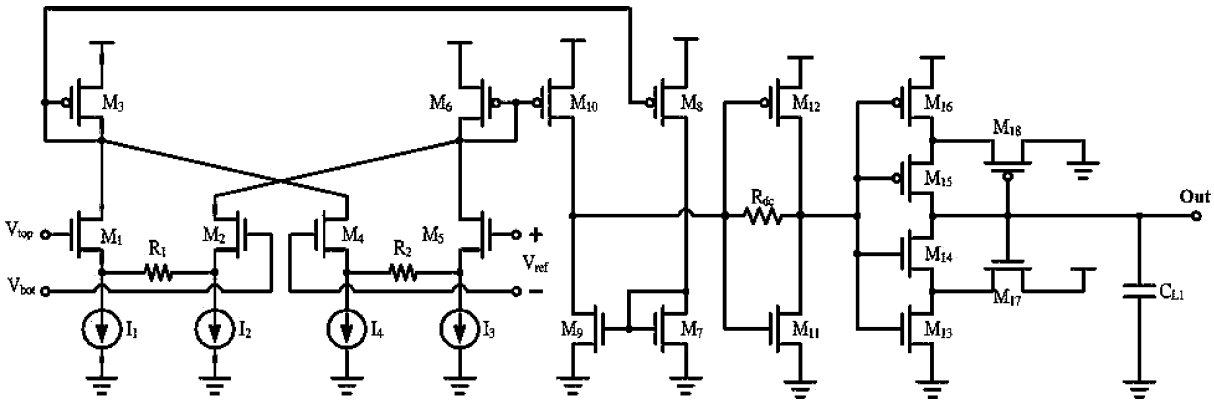


Fig. 7. Gain control circuit.

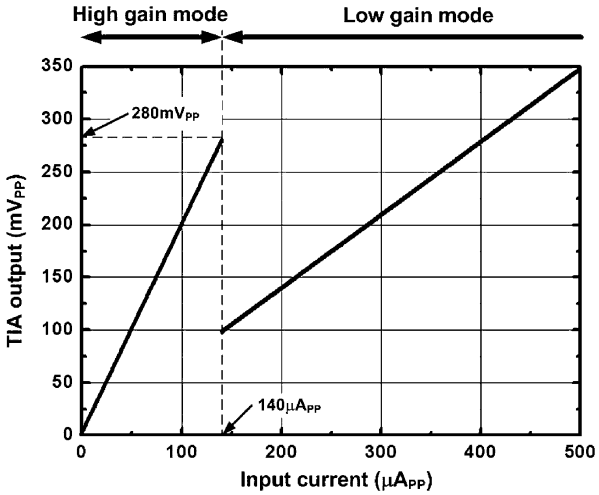


Fig. 8. Dual-gain-mode TIA transfer characteristic.

this issue. Since the voltage divider is composed of an RC low-pass filter, it leads to a slow response if the filter bandwidth is too narrow. Contrarily, it would suffer from a charge-leakage effect if the bandwidth is too wide. To circumvent the aforementioned issues, in this design, an ATC with peak/bottom hold circuits and dual-band voltage divider is proposed.

The detailed ATC circuit is shown in Fig. 6(a). The buffer stages M_3, M_2 and M_7, M_8 perform as level shifters to alleviate the charge leakage in the peak/bottom hold circuits. The threshold level is derived at the output node "Out" after a dual-band low-pass filter $(R_{Lp}1,2, C_{Lp}1,2, M_9{-}M_{12})$. In the initial state, the holding capacitors C_H and C_L are precharged to low (ground) and high (VDD), respectively. The $-$3-dB bandwidth of the low-pass filter is controlled by the variable resistors $(M_9{-}M_{12})$. In the wide band mode, the $-$3-dB bandwidth $(\omega_{\rm WB})$ of the ATC can be approximated as

$$\omega_{\rm WB} = \frac{1}{(R_{\rm Lp1,2}||R_{\rm on})(C_{\rm Lp1,2})} \tag{6}$$

where $R_{\rm on}$ is the turn-on resistance of M_9 and M_{11} (M_{10} and M_{12}) in parallel. On the other hand, the $-$3-dB bandwidth $(\omega_{\rm LB})$ of the ATC in the narrow band mode can be expressed as

$$\omega_{\rm LB} = \frac{1}{R_{\rm Lp1,2}C_{\rm Lp1,2}}. \tag{7}$$

For the threshold tracking circuit to settle within 1% accuracy in the wide band mode during k bits (T_b) 1 and 0 alternating preamble, the criterion for $\omega_{\rm WB}$ can be approximated as

$$\omega_{\rm WB} > \frac{9.2}{k \cdot T_b}. \tag{8}$$

In this design, $\omega_{\rm WB}$ is about 200 MHz for a quicker threshold tracking, and $\omega_{\rm LB}$ is reduced by one order of magnitude to reduce the voltage ripple in the steady state. According to simulation, the ripple voltage at the ATC output is suppressed below 50 μV by employing the dual-band filtering scheme. Compared with the peak–hold output voltage without filtering, it is reduced by more than two orders or magnitude.

The operational amplifier (OP) for the ATC is shown in Fig. 6(b). The unity gain bandwidth of the peak/bottom hold rectifier can be approximated as

$$\omega_{\rm UB} = \frac{g_m}{C_{H,L}} \tag{9}$$

where g_m is the input transconductance of the OP. In this design, $\omega_{\rm UB}$ is chosen to be ten times higher than $\omega_{\rm WB}$, such that the ATC bandwidth would not be deteriorated by the OP finite bandwidth effect. In such a high-speed operation, the mirror pole in the differential to single-ended amplifiers is critical to the offset voltage of the peak/bottom hold rectifier and will lead to the tracking error at the ATC output. To cope with this issue, the OP bandwidth is enhanced by inductive peaking utilizing M_{17}. In this case, a zero at 1.75 GHz is inserted for phase compensation.

C. Gain Control Circuit

The circuit schematic of the gain control circuit is shown in Fig. 7. It is composed of a differential difference preamplifier $(M_1{-}M_{10})$ followed by a single-ended postamplifier $(M_{11}{-}M_{12})$ and a hysteresis comparator $(M_{13}{-}M_{18})$. Here, $V_{\rm top}$ and $V_{\rm bot}$ are derived from peak/bottom hold detectors, and $\rm V_{ref}$ is about 190 mV. The gain mode switching is conducted automatically by the gain control circuit.

The hysteresis comparator is adopted at the output stage of the gain control circuit to avoid gain mode flipping during data receiving. In order to avoid waveform distortion caused by signal overload, the TIA is switched to the low gain mode as the output swing is higher than 280 mV. On the contrary, the TIA is switched to the high gain mode as its output swing is lower than 100 mV for a lower input-referred noise. Incorporating the

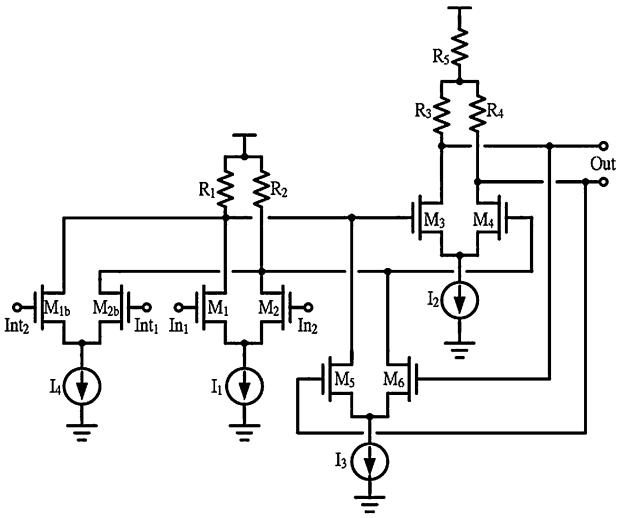


Fig. 9. LA core cell.

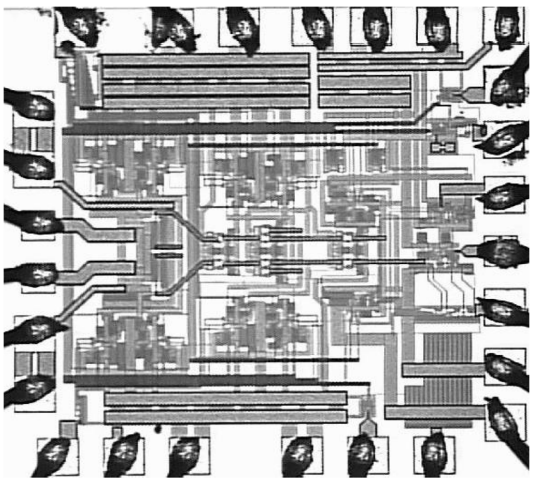


Fig. 10. Chip photograph.

automatic gain control scheme, the transfer characteristic of the dual-gain-mode TIA is shown in Fig. 8. For the incident optical power within the specified input dynamic range, the TIA output voltage is kept less than 280 $\mathrm{mV_{pp}}$.

D. Limiting Amplifier (LA)

The core circuit of the LA is shown in Fig. 9, which is based on the Cherry–Hooper circuit architecture with active feedback [13]. The M_1, M_2 input pair is for the signal path, while the $M_{1\mathrm{b}}$ and $M_{2\mathrm{b}}$ differential pair is used for feedforward offset cancellation. For an N-stage cascaded amplifier, the voltage gain (A_s) and $-$3-dB bandwidth (ω_s) of a single-stage amplifier can be derived in terms of the overall conversion gain (A_c) and cascaded bandwidth (ω_c)[14], where

$$A_s = A_c^{1/N} \tag{10}$$

$$\omega_s = \frac{\omega_c}{\sqrt[4]{2^{1/N}-1}}. \tag{11}$$

For a targeted ω_c of 3 GHz and A_c of 40 dB, we have ω_s of about 4.2 GHz and A_s of approximately 14 dB for a three-stage $(N = 3)$ cascaded gain amplifier. As the gain bandwidth product of the gain cell can be extended beyond the technology f_{T}[13], no peaking inductors are needed in this design.

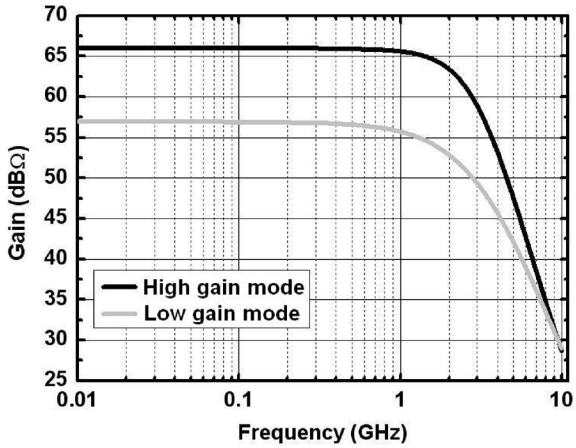


Fig. 11. TIA frequency response.

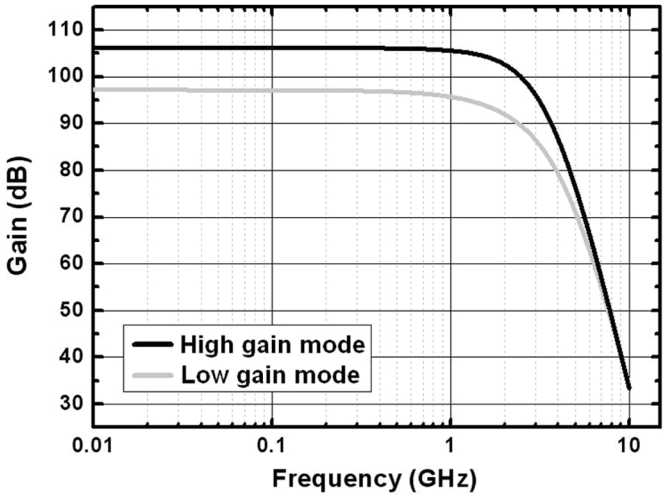


Fig. 12. Optical receiver frequency response.

Since the LA is composed of three gain stages with feedforward offset cancellation, the top level of the output signal must be within the captured range of the ATC. Here, resistor R_5 is inserted to provide a dc drop for the proper operation of the ATC.

IV. Experimental Results

The experimental prototype has been fabricated in a 0.18-μm CMOS process. Fig. 10 shows the chip photograph. The chip size is about 1.2×1.2 mm^2. The substrate noise coupling between the TIA and the post-LA is alleviated by a double guard ring. In addition, the differential architecture diminishes the differential to single-ended (output to input) noise conversion.

For an optical test, the prototype chip is mounted on a printed circuit board with a commercially available 850-nm photodetector (TPD-8D12-012). The responsivity of the detector is about 0.5 A/W, and its parasitic capacitance is 0.4 pF. The bonding pad of the receiver provides additional 60 fF. Furthermore, the extinction ratio for the 850-nm laser source (New Focus 1780) is about 9 dB.

The simulated frequency responses of the TIA in both gain modes are shown in Fig. 11. The conversion gain of the TIA is about 66 dB $\cdot\,\Omega$ in the high gain mode and 57 dB $\cdot\,\Omega$ in the low gain mode, while the $-$3-dB bandwidth is about 0.7 times the

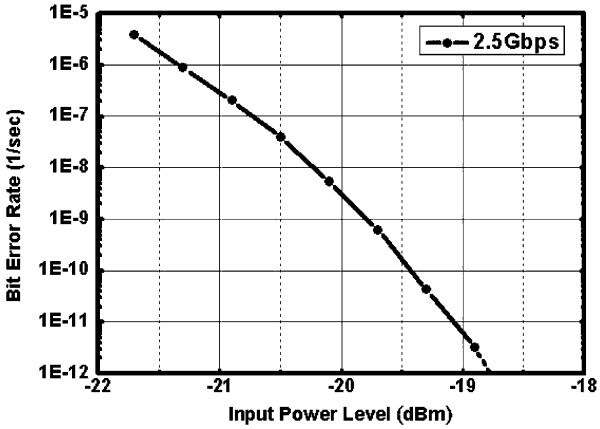


Fig. 13. Measured BER performance.

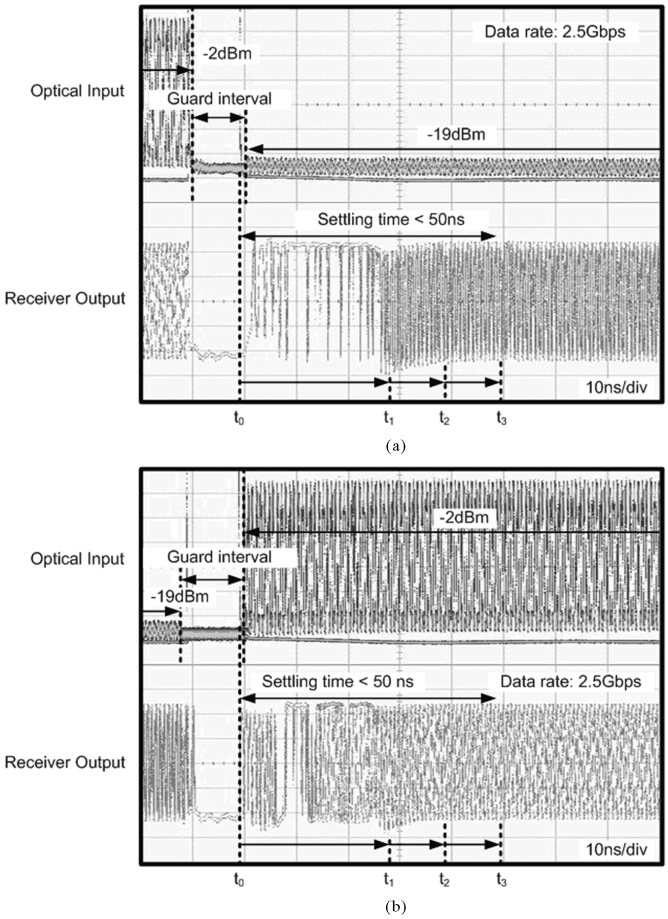
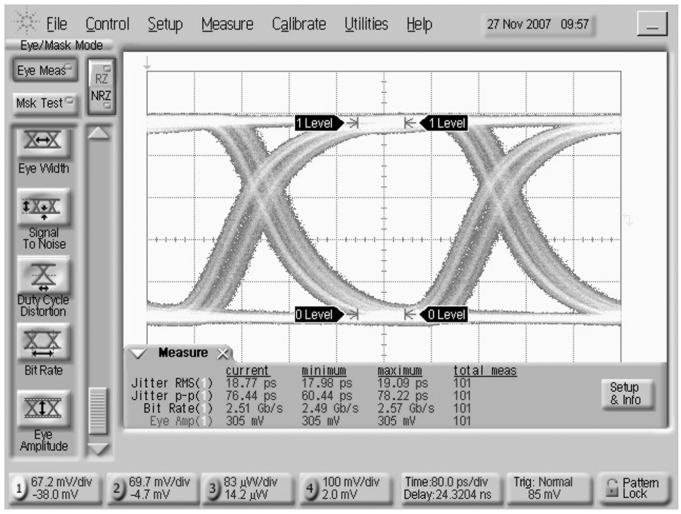


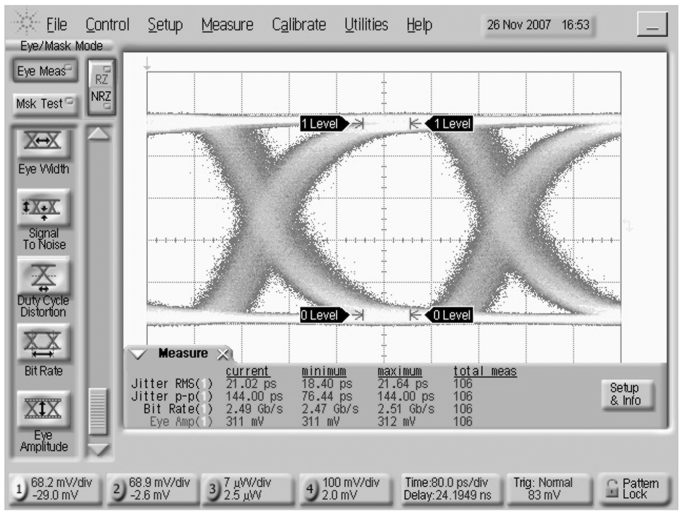
Fig. 14. Measured settling response (a) from loudest (−2 dBm) to softest (−19 dBm) bursts and (b) from softest (−19 dBm) to loudest (−2 dBm) bursts.

bit rate as a compromise between ISI and noise performance. No gain peaking is observed for gain mode switching. Furthermore, the group-delay variation is within ±10 ps by simulation. Fig. 12 shows the simulated frequency response of the overall optical receiver. Its conversion gain is about 106 dB · Ω in the high gain mode and 97 dB · Ω in the low gain mode. The −3-dB bandwidth is limited by the TIA.

Fig. 13 shows the measured input sensitivity and bit error rate (BER) performance. With a $2^{31}-1$ test pattern, which corresponds to 30 CID bits in the test case, the measured input sensitivity and overload level of the optical receiver is about −19 and −2 dBm, respectively, for a BER around 10^{-12}. The input dynamic range is about 17 dB.



(a)



(b)

Fig. 15. Measured eye diagram at 2.5 Gb/s. (a) Loudest bursts (−2 dBm). (b) Softest bursts (−19 dBm).

The measured settling response from the loudest (−2 dBm) to the softest (−19 dBm) bursts and vice versa are shown in Fig. 14(a) and (b), respectively. Here, t_1-t_3 indicates the onset when ATC1–ATC3 resume their narrow band mode. In both cases, the settling time is less than 50 ns. The measured eye diagrams at the loudest (−2 dBm) and softest (−19 dBm) bursts for 2.5-Gb/s operations are shown in Fig. 15(a) and (b). The corresponding peak-to-peak data jitter at the receiver output are about 76.4 and 144 ps, respectively, and the single-ended output swing is over 300 mV in both cases.

Table I summarizes the performance comparison of the proposed optical receiver with the prior art. Thanks to single-chip integration (no power-hungry broadband I/O buffers) and the proposed circuit techniques, it dissipates 50% less power while doubling the operating speed. The input sensitivity of the optical receiver is expected to be further improved with a higher sensitivity photodetector.

TABLE I
PERFORMANCE BENCHMARK

	[2]	[4]	[10]	This work
Optical Receiver	Chip sets	Single chip	Chip sets	Single chip
Speed	1.25 Gbps	1.25 Gbps	1.25 Gbps	2.5 Gbps
Sensitivity	-29 dBm	-26.4 dBm	-29 dBm	-19 dBm
Overload power level	-3 dBm	-5.4 dBm	-2.2 dBm	-2 dBm
Dynamic Range	26 dB	21 dB	27 dB	17 dB
Photodiode responsivity	0.9 A/W	0.85 A/W	0.92 A/W	0.5 A/W
Settling time	16 ns	50 ns	N.A.	50ns
Power Dissipation	300 mW	528 mW	810 mW	122 mW
Technology	SiGe-BiCMOS	0.18 μm CMOS	0.25 μm CMOS	0.18 μm CMOS

V. CONCLUSION

This paper has described the design of a single-chip 2.5-Gb/s burst-mode optical receiver for PON system. To tolerate wide dynamic range input signal, a dual-gain-mode TIA with constant damping factor control has been proposed. The LA is based on Cherry–Hopper architecture with active feedback for a wide band operation. By incorporating an automatic threshold tracking circuit (ATC), the TIA and the LA are dc coupled with feedforward offset cancellation. Dual-band filters are proposed and adopted in the ATC for a rapid response time while keeping the tracking error small. The measured settling time is less than 50 ns.

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