國 立 交 通 大 學

電子工程學系　電子研究所

博 士 論 文

低臨界電壓雙金屬閘極金氧半電晶體製作技術之研發

The Investigation of Low Threshold Voltage Dual Metal Gate MOSFET Technology

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博士論文

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摘要

隨著互補式金氧半電晶體(*C*-MOSFETs)的持續微縮，複晶矽閘極在 45 奈米以下技術將遭遇到許多本質上的限制，包括高電阻率、硼穿隧和複晶空乏。除此之外，高介電常數介電質也將導入製程以取代傳統二氧化矽或氮氧化矽介電質。然而，有研究指出複晶矽閘極跟高介電常數介電質間會有費米能階栓(Fermi-level pinning)效應。因此，金屬閘極顯然是解決以上問題的良好選擇。使用金屬閘極必須符合適當功函數、熱穩定、製程兼容性和更佳的元件效能等需求。在本論文研究中，包含全金屬矽化(FUSI)閘極和低溫處理純金屬閘極這二種類型雙金屬閘極製程技術的研究。

首先，我們先微縮等效氧化層厚度(EOT)從 1.6 奈米到 1.2 奈米，並使用矽化鉿閘極這方面的研究。我們從臨界電壓(V_t)和電子移動率來觀察發現等效氧化層厚度 1.2 奈米之氮氧化鑭鉿 N 型金氧半電晶體，在使用低功率數高溫穩定的矽化鉿閘極有良好的效能。自我對準以及閘極優先的矽化鉿／氮氧化鑭鉿 N 型金氧化電晶體擁有簡單的高溫全金

屬矽化處理以及兼容於現今極大型積體電路整合(VLSI)生產線等優點。

在接下來的研究，我們使用與之前類似的矽化鈦全金屬矽化製程。我們可以從極低的漏電、良好的電洞移動率、1000 度 C 高溫穩定性中看出良好的矽化鈦／氮氧化鑭鉿 P 型金氧化電晶體元件整合特性。然而，在等效氧化層厚度 1.2 奈米下卻觀察到不佳的平帶電壓和高臨界電壓。因此，我們目標是發展出一種新的製程技術來解決這個問題。

為了研究平帶電壓下滑的現象，我們首先比較使用相同矽化鈦閘極在不同等效氧化層厚度下的平帶電壓。最後我們研發出一個新的高功率數鈦／氧化鑭鉿 P 型金氧半電晶體，使用低溫處理淺接面製程。自我對準鈦／氧化鑭鉿 P 型金氧半電晶體的優點為適當的 5.3 電子伏特之等效金屬功率數、+0.05 伏特之低臨界電壓、在電場為-0.3 MV/cm 下 90 cm^2/V-s 之高電洞移動率以及 20 mV 之微小偏壓溫度不穩定性(在 85 度 C，10 MV/cm 以及一小時的條件下)。本實驗結果擁有 1.2 奈米等效氧化層厚度、和簡單的自我對準製類似以及閘極優先之極大型積體電路製程，比之前發表的金屬閘極高介電常數介電質 P 型金氧半電晶體結果不相上下或是較佳。

最後我們也試著同時降低 N 型金氧半電晶體的製程溫度，使用鉿／氧化鑭鉿固態擴散製程。我們研究兩種不同的固態擴散製程。結果發現使用低功函數鉿閘極的氧化鑭鉿 N 型金氧半電晶體在 1.2 奈米等效氧化厚度下，在臨界電壓以及移動率的觀點都有良好的特性。自我對準閘極優先的鉿／氧化鑭鉿 N 型金氧化電晶體擁有的優點包含低於 900 度 C 之低製程溫度、良好的元件特性以應用在極大型積體電路製程上。

總結，金屬矽化物的全金屬矽化物製程擁有適當的金屬功率數、高溫穩定等優點。

然而當氧化層厚度持續的微縮，1000 度 C 的摻雜活化處理變得越來越關鍵。在我們的研究中，使用低溫製程技術可以解決平帶電壓下滑以及不需要的高臨界電壓。因此在我們未來的研究中，同時對N型與P型金氧半電晶體更進一步減低製程溫度技術是必要的。

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ABSTRACT

With the continuous scaling trend of complementary metal-oxide-semiconductor field effect transistors (*C*-MOSFETs) technology, poly-silicon gates encounter several inherent drawbacks beyond the 45 nm technology node including high resistivity, boron penetration and poly-depletion. In addition, high-κ gate dielectrics have also been introduced to replace the conventional silicon dioxide or silicon oxynitride. However, poly-silicon gates have reported to suffer from Fermi-level pinning effect at the poly-silicon/high-κ interface. Therefore, metal gate is obviously a good choice to solve the above problems. The introduction of metal gates should meet the requirement of proper work function, thermal

stability, process compatibility and better device performance. In this dissertation, two novel dual metal gate process technologies including fully silicided (FUSI) gates and low-temperaure-processed pure metal gate were investigated.

At first, scaling the effective oxide thickness (EOT) from 1.6 nm to 1.2 nm using $HfSi_x$ gates was studied. We have found good performance in terms of threshold voltage (V_t) and mobility for $Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs at 1.2 nm EOT using a low work-function and high-temperature-stable $HfSi_x$ gate. The self-aligned and gate-first $HfSi_x$/HfLaON *n*-MOSFETs have the advantages of simple high temperature FUSI processing and compatibility with current very large scale integration (VLSI) lines.

In the following study, similar FUSI process using $IrSi_x$ gates was also investigated. Good device integrity of Ir_3Si/HfLaON *p*-MOSFETs is shown by the very low leakage current, good hole mobility and 1000°C thermal stability. However, poor flat band voltage (V_{fb}) and high V_t is observed at 1.2 nm EOT. As a result, we aimed to develop a new process technology to solve this problem.

In order to study the origin of V_{fb} roll-off phenomenon, we compared the V_{fb} of Ir_3Si gates under different EOT. Finally, we develop a new process technology of high work-function Ir/HfLaO *p*-MOSFETs using low-temperature-processed shallow junction. The merits of self-aligned Ir/HfLaO *p*-MOSFETs are the proper $\phi_{m\text{-}eff}$ of 5.3 eV, low V_t of +0.05 V, high hole mobility of 90 cm^2/V-s at -0.3 MV/cm and small BTI of 20 mV (85°C, 10 MV/cm

& 1 hr). These results are comparable with or better than the previous reported data for metal-gate/high-κ *p*-MOSFETs, with small 1.2 nm EOT, similar simple self-aligned and gate-first process for VLSI IC fabrication.

Finally, we also tried to decrease the process temperature of *n*-MOSFET by Hf/HfLaO using solid phase diffusion (SPD). Two different SPD shallow junctions were studied. We have found good performance in terms of V_t and mobility for HfLaO *n*-MOSFETs at 1.2 nm EOT using a low work-function Hf gate. The self-aligned and gate-first Hf/HfLaO *n*-MOSFETs have the advantages of ≤900°C low processing temperature and good device performance for VLSI fabrication.

In conclusion, metal silicide FUSI processes have the advantage of proper $\phi_{m\text{-}eff}$, high temperature stable. However, as the continuous scaling of oxide thickness, the thermal budge of 1000°C dopant activation process has become more critical. In our study, the V_{fb} roll-off and unwanted high V_t can be solved by low temperature process technology. As a result, it is necessary to further decrease the process temperature for both *n*- and *p*-MOSFETs in our future study.

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Chapter 1

Introduction

1.1 Metal Gate Electrodes

As traditional poly-silicon (poly-Si) gated metal-oxide semiconductor field effect transistors (MOSFETs) scales, the additional series capacitance due to poly-Si depletion becomes an increasingly large fraction of the total gate capacitance [1.1]-[1.13]. Besides, boron penetration from the poly-Si gate will also degrade the performance of the transistors. In order to overcome these problems, metal gate electrodes was used to be a practical way to eliminate poly-gate depletion and boron penetration [1.1]-[1.8]. In addition, metal gates also have the potential to reduce sheet resistance of gate electrodes. Metal electrodes with suitable work functions and sufficient physical and electrical stability are being widely investigated to solve these problems.

1.1.1 Classification of Metal Gate Materials

Metal gate materials are generally classified into four major types including pure metals, metallic alloys, metal silicides and metal nitrides/carbides/oxides.

(1) Pure metals:

Fig. 1-1 shows the periodic table. Group B metals are commonly used in the IC industry. The work functions periodically range from conduction band (E_c) to valence band

(E_v) relative to locations of elements [1.14]. Elements in column IIIB, IVB VB such as Ti, Y, Hf, Ta and Lanthanide series have n-type work functions; elements in column VIB and part elements in column VIIB such as Mo and W have mid-gap work functions; elements in column VIIB such as Rh, Ir, Ni, Pd and Pt tend to have p-type work functions. N-type elements are chemically reactive. As a result, a capping metal layer such as TaN is necessary to prevent possible reaction during thermal process. P-type elements are relatively inert and can sustain the high temperature process. However, the chemical inertia results in the difficulties in patterning and poorness in adhesion.

(2) Metallic alloys:

Typically, metallic alloys are binary alloys consist of n-type metal and p-type metal/mid-gap metals, such as Ta-Pt alloys, Ta-Ru alloys and Hf-Mo alloys [1.15-1.17]. The work function is determined by the atomic composition. Alloys with higher n-type metal content have a lower work function. On contrary, alloy with higher p-type metal content have a higher work function.

(3) Metal silicides:

Metal react with silicon to form metal silicides. The popular metal silicide candidates are hafnium silicide, molybdenum silicide, tungsten silicide, nickel silicide, cobalt silicide, platinum silicide and Iridium silicide. The merit of metal silicide gates is the compatibility with conventional CMOS process. Therefore, metal silicides are thought to be the possible

metal gate materials.

(4) Other metal nitrides/carbides/oxides

Metals react with nitrogen/carbon/oxygen to form metal nitrides/carbides/oxides which are more chemically stable on dielectrics than pure metal. The work function can be adjusted by the nitrogen/carbon/oxygen composition and metal nitrides/carbides/oxides phase, but the tunable range is not wide enough to be used for both *n*- and *p*-MOSFETs. In addition, an obvious drawback is the high resistivity.

1.1.2 Work Function

Metal work functions (ϕ_m) are shown in Fig. 1-2 and they play an important role for metal-gate/high-κ *C*-MOSFETs. The preferred work function of the metals are ~5.2 eV for *p*-MOSFETs and ~4.1 eV for *n*-MOSFETs. Recently, lots of metal or metal-nitride materials have been widely researched and successfully intergraded in advanced *C*-MOSFETs, such as TiN, TaN, Pt, Mo and Ir [1.1]-[1.13]. However, it has been found that thermal annealing of the metal gates at high temperature results in mid-gap values for some metal gate candidates [1.18]. Therefore, the Fermi-level pinning effect needs to be avoided by selecting suitable metal gate and high-κ materials for advanced CMOS technologies.

1.2 High-κ materials

Many materials systems are currently under consideration as potential replacements for SiO_2 as the gate dielectric material for 45 nm node CMOS technology. A systematic

consideration of the required properties of gate dielectrics indicates that the key guidelines for selecting an alternative gate dielectric are [1.19]-[1.24]:

(1) Permittivity

(2) Band gap

(3) Band alignment to silicon

(4) Thermodynamic stability

(5) Film morphology

(6) Interface quality

(7) Compatibility with the current or expected materials to be used in processing for CMOS devices

(8) Reliability

Many dielectrics appear favorable in some of these areas, but very few materials are promising with respect to all of these guidelines. Specifically, a dielectric constant (κ) ~25 is required to satisfy the requirements for CMOS gate dielectrics leading out to years beyond 2010. Similar or larger values are required for dielectrics used in embedded dynamic random access memory (DRAM) cells and radiofrequency (RF) coupling capacitors. The material must also respond positively to a series of other demands relating to such effects as lack of interactivity with the Si substrate, low leakage currents, low interface state density, high electrical barriers against charge injection, etc. The gate leakage current through the gate

oxide increases significantly because direct tunneling is the primary conduction mechanism in down-scaling CMOS technologies. Therefore, the engineering of high- κ gate dielectrics have attracted great attention and played an important role in VLSI technology.

According to the ITRS (International Technology Roadmap for Semiconductor) [1.25], the suitable gate dielectrics must have value more than 8 for 50-70 nm technology nodes and that must be more than 15 when the technology dimension less than 50 nm. Figs. 1-3 and 1-4 show the evolution of CMOS technology requirements. Oxy-nitrides (SiO_xN_y) have been introduced to extend the use of SiO_2 in production but eventually it has to be replaced by a high-κ material, such as Ta_2O_5, TiO_2, HfO_2, ZrO_2, Al_2O_3, La_2O_3 or mixtures of them or metal-oxide-silicates of the mentioned compounds. However, most metal oxides will have the characteristics of crystallization at elevated temperature which cause devices generate non-uniform leakage distribution and give large statistical variation for nano-meter devices across the chip. Materials such as HfLaON can still preserve its amorphous structure up to 1000^{o}C as Fig. 1-5 shows. Fig. 1-6 shows the summaries of the κ value and band offset for popular high-κ dielectric candidates. To predict the M-N thermal stability, in Fig.1-7 we show the bond enthalpy for various metal/dielectric combinations. In general the bond strength is that M-O> M-N> M-C.

1.3 Metal Gate High-κ Strategy

The metal gate high-κ strategy are generally classified into four different type including

Single Metal Single Dielectric (SMSD), Dual Metal Single Dielectric (DMSD), Single Metal Dual Dielectric (SMDD) and Dual Metal Dual Dielectric (DMDD). Table 1-1 lists pros and cons of different metal gate high-κ strategy. In a metal gate technology, one approach employs a metal with mid-gap work function for both *n*- and *p*-MOSFETs. The drawbacks are that the threshold voltages would be too large for a reasonable channel doping, and counter-doping the channel to alleviate this problem degrades short-channel and turn-off characteristics [1.26], [1.27]. Hence, an approach analogous to the established dual-poly-Si gate technology, i.e., a dual-metal gate technology, would be preferred. The major challenge is to find two metals with suitable work functions and a way to integrate them into a CMOS process.

1.4 Overview of Dissertation

At first, scaling the effective oxide thickness (EOT) from 1.6 nm to 1.2nm using $HfSi_x$ gates was studied. In the following study, similar FUSI process using $IrSi_x$ gates was also investigated. However, poor effective metal work function ($\phi_{m\text{-}eff}$) and high threshold voltgage (V_t) is observed at 1.2nm EOT. As a result, we aimed to develop a new process technology to solve this problem.

In order to study the origin of flat-band voltage (V_{fb}) roll-off phenomenon. We compared the V_{fb} of $IrSi_x$ gates under different EOT. Finally, we develop a new process technology of high work-function Ir/HfLaO *p*-MOSFETs using low-temperature-processed

shallow junction. Finally, we also tried to decrease the process temperature of *n*-MOSFET by Hf/HfLaO using solid phase diffusion (SPD). Two different Solid phase diffusion (SPD) shallow junctions were studied. The self-aligned and gate-first Hf/HfLaO *n*-MOSFETs have the advantages of ≤900^{o}C low processing temperature and good device performance using a self-aligned and gate-first process.

Table 1-1 Comparison of different Metal Gate High-κ Strategy.

	Pros	Cons
SMSD	✓Simple process	× Limited range of work function tuning × Metal/Dielectric interface problem × Poor Device performance
SMDD	✓Less complicated process step ✓Wider range of work function tuning ✓Good Device performance	× Two dielectric deposition steps × Metal/Dielectric interface problem × Work function tuning range of dielectric material is not as large as metal gates.
DMSD	✓Less complicated process step ✓Wider range of work function tuning ✓Good Device performance	× Two gate deposition steps × Metal/Dielectric interface problem
DMDD	✓Widest range of work function tuning ✓Most Flexible in metal/dielectric selection ✓Good Device performance	× Two dielectric deposition steps × Two gate deposition steps × Complex etching steps

IA																	0
H	IIA											IIIA	IVA	VA	VIA	VIIA	He
Li	Be											B	C	N	O	F	Ne
Na	Mg	IIIB	IVB	VB	VIB	VIIB		VIIIB			IB	IIB	Al	Si	P	S	Cl	Ar
K	Ca	N Sc	N Ti	N V	M Cr	M Mn	M Fe	M Co	P Ni	M Cu	N Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	N Y	N Zr	N Nb	M Mo	M Tc	M Ru	P Rh	P Pd	P Ag	N Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	N *La	N Hf	N Ta	M W	P Re	M Os	P Ir	P Pt	P Au	M Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	+Ac	Rf	Ha	Sg	Ns	Hs	Mt	110	111	112	113					

*Lanthanide Series	N Ce	N Pr	N Nd	Pm	N Sm	N Eu	N Gd	N Tb	N Dy	N Ho	N Er	N Tm	N Yb	N Lu
+Actinide Series	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

Fig. 1-1 The common elements in periodic table. The elements were marked with p, n and m according to its work function near the valence band, conduction band and mid-gap of silicon energy band, respectively.

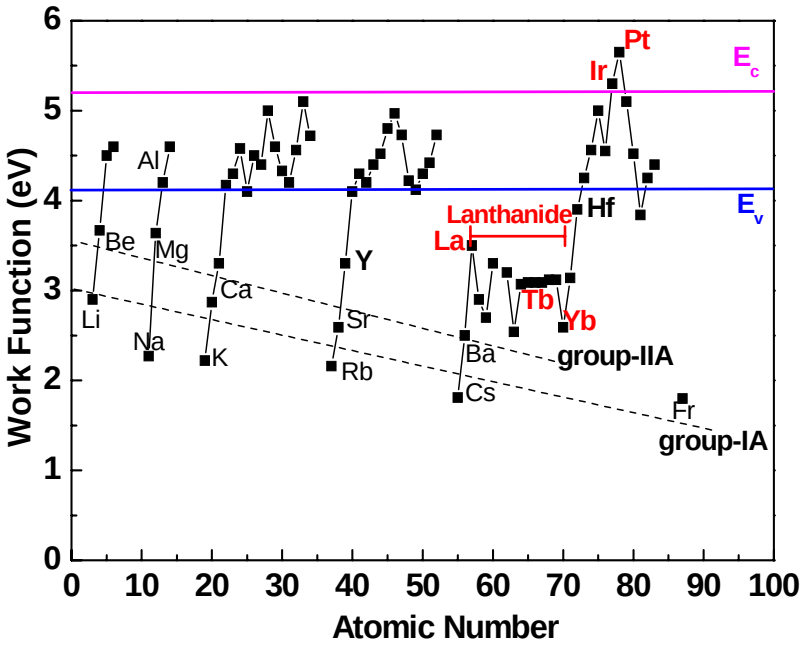


Fig. 1-2 Work Function variation versus atomic number

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	L_g: Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
	EOT: Equivalent Oxide Thickness [2]									
IS	Extended planar bulk (Å)	12	11	11	10	9	6.5	5	5	
Delete	UTB FD (Å)				~~9~~	~~8~~	7	6	5	5
	DG (Å)							8	7	6
	Gate Poly Depletion and Inversion-Layer Thickness [3]									
IS	Extended Planar Bulk (Å)	7.3	7.4	7.4	7.0	7.0	2.7	2.5	2.5	
Delete	UTB FD (Å)				~~4~~	~~4~~	4	4	4	4
	DG (Å)							4	4	4
	EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
IS	Extended Planar Bulk (Å)	19.3	18.4	18.4	17.0	16.0	9.2	7.5	7.5	
Delete	UTB FD (Å)				~~13~~	~~12~~	11	10	9	9
	DG (Å)							12	11	10
	$J_{g,limit}$: Maximum gate leakage current density [5]									
IS	Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	1.18E+03	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
Delete	UTB FD (A/cm^2)				~~7.73E+02~~	~~9.50E+02~~	1.22E+03	1.38E+03	2.07E+03	2.23E+03
	DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
	V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
	$V_{t,sat}$: Saturation Threshold Voltage [7]									
IS	Extended Planar Bulk (mV)	195	168	165	164	237	151	146	148	
Delete	UTB FD (mV)				~~169~~	~~168~~	167	170	166	167
	DG (mV)							181	184	185
	$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
IS	Extended Planar Bulk (µA/µm)	0.06	0.15	0.2	0.26	0.22	0.28	0.32	0.34	
Delete	UTB FD (µA/µm)				~~0.17~~	~~0.19~~	0.22	0.22	0.29	0.29
	DG (µA/µm)							0.1	0.11	0.11
	$I_{d,sat}$: effective NMOS Drive Current [9]									
IS	Extended Planar Bulk (µA/µm)	1.02E+03	1.13E+03	1.20E+03	1.21E+03	1.18E+03	2.05E+03	2.49E+03	2.30E+03	
Delete	UTB FD (µA/µm)				~~1496~~	~~1625~~	1815	2015	2037	2198
	DG (µA/µm)							1899	1932	2220
	Mobility Enhancement Factor for $I_{d,sat}$ [10]									
	Extended Planar Bulk	1.09	1.09	1.08	1.09	1.1	1.1	1.12	1.11	
Delete	UTB FD				~~1.06~~	~~1.06~~	1.06	1.06	1.05	1.05
	DG							1.05	1.04	1.05

Fig. 1-3 High-performance logic technology requirements (the international technology roadmap for semiconductors:2006 update)

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	Effective Ballistic Enhancement Factor [11]									
	Extended Planar Bulk	1	1	1	1	1	1	1	1	
Delete	UTB FD				~~1~~	~~1~~	1	1	1	1.1
	DG							1.17	1.25	1.31
	R_{sd}: Effective Parasitic series source/drain resistance [12]									
	Extended Planar Bulk (Ω-μm)	180	170	140	140	120	105	80	70	
Delete	UTB FD (Ω-μm)				~~155~~	~~140~~	125	110	90	75
	DG (Ω-μm)							110	100	90
	$C_{g,ideal}$: Ideal NMOS Device Gate Capacitance [13]									
IS	Extended Planar Bulk (F/μm)	5.73E-16	5.25E-16	4.69E-16	4.46E-16	4.31E-16	6.78E-16	7.39E-16	6.41E-16	
Delete	UTB FD (F/μm)				~~5.84E-16~~	~~5.75E-16~~	5.65E-16	5.52E-16	5.37E-16	4.98E-16
	DG (F/μm)							4.60E-16	4.39E-16	4.48E-16
	$C_{g,total}$: Total gate capacitance for calculation of CV/I [14]									
IS	Extended Planar Bulk (F/μm)	8.13E-16	7.65E-16	6.99E-16	6.56E-16	6.01E-16	8.28E-16	8.59E-16	7.51E-16	
Delete	UTB FD (F/μm)				~~9.04E-16~~	~~7.55E-16~~	7.35E-16	6.92E-16	6.67E-16	6.18E-16
	DG (F/μm)							6.50E-16	6.29E-16	6.28E-16
IS	τ = CV/I: NMOSFET intrinsic delay (ps) [15]	0.87	0.74	0.64	0.54	0.51	0.4	0.34	0.29	0.25
IS	1/τ: NMOSFET intrinsic switching speed (GHz) [16]	1149	1351	1563	1852	1961	2500	2941	3448	4000

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

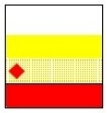


Fig. 1-4 High-performance logic technology requirements (continued) (the international technology roadmap for semiconductors:2006 update)

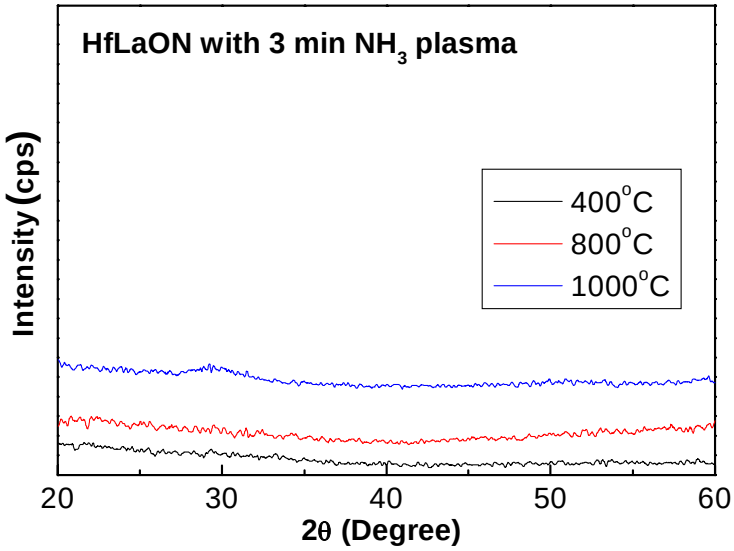


Fig. 1-5 Grazing incident XRD spectra of HfLaON with NH_3 plasma after different RTA annealing. In contrast to the HfLaO case, the HfLaON stays amorphous state after 1000°C RTA.

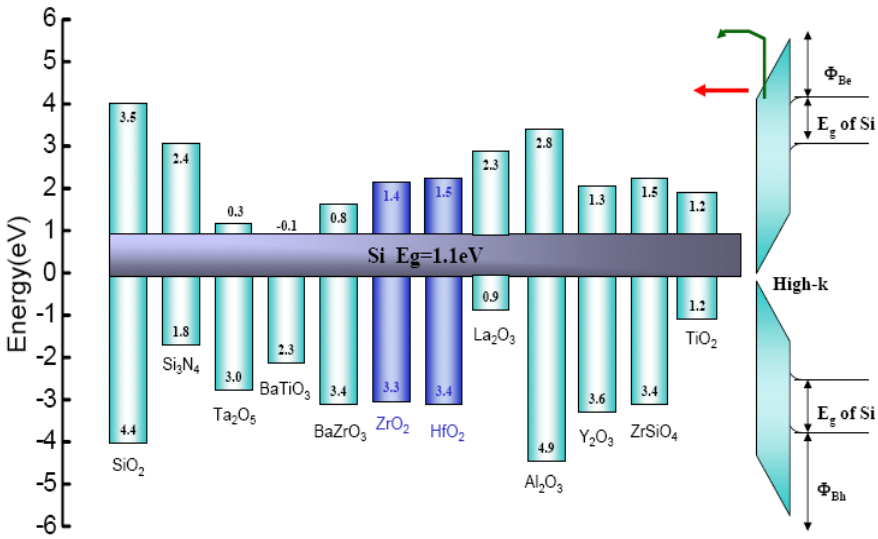


Fig. 1-6 The band offset of popular high-κ materials.

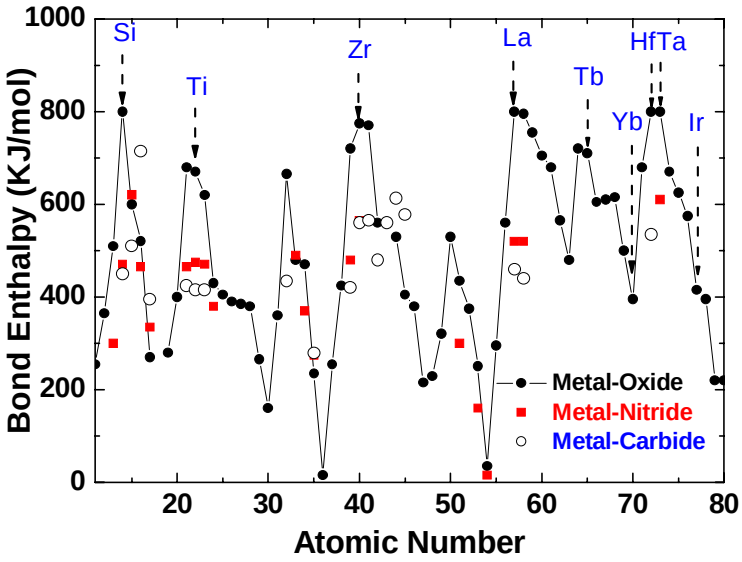


Fig. 1-7 Bond enthalpy for M-O, M-N and M-C in the Periodic Table for thermal stability prediction, with M-O>M-N>M-C in general. The bond enthalpy peaked at La, Hf and Ta.

Chapter 2

HfLaON *n*-MOSFETs Using Low Work Function $HfSi_x$ Gate

2.1 Introduction

Metal gates and high-κ gate dielectrics are necessary for *C*MOSFETs at the 45 nm nodes and beyond [2.1]-[2.15], to reduce the DC power consumption from the gate current and continue the VLSI scaling. This poses a difficult technological challenge in that the large threshold voltage (V_t) that results from Fermi-level pinning is opposite to the trend needed for device scaling. To avoid this requires appropriate choices of the metal-gate work-function and high-κ dielectric - to reduce the pinning to achieve the required low V_t. Previously, we have shown that Fermi-level pinning can be reduced, even after surface plasma nitridation, by adding La_2O_3 to HfO_2, to produce the gate dielectric $Hf_{0.5}La_{0.5}ON$ at 1.6 nm equivalent oxide thickness (EOT). Thus, a relatively low V_t can be achieved with a conventional TaN gate [2.15]. Here we report the use of a low work-function Fully Silicided (FUSI) $HfSi_x$ gate for $Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs, at a scaled EOT of 1.2 nm and reduced La composition of 30%. This gate yields a more negative flat band voltage (V_{fb}) than does a TaN gate. The resulting MOSFETs show a V_t of 0.18 V, a low leakage current of 9.2×10^{-4} A/cm^2 at 1 V above V_{fb} and 1.2 nm EOT, with an electron mobility of 215 cm^2/V-s. These devices can endure a rapid thermal annealing (RTA) temperature of 1000^{o}C, common in current poly-Si gate technology.

2.2 Experimental procedure

We used the 4-inch p-type Si wafers in these experiments. After a standard RCA clean, the $Hf_{0.7}La_{0.3}O$ was deposited on Si wafers by physical vapor deposition. Then the $Hf_{0.7}La_{0.3}O$ surface was exposed to nitrogen plasma to form the $Hf_{0.7}La_{0.3}ON$ gate dielectric. Amorphous Si of 5 nm thickness was deposited on the $Hf_{0.7}La_{0.3}ON$ followed by a PVD deposition of 20 nm thick Hf. To prevent Hf oxidation, a 30 nm thick Mo was subsequently deposited above the Hf/Si/$Hf_{0.7}La_{0.3}ON$ to form n-MOS capacitors. For *n*-MOSFETs, an additional 150 nm thick amorphous-Si was deposited to avoid ion implantation damage through the gate. The n^+ source-drain regions were formed by using a 35 KeV phosphorus ion implantation (at a 5×10^{15} cm^{-2} dose) followed by RTA activation at 1000°C for 5 sec. (Note that the FUSI $HfSi_x$ gate was formed at a high RTA temperature, similar to Ir_3Si[2.14], which is different from a conventional low temperature salicide process.) For comparison, TaN gates were also deposited on the $Hf_{0.7}La_{0.3}ON$ to form the *n*-MOS capacitors. The fabricated devices were characterized by *C-V* and *I-V* measurements using an HP4284A precision LCR meter and HP4156 semiconductor parameter analyzer, respectively.

2.3 Result and Discussion

In Figures 2-1 and 2-2, we show the *C-V* and *J-V* characteristics of $HfSi_x$/$Hf_{0.7}La_{0.3}ON$ and control TaN/$Hf_{0.7}La_{0.3}ON$ capacitors respectively. For comparison, the characteristics of a capacitor with a TaN gate on $Hf_{0.7}La_{0.3}ON$ are included. The FUSI $HfSi_x$ gate without poly-Si

depletion – as formed by Hf deposition on thin 5 nm amorphous-Si at 1000°C RTA – produces devices with a high capacitance density, close to those using a TaN gate. However, the V_{fb} of the $HfSi_x$ gate is more negative than for the TaN gate, which is needed for low V_t operation. An EOT of 1.2 nm was found using a quantum-mechanical (QM) *C-V* simulation. A low $\phi_{m\text{-}eff}$ of 4.33 eV was obtained from a V_{fb}-*EOT* plot for the $HfSi_x/Hf_{0.7}La_{0.3}ON$ devices, making them suitable for *n*-MOS applications. The leakage current of 9.2×10^{-4} A/cm^2 (at 1 V beyond V_{fb}) is ~5 orders of magnitude lower than that of SiO_2 at a 1.2 nm EOT. This low leakage current is due to the high-κ $Hf_{0.7}La_{0.3}ON$, highlighting the good thermal stability of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ gate structure after a 1000°C RTA. The higher leakage current at low voltages using TaN gate than that of $HfSi_x$ may be due to the sputter-induced damage to $Hf_{0.7}La_{0.3}ON$ gate dielectric. Thus, both low $\phi_{m\text{-}eff}$ and low gate dielectric leakage current can be achieved in $HfSi_x/Hf_{0.7}La_{0.3}ON$ MOS capacitors.

Figures 2-3 and 2-4 show the I_d-V_d and I_d-V_g transistor characteristics of the 1.2 nm EOT $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs. A small V_t of only 0.18 V was measured from the linear I_d-V_g plot - this is due to the low $\phi_{m\text{-}eff}$ of 4.33 eV found from the *C-V* measurements.

The electron mobility as a function of effective electric field for the $HfSi_x/Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs is shown in Fig. 2-5, where the data was derived from measured I_d-V_g curves. High peak electron mobility of 215 cm^2/V-s is obtained, at a small EOT of 1.2 nm. In Table 1 we summarize and compare the important transistor characteristics for various

metal-gate/high-κ *n*-MOSFETs. The merits of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs are the small EOT of 1.2 nm, low V_t of 0.18 V, good peak mobility of 215 cm^2/V-s and simple high-temperature FUSI processing.

2.4 Conclusion

We have found good performance in terms of V_t and mobility for $Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs at 1.2 nm EOT using a low work-function and high-temperature-stable $HfSi_x$ gate. The self-aligned and gate-first $HfSi_x$/HfLaON *n*-MOSFETs have the advantages of simple high temperature FUSI processing and compatibility with current VLSI lines.

Table 2-1 Comparison of device parameters for metal-gate/high-κ *n*-MOSFETs.

High-κ	Metal Gate	EOT (nm)	V_t (V)	Process Temp.
HfLaON This work	**$HfSi_x$**	**1.2**	**0.18**	**1000°C**
HfAlON [2.11]	Yb_xSi	1.7	0.1	Low Temp. FUSI
HfTaO [2.10]	TaN	1.6	-	1000°C
HfSiON [2.13]	TaC	1.2	~0.4	1000°C
HfSiON [2.12]	NiSi	1.5	0.5	Low Temp. FUSI
HfSiON [2.9]	$NiSi_2$	1.7	0.47	Low Temp. FUSI

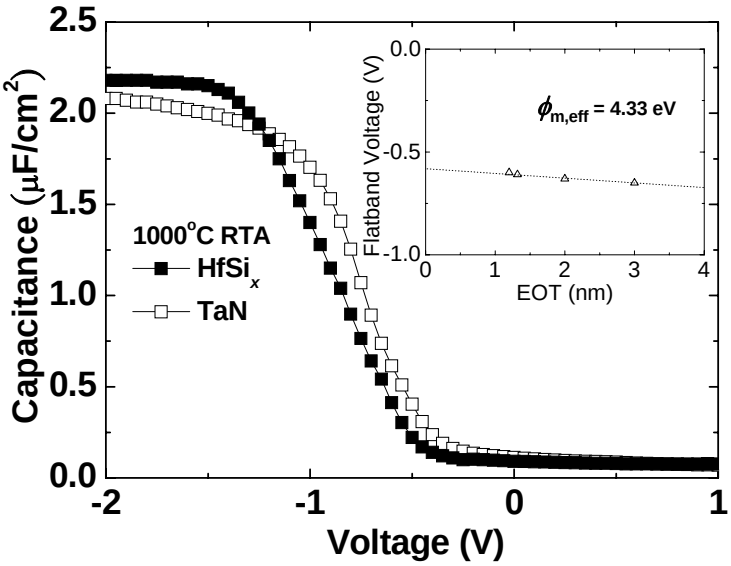


Fig. 2-1 *C-V* characteristics of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ *n*-MOS capacitors, after a 1000°C RTA. The inserted figure is a V_{fb}-*EOT* plot.

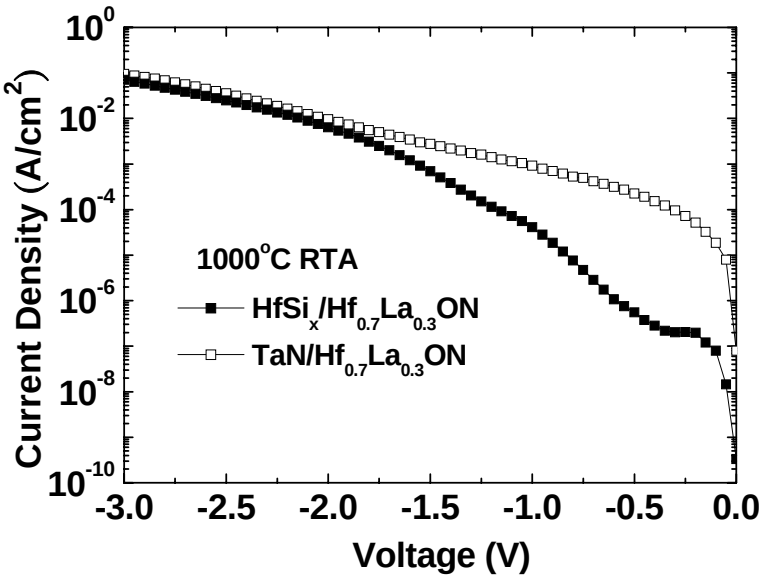


Fig. 2-2 *J-V* characteristics of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ *n*-MOS capacitors, after a 1000°C RTA.

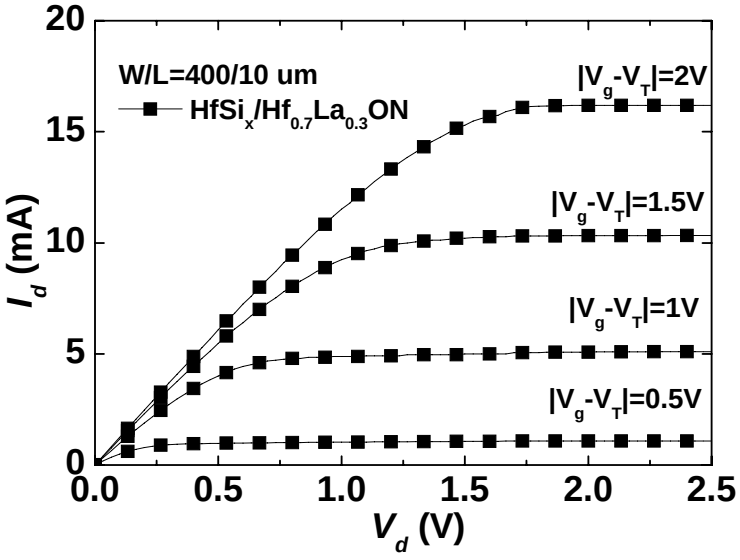


Fig. 2-3 The I_d-V_d characteristics of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs.

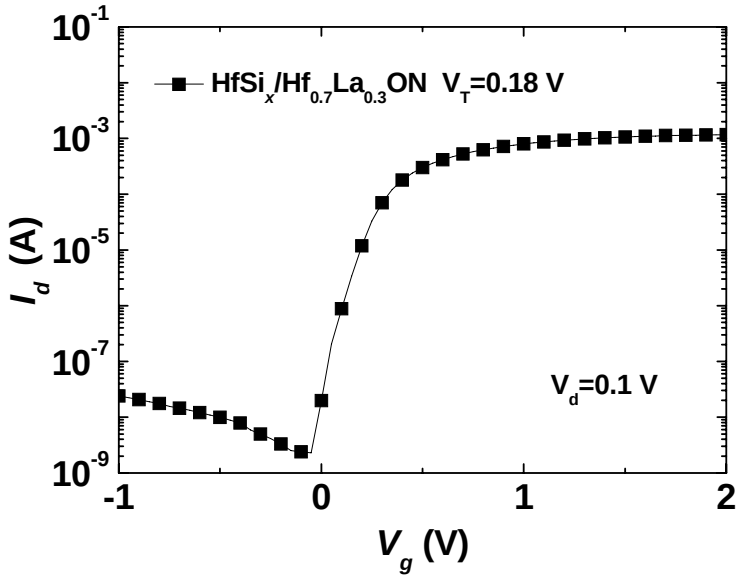


Fig. 2-4 The I_d-V_g characteristics of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs.

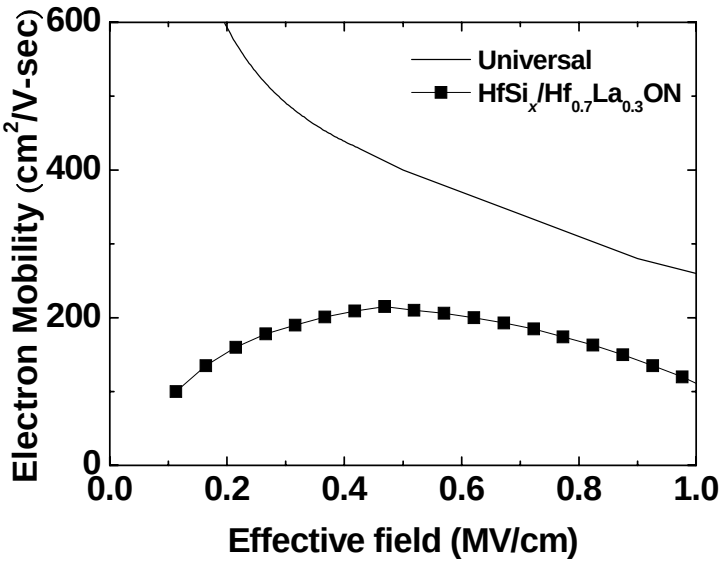


Fig. 2-5 The electron mobility vs. effective electric field for the $HfSi_x/Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs.

Chapter 3

HfLaON *p*-MOSFETs Using High Work Function Ir_3Si Gate

3.1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS), the metal-gate/high-κ is the required technology for the future generation *C*-MOSFETs to reduce the undesired large gate leakage current and continue the gate oxide scaling [3.1]-[3.11]. Recently, the HfSiON gate dielectric is a promising candidate beyond SiON with merits of high κ value, low gate leakage current and similar amorphous structure after 1000°C RTA for VLSI process. However, the lack of a high work function gate for HfSiON *p*-MOSFETs is the challenge since only Ir (5.27 eV) and Pt (5.65 eV) in the Periodic Table [3.8] have the needed work function larger than target 5.2 eV. The other problem of HfSiON is the relative lower κ of 10~14 that causes limited scaling capability. In this paper, we developed the high temperature stable Ir_3Si/HfLaON *p*-MOSFET to address above issues. The novel HfLaON dielectric can preserve the amorphous structure after 1000°C RTA and is similar to HfSiON but with significantly higher κ value. Using high work-function Ir_3Si gate electrode [3.8]-[3.9], the *p*-MOSFETs show good device integrity of low leakage current of 1.8×10^{-5} A/cm^2 at 1 V above flat band voltage (V_{fb}), high hole mobility of 84 cm^2/Vs and good 1000°C RTA thermal stability at equivalent oxide thickness (EOT) of 1.2 nm. These results are compatible with or

better than the best reported metal-gate/high-κ *p*-MOSFETs [3.1]-[3.7].

3.2 Experimental procedure

Standard N-type Si wafers with resistivity 1~10 Ω-cm (10^{15}-10^{16} cm^{-3} doping level) were used in this study. After standard RCA clean, the HfLaO was deposited on N-type Si wafers by PVD and post deposition anneal (PDA). The HfLaON was formed by applying NH_3 plasma surface nitridation on HfLaO. Then 5 nm amorphous Si and 20 nm Ir was subsequently deposited on HfLaON and RTA annealed at 1000°C for 5 sec to form the MOS capacitors. For *p*-MOSFETs, additional thick TaN capping layer is added on Ir/Si/HfLaON to prevent subsequent ion implantation penetration, where the Ir_xSi gate was formed during RTA. After patterning, self-aligned B^+ implantation was applied at 25 KeV and source-drain doping was activated at 1000°C RTA for 5 sec. The fabricated *p*-MOSFETs were characterized by *C*-*V* and *I*-*V* measurements.

3.3 Result and Discussion

In Figures 3-1 and 3-2 we show the *C*-*V* and *J*-*V* characteristics of Ir_3Si/HfLaON and TaN/HfLaON capacitors respectively. For comparison, the characteristics of a capacitor with a TaN gate on HfLaON are included. The FUSI Ir_3Si gate without poly-Si depletion – as formed by Ir deposition on thin 5 nm amorphous-Si at 1000°C RTA – produces devices with a high capacitance density, close to those using a TaN gate. However, the V_{fb} of the Ir_3Si gate is more positive than for the TaN gate, which is needed for low V_t operation. An EOT of 1.2 nm

was found using a quantum-mechanical (QM) *C-V* simulation. However, unexpected V_{fb} roll-off is observed which will cause high V_t and result in poor device performance. The leakage current of 5.29×10^{-4} A/cm^2 (at 1 V beyond V_{fb}) is ~5 orders of magnitude lower than that of SiO_2 at a 1.2 nm EOT. This low leakage current is due to the high-κ HfLaON, highlighting the good thermal stability of the Ir_3Si/HfLaON gate structure after a 1000°C RTA. Thus, only low gate dielectric leakage current can be achieved in Ir_3Si/HfLaON MOS capacitors.

Figures 3-3 and 3-4 show the I_d-V_d and I_d-V_g transistor characteristics of the 1.2 nm EOT Ir_3Si/HfLaON *p*-MOSFETs. A high V_t of 0.25 V was measured from the linear I_d-V_g plot - this is due to the roll-off of V_{fb} that can be found from the *C-V* measurements.

The hole mobility as a function of effective electric field for the Ir_3Si/HfLaON *p*-MOSFETs is shown in Fig. 3-5, where the data was derived from measured I_d-V_g curves. High peak hole mobility of 86 cm^2/V-s could still be obtained, at a small EOT of 1.2 nm. The merits of the Ir_3Si/HfLaON *p*-MOSFETs are the small EOT of 1.2 nm, good peak mobility of 215 cm^2/V-s and simple high-temperature FUSI processing.

3.4 Conclusion

Good device integrity of Ir_3Si/HfLaON p-MOSFETs is shown by the very low leakage current, good hole mobility and 1000°C thermal stability. However, poor V_{fb} and high V_t is observed at 1.2nm EOT. This gate-first and self-aligned process is fully comparable to current

VLSI fabrication lines.

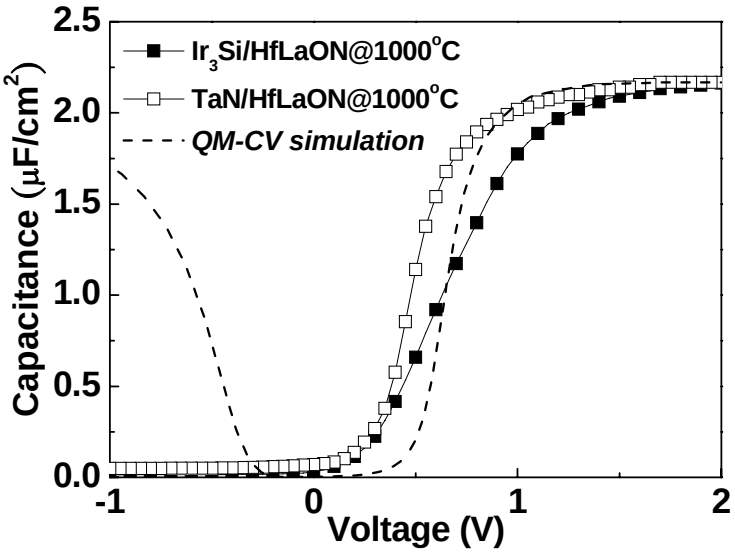


Fig. 3-1 *C-V* characteristics of Ir_3Si/HfLaON and TaN/HfLaON capacitors respectively, after a 1000°C RTA.

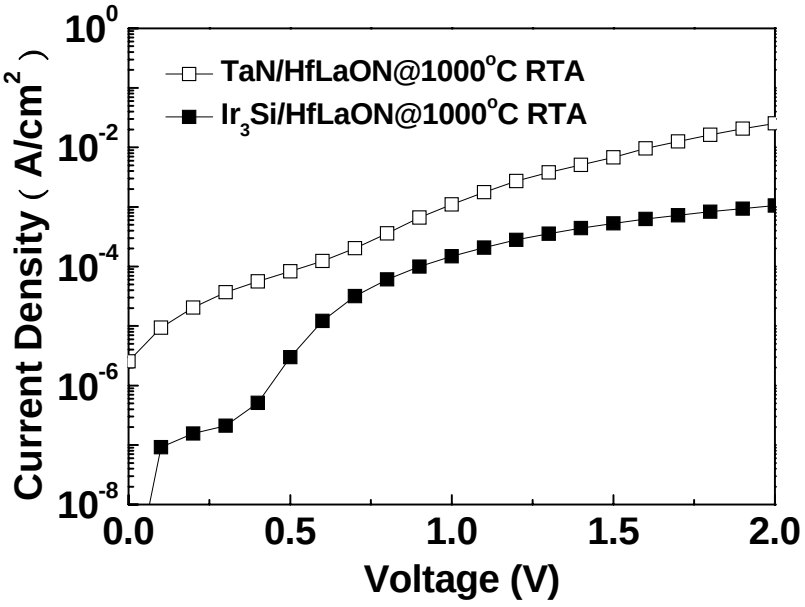


Fig. 3-2 *J-V* characteristics of Ir_3Si/HfLaON and TaN/HfLaON capacitors respectively, after a 1000°C RTA.

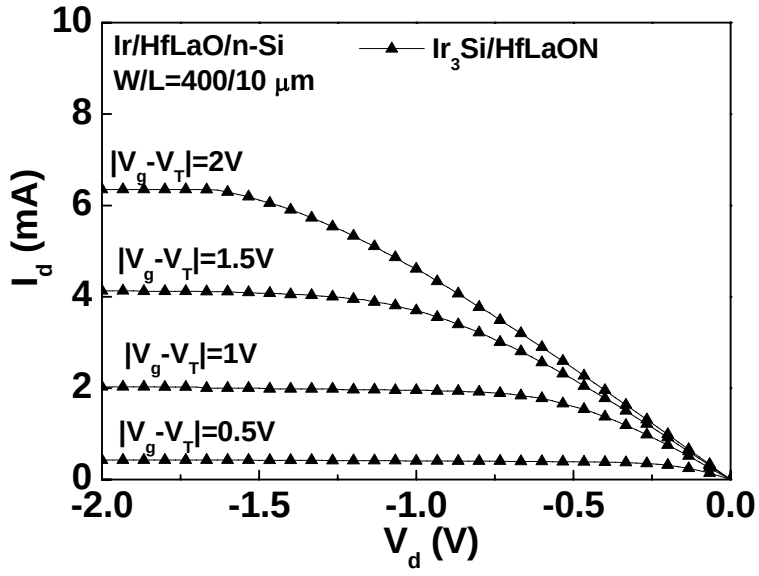


Fig. 3-3 The I_d-V_d characteristics of the Ir_3Si/HfLaON *p*-MOSFETs.

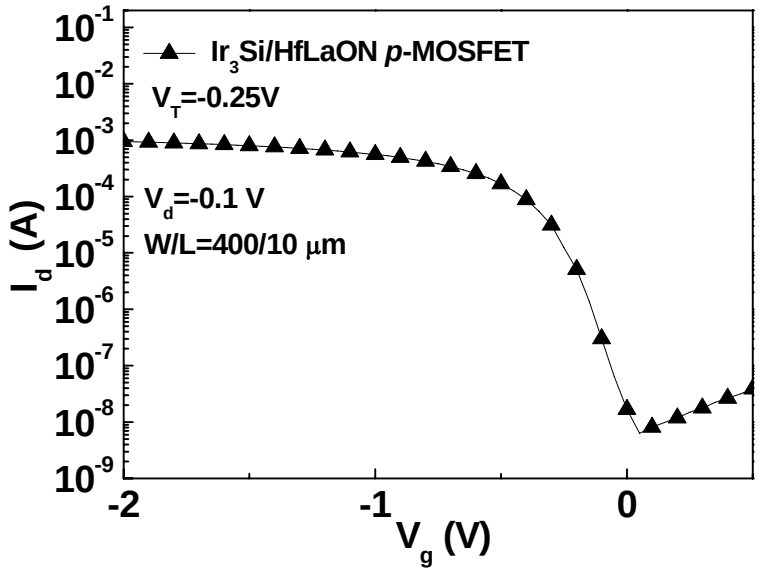


Fig. 3-4 The I_d-V_g characteristics of the Ir_3Si/HfLaON *p*-MOSFETs.

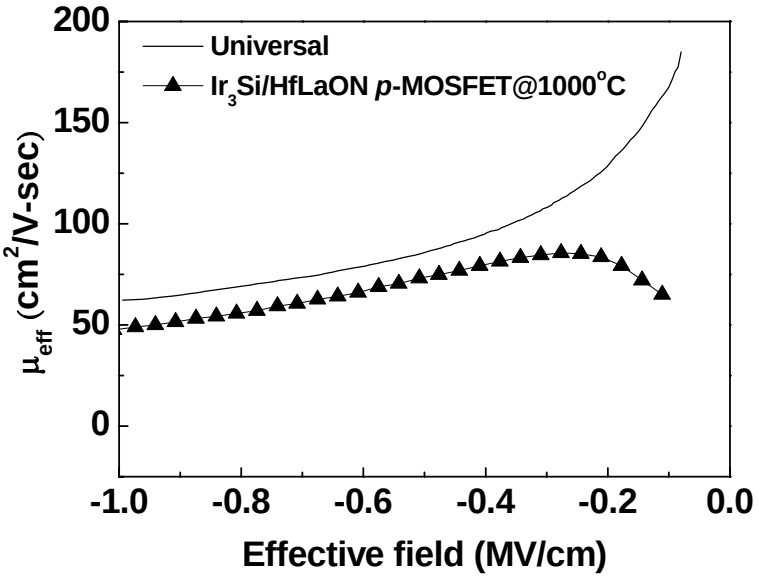


Fig. 3-5 The hole mobility vs. effective electric field for the Ir_3Si/HfLaON *p*-MOSFETs.

Chapter 4

High Work-Function Ir/HfLaO *p*-MOSFETs Using Low-Temperature-Processed Shallow Junction

4.1 Introduction

To reduce the unwanted gate leakage current and continue the logic device evolution, metal-gates and high-κ technology are required for *C*-MOSFETs used for 45 nm node and beyond [4.1]-[4.19]. The major challenge for metal-gate/high-κ *C*-MOSFETs is the undesired high threshold voltage (V_t); this is especially difficult for *p*-MOS requiring high effective work-function ($\phi_{m\text{-}eff}$) gate, since only Ir and Pt in the Periodic Table has the needed >5.2 eV values [4.13]. Furthermore, Ir can be patterned by Reactive-Ion etching (RIE) [4.20]-[4.21] but not the case for Pt, which makes Ir the very few choice for high $\phi_{m\text{-}eff}$ *p*-MOS. Previously, we showed that the self-aligned Ir_3Si/HfLaON *p*-MOSFET [4.15] has the required low V_t of -0.1 V by using high $\phi_{m\text{-}eff}$ Ir_3Si gate of 5.08 eV at 1.6 nm effective oxide thickness (EOT). This is achieved even after 1000°C rapid thermal annealing (RTA) used for source-drain doping activation after ion implantation. In this paper, we have studied the *p*-MOSFET with EOT scaling to 1.2 nm. Unfortunately, the V_t of Ir_3Si/HfLaON *p*-MOS increases largely to -0.25 V. To address this V_t increase by flat-band voltage (V_{fb}) roll-off [4.18], we have developed a novel low temperature processed Ir/HfLaO *p*-MOSFET using solid-phase

diffused (SPD) shallow junction. This self-aligned and gate-first *p*-MOSFET showed proper $\phi_{m\text{-}eff}$ of 5.3 eV, low V_t of +0.05 V, high mobility of 90 cm^2/Vs at -0.3 MV/cm and small 85°C negative bias-temperature instability (NBTI) of 20 mV at 10 MV/cm for 1 hr. Besides, the achieved p^+/n contact junction depth is in the range of 9.6~20 nm and useful for sub-90 nm regime [4.22]. In comparing with 1000°C RTA-annealed Ir_3Si/HfLaON *p*-MOSFET, this achieved good device integrity in Ir/HfLaO is attributed to the using novel low-temperature (≤900°C) ultra-shallow junction process, where the reaction at high-κ interface decreases exponentially followed by Arrhenius law. These results compare well with the best report metal-gate/high-κ *p*-MOSFETs [4.1]-[4.19], with lower V_t, smaller EOT, similar simple self-aligned and gate-first process for VLSI IC fabrication.

4.2 Experimental Procedure

Standard n-type Si wafers with resistivity of 1-10 Ω-cm were used in this study. After regular RCA cleaning, the HfLaO was deposited on n-Si substrate by physical vaper deposition (PVD) and post-deposition annealing (PDA). The La content in HfLaO is controlled to be 50%. Then, 20 nm Ir and 150 nm TaN were deposited by PVD. After gate patterning, the self-aligned 5 nm Ga or 10-nm-Ni/5-nm-Ga, covered with 100 nm SiO_2, was deposited for *p*-MOS, followed by 550~900°C RTA SPD. Finally, source-drain metal contact was added to reduce the source-drain contact resistance in Ga doped case. For comparison, the Ir_3Si/HfLaON *p*-MOSFETs were also fabricarted using 25 keV B^+ implantion with 5×10^{15}

cm^{-2} dose and followed by 1000°C RTA dopant activation, where the HfLaON was formed by applying NH_3 plasma surface nitridation on HfLaO. More detailed fabricateion process can be found elsewhere [4.15]. The fabricated *p*-MOSFETs were characterized by capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements using an HP4284A precision LCR meter and an HP4156 semiconductor parameter analyzer, respectively.

4.3 Result and Discussion

4.3.1 V_{fb} roll-off issue at thinner EOT:

Figures 4-1(a) and 4-1(b) show the *C-V* characteristics of Ir_3Si/HfLaON and Ir/HfLaO *p*-MOSFETs after 1000°C and 850°C RTA, respectively. Although proper high V_{fb} is obtained in Ir_3Si/HfLaON *p*-MOS at 1.6 nm EOT, the V_{fb} is largely decreased with further down-scaling the EOT to 1.2 nm. Here the 1.2 nm EOT is confirmed from the quantum-mechanical (QM) *C-V* simulation. In sharp contrast, the Ir/HfLaO *p*-MOSFETs after 850°C RTA did not show such lower V_{fb} effect at thinner 1.2 nm EOT. Similar band-edge work-function for *p*-MOS was also reported using Pt electrode [4.14]. It is important to notice that the measured *C-V* curve of 1000°C RTA-annealed Ir_3Si/HfLaON *p*-MOS is deviated from the ideal QM *C-V* values, but closer agreement is reached in 850°C RTA-annealed Ir/HfLaO *p*-MOS. This result suggests that the interface charges may be one of the possible reasons to cause V_{fb} roll-off at thinner 1.2 nm EOT of Ir_3Si/HfLaON devices. The possible derivation for

interface oxide charges may come from the charged oxide vacancies and dangling bonds of non-stoichiometric oxides (x<2) caused by unavoidable interface reaction and inter-diffusion:

$$Si + HfO_2 \xrightarrow[\Delta]{} SiO_x + HfO_{2-x} \quad (1)$$

Such reactions are possible at high temperature owing to the similar bond enthalpies of 800 and 802 kJ/mol for respective SiO_2 and HfO_2 [4.13]. Although such silicate formation can be decreased by inserting interfacial SiO_2, unfortunately this will increase the EOT and degrade the required high κ value for achieving low leakage current.

To exam this assumption, we have measured the interface trap density (D_{it}) of gate dielectrics with different RTA temperature. Figure 4-2 shows the measured charge-pumping current as a function of frequency. Linear dependences of the current on frequency were measured. The D_{it} of 9.7×10^{11} $cm^{-2}eV^{-1}$ was obtained for 1000°C RTA processed HfLaON from Groeseneken's formula [4.23], which decreases to only 3.6×10^{11} $cm^{-2}eV^{-1}$ for 850°C RTA thermal-cycled HfLaO. Such decreased D_{it} is very important to improve the device performance in following sections.

On the other hand, the Ir/HfLaO device failed completely at 1000°C, this is due to the inevitable metal diffusion [4.17] of Ir into HfLaO at higher temperatures. Similar Ir diffusion into HfO_2 was reported and confirmed by SIMS measurement [4.2]. Although this metal diffusion through oxide can be decreased by using surface nitrided HfLaON, it still cannot meet the 1000°C RTA requirement for source-drain doping activation. To address this issue,

we have developed a low temperature shallow junction process for high-κ *p*-MOSFETs.

4.3.2 Low temperature shallow junction formed by SPD:

Figures 4-3(a) and 4-3(b) show the *J-V* characteristics of p^+/n junctions formed by SiO_2/Ga and SiO_2/Ni/Ga SPD, respectively. Good p^+/n junction characteristics are obtained using SiO_2/Ga SPD at 900°C RTA with reasonable ideality factor and low leakage current close to B^+ implanted controlled sample at 1000°C RTA. However, this process has relatively high sheet resistance of ~1050 Ω/sq. due to the ultra shallow junction of 9.6 nm at 10^{18} cm^{-3} concentration [4.24] shown in the Secondary Ion Mass Spectroscopy (SIMS) profile of Fig. 4-4. The improved ideality factor from 1.7 to 1.5 was obtained with increasing RTA time from 10 to 20 sec. This suggests the deeper junction to give better diode characteristics, which may be related to the reduced residue Ga in the depletion region.

To further improve the sheet resistance, the Ni-silicide is used. The incorporate Ni into Ga decreases the sheet resistance to only 10 Ω/sq., where good ideality factor and reverse leakage current are also obtained. The degradation of Ni/Ga formed junction in both ideality factor and leakage current at 850°C may be due to the deformation of NiSi. From the SIMS profile shown in Fig. 3, the adding Ni to Ga SPD causes the Ni-Ga co-diffusion and silicide formation. A junction depth of 20 nm is obtained, which was defined at 10^{18} cm^{-3} [4.24]. The degraded ideality factor from 1.36 to 1.8 with increasing RTA temperature from 700 to 850°C may be due to the excessive Ni within the p^+/n junction.

4.3.3 Device characteristics of low temperature SPD formed Ir/HfLaO p-MOS:

Based on the above shallow junctions, we have fabricated the Ir/HfLaO *p*-MOSFETs. The high-κ HfLaO was subjected to a PDA of 850°C RTA in nitrogen ambient to reduce the oxide defects. Figures 4-5(a) and 4-5(b) are the *J-V* and V_{fb}-*EOT* characteristics of TaN/Ir on HfLaO devices, respectively. Here different HfLaO thickness was used to extract the V_{fb}. At 1.2 nm EOT, low leakage current of 2.4×10^{-4} is obtained at 1 V for *p*-MOS capacitors. However, the Ir/HfLaO *p*-MOS devices were failed after 1000°C RTA due to Ir metal diffusion through high-κ [4.2]-[4.16]. Therefore, the decreasing temperature to ≤900°C is vitally important to use the high work-function Ir electrode. A proper $\phi_{m\text{-}eff}$ of 5.3 eV is obtained for Ir/HfLaO device that is close to the ideal required band edge value of 5.2 eV used for *p*-MOSFETs.

Figure 4-6 shows the transistor I_d-V_d characteristics as a function of $|V_g\text{-}V_t|$ for Ir/HfLaO *p*-MOSFETs with 900°C RTA-annealed SiO_2/Ga SPD and 700°C RTA-annealed SiO_2/Ni/Ga contacts. For comparison, the I_d-V_d characteristics of Ir_3Si/HfLaON *p*-MOSFETs with B^+ implant junction at 1000°C RTA are also shown for comparison. At 1.2 nm EOT, the well-behaved I_d-V_d curves of these *p*-MOSFETs show good transistors performance using the SPD junctions.

Figure 4-7 shows the I_d-V_g characteristics of Ir/HfLaO and Ir_3Si/HfLaON *p*-MOSFETs. For Ir/HfLaO *p*-MOSFETs, a small V_t as low as +0.05 V is obtained from the linear I_d-V_g plot

at 1.2 nm EOT. This is consistent with the large $\phi_{m\text{-}eff}$ of 5.3 eV from the V_{fb}-*EOT* plot shown in Fig. 4-5(b). For Ir_3Si/HfLaON *p*-MOSFETs, the V_t of -0.25V is obtained. This is due to the V_{fb} *roll-off* shown in Fig. 1(a) that is attributed to the charged oxide vacancies in *eq.* (1) and higher D_{it} value measured by charge-pumping current caused by higher 1000°C RTA.

Figure 8 shows the extracted hole motility versus gate electric field from the measured I_d-V_g characteristics for Ir/HfLaO and Ir_3Si/HfLaON *p*-MOSFETs using SPD and B^+ implanted junctions at 1.2 nm EOT. High peak hole mobility of 90 at -0.3 MV/cm and 86 cm^2/V-s at -0.33 MV/cm is obtained for Ir/HfLaO and Ir_3Si/HfLaON *p*-MOSFETs respectively, which is comparable with the published data in the literature [1]-[19]. For Ir_3Si/HfLaON device, the sub-threshold swing (SS) is 81 mV/dec. For Ir/HfLaO with Ga/Ni SPD case, a smaller SS of 74 mV/decade is obtained that is is close to the reported value of LaO-capped HfSiON [4.19]. The improved SS is related to the measured lower D_{it} value shown in Fig. 4-2.

The reliability is an important factor of high-κ MOSFETs. We have measured the NBTI as shown in Fig. 4-9, under the condition of 10 MV/cm bias for 1 hr at 85°C. Here the stress field is defined as $(V_g\text{-}V_t)$/CET; CET is the capacitance equivalent thickness. Small NBTI of 20 and 26 mV are measured for Ir/HfLaO and Ir_3Si/HfLaON *p*-MOSFETs at 1.2 nm EOT after 1 hr stress at 85°C, respectively. These small NBTI value for 1000°C RTA-annealed Ir_3Si/HfLaON *p*-MOSFETs is attributed to the amorphous structure HfLaON [4.15].

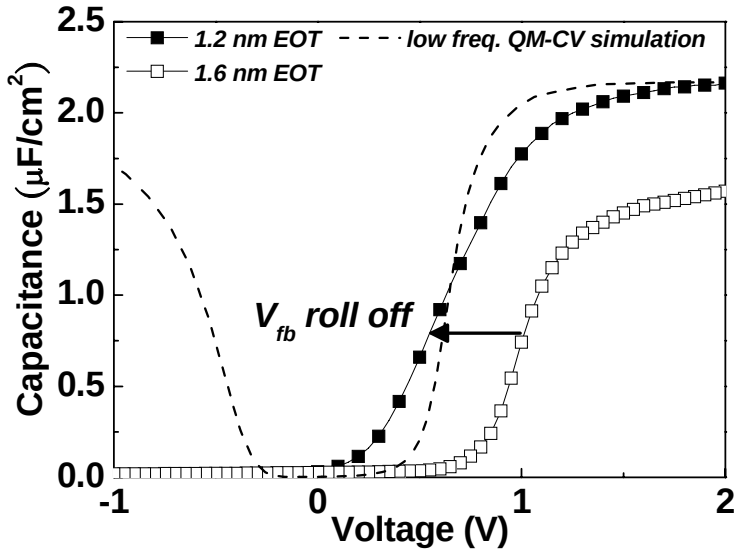
Table 4-1 summarizes and compares the important device parameters of metal-gate/high-k *p*-MOSFETs. The merits of self-aligned Ir/HfLaO *p*-MOSFETs with SPD shallow contact junction are the proper $\phi_{m\text{-}eff}$ of 5.3 eV, low V_t of +0.05 V, high mobility of 90 cm^2/V-s at -0.3 MV/cm, and small BTI of 20 mV (85°C, 10 MV/cm & 1 hr). These results are comparable with or better than the best reported data for metal-gate/high-κ *p*-MOSFETs, with small 1.2 nm EOT, similar simple self-aligned and gate-first process for VLSI IC fabrication.

4.4 Conclusion

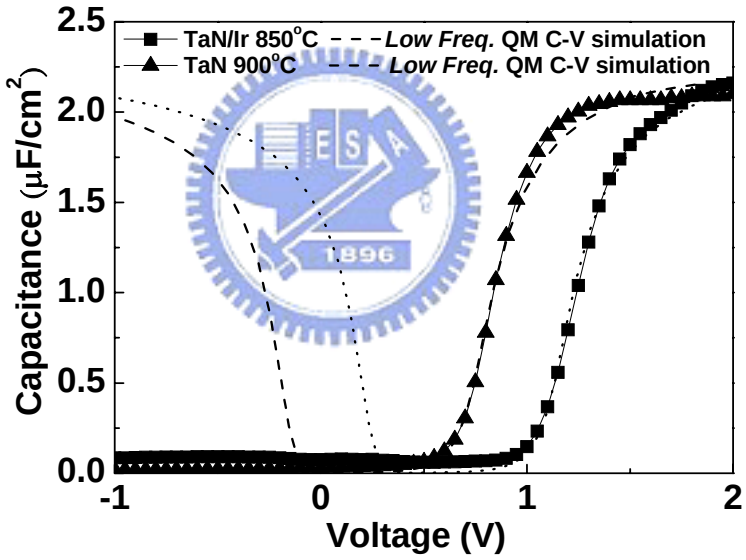
Good device performance of Ir/HfLaO *p*-MOSFETs is shown by the high $\phi_{m\text{-}eff}$ of 5.3 eV, low V_t of +0.05 V, shallow junction of 9 or 20 nm, high hole mobility of 90 cm^2/V-s at -0.3 MV/cm, and small BTI <20 mV (85°C, 10 MV/cm & 1 hr) with advantage of self-aligned and gate-first process for VLSI line.

Table 4-1 Comparison of important device parameters among metal-gate/high-κ *p*-MOSFETs.

High-κ	Metal-Gate	EOT (nm)	$\phi_{m\text{-}eff}$ (eV)	V_t (V)	Process Temp.	Mobility (cm^2/Vs)
This work HfLaO	**Ir**	**1.2**	**5.3**	**+0.05**	**≤850°C SPD**	**90**
Chapter 3 HfLaON	**Ir_3Si**	**1.2**	**5.0**	**-0.25**	**1000°C**	**86**
HfLaON [4.15]	Ir_3Si	1.6	5.08	-0.1	1000°C	84
HfAlON [4.16]	Ir_xSi	1.7	4.9	-0.29	950°C	80
HfSiON [4.11]	$Ni_{31}Si_{12}$	1.5	~4.8	-0.4	Low Temp. FUSI	~70
HfSiON [4.9]	NiSiGe	1.3	-	-0.5	Low Temp. FUSI	70
HfSiON [4.6]	Ni_3Si	1.7	4.8	-0.69	Low Temp. FUSI	65



(a)



(b)

Fig. 4-1 *C-V* characteristics of (a) Ir_3Si/HfLaON *p*-MOSFETs after 1000°C RTA and (b) Ir/HfLaO *p*-MOSFETs after 850°C RTA. The C-V characteristics were measured at 500 kHz.

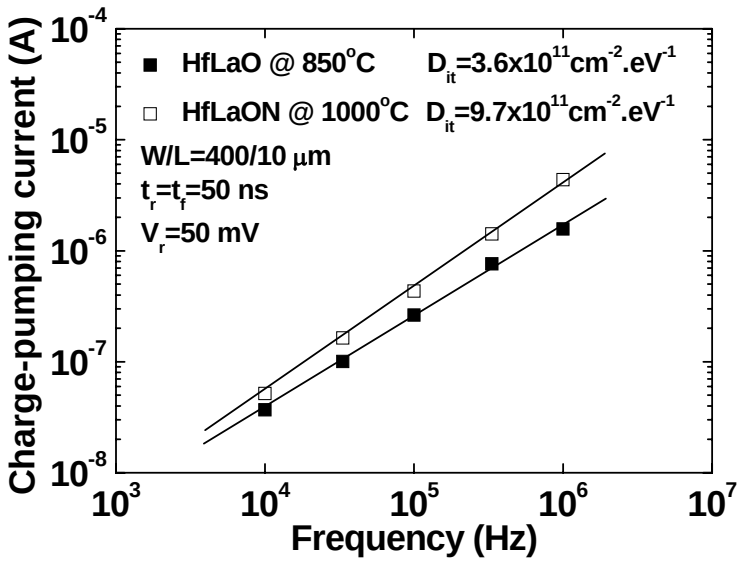
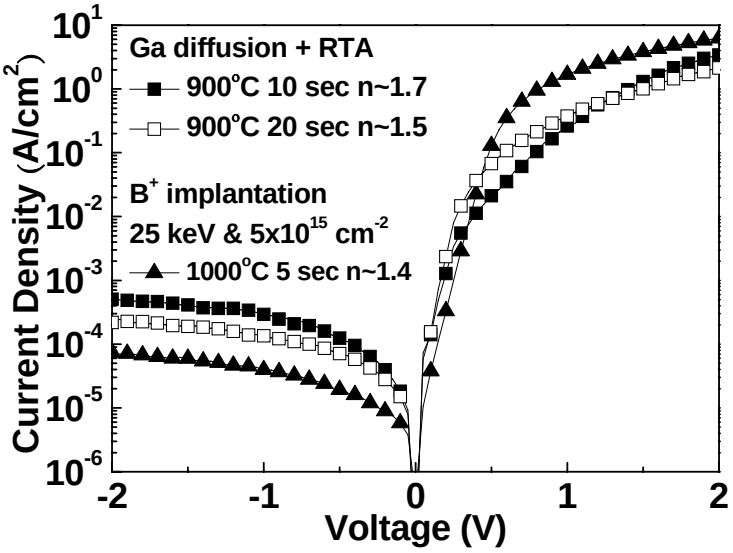
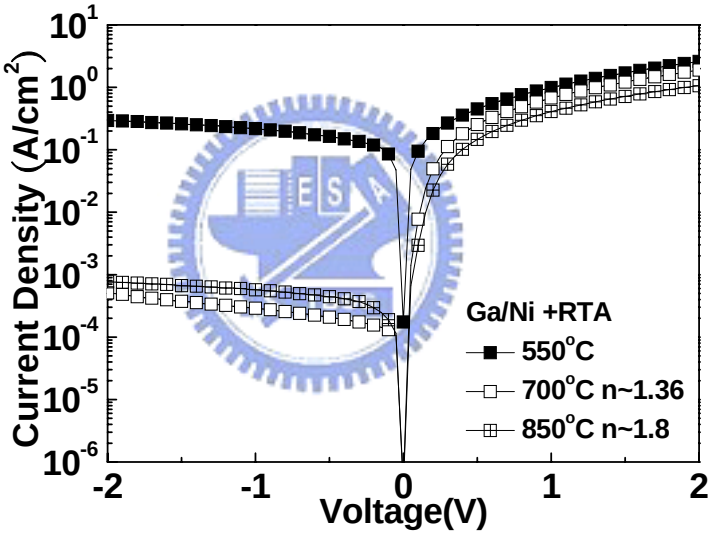


Fig. 4-2 Charge pumping current as a function of gate pulse frequency for 1000°C processed HfLaON and 850°C processed HfLaO.



(a)



(b)

Fig. 4-3 *J-V* characteristics of p^+/n junction formed by (a) SiO_2/Ga SPD at 900°C RTA and control B^+ implantation at 1000°C RTA; (b) SiO_2/Ni/Ga SPD at 550~850°C RTA.

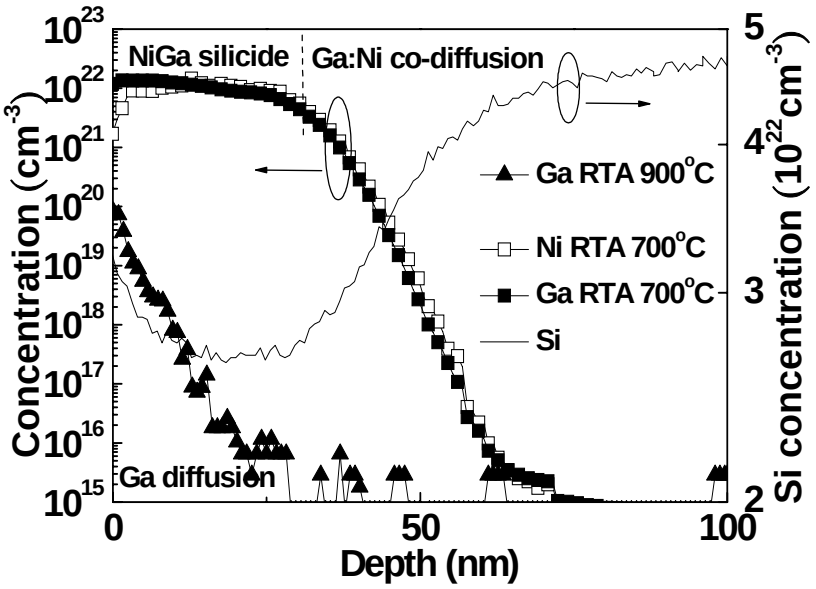
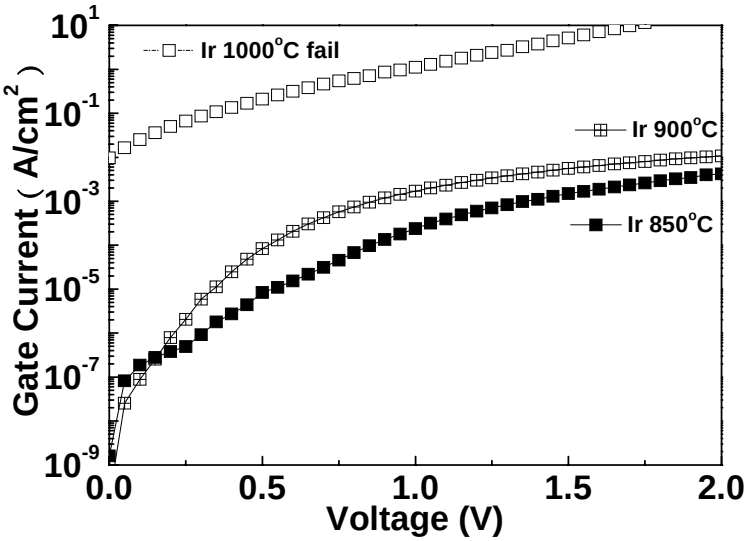
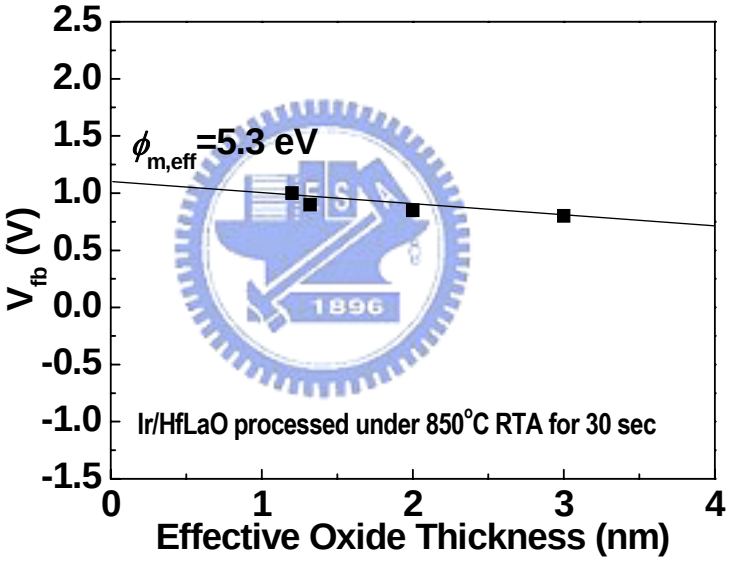


Fig. 4-4 SIMS profile of Ga and Ni/Ga-silicide p^+/n junction formed by SPD.



(a)



(b)

Fig. 4-5 (a) *J-V* and (b) V_{fb}-*EOT* characteristics of Ir/HfLaO *p*-MOS after 850°C RTA.

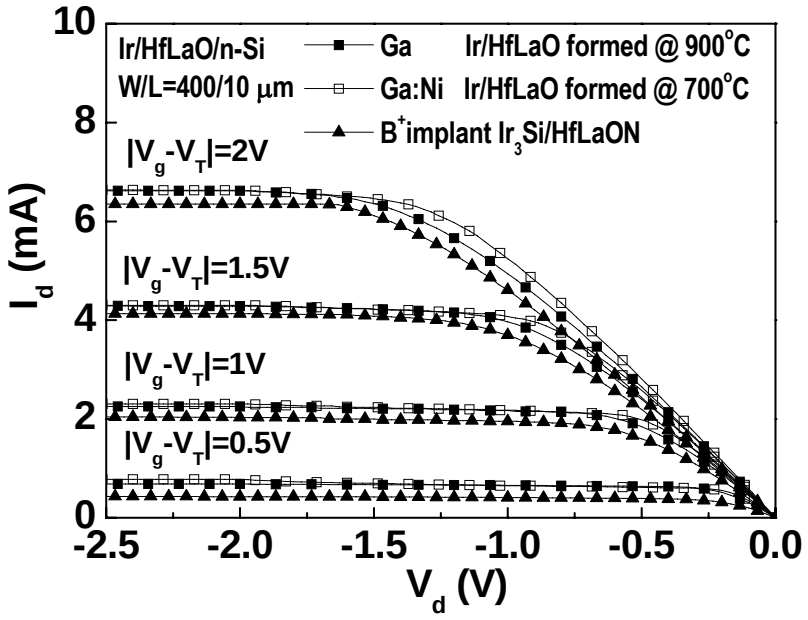


Fig. 4-6 The I_d-V_d characteristics of Ir/HfLaO *p*-MOSFET using Ga or NiGa-silicide S/D.

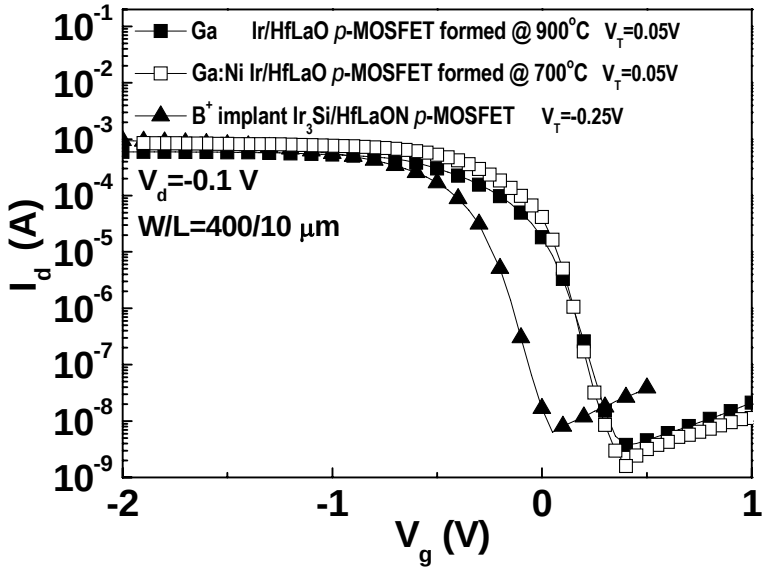


Fig. 4-7 The I_d-V_g characteristics of Ir/HfLaO or Ir_3Si/HfLaON *p*-MOSFETs.

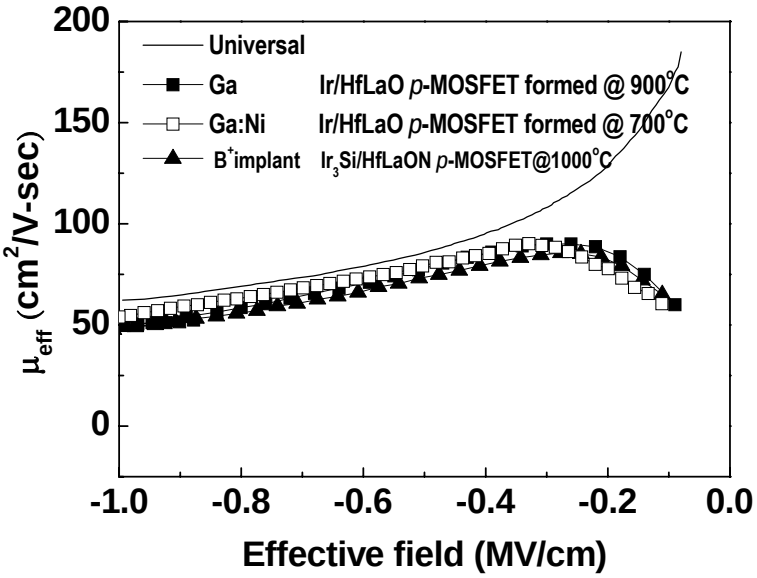


Fig. 4-8 The extracted hole mobility from I_d-V_g characteristics of Ir/HfLaO or Ir_3Si/HfLaON *p*-MOSFETs.

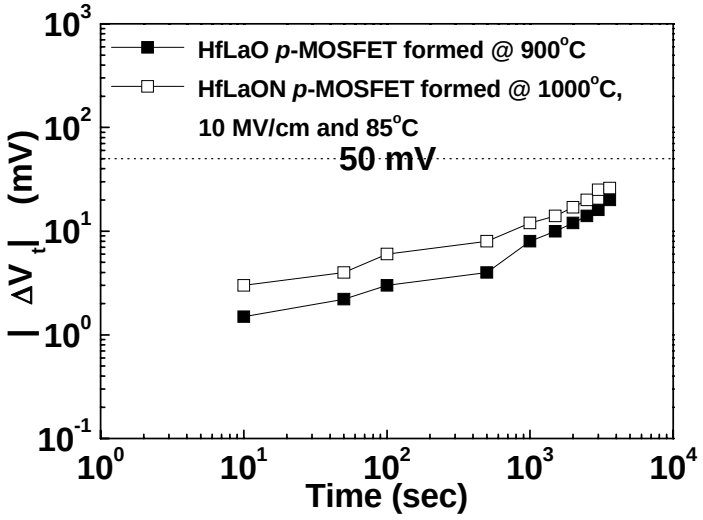


Fig. 4-9 The ΔV_t shift of Ir/HfLaO *p*-MOSFETs stressed at 85°C and 10 MV/cm for 1 hour.

Chapter 5

Very Low V_t Hf/HfLaO *n*-MOSFETs Using Self-Aligned Low Temperature Shallow Junction

5.1 Introduction

Both metal gate and high-κ gate dielectric are needed to reduce the DC power consumption and gate depletion to continue the VLSI scaling trend, [5.1]-[5.12]. However, one of the difficult challenges for metal-gate/high-κ MOSFET is the large threshold voltage (V_t) by Fermi-level pinning that is opposite to scaling trend. To overcome this problem, low and high work-function metal-gates are required to reduce the pinning effect. Previously, we have reported the $HfSi_x$ gate on HfLaON has low effective work-function ($\phi_{m\text{-}eff}$) of 4.33 eV [5.12] and useful for *n*-MOS. For *n*-MOSFET, the novel TaC gate has shown low $\phi_{m\text{-}eff}$ [5.1]-[5.2]. However, the Full Silicidation (FUSI) gate [5.3]-[5.5], [5.8]-[5.13] for *n*-MOS is still needed to develop, which is due to the inherent advantage of the process compatibility with current poly-Si gate CMOS technology. In this chapter, we used the similar method of previously reported Ir for *p*-MOS to develop the low work-function Hf gate for *n*-MOSFET. This is because the Hf has very low work function of 3.5 eV in the Periodic Table. The Hf gate on HfLaO gives a low $\phi_{m\text{-}eff}$ of 4.1 eV and a good electron mobility of 243 cm^2/V-s. In addition, solid phase diffusion (SPD) process can reduce to process temperature down to

850°C. These results indicate the potential application for metal-gate/high-κ *n*-MOSFETs.

5.2 Experimental procedure

We used the 4-inch p-type Si wafers in these experiments. After a standard RCA clean, the HfLaO was deposited on Si wafers by physical vapor deposition (PVD). Then Hf of 20 nm thickness was deposited on the HfLaO by PVD. To prevent Hf oxidation, a 50 nm thick TaN and 20 nm thick Ir were subsequently deposited above the Hf/HfLaO to form n-MOS capacitors. Then, NiAl-silicide Schottky contact for sub-45-nm node was made [5.15], or self-aligned H_3PO_4 was spun deposited, transformed to P_2O_5 at 200°C and SPD at 850~900°C RTA. Such wet H_3PO_4 spray and doping processes are used for commercial Si solar cell manufacture. Finally, source-drain metal contacts were added. For comparison, $HfSi_x$/HfLaON *n*-MOSFET using As^+ 35 KeV ion implantation (at a 5×10^{15} cm^{-2} dose) followed by RTA activation at 1000°C for 5 sec were also fabricated. The fabricated devices were characterized by *C-V* and *I-V* measurements using an HP4284A precision LCR meter and HP4156 semiconductor parameter analyzer, respectively.

5.3 Result and Discussion

5.3.1 Low temperature shallow junction formed by SPD

Fig. 1 shows the variation *Rs* of NiAl (insert), H_3PO_4 spin SPD and As^+ implant with RTA condition. Data for the 1 keV As^+ implant and 1020oC RTA are from [5.16]. For NiAl case, very low Rs ~10 Ω/sq. could be achieved after 450~650°C RTA. For H_3PO_4 spin SPD

compared with As^+ implant with 1020°C RTA condition, H_3PO_4 spin SPD at 850°C has comparable *Rs* compared with X_j of 29 nm As^+ implant with 1020°C RTA. Moreover, H_3PO_4 spin SPD at 875~900°C has lower *Rs* compared with X_j of 29 nm As^+ implant with 1020°C RTA. In order to further check the reason of relative low *Rs*, we measured phosphorus SIMS profile for H_3PO_4 spin SPD. The X_j data from [5.16] are also included for comparison. A *USJ* X_j of 23 or 35 nm was measured by SIMS after 850 or 875°C RTA – this is better than that for a 1 keV As^+ implant and spike RTA at the same R_s [5.16]. This is due to the free from defect-assisted diffusion caused by As^+ implant damage. This ≤900°C process temperature is important for HfLaO in preserving its amorphous structure at 900°C, as Fig. 5-3 shows, without using the nitrided HfLaON, which reduces the possible pinning at metal-gate/high-κ interface. The amorphous structure of HfLaO at 900°C is better than crystallized HfO_2 for achieving good BTI, by avoiding charge trapping at poly-HfO_2 grain boundaries.

Figs. 5-4 (a) and 5-4(b) show the *J-V* of n^+/p junctions. Although the NiAl-silicide Schottky contact has an *n* of 1.9, the self-aligned H_3PO_4 spin process improves *n* to 1.4, gives a 10X smaller leakage and a low R_s. As a result, we finally choose the self-aligned H_3PO_4 spin process for MOSFET fabrication.

5.3.2 Device characteristics of low temperature SPD formed Hf/HfLaO n-MOS

Figs. 5-5 and 5-6 are the *C-V* and *J-V* characteristics of Ir/TaN/Hf on HfLaO devices. At 1.2 nm EOT, the gate leakage current was only 1.8×10^{-4} A/cm^2 at -1 V. Reducing the RTA

temperature to ≤900°C is vital for choosing proper $\phi_{m\text{-}eff}$ pure metal gate electrode. Furthermore, we have also plotted the V_{fb}-EOT in Fig. 5-7 and proper $\phi_{m\text{-}eff}$ of 4.1 eV is obtained for Hf/HfLaO *n*-MOS.

The I_d-V_d, I_d-V_g characteristics of Hf/HfLaO *n*- MOSFETs are shown in Figs. 5-8 and 5-9, respectively. Good transistor characteristics, high drive current and low V_t of 0.03 V, are measured.

The μ_{eff}-E characteristics of Hf/HfLaO *n*- MOSFETs is derived from I_d-V_g characteristics and is shown in Fig. 5-10. High electron mobility of 243 cm^2/Vs is also observed. The improved mobility, compared with 1000°C RTA $HfSi_x$/HfLaON *n*-MOSFET, is consistent with lower charged vacancies associated with interfacial reactions. Table 5-1 compares various metal-gate/high-κ *n*-MOSFET data.

The merits of self-aligned Hf/HfLaO *n*-MOS with SPD *USJ* are proper $\phi_{m\text{-}eff}$ of 4.1 eV, low V_t of 0.03 V and high mobility of 243 cm^2/Vs. Our results are comparable with or better than the best reported data for metal-gate/high-κ *n*-MOSFET, with a small 1.2 nm EOT, and using a self-aligned and gate-first process.

5.4 Conclusion

We have found good performance in terms of V_t and mobility for HfLaO *n*-MOSFETs at 1.2 nm EOT using a low work-function Hf gate. The self-aligned and gate-first Hf/HfLaO *n*-MOSFETs have the advantages of ≤900°C low processing temperature and good device

performance using a self-aligned and gate-first process.

Table 5-1 Comparison of device parameters for metal-gate/high-κ *n*-MOSFETs.

High-κ	Metal Gate	EOT (nm)	V_t (V)	Process Temp.
HfLaO This work	**Hf**	**1.2**	**0.03**	**≤900°C**
HfLaON Chapter 2	**$HfSi_x$**	**1.2**	**0.18**	**1000°C**
HfAlON [5.11]	Yb_xSi	1.7	0.1	Low Temp. FUSI
HfTaO [5.17]	TaN	1.6	-	1000°C
HfSiON [5.18]	TaC	1.2	~0.4	1000°C
HfSiON [5.8]	$NiSi_2$	1.7	0.47	Low Temp. FUSI

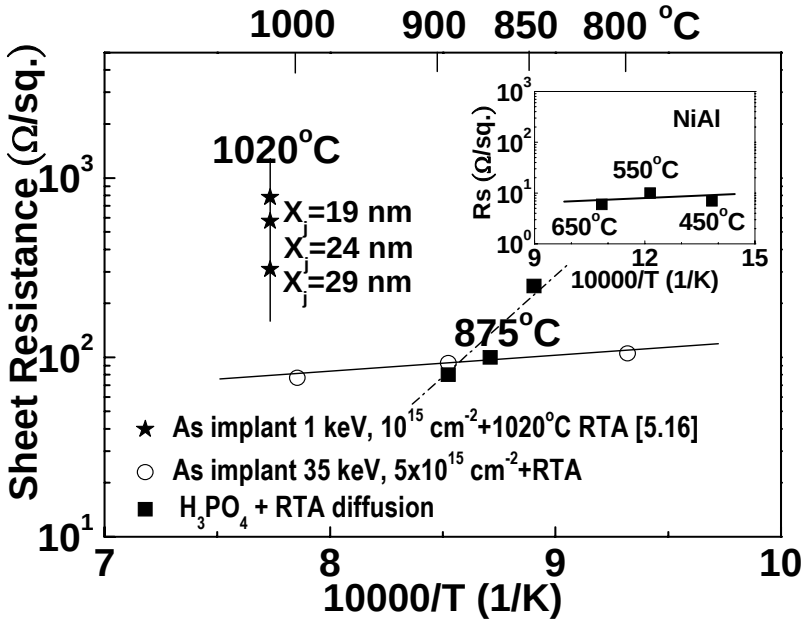


Fig. 5-1 Variation *Rs* of NiAl (insert), H3PO4 spin SPD and As^+ implant with RTA condition. Data for the 1 keV As^+ implant and 1020oC RTA are from [5.16].

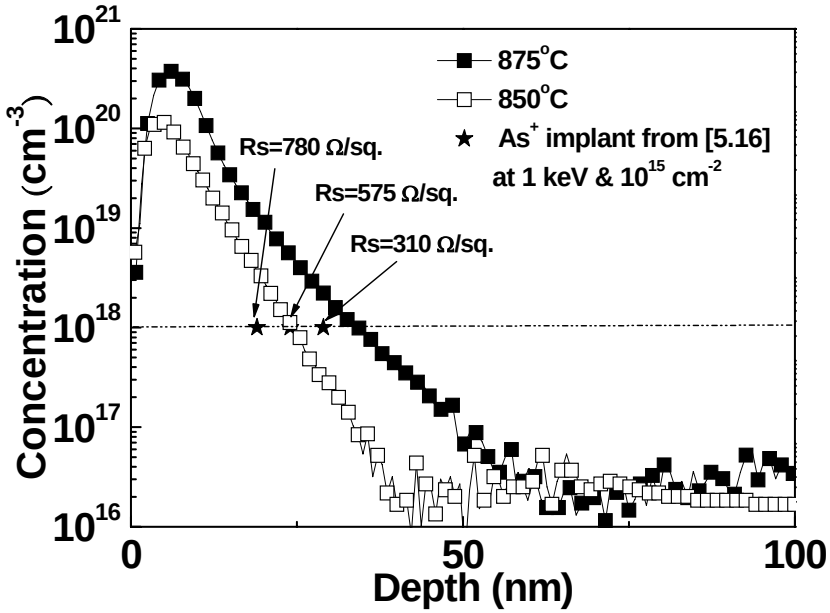


Fig. 5-2 Phosphorus SIMS profile for H_3PO_4 spin SPD, with X_j of 23 and 35 nm, for 850 and 875°C RTAs. The X_j data from [5.16] are included for comparison.

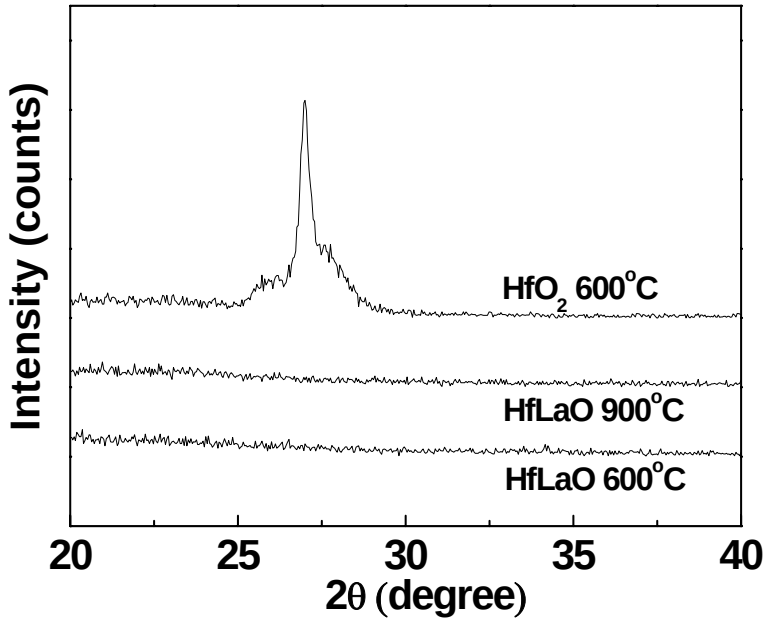
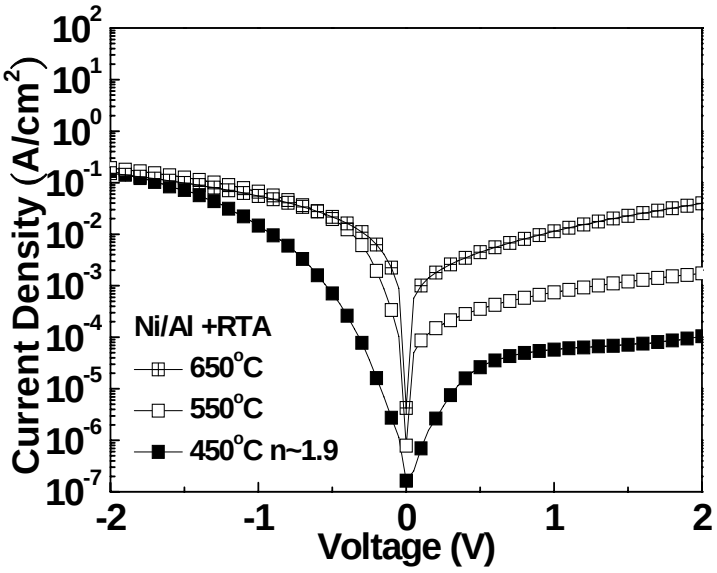
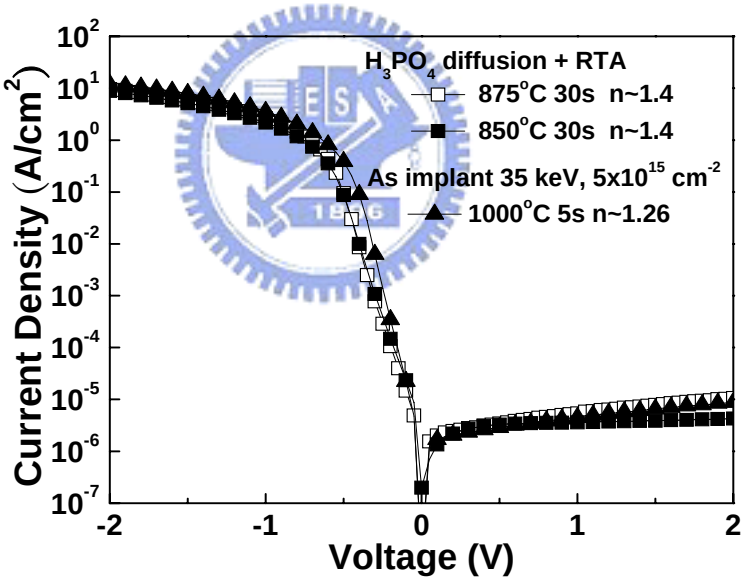


Fig. 5-3 XRD of HfLaO after 600°C and 900°C 30 sec RTA. Amorphous structure w/o crystallization is still preserved and important for BTI.



(a)



(b)

Fig. 5-4 (a) *J-V* of *n+/p* junction with NiAl Schottky contact. Although *Rs*<10 *Ω*/sq, the leakage and *n* are poor. (b) *J-V* of n^+/p junctions made by H_3PO_4 spin SPD at 850 and 875°C RTA. The leakage and *n* are similar to those for the As^+ implant and 1000°C RTA case.

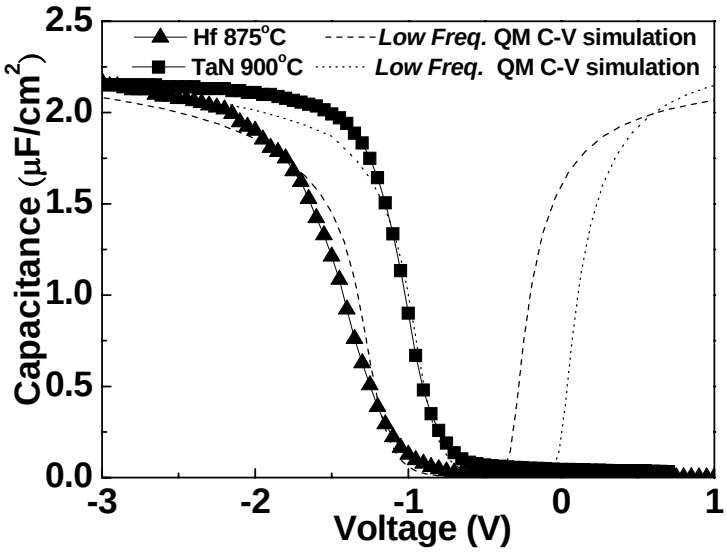


Fig. 5-5 *C-V* of HfLaO *n*-MOS with Ir/TaN/Hf and TaN gates after 875 and 900°C RTAs. Data from a quantum-mechanical C-V simulation are included.

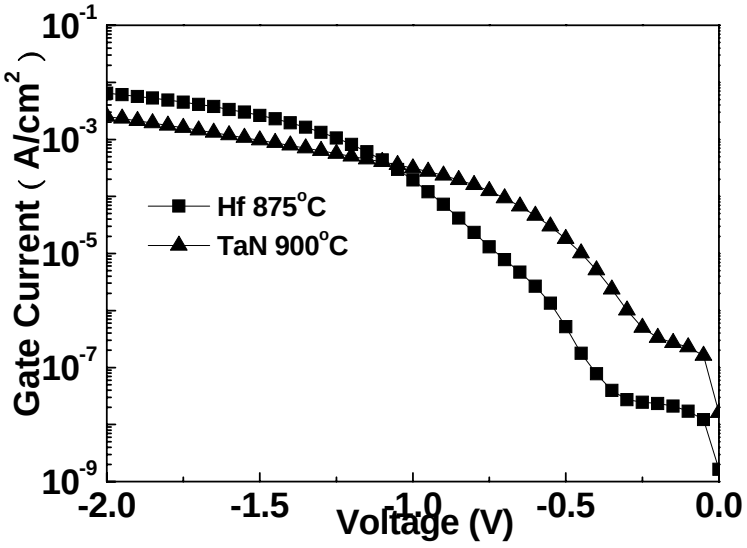


Fig. 5-6 *J-V* of HfLaO *n*-MOS with Ir/TaN/Hf and TaN gates, after 875 and 900°C RTAs.

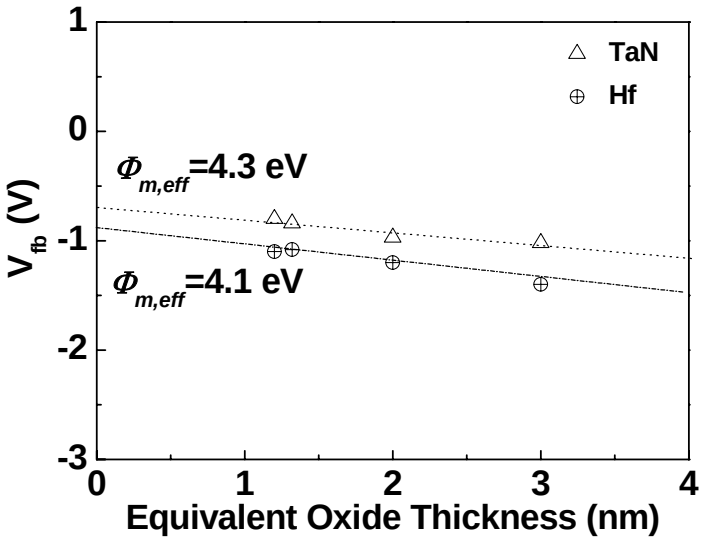


Fig. 5-7 V_{fb}-*EOT* for TaN and Hf gates. Effective work-functions are 4.3 and 4.1 eV.

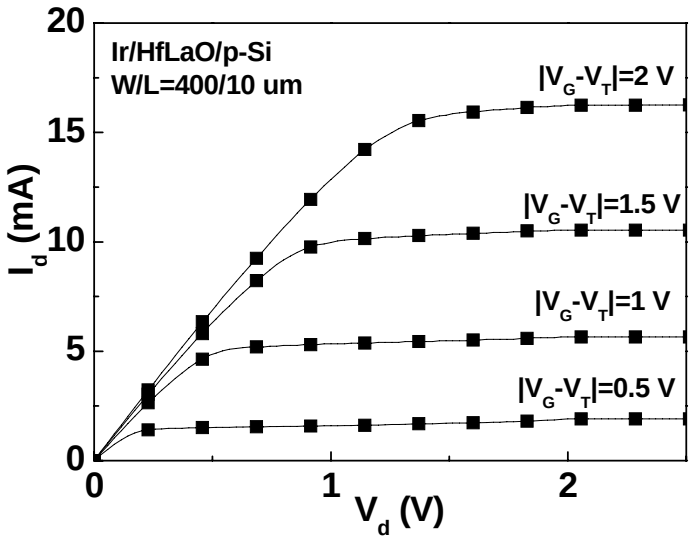


Fig. 5-8 The I_d-V_d characteristics of the Hf/HfLaO *n*-MOSFETs.

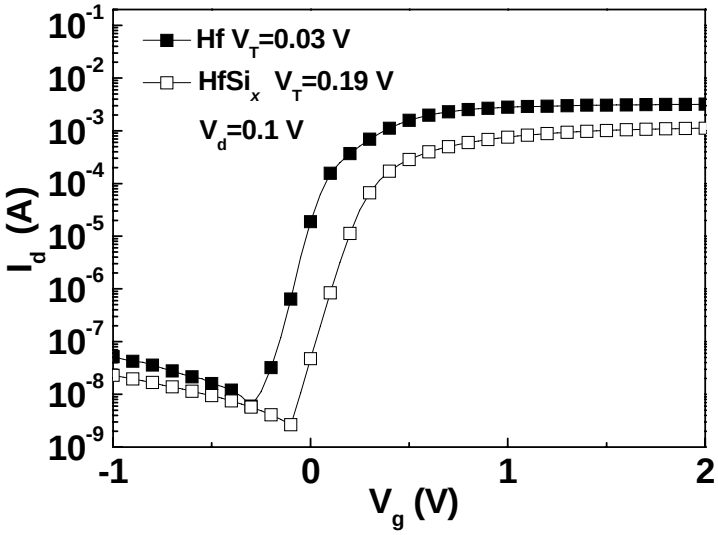


Fig. 5-9 The I_d-V_g characteristics of the Hf/HfLaO *n*-MOSFETs.

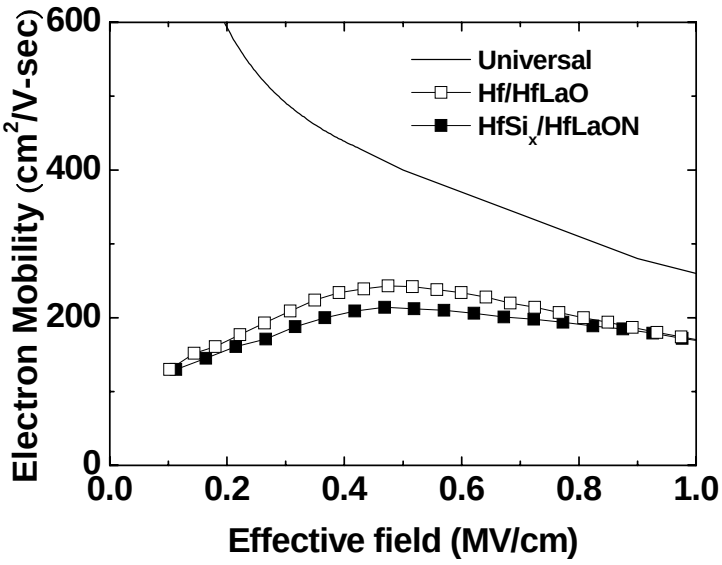


Fig. 5-10 The electron mobility vs. effective electric field for the Hf/HfLaO and HfSi$_x$/HfLaON *n*-MOSFETs.

Chapter 6

Summary and Conclusions

In this dissertation, two novel dual metal gate process technologies including fully silicided (FUSI) gates and low-temperaure-processed pure metal gate were investigated. At first, scaling the effective oxide thickness (EOT) from 1.6 nm to 1.2nm using $HfSi_x$ gates was studied. We have found good performance in terms of threshold voltage (V_t) and mobility for $Hf_{0.7}La_{0.3}ON$ *n*-MOSFETs at 1.2 nm EOT using a low work-function and high-temperature-stable $HfSi_x$ gate. The self-aligned and gate-first $HfSi_x$/HfLaON *n*-MOSFETs have the advantages of simple high temperature FUSI processing and compatibility with current very large scale integration (VLSI) lines.

In the following study, similar FUSI process using $IrSi_x$ gates was also investigated. Good device integrity of Ir_3Si/HfLaON p-MOSFETs is shown by the very low leakage current, good hole mobility and 1000^oC thermal stability. However, poor flat band voltage (V_{fb}) and high V_t is observed at 1.2 nm EOT. As a result, we aimed to develop a new process technology to solve this problem.

In order to study the origin of V_{fb} roll-off phenomenon, we compared the V_{fb} of $IrSi_x$ gates under different EOT. Finally, we develop a new process technology of high work-function Ir/HfLaO *p*-MOSFETs using low-temperature-processed shallow junction. The

merits of self-aligned Ir/HfLaO *p*-MOSFETs are the proper $\phi_{m\text{-}eff}$ of 5.3 eV, low V_t of +0.05 V, high hole mobility of 90 cm^2/V-s at -0.3 MV/cm, and small BTI of 20 mV (85^oC, 10 MV/cm & 1 hr). These results are comparable with or better than the previous reported data for metal-gate/high-κ *p*-MOSFETs, with small 1.2 nm EOT, similar simple self-aligned and gate-first process for VLSI IC fabrication.

Finally, we also tried to decrease the process temperature of *n*-MOSFET by Hf/HfLaO using solid phase diffusion (SPD). Two different SPD shallow junctions were studied. We have found good performance in terms of V_t and mobility for HfLaO *n*-MOSFETs at 1.2 nm EOT using a low work-function Hf gate. The self-aligned and gate-first Hf/HfLaO *n*-MOSFETs have the advantages of <900^oC low processing temperature and good device performance for VLSI fabrication.

In conclusion, metal silicide FUSI processes have the advantage of proper $\phi_{m,eff}$, high temperature stable. However, as the continuous scaling of oxide thickness, the thermal budge of 1000^oC dopant activation process has become more critical. In our study, the V_{fb} roll-off and unwanted high V_t can be solved by low temperature process technology. As a result, it is necessary to further decrease the process temperature for both *n*- and *p*-MOSFETs in our future study.

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(A) International Journal:

[1] **C. F. Cheng**, C. H. Wu, N. C. Su, S. J. Wang, S. P. McAlister and A. Chin, "High Work-Function Ir/HfLaO p-MOSFETs Using Low-Temperature- Processed Shallow Junction," IEEE Trans. Electron Devices, accepted to be published on March 2008.

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