參考文獻

[1] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, **"**Design of ion-implanted MOSFET's with very small physical dimensions", *IEEE J. Solid-state Circuit*, Vol.SC-9, 1974, pp.256-268.

[2] S. M. Sze, Physics of Semiconductor Devices, 2nd edition, Ch.8, Central 1985

[3] R. Rios, and N. D. Arora, "Determination of ultra-thin gate oxide thicknesses for CMOS structures using quantum effects", in *IEDM Tech. Dig.*, 1994, pp.613-616

[4] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's", *IEEE Electron Device Lett.*, Vol.18, NO. 5, May 1997, pp.209-211

[5] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Makamura, M. Saito, and H. Iwai, **"**1.5 nm direct-tunneling gate oxide Si MOSFET's", *IEEE Trans. Electron Devices*, Vol.43, August 1996, pp.1233-1242

[6] J. Lee, G. Bosman, K. R. Grenn, and D. Ladwig, **"**Model and analysis of gate leakage current in ultrathin nitrided oxide MOSFETs", *IEEE Trans. Electron Devices*, Vol.49, NO.7, July 2002, pp.1232-1241

[7] International Technology Roadmap for Semiconductor, Semiconductor Industry Association, 2004 update.

[8] G. D. Wilk, R. M. Wallace, and J. M. Anthony, **"**High-k gate dielectrics: Current status and materials properties considerations", *J. Appl. Phys.*, Vol.89, May 2001, pp.5243-5275

[9] J. C. Lee., *handout of IEEE EDS Vanguard Series Short Course*, National Chiao Tung University, Taiwan, Apr. 26 2001

[10] G. C. F. Yeap, S. Krishnan, and M.R. Lin, "Fringing-induced barrier lowering (FIBL) in sub-100-nm MOSFETs with high-k gate dielectrics", *Electron. Lett.*, vol. 34, no. 11, 1998, pp.1150-1152

[11] N. R. Mohapatra, M. P. Desai, and V. R. Rao, "Detailed analysis of FIBL in MOS transistors with high-k gate dielectrics", in *Proc. 16th Int. Conf. VLSI Design*, 2003,

pp.99-104

[12] C. H. Lai, L. C. Hu, H. M. Lee, L. J. Do, and Y. C. King, “New stack gate insulator structure reduce FIBL effect obviously”, in *Proc. VLSI-TSA*, 2001, pp.216-219.

[13] B.-Y. Tsui, and L.-F. Chin, “A comprehensive study on the FIBL of nanoscale MOSFETs”, *IEEE Trans. Electron Devices*, Vol. 51, Issue: 10, Oct. 2004, pp.1733-1735

[14] J. Robertson, “Electronic structure and band offsets of high-dielectric-constant gate oxides”, *MRS bulletin*, March 2002, pp.217-221

[15] K. Yudong, G. Gebara, M. Freiler, J. Barnett, D. Riley, J. Chen, K. Torres,L. JaeEun, B. Foran, F. Shaapur, A. Agarwal,P. Lysaght, G.A. Brown, C. Young, S. Borthakur, Li. Hong-Jyh, B. Nguyen, P. Zeitzoff, G. Bersuker, D. Derro, R. Bergmann, R.W. Murto, A. Hou, H.R.Huff, E. Shero, C. Pomarede, M. Givens, M. Mazanez, and C. Werkhoven, **“**Conventional n-channel MOSFET devices using single layer HfO_2 and ZrO_2 as high-k gate dielectrics with polysilicon gate electrode”, in *IEDM Tech. Dig.*, 2001, pp.455-458

[16] A.Callegari, E. Cartier, M. Gribelyuk, H. K. Okorn-Schmidt, and T. Zabel, **“**Physical and electrical characterization of Hafnium oxide and Hafnium silicate sputtered films”, *J. Appl. Phys.*, **90**, 2001, pp.6466-6475

[17] D.G. Schlom, and J.H. Haeni, “A thermodynamic approach to selecting alternative gate dielectrics”, *MRS bulletin*, March 2002, pp.198-204

[18] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C. S. Kang, B. H. Lee, R. N. Nieh, and J. C. Lee, **“**Dopant penetration effects on polysilicon gate HfO_2 MOSFET's”, in *IEEE Symp. VLSI Tech. Dig.*, 2001, pp.131-132

[19] H. J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan, and J.C. Lee, **“**Novel nitrogen profile engineering for improved TaN/HfO_2/Si MOSFET performance**”,** in *IEDM Tech. Dig.*, 2001, pp.655-658

[20] S. Guha, E. Gusev, E. Gusev, M. Copel, L. Ragnarsson, and D. A. Buchanan, “Compatibility challenge for high-k materials integration into CMOS technology”, *MRS bulletin*, March 2002, pp.226-229

[21] Y.H. Kim, K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, R. Nieh, J. Han, S. Krishnan, A.

Shahriar, and J.C. Lee, **"**Hard and soft-breakdown characteristics of ultra-thin HfO_2 under dynamic and constant voltage stress", in *IEDM Tech. Dig.*, Dec. 2002, pp.629-632

[22] T. Kauerauf, R. Degraeve, E. Cartier, and B. Goveoreanu, **"**Towards understanding degradation and breakdown of SiO_2/high-k stacks", P. Blomme, B. Kaczer, L. Pantisano, A. Keber, and G. Groeseneken, in *IEDM Tech. Dig.*, Dec. 2002, pp.521-524

[23] C. Hobbs, H. Tseng, K. Reid, B. Taylor, L. Dip, L. Hebert, R. Garcia, R. Hegde, J. Grant, D. Gilmer, A. Franke, V. Dhandapani, M. Azrak, L. Prabhu, R. Rai, S. Bagchi, J. Conner, S. Backer, F. Dumbuya, B. Nguyen, and P. Tobin, **"**80 nm poly-Si gate CMOS with HfO_2 gate dielectric", in *IEDM Tech. Dig.*, 2001, pp.651-654

[24] B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, **"**Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application", in *IEDM Tech. Dig.*, 1999, pp.133-136

[25] W. Tsai, L. Ragnarsson, P.J. Chen, B. Onsia, R.J. Carter, E. Cartier, E. Young, M. Green, and M. Caymax, "Comparison of sub 1nm TiN/HfO_2 with poly-Si/HfO_2 gate stacks using scaled chemical oxide interface", in *IEEE Symp. VLSI Tech. Dig.*, 2003, pp.21-22

[26] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. C. Lee, "Effects of high-temperature forming gas anneal on HfO_2 MOSFET performance", in *IEEE Symp. VLSI Tech. Dig.*, 2002, pp.22-23

[27] B. Tavel, X. Garros, T. Skotnicki, F. Martin, C. Leroux, D. Bensahel, M.N. Semeria, Y. Morand, J.F. Damlencourt, S. Descombes, F. Leverd, Y. L-Friec, P. Leduc, M. Rivoire, S. Jullian, and R. Pantel, "High performance 40nm nMOSFETs with HfO_2 gate dielectric and poltsilicon damascene gate", in *IEDM Tech. Dig.*, 2002, pp.429-432

[28] Y.H. Kim, K. Onishi, C.S. Kang, H.J. Cho, R. Choi, S. Krishnan, M.S. Akbar, and J. C. Lee, "Thickness dependence of weibull slopes of HfO_2 gate dielectrics", *IEEE Electron Device Lett.*, Vol.24, NO. 1, January 2003, pp.40-42

[29] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R.E. Nieh, S.A. Krishnan, and J. C. Lee, "Improvement of surface carrier mobility of HfO_2 MOSFETs by high-temperature forming gas annealing", *IEEE Trans. Electron Devices*, Vol. 50, Issue: 2, Feb. 2003,

pp.384-390

[30] H. Kim, and P.C. Mclntyre, “Effects of crystallization on the electrical properties of ultrathin HfO_2 dielectrics grown by atomic layer deposition”, *Appl. Phys. Lett.*, **82**, 2003, pp.106-108

[31] H. Kim, A. Marshall, and P.C. Mclntyre, “Crystallization kinetics and microstructure-dependent leakage current behavior of ultrathin HfO_2 dielectrics: in situ annealing studies”, *Appl. Phys. Lett.*, **84**, 2004, pp.2064-2066

[32] W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, “Effect of Al inclusion in HfO_2 on the physical and electrical properties of the dielectrics”, *IEEE Electron Device Lett.*, Vol.23, NO. 11, November 2002, pp.649-651

[33] W. J. Zhu, and T. P. Ma, “Charge trapping in ultrathin hafnium oxide”, *IEEE Electron Device Lett.*, Vol.23, NO. 10, January 2002, pp.597-599

[34] E. J. Preisler, S. Guha, M. Copel, N. A. Bojarczuk, M. C. Reuter, and E. Gusev, “Interfacial oxide formation from intrinsic oxygen in W-HfO_2 gated silicon field-effect transistors”, *Appl. Phys. Lett.*, **85**, 2004, pp.6230-6232

[35] L. Kang, Y. Jeon, K. Onishi, B. H. Lee, W.-J. Qi. R. Nieh, S. Gopalan, and J. C. Lee, “Single-layer thin HfO_2 gate dielectric with n+-polysilicon gate”, in *IEEE Symp. VLSI Tech. Dig.*, 2000, pp.44-45

[36] M. Cho, H. B. Park, J. Park, S. W. Lee, and C. S. Hwang, “High-k properties of atomic-layer-deposited HfO_2 films using a nitrogen-containing $Hf[N(CH_3)_2]_4$ precursor and H_2O oxidant”, *Appl. Phys. Lett.*, **83**, 2003, pp.5503-5505

[37] L. Kang, B. H. Lee, W.-J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. C. Lee, “Electrical characteristics of highly reliable ultrathin hafnium oxide gate dielectrics”, *IEEE Electron Device Lett.*, Vol.21, NO. 4, January 2000, pp.181-183

[38] K.-J. Choi, W.-C. Shin, and S.-G. Yoon, “Effect of annealing conditions on a hafnium oxide reinforced SiO_2 gate dielectric deposited by plasma-enhanced metallorganic CVD”, *J. Electro. Soc.*, **149**, 2002, pp.18-21.

[39] W. Tsai, L.-A. Ragnarsson, P.J. Chen, B. Onsia, T. Scram, E. Cartier, A. Kerber, E. Young,

M. Caymax, S. D. Gendt, and M. Heyns, “Performance comparison of sub 1nm sputterd TiN/HfO_2 nMOS and pMOSFETs”, in *IEDM Tech. Dig.*, 2003, pp.311-314

[40] Z. Xu, M. Houssa, S. D. Gendt, and M. Heyns, “Polarity effect on the temperature dependence of leakage current through HfO_2/SiO gate dielectric stacks”, *Appl. Phys. Lett.*, **80**, 2002, pp.1975-1977

[41] R. Choi, K. Onishi, C. S. Kang, S. Gopalan, R. Nieh, Y. H. Kim, J. H. Han, S. Krishnan, H.-J. Cho, A. Shahriar, and J. C. Lee, “Fabrication of high quality ultra-thin HfO_2 gate dielectric MOSFETs using deuterium anneal”, in *IEDM Tech. Dig.*, 2002, pp.613-616

[42] B. H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W.-J. Qi, C. Kang, and J. C. Lee, “Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8Å-12Å)”, in *IEDM Tech. Dig.*, 2000, pp.39-42

[43] R. Choi,C. S> Kang, H.-J. Cho, Y.-H. Kim, M. S. Akbar, and J. C. Lee, “Effects of high temperature forming gas anneal on the characteristics of metal-oxide-semiconductor filed-effect transistor with HfO_2 gate stack”, *Appl. Phys. Lett.*, **84**, 2004, pp.4839-4841

[44] C.W. Yang, Y.K. Fang, S.F. Chen, C.Y. Lin, M.F. Wang, Y.M. Lin, T.H. Hou, L.G. Yao, S.C. Chen, and M.S. Liang, ”Effective improvement of high-k Hf-silicate/silicon interface with thermal nitridation”, *Electronics Letters* , Volume: 39 , Issue: 5 , 6 March 2003, pp.421-422

[45] R. Choi, C.S. Kang, B.H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J. C. Lee, “High-quality ultra-thin HfO_2 gate dielectric MOSFETs with TaN electrode and nitridation surface preparation”, in *IEEE Symp. VLSI Tech. Dig.*, 2001, pp.15-16

[46] H.B. Park, M. Cho, J. Park, S.W. Lee, T.J. Park, and C.S. Hwang, “Improvements in reliability and leakage current properties of HfO_2 gate dielectric films by in situ O_3 oxidation of Si substrate”, *Electrochemical and Solid-state Letters*, **7**,2004, pp.254-257

[47] Y.B. Kim, M.S. Kang, T. Lee, J. Ahn, and D.K. Choi, “Characterization of atomic-layer-deposited hafnium oxide/SiON stacked-gate dielectrics”, *J. Vac. Sci. Technol.*, 2003, pp.2029-2033

[48] X. Wang, J. Liu, F. Zhu, N. Yamada, and D.L. Kwong, “A simple approach to fabrication

of high-quality HfSiON gate dielectrics with improved nMOSFET oerformance", *IEEE Trans. Electron Devices*, Vol. 51, Issue: 11, Nov. 2004, pp.1798-1804

[49] M. Saitoh, N. Ikarashi, H. Watanabe, S. Fujieda, H. Watanabe, T. Iwamoto, A. Morioka, T. Ogura, M. Terai, K. Watanbe, M. Miyamura, T. Tatsumi, T. Ikarashi, K. Masuzaki, Y. Saito, and Y. Tabe, "1.2nm HfSiON/SiON stacked gate insulators for 65nm-node MISFETs", *the 2004 International Conference on Solid State Devices and Materials*, 2004, pp.38-39

[50] M.L. Green, M.-Y. Ho, B. Busch, G.D. Wilk, and T. Sorsch, "Nucleation and growth of atomic layer deposited HfO_2 gate dielectric layers on chemical oxide (Si-O-H) and thermal oxide (SiO_2 or Si-O-N) underlayers", *J. Appl. Phys.*, **92**, 2002, pp.7168-7174

[51] B-Y. Tsui, and C-F Huang, "Wide range work function modulation if binary alloys for MOSFET application", *IEEE Electron Device Lett.*, Vol.24, NO. 3, March 2003, pp.153-155

[52] Z. Kuo, and T. P. Ma, "A new method to extract EOT of ultrathin gate dielectric with high leakage current", *IEEE Electron Device Lett.*, Vol.25, NO. 9, September 2004, pp.655-657

[53] Bing-Yue Tsui, Yun-Pei Huang, and Feng-Chiu Hsieh, and Wei-Hao Wu, "A New Method to Correct Capacitance of High-leakage Ultra-thin Gate Dielectric," accepted by the Int. Conf. on Solid State Devices and Materials, 2005.

[54] R.Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-k/metal-gate stack and its MOSFET characteristics", *IEEE Electron Device Lett.*, Vol.25, NO. 6, June 2004, pp.408-410

[55] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-k insulator:The role of remote phonon scattering", *J. Appl. Phys.*, **90**, 2001, pp.4587-4608

[56] A. Kerber, E. Cartier, , L. Pantisano, R. Degraeve, T. Kauerauf, Y. Kim, A. Hou, G. Groeseneken, H. E. Maes, and U. Schwalke, "Origin of the threshold voltage instability in SiO_2/HfO_2 dual layer gate dielectrics", *IEEE Electron Device Lett.*, Vol.24, NO. 2,

February 2003, pp.87-89

[57] A. Shanware, M. R. Visokay, J. J.Chambers, A. L. P. Rotondaro, H. Bu, M. J. Bevan, R. Khamankar, S. Aur, P. E. Nicollian, J. McPherson, and L. Colombo, "Evaluation of the positive biased temperature stress stability in HfSiON gate dielectrics", *IEEE* International Reliability Physics Symposium, 2003, pp.208-213

[58] W. H. Wu, M. C. Chen, M. F. Wang, T. H. Hou, L. G. Yao, Y. Jin, S. C. Chen, and M. S. Liang, "Effects of base oxide in HfSiO/SiO_2 high-k gate stacks", *IEEE* Proceeding of 11th IPFA 2004, pp.25-28

[59] C. Seok, H-J Cho, R. Choi, Y-H. Kim, C. Y. Kang, S. J. Rhee, Changhwan Choi,Mohammad Shahariar Akbar, and Jack C. Lee, "The electrical and material characterization of hafnium oxynitride gate dielectrics with TaN-gate electrode", *IEEE Trans. Electron Devices*, Vol. 51, Issue: 2, Feb. 2004, pp.220-227

[60] R. Degraeve, J. L. Ogier, R. Bellens, P. J. Roussel, G. Groeseneken, and H. E. Maes, "A new model for the field dependence of intrinsic and extrinsic Time-Dependent Dielectric Breakdown", *IEEE Trans. Electron Devices*, Vol. 45, Issue: 2, Feb. 1998, pp.472-481

[61] Y. H. Kim, R. Choi, R. Jha, J. H. Lee, V. Misra, and J. C. Lee, "Effects of gate electrodes and barrier heights on the breakdown characteristics and weibull slopes of HfO_2 MOS devices", *IEEE* International Reliability Physics Symposium, 2004, pp.595-596

[62] R. Degraeve, T. Kauerauf, A. Kerber, E. Cartier, B. Govoreanu, Ph. Roussel, L. Pantisano, P. Blomme, B. Kaczer, and G.. Groeseneken, "Stress polarity dependence of degradation and breakdown of SiO_2/high-k stacks", *IEEE* International Reliability Physics Symposium, 2003, pp.23-28

[63] W-Y. Loh, B. J. Cho, M. S. Joo, M-F. Li, D. S. H. Chan, and D-L. Kwong, "Charge trapping and breakdown mechanism in HfAlO/TaN gate stack analyzed using carrier separation", *IEEE Trans. Device and materials reliability*, Vol. 4, NO.2, Dec. 2004, pp.696-703

[64] T. Yamaguchi, T. Ino, H. Satake, and N. Fukushima, "Novel dielectric breakdown model of Hf-silicate with high temperature annealing", *IEEE* International Reliability Physics

Symposium, 2003, pp.34-40