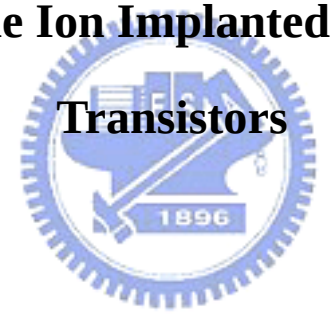
國立交通大學

電子工程學系　　電子研究所碩士班

碩士論文

氟離子佈植對低溫多晶矽薄膜電晶體之研究

The Study on Fluorine Ion Implanted Polysilicon Thin Film Transistors



研 究 生: 楊哲育

指導教授: 張俊彥　　博士

張鼎張　　博士

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The Study on Fluorine Ion Implanted Poly-Si Thin Film Transistors

研 究 生：楊哲育　　Student：Che-Yu Yang

指導教授：張俊彥 博士　　Advisor：Dr. Chun-Yen Chang

張鼎張 博士　　Dr. Ting-Chang Chang

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氟離子佈植對低溫多晶矽薄膜電晶體之研究

研究生:楊哲育　　指導教授:張俊彥&張鼎張

國立交通大學

電子工程學系　電子研究所碩士班

摘要

本論文主要在研究氟離子佈值對多晶矽薄膜電晶體特性的影響，在製程步驟上，我們並不沉積襯墊氧化層(pad oxide)來使氟離子堆積在多晶矽通道與氧化層介面，而是直接利用熱退火步驟產生的氧化層來代替積襯墊氧化層的角色，因而能在減少製程的步驟情況下，同樣得到氟離子鈍化(passivation)缺陷的效果。

由實驗結果顯示在 $5x10^{13}cm^{-2}$的劑量下，不管是利用固相結晶法(solid phase crystallization)，或是準分子雷射退火結晶法(excimer laser annealing)製作的元件，其特性將得到改善，包括較高的遷移率(mobility)、開關電流比(on/off ratio)、較陡峭的次臨界導通斜率(subthreshold swing)與較佳的可靠度(relibility)。這是由於氟離子可以打斷扭曲的鍵結，如矽-氧-矽或

矽-矽的鍵結，形成強度較高的矽-氟鍵，使應力得到舒緩，以減少tail state的數目，氟離子也會和一些斷鍵(dangling bonds)鍵結，讓deep state的數目降低，此外，由於矽-氟鍵的鍵結強度比矽-氫鍵結高，因而能得到比一般薄膜電晶體更佳的可靠度。實驗結果也顯示當劑量增加時，元件的特性將反而劣化，由萃取缺陷密度的結果，我們發現過量的氟離子反而會導致較高的缺陷密度，因而使元件的電性劣化。

由於此製程只需外加一道氟離子佈植的製程，因此可以較低的製程成本與複雜度來達到元件效能的提升，此元件可被運用於高效能的複晶矽薄膜電晶體之運用，尤其是在主動式薄膜電晶體液晶顯示器(AMLCD)，以及三維立體的金氧半場效電晶體電路。

The Study on Fluorine Ion Implanted Poly-Si Thin Film Transistors

Student :Che-Yu Yang Advisor :Dr. Chun-Yen Chang & Dr. Ting-Chang Chang

Department of *Electronics* &

Institute of Electronics, National Chiao Tung University

Abstract

In this thesis, Polycrystalline silicon thin film transistors (Poly-Si TFTs) with fluorine ion implantation was investigated. In the process step, we used the surface-oxidized Si generated during thermal annealing in place of the pad oxide to make the drive force for fluorine atoms segregated to the poly-Si/oxide interface. Compared to the conventional fluorine incorporated poly-Si TFTs technology, the method we proposed needed no extra thermal annealing step and additional process steps.

From the experiment result, it is found that the electrical characteristics of solid phase re-crystallized (SPC) and excimer laser annealing (ELA) fluorine ion implanted poly-Si TFTs will be improved, such as a higher mobility (μ_{FE}), a higher on/off current ratio (*Ion/Ioff*), a steep subthreshold swing (*S.S*) and a improved reliability. It is believed that the fluorine atoms can break the stress induced strained bonds, likely

the strained Si-O-Si bonds and Si-Si bonds to form stronger Si-F bonds, leading to local stress relaxation and thus decreasing the tail state density. Moreover, the fluorine atoms in the poly-Si channel can also passivate the dangling bonds to decrease deep state density. In addition, the Si-F bonds is stronger than Si-H bonds, result in the improved reliability compared to conventional TFT. Experiment result show that the over amount of fluorine ion implantation doses cause the degraded electrical characteristics, result from the increase of the trap state density.

This process only needs to increase one additional fluorine ion implantation process. The device can be improved by low cost and complication. Such TFTs are thus highly promising for use in future high-performance poly-Si TFT applications, especially in AMLCD and 3D MOSFET stacked circuits.

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僅以此篇論文獻給我親愛的父母，感謝他們多年來的支持與鼓勵，讓我能無後顧之憂的從事實驗研究，順利完成我的學業。

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同時要感謝和我一起奮鬥的同學，立偉、武陵、道彥、兆欽等...由於各位的勉勵和幫助才讓此論文得以如期完成。最後感謝國家奈米元件實驗室提供良好的設備和研究環境，以及相關人員的協助。

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$V_D = V_G = 20V$.

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Chapter 1
Introduction

1-1. Overview of Poly-silicon Thin-Film Transistor Technology

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have drawn much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1], and organic light-emitting displays (OLEDs) [2]. Except large area displays, poly-Si TFTs also have been applied into some memory devices such as dynamic random access memories (DRAMs) [3], static random access memories (SRAMs) [4], electrical programming read only memories (EPROM) [5], electrical erasable programming read only memories (EEPROMs) [6], linear image sensors [7], thermal printer heads [8], photo-detector amplifier [9], scanner [10], neutral networks [10]. Lately, some superior performances of poly-Si TFTs also have been reported by scaling down device dimension or utilizing novel crystallization technologies to enhance poly-Si film quality [11-12]. This provides the opportunity of using poly-Si TFTs into three-dimension (3-D) integrated circuit fabrication. Of course, the application in AMLCDs is the primary trend, leading to rapid developing of poly-Si TFT technology.

The major attraction of applying polycrystalline silicon thin-film transistors (poly-Si TFTs) in active matrix liquid crystal display (AMLCDs) lies in the greatly improved carrier mobility in poly-Si film and the capability of integrating the pixel switching elements and the capability to integrate panel array and peripheral driving circuit on the same substrates [13-15]. In poly-Si film, carrier mobility larger than 15

cm^2/Vs can be easily achieved, that is enough to used as peripheral driving circuit including n- and p-channel devices. This enables the fabrication of peripheral circuit and TFT array on the same glass substrate, bring the era of system-on-glass (SOG) technology. The process complexity can be greatly simplified to lower the cost. In addition, the mobility of poly-Si TFTs is much better than that of amorphous ones, the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high density、high resolution AMLCDs, and the aperture ratio in TFT array can be significantly improved by using poly-Si TFTs as pixel switching elements. This is because that the device channel width can be scaled down while meeting the same pixel driving requirements as in α-Si TFT AMLCDs.

For making high performance poly-crystalline silicon (poly-Si) thin film transistors (TFTs) [16], low-temperature technology is required for the realization of commercial flat-panel displays (FPD) on inexpensive glass substrate, since the maximum process temperature is limited to less than 600^0C. There three major low-temperature amorphous-Si crystallization methods to achieve high performance poly-Si thin film, solid phase crystallization (SPC), excimer laser crystallization (ELC), and Metal-Induced Lateral Crystallization (MILC)

However, some problems still exist in applying poly-Si TFTs on large-area displays. In comparison with single-crystalline silicon, poly-Si is rich in grain boundary defects as well as intra-grain defects, and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain boundary regions to degrade the ON current seriously [17]. Moreover, the relatively large leakage current is one of the most important issues of conventional poly-Si TFTs under OFF-state operation [18-19]. In most application, a low-cost substrate is essential and therefore a low temperature process (i.e., <650°C) compatible with glass

substrates is developed [20]. In summary, it is expected that the poly-Si TFTs will becomes more important in future technologies, especially when the 3-D circuit integration era is coming. More researches studying the related new technologies and the underlying mechanisms in poly-Si devices with shrinking dimensions are therefore worthy to be indulged in.

1-2. Defects in Poly-Si Film

Due to the granular structure of the poly-Si film, a lot of grain boundaries and intragranular defects exist in the film. The dangling bonds in grain boundaries will affect device characteristics seriously because they act as trapping centers to trap carriers. Carriers trapped by these low energy traps can no longer contribute to conduction, which results in the formation of local depletion region and potential barriers in these grain boundaries. Thus, the typical characteristics such as threshold voltage, subthreshold swing, ON current, mobility and transconductance of TFTs are inferior to those of devices fabricated on single crystal silicon film. As for the leakage current, it is well known that the leakage current increase with the drain voltage and gate voltage. The dominant mechanism of the leakage current is field emission via grain boundary traps due to the high electric field near the drain junction [21-24].

To overcome this inherent disadvantage of poly-Si film, many researches have been focused on modifying or eliminating these grain boundary traps. Traps are associated with dangling bonds arising from lattice discontinuities between different oriented grains or at the Si/SiO_2 interface. The most useful method so far to remove traps is to passivate these dangling bonds, such as hydrogen plasma treatment has been utilized for the passivation [25-26], but it is difficult to control the hydrogen

concentration in the TFT. The Si-H bonds may be broken under hot-carrier stress [27-28], leading to degradation of electrical characteristics after a long-term operation time. As the number of trapped carrier decreases, the potential barriers in grain boundaries decrease. And the leakage current decreases because of the fewer trap density near the drain region.

1-3. Motivation

To meet the requirement of higher circuit density and higher speed, it is necessary to improve the performance of the poly-Si TFTs. However, it has been shown that the performances of poly-Si are affected by the trap states at grain boundaries. In the preview research, Enlarging the grain size and passivating the defects at the grain boundary were widely used methods to reduce the trap states in the grain boundary. Generally, hydrogen plasma treatment has been utilized for the passivation, but it is difficult to control the hydrogen concentration in the TFTs. In recent years, fluorine ion implantation was applied to improve the electrical characteristics by eliminating the defects in the grain boundary [29-30]. It is found that the fluorine atoms piled up at the interface between the poly-Si and oxide to break the stress induced strained bonds to form stronger Si-F bonds, leading to local stress relaxation and thus decreasing the tail state density [31]. The fluorine atoms can also be the terminator of dangling bonding in poly-Si. Hence, the TFT with fluorine implantation has the superior electrical characteristics than conventional poly-Si TFTs. However, it needs additional oxide layer deposition and additional thermal annealing. The extra process steps will increase the difficulty for the fabrication of poly-Si TFTs. In this work, the electrical characteristics behaviors of poly-Si TFTs by various

fluorine ion implantation dosages were investigated. In addition, there was no any pad oxide deposited firstly before thermal annealing. Hence, it also needed no additional thermal annealing step. The electrical characteristics, including I-V measurement and DC bias stress reliability, were reported in this study.

1-4. Thesis Outline

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Chapter 2

Poly-Si conduction mechanism

2-1. Transport Properties of Poly-Si

As mentioned in section 1-1 and 1-2, the device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. Even though the inversion channel region is also induced by the gate voltage as in MOSFETs, the existence of grain structure in channel layer bring large differences in carrier transport phenomenon. Many researches studying the electrical properties and the carrier transport in poly-Si TFTs have been reported. A simple grain boundary-trapping model has been described by many authors in details [1-3]. In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size L_g and the grain boundary trap density N_t. The charge trapped at grain boundaries is compensated by oppositely charged depletion regions surrounding the grain boundaries. It is shown in Figure. 2-1. From Poisson's equation, the charge in the depletion regions causes curvature in the energy bands, leading to potential barriers that impede the movement of any remaining free carriers from one grain to another. When the dopant/carrier density n is small, the poly-Si grains will be fully

depleted. The width of the grain boundary depletion region x_d extends to be $L_g/2$ on each side of the boundary, and the barrier height V_B can be expressed as

$$V_B = \frac{qn}{2\varepsilon_s} x_d^{\,2} = \frac{qnL_g^{\,2}}{8\varepsilon_s} \tag{2-1}$$

As the dopant/carrier concentration is increased, more carriers are trapped at the grain boundary. The curvature of the energy band and the height of potential barrier increase, making carrier transport form one grain to another more difficult. When the dopant/carrier density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si grains turn to be partially depleted and excess free carriers start to spear inside the grain region. The depletion width and the barrier height can be expressed as

$$x_d = \frac{N_t}{2n} \tag{2-2}$$

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t^{\,2}}{8\varepsilon_s n} \tag{2-3}$$

The depletion width and the barrier height turn to decrease with increasing dopant/carrier density, leading to improved conductivity in carrier transport.

The carrier transport in fully depleted poly-Si film can be described by the thermionic emission over the barrier. Its' current density can be written as [4].

$$J = qnv_c \exp[-\frac{q}{kT}(V_B - V)] \tag{2-4}$$

where n is the free-carrier density, v_c is the collection velocity ($v_c = \sqrt{kT/2\pi m^*}$), V_B is the barrier height without applied bias, and V_g is the applied bias across the grain

boundary region. For small applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decreases by an amount of $V_g/2$. In the reserve-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J_F = qnv_c \exp[-\frac{q}{kT}(V_B - \frac{1}{2}V_g] \tag{2-5}$$

$$J_R = qnv_c \exp[-\frac{q}{kT}(V_B + \frac{1}{2}V_g)] \tag{2-6}$$

the net current density is then given by

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_g}{2kT}) \tag{2-7}$$

at low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage kT/q, Eq. (1.7) then can be simplified as

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\frac{qV_g}{2kT} = \frac{q^2nv_cV_g}{kT}[\exp(-\frac{qV_B}{kT})] \tag{2-8}$$

the average conductivity $\sigma = J / E = JL_g / V_g$ and the effective mobility $\mu_{eff} = \sigma / qn$ then can be obtained

$$\sigma = \frac{q^2nv_cL_g}{kT}\exp(-\frac{qV_B}{kT}) \tag{2-9}$$

$$\mu_{eff} = \frac{qv_cL_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv \mu_0 \exp(-\frac{qV_B}{kT}) \tag{2-10}$$

where μ_0 represents the carrier mobility inside grain regions. It is found that the conduction in poly-Si is an activated process with activation energy of approximately qV_B, which depends on the dopant/carrier concentration and the grain boundary trap

density.

Applying gradual channel approximation to poly-Si TFTs, which assumes that the variation of the electric field in the y-direction (along the channel) is much less than the corresponding variation in the z-direction (perpendicular to the channel), as shown Fig. 2-2. The carrier density n per unit area (cm^{-2}) induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_{TH} - V_{(y)})}{qt_{ch}} \tag{2-11}$$

$$I_D = \iint J.dx.dz = \iint nq\mu_{eff}.\frac{dv_y}{dy}.dx.dz \tag{2-12}$$

$$= \int_0^W \mu_{eff}\,dz \int_0^{t_{ch}} nqdx.\frac{dV_y}{dy} = W\mu_{eff}.C_{ox}(V_g - V_{th} - V_y)\frac{dV_y}{dy}$$

where t_{ch} is the thickness of the inversion layer. Therefore, the drain current I_D of poly-Si TFT then can be given by

$$\int_0^L I_D dy = W\mu_{ff}C_{ox}\left[(V_g - V_{th})V_D - \frac{1}{2}V_D{}^2\right]$$

$$I_D = \frac{W}{L}\mu_{ff}C_{ox}\left[(V_g - V_{th})V_D - \frac{1}{2}V_D{}^2\right] \tag{2-13}$$

Obviously, this I-V characteristic is very similar to that in MOSFETs, except that the mobility is modified.

2-2. Non-ideal Effect

There are two major non-ideal effects will limit the TFTs application, including leakage current and kink-effect. The mechanism of these two non-ideal effects is

described briefly as bellow.

2-2-1. Leakage current

In AMLCD, TFTs play a switching device to turn ON/OFF the current path for charging/discharging the liquid crystal capacitor. Thus, the leakage current should be low enough to remain a pixel gray level before it must be refreshed. The leakage current mechanism in poly-Si has been studied by Olasupe [5]. The leakage current resulted from carrier generation from the poly-Si grain boundary defects. There are three major leakage mechanisms, as shown in Fig. 2-3. The dominant mechanism is a function of the prevailing drain bias. They pointed out carrier generation from grain boundary defects via thermionic emission and thermionic field emission to be prevalent at a low and medium drain biases, and carrier pure tunneling from poly-Si grain boundary defects to be the dominant mechanism at higher drain bias.

2-2-2. Kink effect[6]

During devices operation, a high field near the drain could induce impact ionization there. Majority carriers, holes in the p-substrate for an n-channel poly-Si TFTs, generated by impact ionization will be stored in the substrate, since there is no substrate contact to drain away these charges. Therefore the substrate potential will be

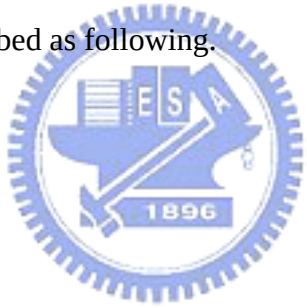
changed and will result in a reduction of the threshold voltage. This, in turn, may cause an increase or a kink in the current-voltage characteristics. The kink phenomenon is shown in Fig. 2-4. This float-body or kink effect is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons. The kink effect can be eliminated by forming a substrate contact to the source of the transistor.

Chapter 3

Experiment

3-1. Fabrication Process of Poly-Si TFTs

In this thesis, the poly-Si TFTs with various Fluorine ion implantation doses were proposed and fabricated. The top view of the devices and the schematic cross section view of devices were shown in Fig. 3-1 and Fig. 3-2, respectively. The fabrication procedure is described as following.



Step1. Substrate.

6-inch 100-mm-thick p-type single-crystal silicon wafers with (100) orientation were used as the starting materials. After a standard cleaning procedure, silicon wafers were coated with 500-nm-thick thermally grown SiO_2 in steam oxygen ambient at 1000ºC. In order to simulate the thin film transistor environment, the thick thermal oxide was grown on Si wafers.

Step2. Amorphous-Si thin film formation .

Undoped amorphous-Si(a-Si) layers of thickness about 50-nm were deposited by

low pressure chemical vapor deposition (LPCVD) on oxide by pyrolysis of silane (SiH_4) at 550ºC. The transition temperature of Si material is about 575 ºC.

Step3. Fluorine ion implantation

The fluorine ions implanted to the middle of the amorphous-Si layer without any pad oxide deposition first. The ion accelerating energy is 11 KeV and the doping dosages are $5x10^{13}$, $5x10^{14}$ and $5x10^{15}$ cm^{-2}, respectively.

Step4-1. Poly-Si thin film formation (solid phase crystallization) .

The amorphous-Si films were recrystallized by solid phase crystallization (SPC) method at 600ºC for 24hrs in N_2 ambient. Then, the active regions were defined and etched. The etching was performed by dry etching by using transformer couple plasma (TCP) etching system.

Step4-2. Poly-Si thin film formation (excimer laser annealing) .

The amorphous-Si films were recrystallized by excimer laser annealing (ELA) method at room temperature with an energy density of 300 mJ/cm^2. Then, the active regions were defined and etched. The etching was performed by dry etching by using transformer couple plasma (TCP) etching system.

Step5. Gate oxide formation.

After defining the active region, the photoresist was removed by using O_3 plasma etching and pure H_2SO_4 solution. The following step was to remove the polymer which was formed during the plasma etching. The remove for residue of polymer was realized by SC1 solution ($NH_4OH:H_2O_2:H_2O=0.25:1:5$). Before gate oxide deposition, the STD clean was used to clean the wafers. The HF dip was necessary to remove the native oxide at the poly-Si surface. Then, a 50nm layer of tetra-ethyl-ortho-silicate (TEOS) gate oxide was deposited by LPCVD at 700^0C. The thickness of gate oxide was determined by N&K optical analyzer.

Step6. Gate electrode formation.

After deposition of gate insulators, 200-nm-thick poly-silicon films were formed immediately on the gate insulators by LPCVD at 620°C. There was no any chemical solution clean between the deposition of TEOS oxide and poly-Si gate. The second poly-Si layer was then patterned by transformer couple plasma (TCP) etching to define the gate regions.

Step7. Source/drain formation.

After the gate definition, source and drain regions were formed by phosphorous

ions implantation. The ion accelerating energy is at 17 KeV and the dosage is $5x10^{15}$ cm^{-2}.

Step8. Passivation layer and contact hole formation.

The activation of source/drain regions was performed by the thermal budget of passivation layer deposition. The passivation layer was used TEOS oxide by LPCVD system. The duration and the temperature of passivation deposition were 3hrs and 700C, respectively. After the deposition of passivation layer, the activation was also finished. The passivation layer was 500-nm-thick to cap the poly-Si TFTs devices. The contact holes were patterned and then etched by buffer oxide etching (BOE) solution. The size of contact holes were 5x5 um^2.

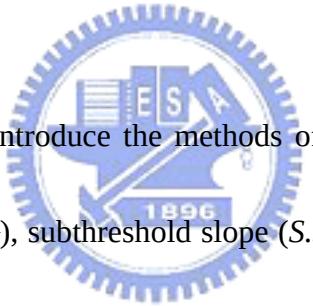
Step9. Metallization.

The 500-nm aluminum layers were deposited by physical vapor deposition (PVD) and then patterned at the source, drain, and gate electrode as the metal pads. Finally, the devices were sintered at 350°C in hydrogen ambient for 30 min.

3-2. Measurement

In this thesis, the thickness of poly-Si, amorphous-Si, and TEOS oxide films were measured by N&K analyzer. The current-voltage characteristic measurement of thin film transistor devices was performed by KEITHLEY 4200 semiconductor parameter analyzer with source grounded and body floating.

3-3. Methods of Device Parameter Extraction



In this section, we will introduce the methods of typical parameters extraction such as threshold voltage (V_{TH}), subthreshold slope (*S.S*), drain current ON/OFF ratio (I_{ON}/I_{OFF})**,** field-effect mobility (μ_{FE}) and the trap density (*Nt*) inside the channel.

3-3-1. Determination of the threshold voltage

Many methods are used to determinate the threshold voltage (V_{TH}) which is the most important parameter required for TFT application. In poly-Si TFTs, the method used to determinate the threshold voltage is constant drain current method where the gate voltage at a specified drain current I_N value is taken as the threshold voltage. This technique is adopted in most studies of TFTs. Typically, the threshold current $I_N = I_D /$

(W_{eff}/ L_{eff}) is specified at 10 nA for V_D = 0.1V (linear region) and 100 nA for V_D = 5V (saturation region) in most papers to extract the threshold voltage of poly-Si TFTs.

3-3-2. Determination of the subthreshold swing

Subthreshold swing (V/dec.) is a typical parameter to describe the gate control ability of gate toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, subthreshold swing might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The subthreshold swing is also related to gate voltage due to undesirable factors such as serial resistance and interface state.

In this experiment, the subthreshold swing is defined as the gate voltage required to decrease the threshold current by one orders of magnitude (from 10^{-9}A to 10^{-10}A).

3-3-3. Determination of On/Off Current Ratio

Drain On/Off current ratio is another important factor of TFTs. High On/Off ratio represents not only large turn-on current but also small off current (leakage current). It affects gray levels (the bright to dark state number) of TFT AMLCD directly.

There are a lot of methods to specify the on and off current. In this experiment, the On current is equal to the maximum current, and the off current is defined as minimum leakage current while drain voltage is applied at 0.1V.

3-3-4. Determination of the field-effect mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain voltage (V_D=0.1V). The transfer I-V characteristics of poly-Si TFT can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{TH})V_D - \frac{1}{2}V_D{}^2] \quad (3\text{-}1)$$

where

C_{ox} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{TH} is the threshold voltage.

If V_D is much smaller than V_G-V_{TH} (i.e. $V_D << V_G$-V_{TH}) and $V_G > V_{TH}$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \quad (3\text{-}2)$$

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \quad (3\text{-}3)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \qquad (3\text{-}4)$$

3-3-5. Determination of the poly-Si grain boundary trap density

As described in Eq. (2-3), the grain boundary potential barrier height V_B is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density N_t can be extracted from the current-voltage characteristics of poly-Si TFTs. As proposed by Levinson *et al*[1], the *I-V* characteristics including the trap density can be obtained by :

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D \exp\left(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox} (V_G - V_{TH})}\right) \qquad (3\text{-}5)$$

This equation had been further corrected by Proano et al. by considering the mobility under low gate bias. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. Moreover, a better approximation for channel thickness tch in an undoped material is given by defining the channel thickness as the thickness at which 80 percent of the total charge resides. Therefore, by solving the poisson's equation, the channel thickness is given by :

$$t_{ch} = \frac{8KT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})}$$

The drain current of TFTs should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \exp(-\frac{q^2 N_t^{\ 2}\sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^{\ 2}(V_G - V_{FB})^2})$$

The effective trap state density then can be obtained from the slope of the curve $\ln[I_D/(V_G-V_{FB})]$versus$(V_G-V_{FB})^{-2}$.

Chapter 4

Results and discussion

4-1. Poly-Silicon Thin Film Transistor Fabricated by Solid Phase Crystallization (SPC) Method

4-1-1. Device characteristic of poly-silicon TFTs

Figure. 4-1 and Fig. 4-2 show typical transfer characteristics for various fluorine ion implantation dosages and standard poly-Si TFTs at V_D=0.1V and V_D=5V, respectively. Table I lists key parameters of poly-Si TFTs. Fig. 4-3 to 4-6 show the TFTs' field effect mobility (μ_{FE}), threshold voltage (V_{TH}), subthreshold swing (*S.S*) and ON/OFF ratio (*Ion/Ioff*) versus different fluorine ion implantation dosage. This result showed that the electrical characteristics could be improved for the fluorine ion implantation dosage was at $5x10^{13}$ cm^{-2}. The field effect mobility increased from 19.74 to 54.48 cm^2/volt-sec. The decreasing V_{TH}, steep *S.S* and high On/Off ratio make it more potential for poly-Si TFTs application. As the implantation dosage increased to $5x10^{14}cm^{-2}$, the electrical characteristics had a little degradation compared with $5x10^{13}$ cm^{-2} implanted devices, but it was still better than conventional poly-Si TFTs. When the implantation dosage was $5x10^{15}$ cm^{-2}, the electrical

characteristics were degraded seriously as shown in experimental result. It was found that the over amount of fluorine ion implantation doses caused the degraded electrical characteristics. The mechanism will be discussed in the following sections.

The output characteristics of the fluorine implanted TFT and standard TFT are compared as shown in Fig. 4-7. It was found that the TFT with $5x10^{13}$ cm^{-2} implantation doses had the highest drain current in the same drain voltage, and drain current had degradation when the implantation dosage increased. This trend is the same as the transfer characteristics as shown in Fig. 4-1 and Fig. 4-2.

4-1-2. The effects of fluorine passvation

Figure. 4-8 shows the secondary-ion mass spectrometry (SIMS) depth profile of fluorine with different dosage. The depth profile showed a high concentration of fluorine near the poly-Si/oxide interface and surface. During the solid phase re-crystallization, the fluorine atoms segregated to the surface of poly-Si and the interface between poly-Si and oxide. It is believed that the surface-oxidized Si made the drive force for fluorine atoms segregated to the surface of poly-Si. Compared to the conventional fluorine ion incorporated poly-Si TFTs technology [1], the method we proposed needed no extra thermal annealing step and additional process steps.

Figure.4-9 shows the trap state density with different Fluorine ion implantation

dosages. It was known that the electrical characteristics of poly-Si TFTs, such as field effect mobility (μ_{FE}), threshold voltage (V_{TH}), subthreshold swing (*S.S*) and ON/OFF ratio (*Ion/Ioff*), were affected by the trap state density [2-4]. The trap state density *(Nt)* of fluorine atoms incorporated poly-Si were various with the implantation dose in our experimental. As shown in Fig. 4-9, the implantation dosage of $5x10^{13}cm^{-2}$ leaded to the decreased trap state density. We could calculate that the average fluorine concentration in poly-Si was about $10^{14}cm^{-3}$($\frac{10\mu m * 5 * 10^{13} cm^{-2}}{50nm}$), which was enough to passivate the defects in the poly-Si. As the implantation dose increasing, the trap state density increased. The over amount implantation doses caused even more trap state density than conventional poly-Si TFTs. It was reported that the fluorine atoms can break the stress induced strained bonds, likely the strained Si-O-Si bonds and Si-Si bonds to form stronger Si-F bonds, leading to local stress relaxation and thus decreasing the tail state density. Moreover, the fluorine atoms in the poly-Si channel can also passivate the dangling bonds to decrease deep state density [1], resulted in the subthreshold swing of the implanted device were improved. Fig.4-10 shows the scanning electron microscope (SEM) image of poly-Si grain with different fluorine dose after SPC method. It was found that the grain size didn't vary obviously when the fluorine implantation dose was $5x10^{13}cm^{-2}$ and $5x10^{14}cm^{-2}$. However, the grain size decreased obviously when the implantation dose was $5x10^{15}cm^{-2}$. This result

showed that the higher concentration of fluorine atoms may hinder the grain growth, which caused increase of trap state density. In addition, the fluorine atoms behave as acceptors with their energy level in the valence band, and further shift the Fermi level toward the valence band [5]. This effect made the threshold voltage of $5x10^{14}cm^{-2}$ implantation dosage become higher than that of standard TFT, which was different from the other parameter. Moreover, the over amount fluorine atoms might form the clusters [6], it also increased the trap states, resulted in the degradation of the electrical characteristics, such as μ_{FE}, *Vth*, *S.S* and *Ion/Ioff* in the experimental result.

It was clear that the fluorine ions played two important roles in the poly-Si TFTs. One was the trap state density terminal, the other was the hole generator. In order to eliminate the trap state density, the over amount fluorine ions dosage was concerned. However, the extra trap states were generated to cause serious degraded electrical characteristics, resulted from the reduction of grain size and the formation of the clusters. From our experimental result, the appropriated fluorine ion implantation dose was $5x10^{13}cm^{-2}$.

4-1-3. The activation energy variation with fluorine incorporation

Fig. 4-11 shows the activation energy of drain current as a function of gate voltage measured at V_D=5V for standard and fluorine ions implanted poly-Si TFTs.

The activation energy was extracted by the measurement of I_D-V_G characteristic in the temperature range from 20°C to 150°C. From the equation $I_D = I_0 e^{\frac{-Ea}{KT}}$, using the linear fitting of the ln(I_D) versus the 1/KT plot. Then the activation energy can be obtained. K is the Boltzmann constant and T is the temperature. In the preview research [7], the activation energy mean the carriers transportability which was related with the barrier height in the poly-Si channel. It was found that the activation energy was reduced for fluorine ions implanted poly-Si TFTs. It implied that the trap density eliminate by using fluorine ions implantation. This result is consistent with the above discussion.

4-1-4. Stress result of poly-Si TFTs with/without fluorine implantation

The reliability for various fluorine ion dosage implanted poly-Si TFTs were also investigated in this study. Fig. 4-12 to 4-14 shows threshold voltage variation ($\triangle V_{TH}$) , On current degradation and subthreshold swing variation ($\triangle S.S$) versus stress time with/without fluorine implantation, and the stress condition was V_D=V_G=20V. The stress time is 0, 100, 200, 600, 1000, 2000, 6000, 10000sec. It was found that the standard TFT showed serious degradation compared with the TFT with Fluorine implantation. Degradation of V_{TH}, *Ion* and *S.S* is resulted from hot carrier multiplication near the drain side [8]. It was reported that the hot-carrier stress

induced degradation is attributed to the generation of gate-oxide/poly-Si interface states and/or the breaking of the Si-Si and/or Si-H weak bonds in the poly-Si channel [9-10]. Thus, the fluorine implanted into the channel with an appropriate dosage would result in the passivation of trap states and the formation of strong Si-F bonds in place of the weak Si-Si and Si-H bonds. The table Ⅱ shows the association energy of the different bonding. It is found the the Si-F bonds have the highest association energy, which lead to superior reliability of fluorine implanted poly-Si TFTs in comparison with TFTs without fluorine implantation.

4-2. Poly-Silicon Thin Film Transistor Fabricated by Excimer Laser Annealing(ELA) Method

4-2-1. Device characteristic of poly-silicon TFTs

Figure. 4-15 and 4-16 show typical transfer characteristics with various fluorine ion implantation dosages and standard poly-Si TFTs at $V_D=0.1V$ and $V_D=5V$ respectively. Table Ⅲ lists key parameters of poly-Si TFTs. Fig. 4-17 to 4-20 show the TFTs' field effect mobility (μ_{FE}), threshold voltage (V_{TH}), subthreshold swing (*S.S*) and ON/OFF ratio (*Ion/Ioff*) versus different fluorine ion implantation dosages. These result show that the electrical characteristics can be improved for the Fluorine ion implantation dosage is at $5x10^{13}$ cm^{-2}, which have good agreement with the SPC poly-Si TFT. It was also found that the electrical characteristics were degraded seriously when the implantation dosage increased to $5x10^{15}$ cm^{-2}.

The output characteristics of the fluorine implanted TFT and standard TFT are compared as shown in Fig. 4-21. It was found that the TFT with implantation dosage of $5\times10^{13}cm^{-2}$ owned the largest drain current in this work. However, drain current was degraded when the implantation dosage increase. This trend is the same as the output characteristics of the SPC poly-Si TFTs as shown in Fig. 4-7.

4-2-2. The effects of fluorine passvation

Figure. 4-22 shows the secondary-ion mass spectrometry (SIMS) depth profile of fluorine with $5x10^{13}$ cm^{-2} dosages. The depth profile showed the same distribution as the SPC poly-Si TFTs. Fig. 4-23 shows the SEM result of poly-Si grain with different fluorine dose after ELA method. It was observed that the TFTs obtain the largest grain size with $5x10^{13}$ cm^{-2} fluorine doses. This result is different from solid phase crystallization (SPC) method. It was also observed that there were bubbles generated with $5x10^{15}$ cm^{-2} fluorine doses, resulted from the high temperature process during ELA. This result has a good agreement with the previous report [11-12]. Fig. 4-24 shows the trap state density *(Nt)* with different fluorine ion implantation dosages. It was found that the trap state density decreased obviously at implantation dosage $5x10^{13}$ cm^{-2}, and the passivation effect of trap state density for ELA method was more excellent than SPC method in the experimental results. This might result from the grain size increases at $5x10^{13}$ cm^{-2} implantation doses for ELA method. Hence, the trap state density can be effectively eliminated for ELA poly-Si TFTs.

However, it was found that the trap states increased with the implantation dosage, resulted from the the formation of the clusters and bubbles. This result was different as that of the SPC poly-Si TFTs.

4-2-3. The activation energy variation with fluorine incorporation

Fig. 4-25 shows the activation energy of drain current as a function of gate voltage measured at V_D=5 V for standard and fluorine ion implanted poly-Si TFTs. the activation energy was extracted by the measurement of I_D-V_G characteristic in the temperature range from 20°C to 150°C. It was found that the activation energy was reduced for fluorine ions implanted poly-Si TFTs when the devices turn on. It implied that the trap density eliminate by using fluorine ions implantation which is the same as the result of the SPC TFT. However, In the off state we found that the activation energy of the fluorine ions implanted TFTs was lower than that of the standard TFTs, resulted from large leakage current as shown in Fig. 4-15.

4-2-4. Stress result of poly-Si TFT with/without fluorine implantation

The reliability for various fluorine ion dosages implanted poly-Si TFTs were investigated in this study. Fig. 4-26 to 4-28 shows the threshold voltage variation ($\triangle V_{TH}$), On current degradation and subthreshold swing variation ($\triangle S.S$) versus stress time with/without fluorine implantation, and the stress condition was V_D=V_G=20V. It was found that the standard TFT shows serious degradation compared with the TFT with Fluorine implantation. The fluorine implanted into the channel

would result in the formation of Si-F bonds. The Si-F bonds have the higher association energy, which lead to superior reliability of fluorine implanted poly-Si TFTs in comparison with TFTs without fluorine implantation.

4-3. Comparison between SPC and ELA Poly-Silicon Thin Film Transistors

4-3-1. Comparison of the electrical characteristics improvement

Table III shows the electrical characteristics improvement by fluorine implantation of SPC and ELA poly-Si TFTs. It was found that the SPC TFTs showed higher field effect mobility (μ_{FE}) improvement than that of ELA TFTs by fluorine incorporation. However, the ELA poly-Si TFTs revealed higher improvement in threshold voltage (V_{TH}), subthreshold swing (*S.S*), ON/OFF ratio (*Ion/Ioff*) and trap state density *(Nt)*. Table IV shows the relation between the electrical parameter and the location of the trap states. It was found that the field effect mobility (μ_{FE}) is mainly affected by the amounts of tail states. Contrarily, threshold voltage (V_{TH}) and subthreshold swing (*S.S)* is affected by the amounts of deep states. This result indicated that the fluorine passivation of tail states for SPC TFTs was more effective than that for ELA TFTs, and the ELA TFTs had higher passivation effect for deep trap

states. It was also found that the ELA TFTs have lower trap states than SPC TFTs, resulted from the higher quality film formed by ELA method.

4-3-2. Comparison of the reliability between ELA and SPC TFTs

Figure. 4-29 to 4-31 shows the threshold voltage variation ($\triangle V_{TH}$), On current degradation and subthreshold swing variation ($\triangle S.S$) versus stress time of ELA and SPC TFT with/without fluorine implantation. It was found that the SPC TFTs showed better reliability than ELA TFTs. When the fluorine implanted, the improvement of On current degradation and subthreshold swing variation ($\triangle S.S$) was almost the same between the SPC and ELA TFTs. However, the ELA TFTs showed smaller threshold voltage variation ($\triangle V_{TH}$) than SPC TFTs with fluorine implantation, which was different from the result of On current degradation and subthreshold swing variation ($\triangle S.S$).

Chapter 5
CONCLUSION

The fluorine ion implanted poly-Si TFTs were investigated in this study. The implantation dosage affected the electrical characteristics of the poly-Si TFTs. We found that as the implantation dose is $5x10^{13}cm^{-2}$, the device has the lowest trap state density, result in the superior characteristics, such as a higher mobility, a lower threshold voltage, a steep subthreshold swing and high On/Off ratio. It is believed that the fluorine atoms can break the stress induced strained bonds, likely the strained Si-O-Si bonds and Si-Si bonds to form stronger Si-F bonds, leading to local stress relaxation and thus decreasing the tail state density. Moreover, the fluorine atoms in the poly-Si channel can also passivate the dangling bonds to decrease deep state density. In addition, the Si-F bonds is stronger, result in the improved reliability compared to conventional TFT. The electrical characteristic will be degraded as the fluorine ion implantation dosage is over-increasing, result from the formation of the cluster. The directly re-crystallized method made the fluorine atoms segregated in the poly-Si/gate oxide interface which reduced the process step compared to conventional fluorine ion implantation investigation. The fluorine ion implantation is consisted with the conventional poly-Si TFTs process flow and the process is uncomplicated.

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[4.11] C. W. Nieh and L. J. Chen, "Formation of bubbles in BF_2^+-implanted silicon, "*Appl. Phys Lett.* Vol.48, No.22, 1986.

[4.12] C. W. Nieh and L. J. Chen, "Cross-sectional transmission electron microscope study of residual defects in BF_2^+-implanted (001)Si, "*J. Appl. Phys.* Vol.60, 1986.

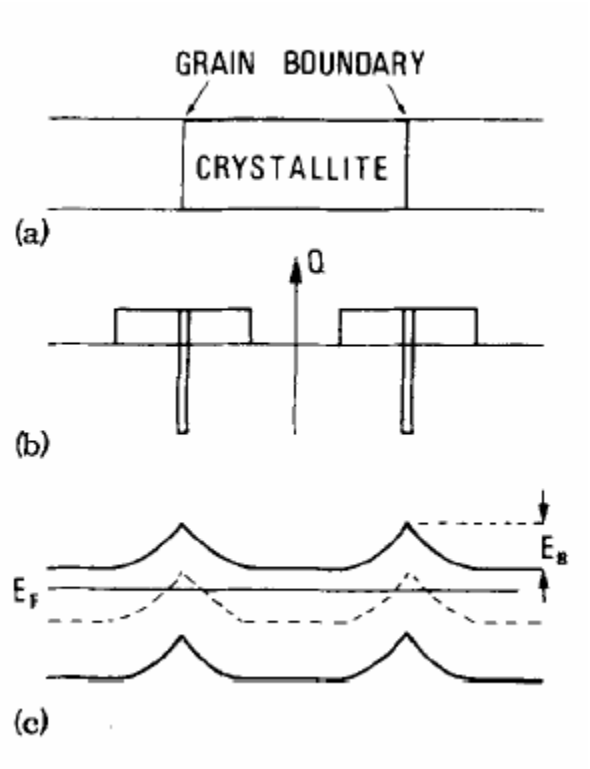

Fig. 2-1 Sketch of the band diagram of the polycrystalline silicon films

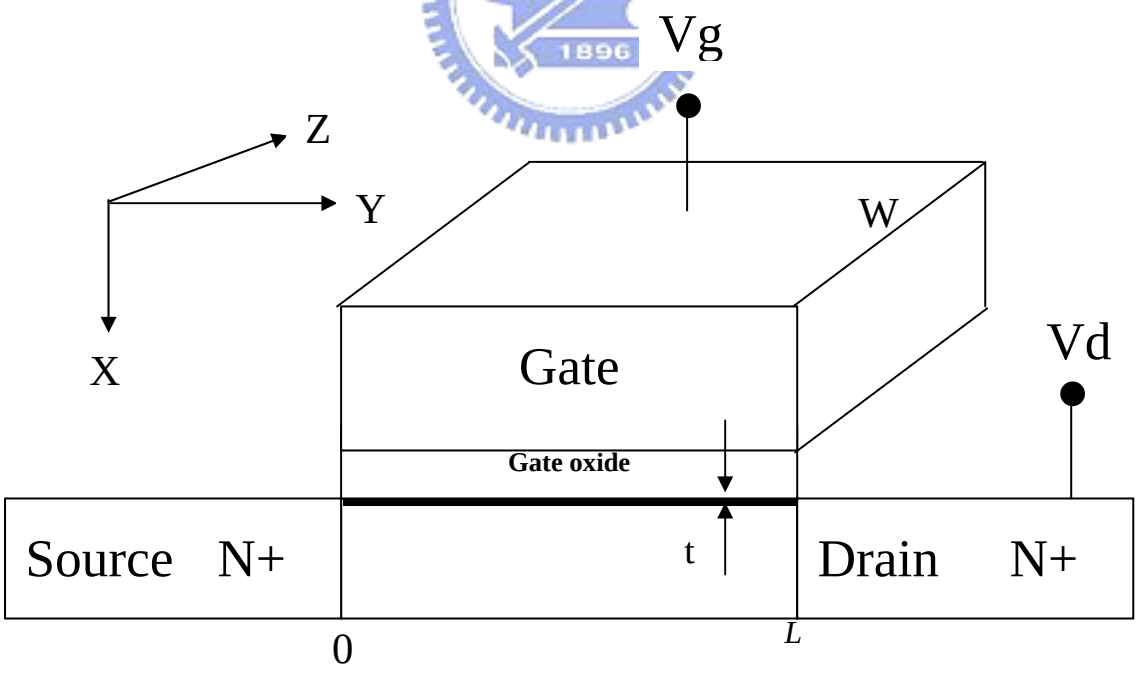

Fig. 2-2 A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model.

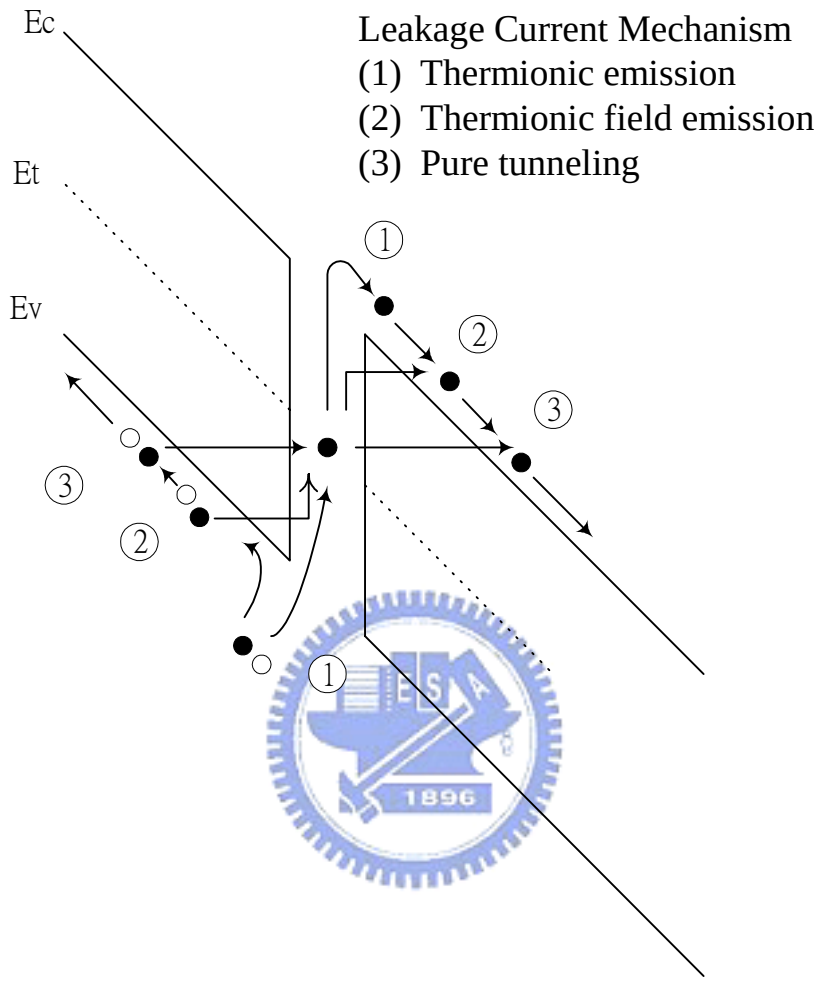

Fig. 2-3 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling

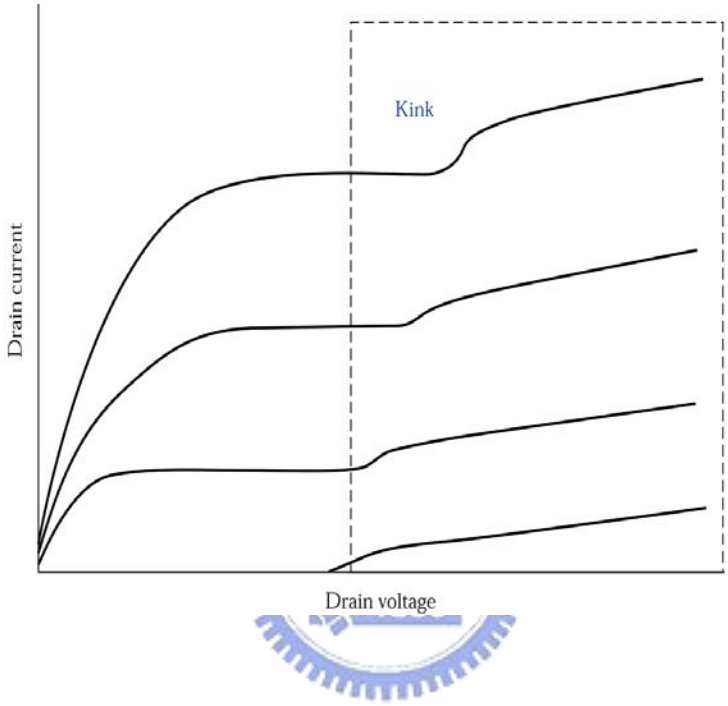

Fig. 2-4 The kink effect in the output characteristics of an *n*-channel SOI MOSFET[6]

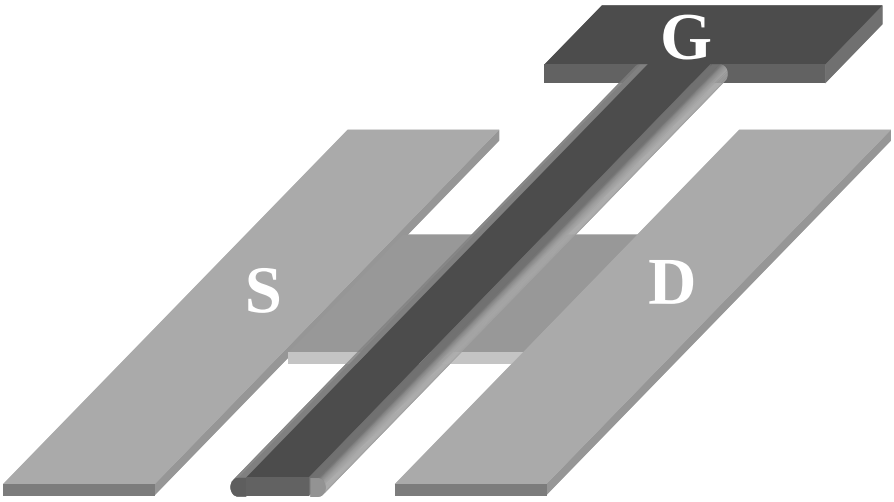

Fig 3-1 The top view of TFT

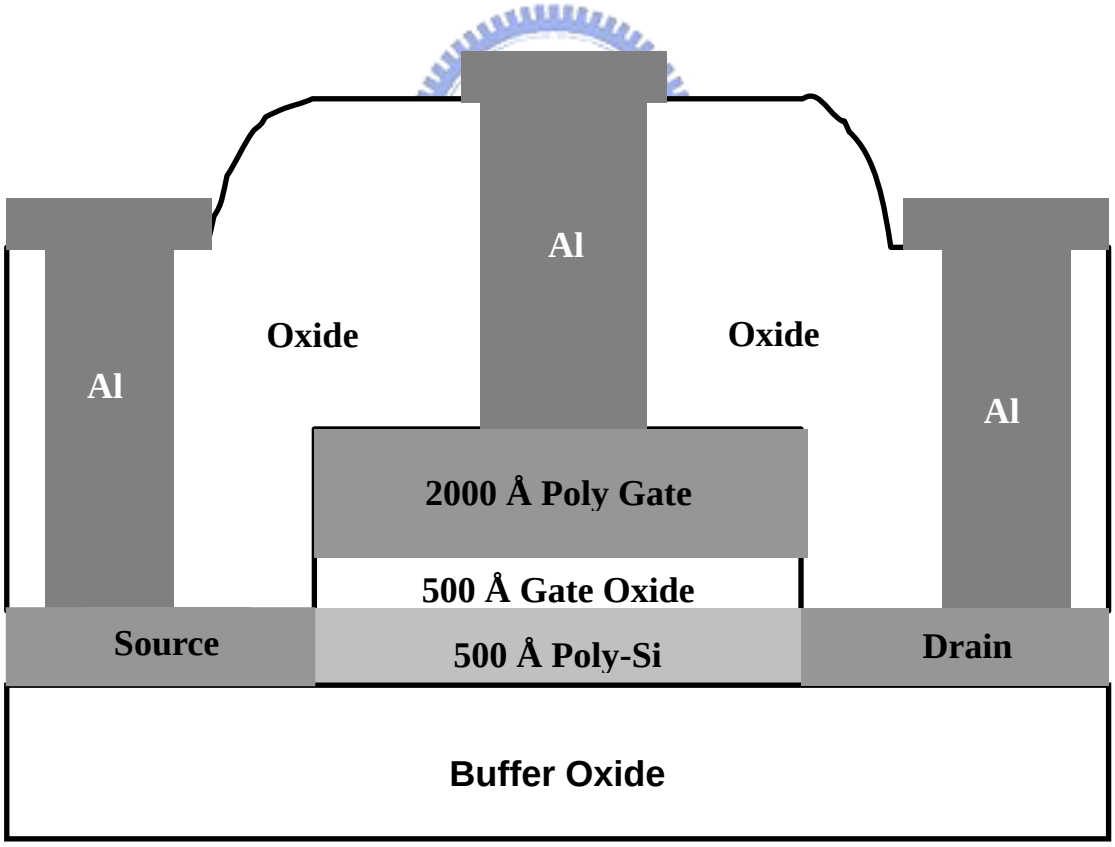

Fig 3-2 Cross-section view of TFT

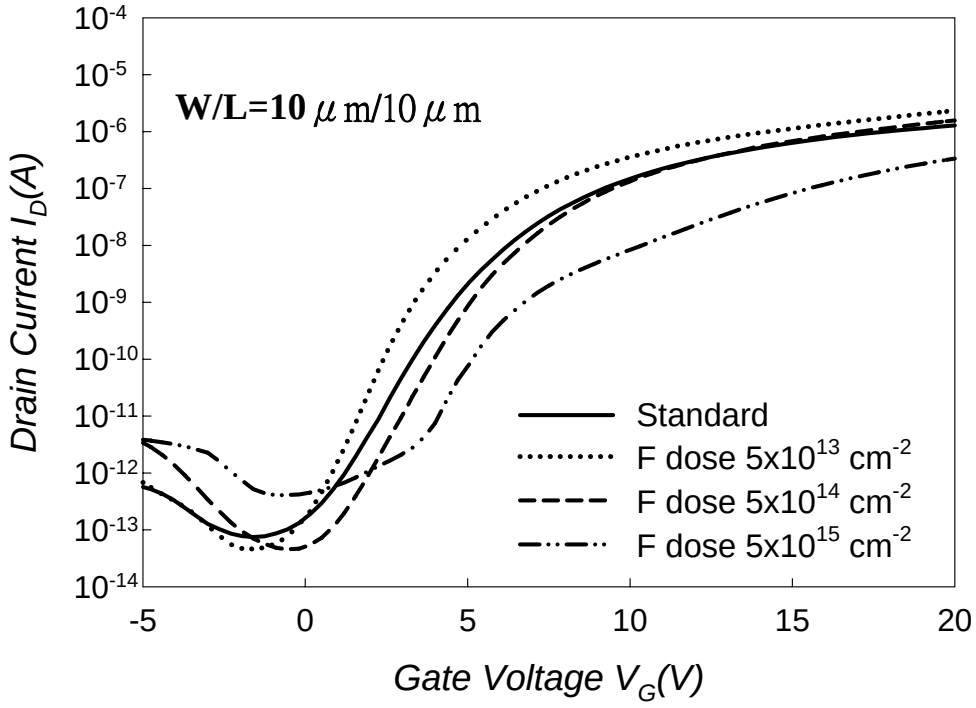

Fig.4-1 Transfer characteristic for fluorine implanted SPC TFT and standard SPC TFT at V_D=0.1V

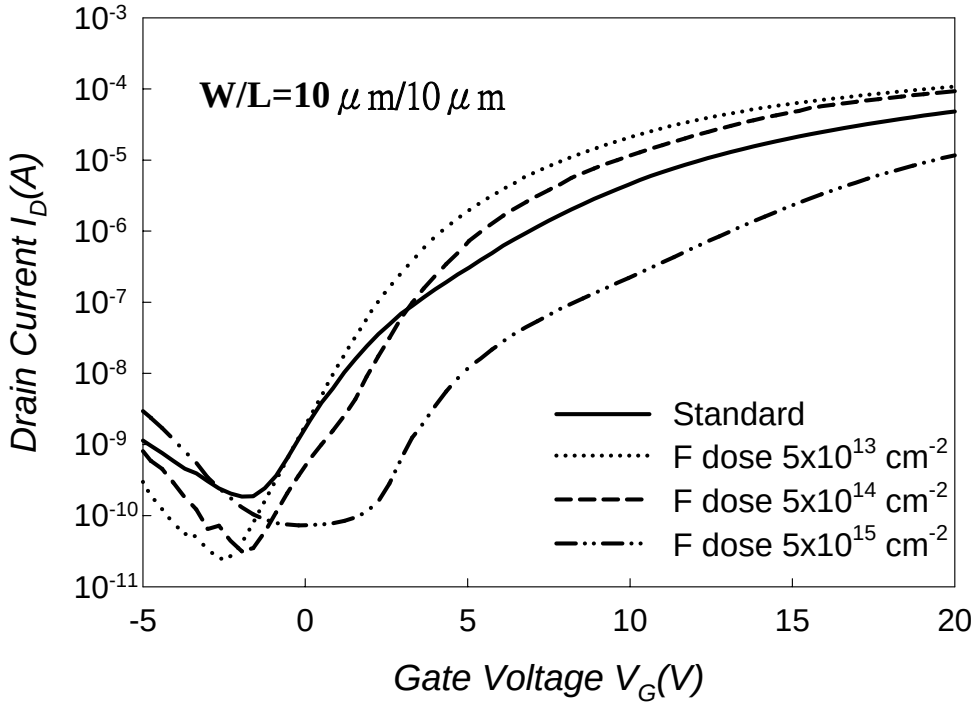

Fig.4-2 Transfer characteristic for fluorine implanted SPC TFT and standard SPC TFT at V_D=5V

	Mobility (cm^2/VS)	V_{TH} (V)	SS (V/dec.)	Ion / Ioff ($*10^6$)	Nt ($*10^{12}cm^{-2}$)
Standard	19.74	6.24	1.20	26.01	9.48
F dose $5x10^{13}$	54.48	4.78	0.97	87.62	8.37
F dose $5x10^{14}$	48.12	6.69	1.13	67.31	9.17
F dose $5x10^{15}$	15.17	10.36	1.62	1.94	10.90

Table I Device parameters for standard SPC TFT and fluorine implanted SPC TFT, including mobility, threshold voltage(V_{TH}), subthreshold swing($S.S$), Ion/Ioff ratio and trap state density(Nt). All parameters were extracted at V_D=0.1V

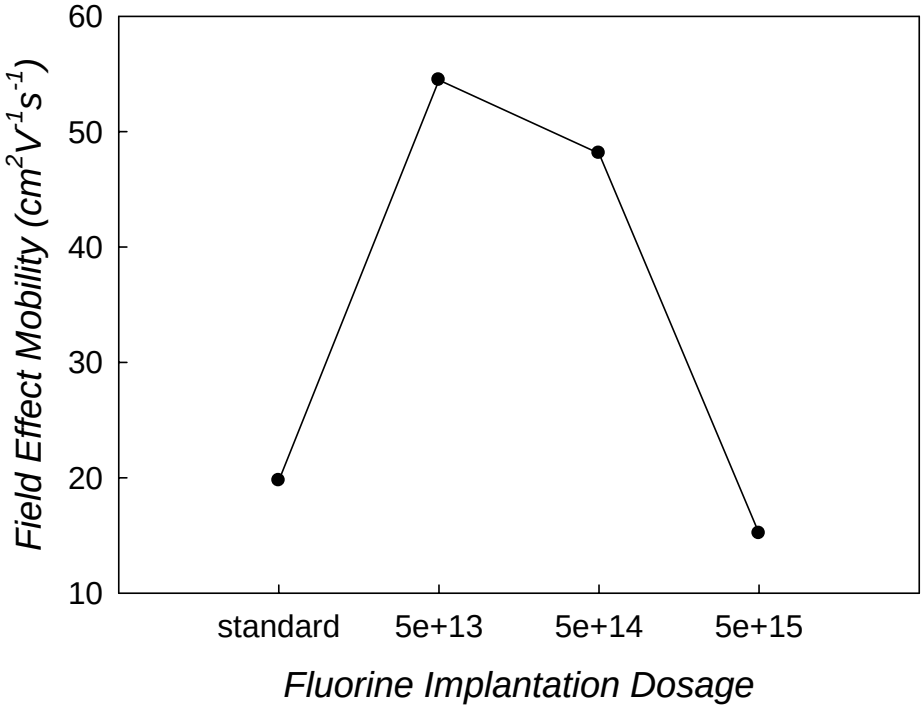

Fig.4-3 Field effect mobility (μ_{FE}) versus different fluorine implantation dosage SPC poly-Si TFTs.

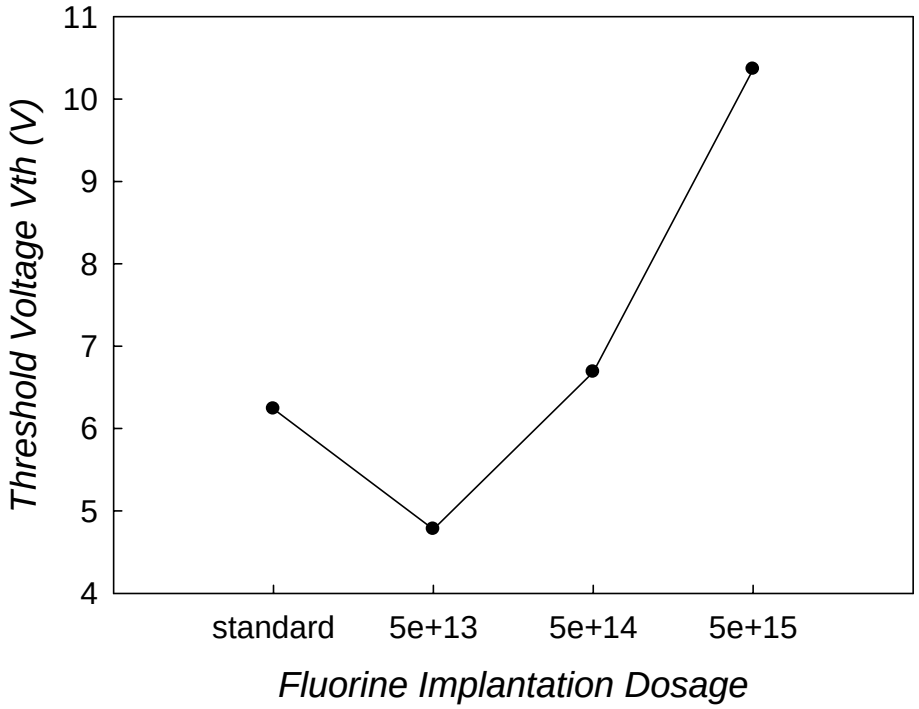

Fig.4-4 Threshold voltage (V_{TH}) versus different fluorine implantation dosage SPC poly-Si TFTs.

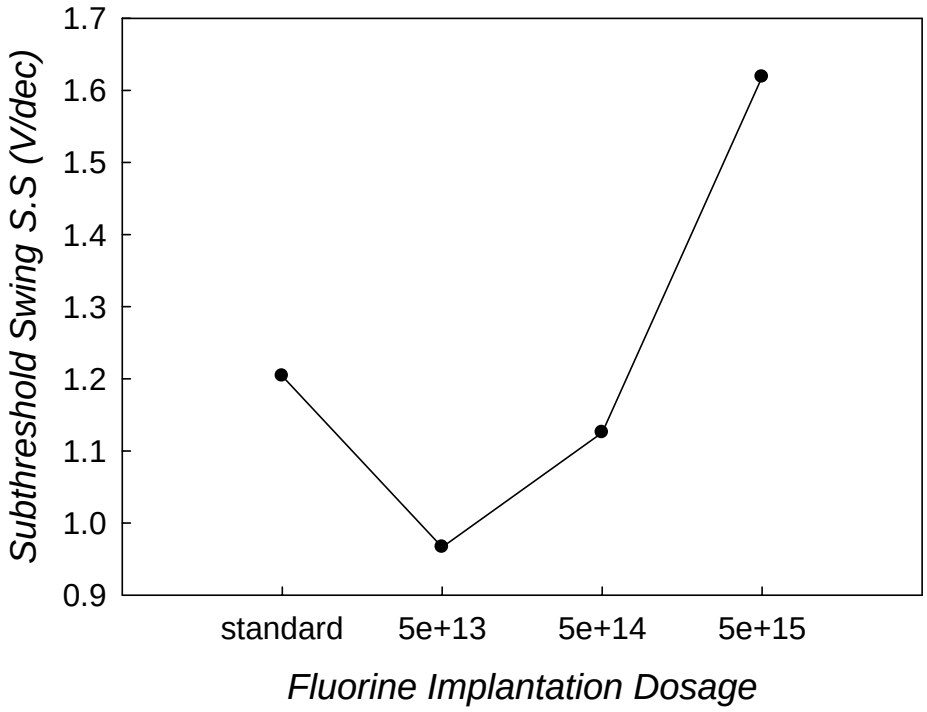

Fig.4-5 Subthreshold swing (*S.S*) versus different fluorine implantation dosage SPC poly-Si TFTs.

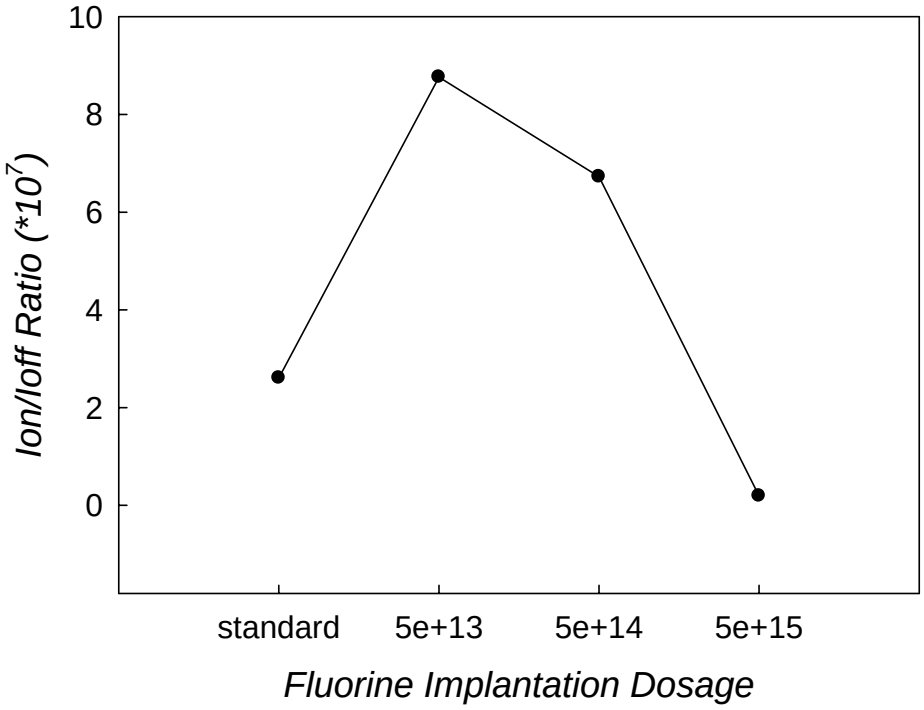

Fig.4-6 Ion/Ioff ratio versus different fluorine implantation dosage SPC poly-Si TFTs.

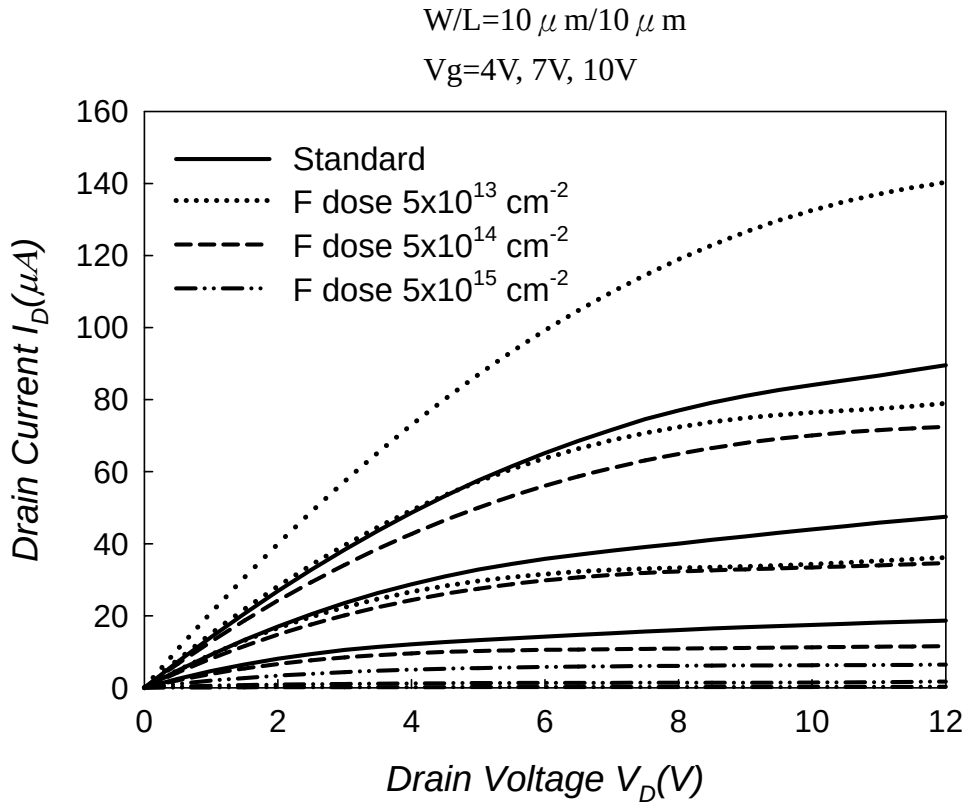

Fig.4-7 Output characteristic for fluorine implanted SPC TFT and standard SPC TFT.

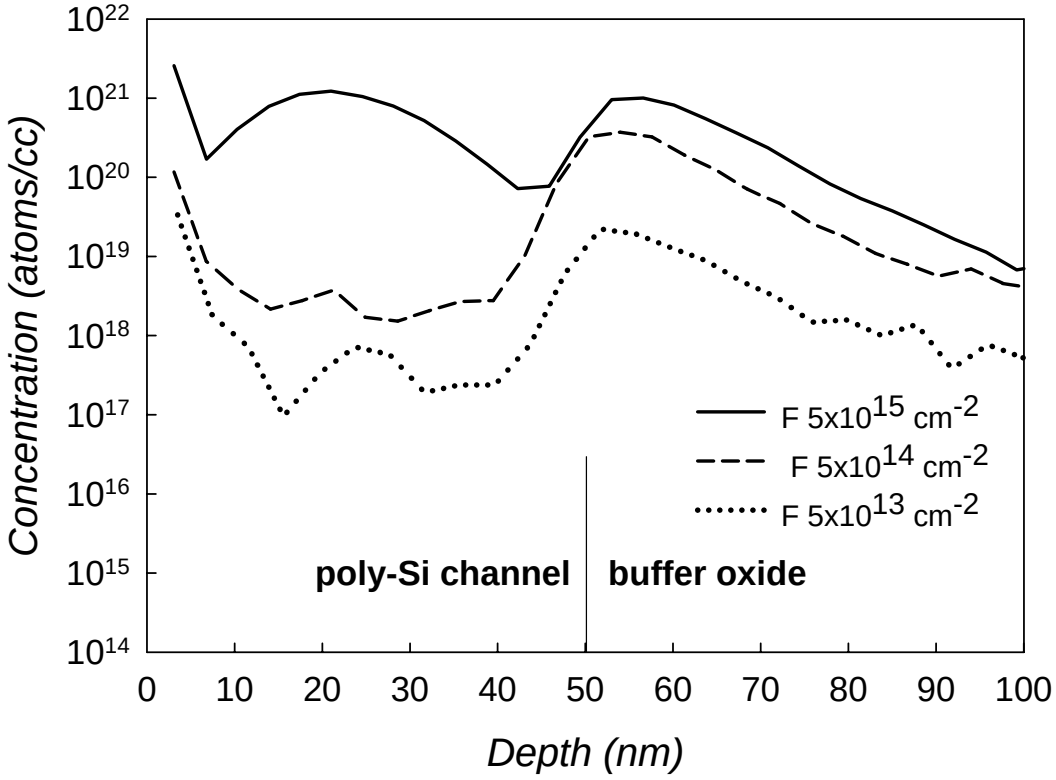

Fig.4-8 Secondary-ion mass spectrometry (SIMS) depth profile with various fluorine ion implantation doses after solid phase re-crysatllization(600℃ for 24 hrs).

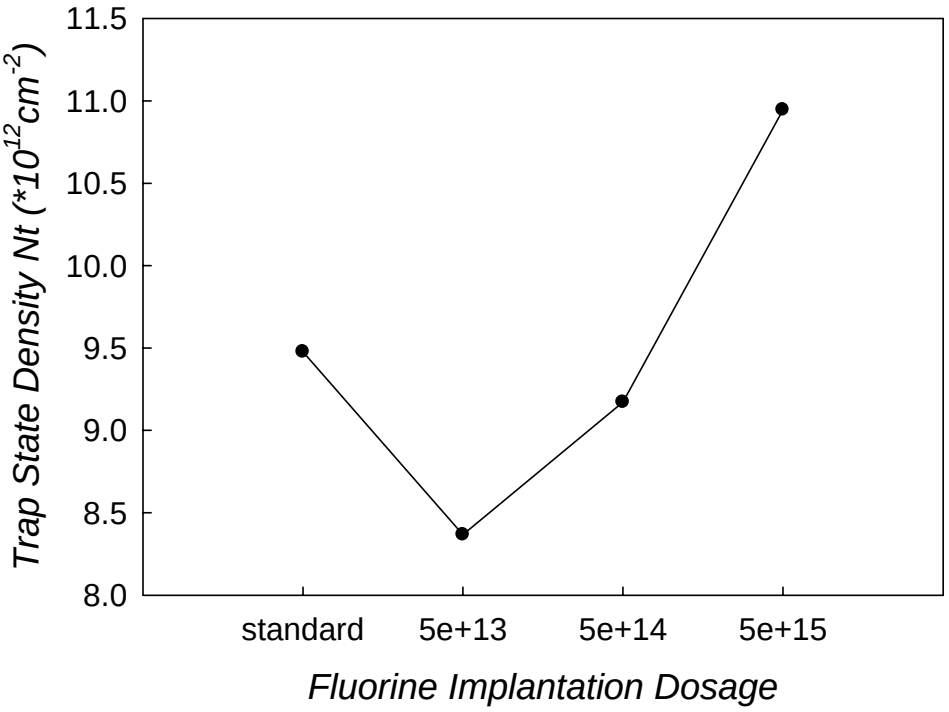

Fig.4-9 Trap state density (*Nt*) versus different fluorine implantation dosage SPC poly-Si TFTs.

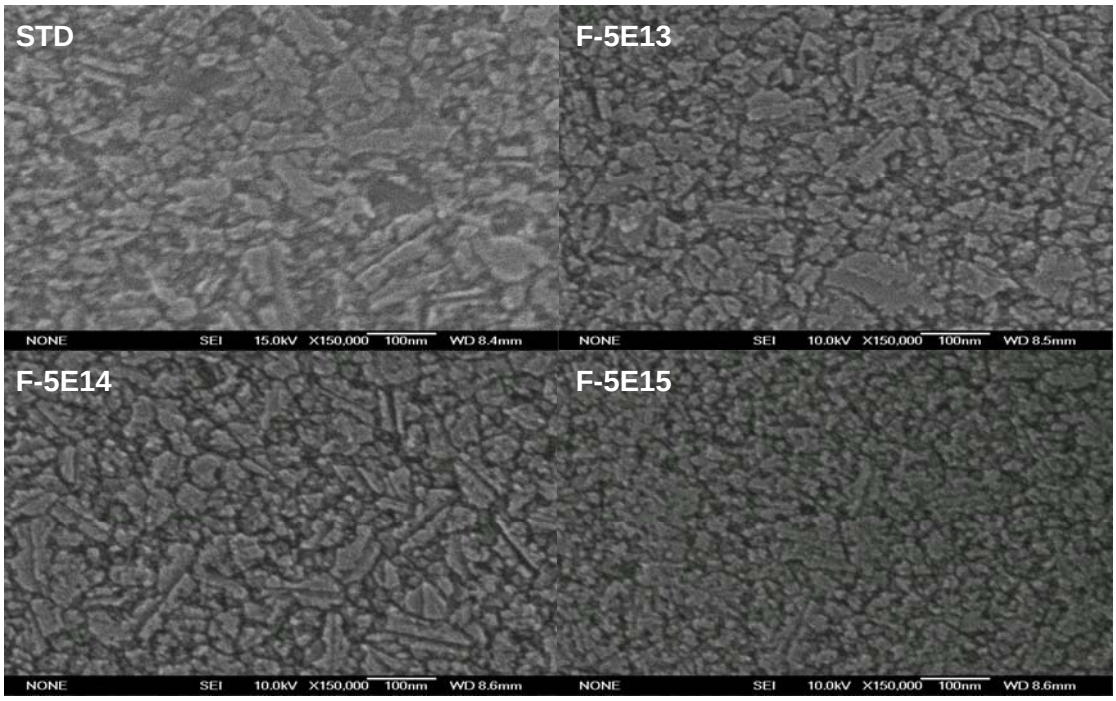

Fig.4-10 The scanning electron microscope (SEM) image of poly-Si grain with different fluorine doses after SPC method.

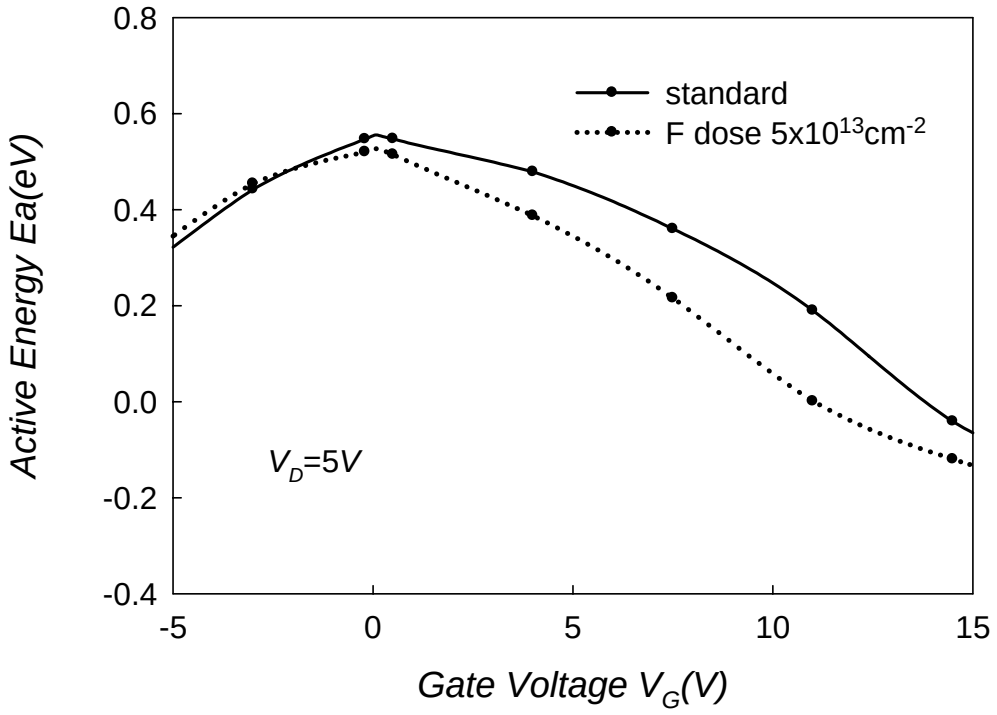

Fig.4-11 The activation energy of drain current as a function of gate voltage measured at V_D=5 *V* for standard and fluorine ion implanted SPC poly-Si TFTs

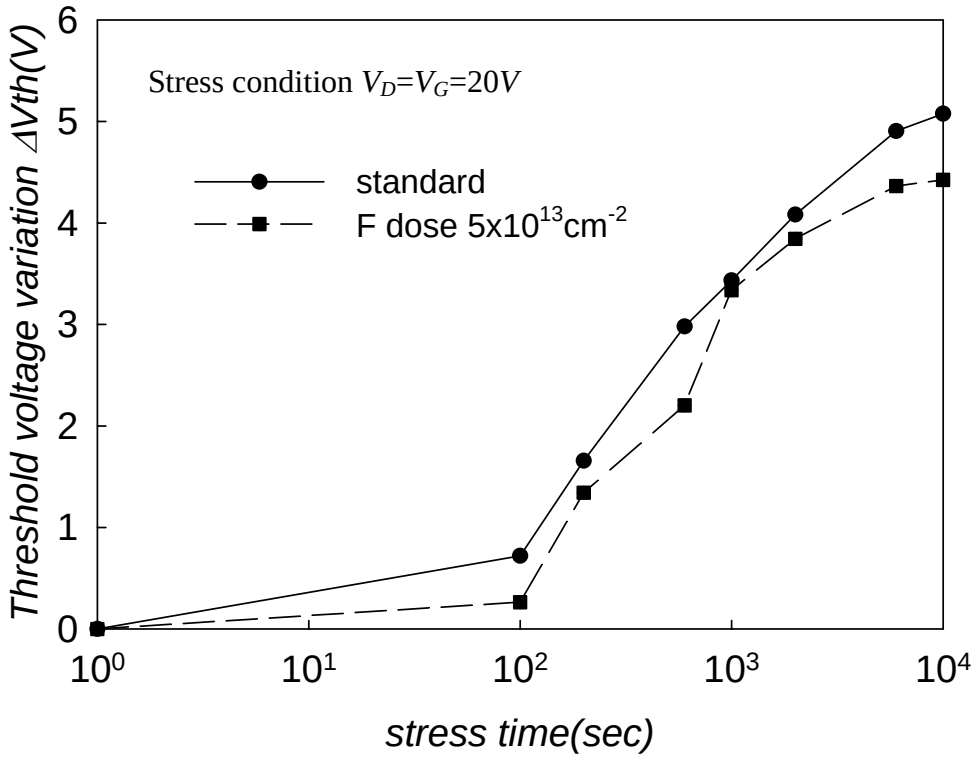

Fig.4-12 Threshold voltage variation (ΔV_{TH}) of SPC poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

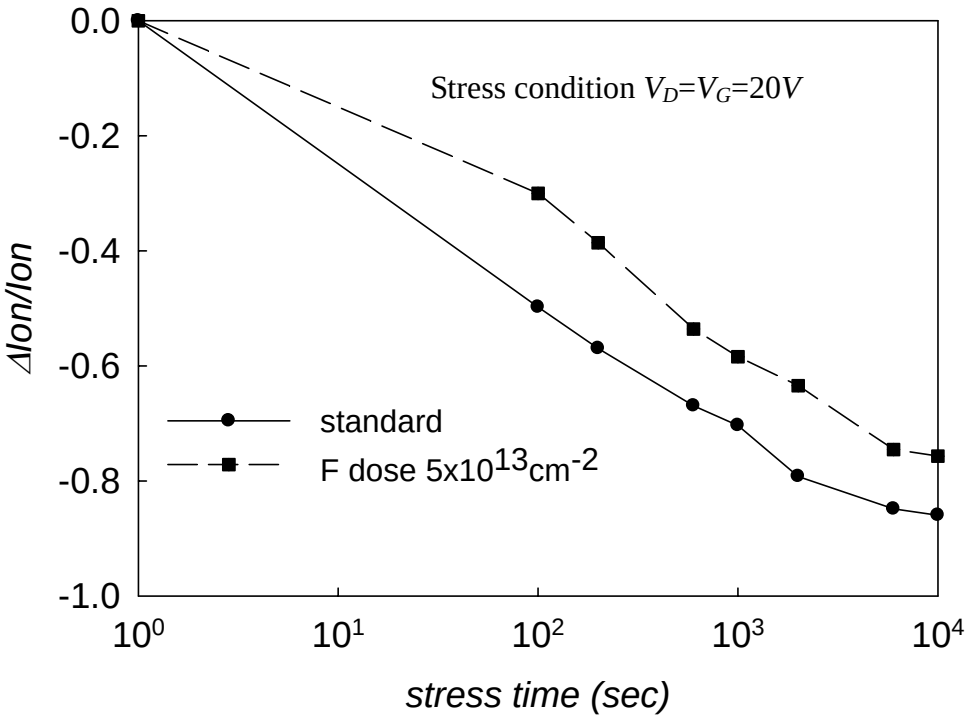

Fig.4-13 On-current degradation of SPC poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

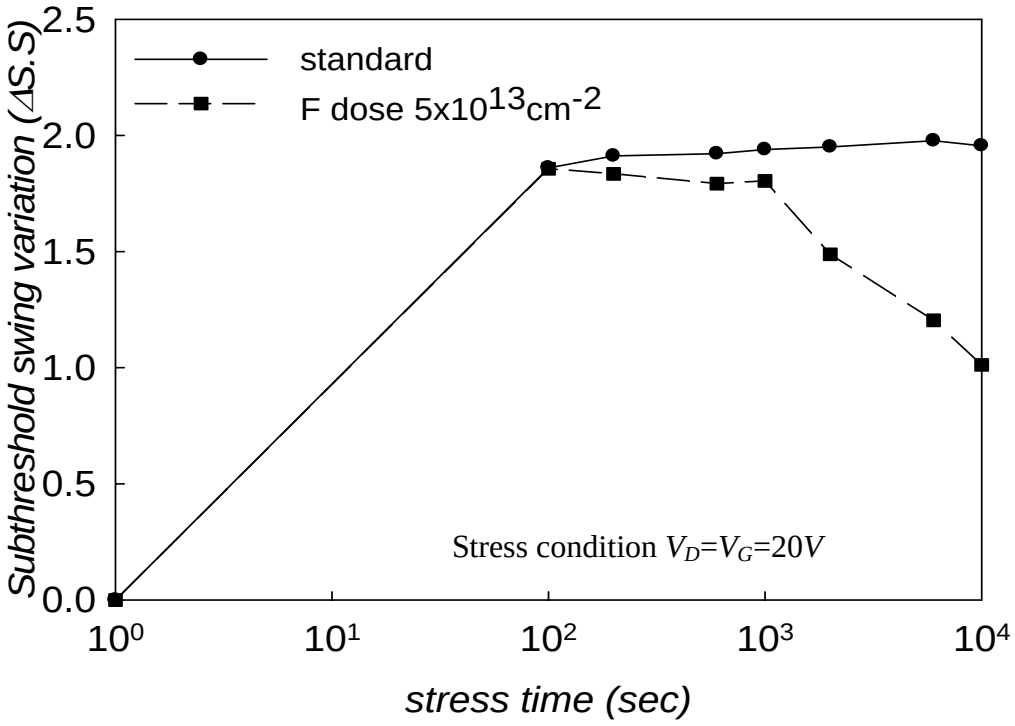

Fig.4-14 Subthreshold swing variation ($\Delta S.S$) of SPC poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

bond dissociation energy:

Si-F = 152 kcal/mol

Si-O = 129 kcal/mol

Si-H = 92-97 kcal/mol

Table Ⅱ The association energy of the different bonding

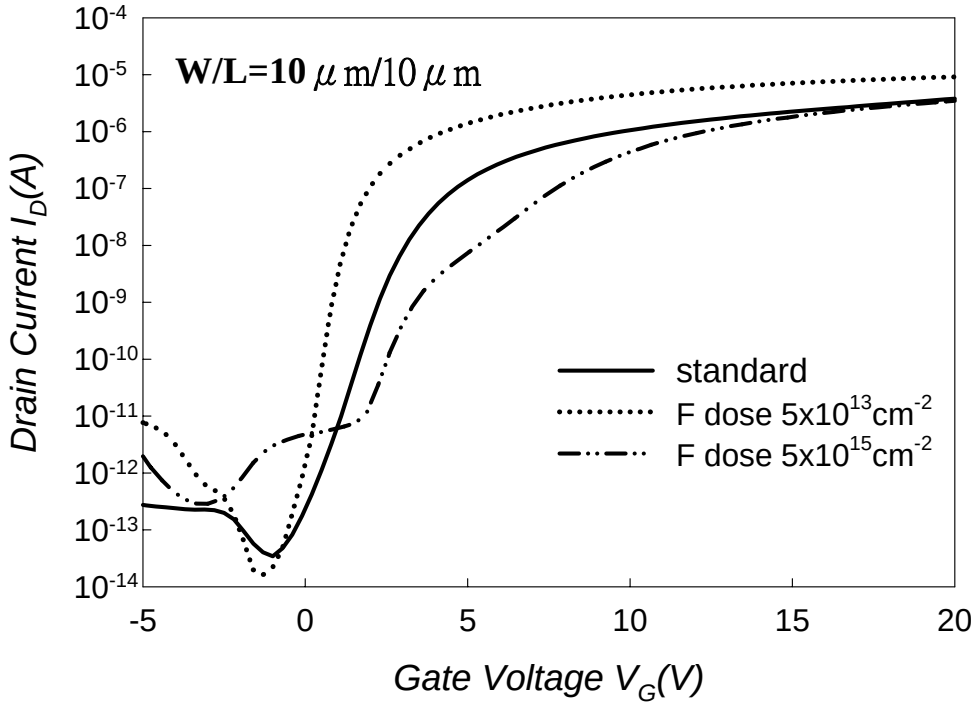

Fig.4-15 Transfer characteristic for fluorine implanted ELA TFT and standard ELA TFT at V_D=0.1V

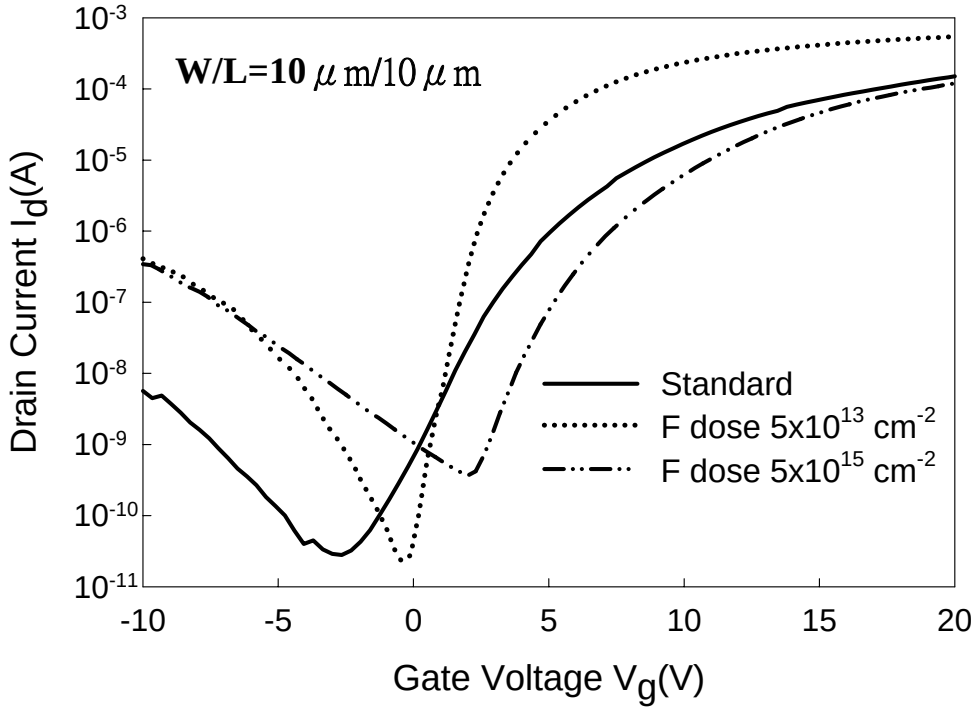

Fig.4-16 Transfer characteristic for fluorine implanted ELA TFT and standard ELA TFT at V_D=5V

	Mobility (cm^2/VS)	V_{TH} (V)	SS (V/dec.)	Ion / Ioff ($*10^7$)	Nt ($*10^{12}cm^{-2}$)
Standard	56.65	3.07	0.61	11.10	5.18
F dose $5x10^{13}$	103.94	1.19	0.30	56.38	3.07
F dose $5x10^{15}$	57.83	5.32	0.88	2.02	11.10

Table Ⅲ Device parameters for standard ELA TFT and fluorine implanted ELA TFT, including mobility, threshold voltage(V_{TH}), subthreshold swing($S.S$), Ion/Ioff ratio and trap state density(Nt). All parameters were extracted at V_D=0.1V

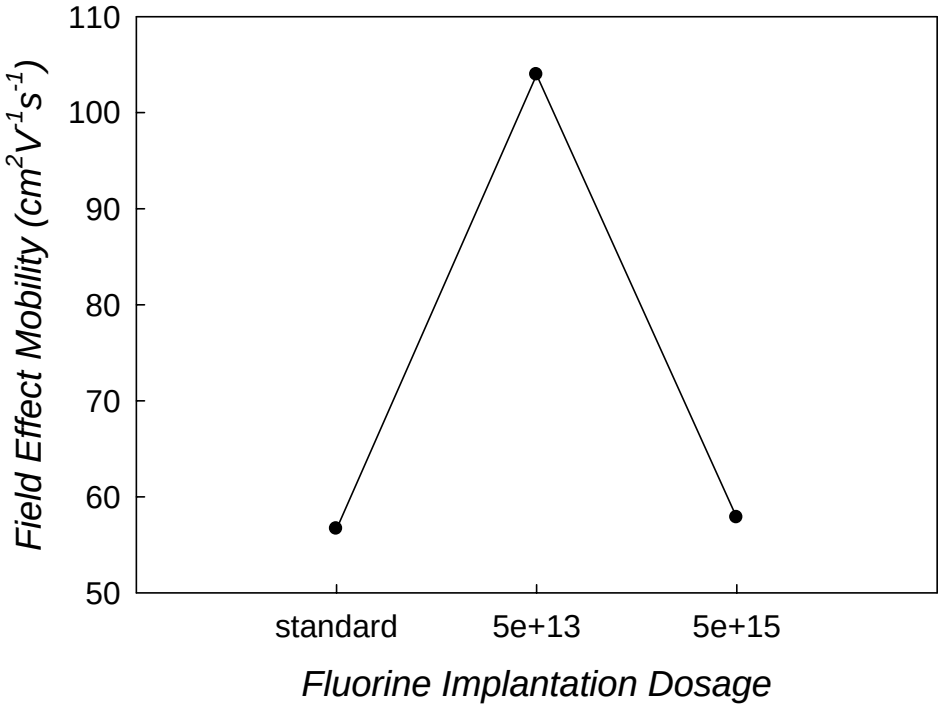

Fig.4-17 Field effect mobility (μ_{FE}) versus different fluorine implantation dosage ELA poly-Si TFTs.

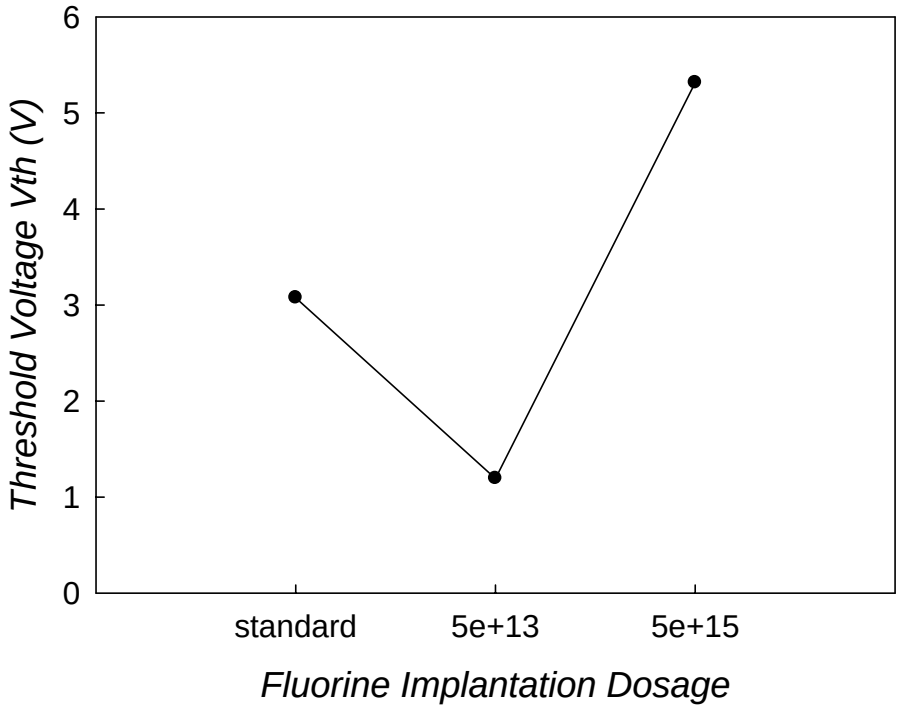

Fig.4-18 Threshold voltage (V_{TH}) versus different fluorine implantation dosage ELA poly-Si TFTs.

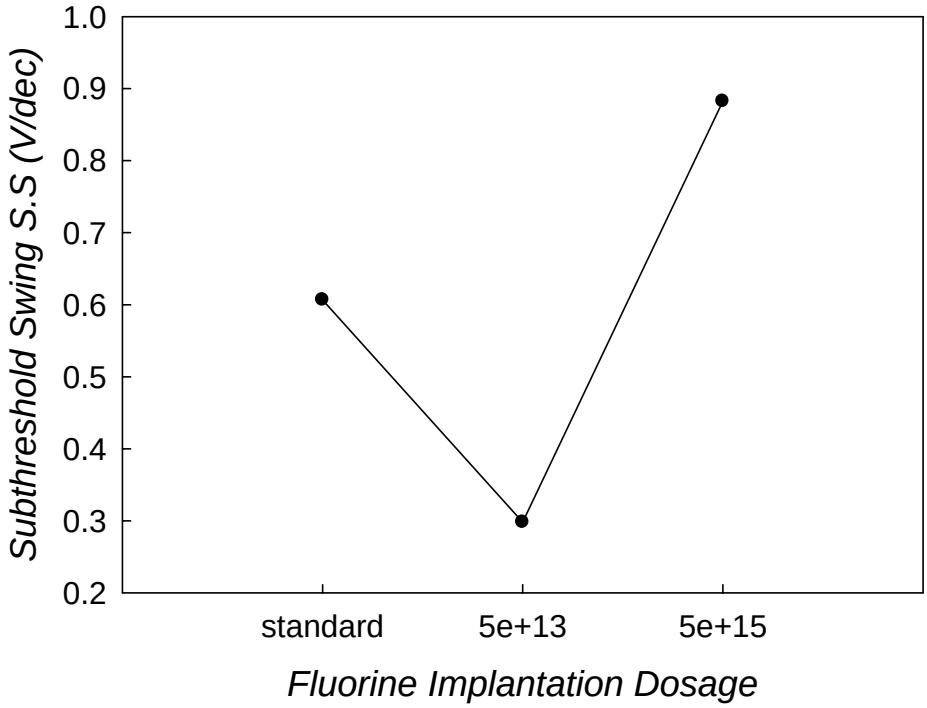

Fig.4-19 Subthreshold swing (*S.S*) versus different fluorine implantation dosage ELA poly-Si TFTs.

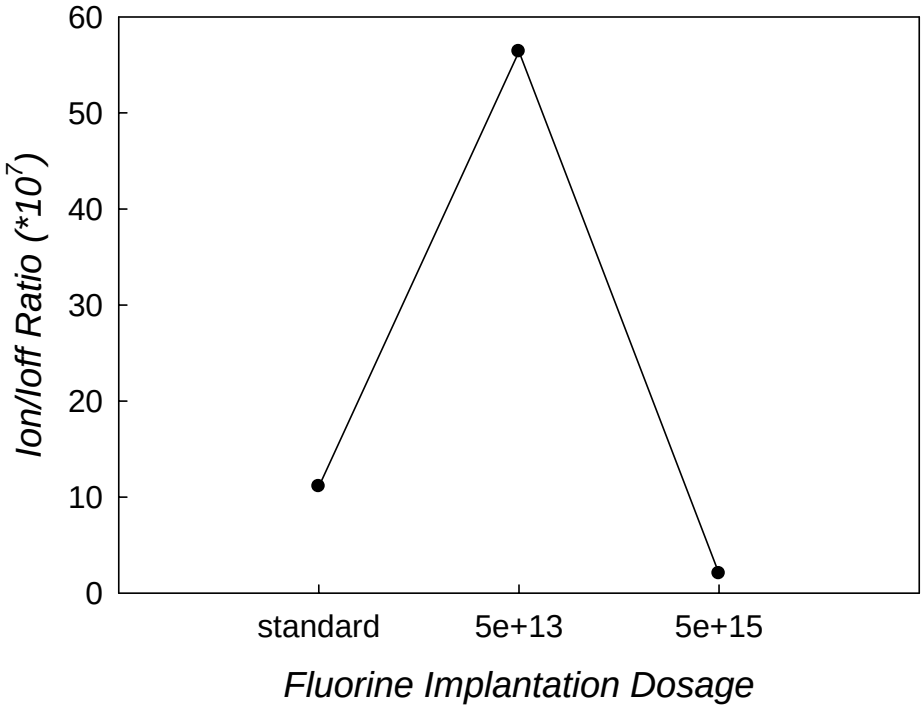

Fig.4-20 Ion/Ioff ratio versus different fluorine implantation dosage ELA poly-Si TFTs.

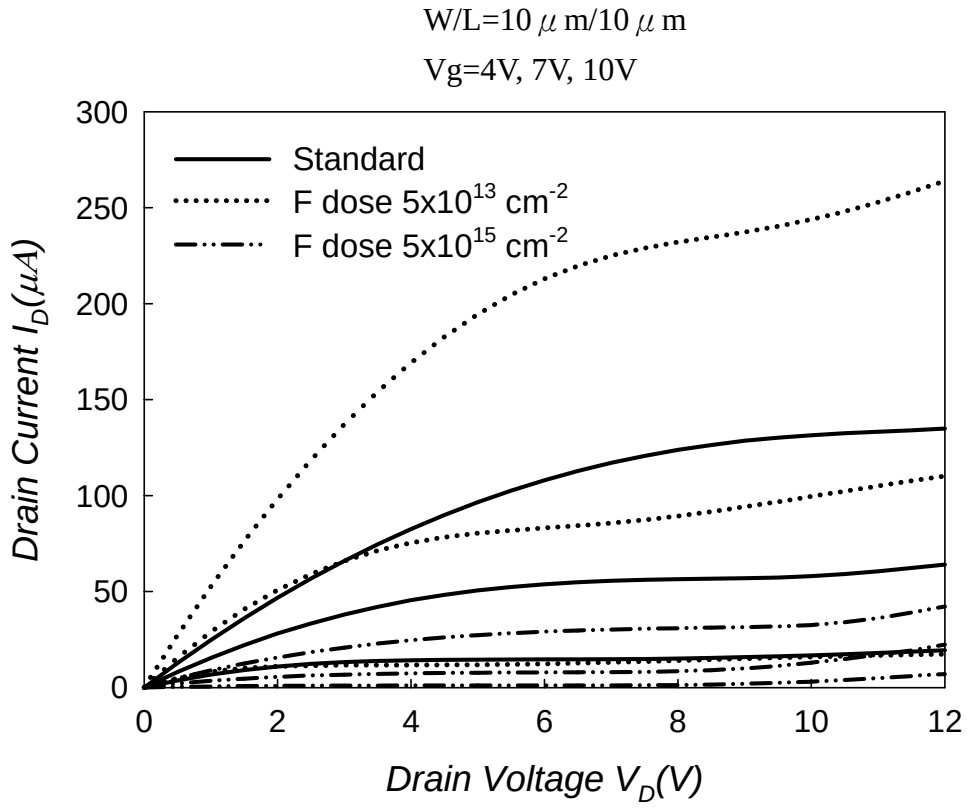

Fig.4-21 Output characteristic for fluorine implanted ELA TFT and standard ELA TFT.

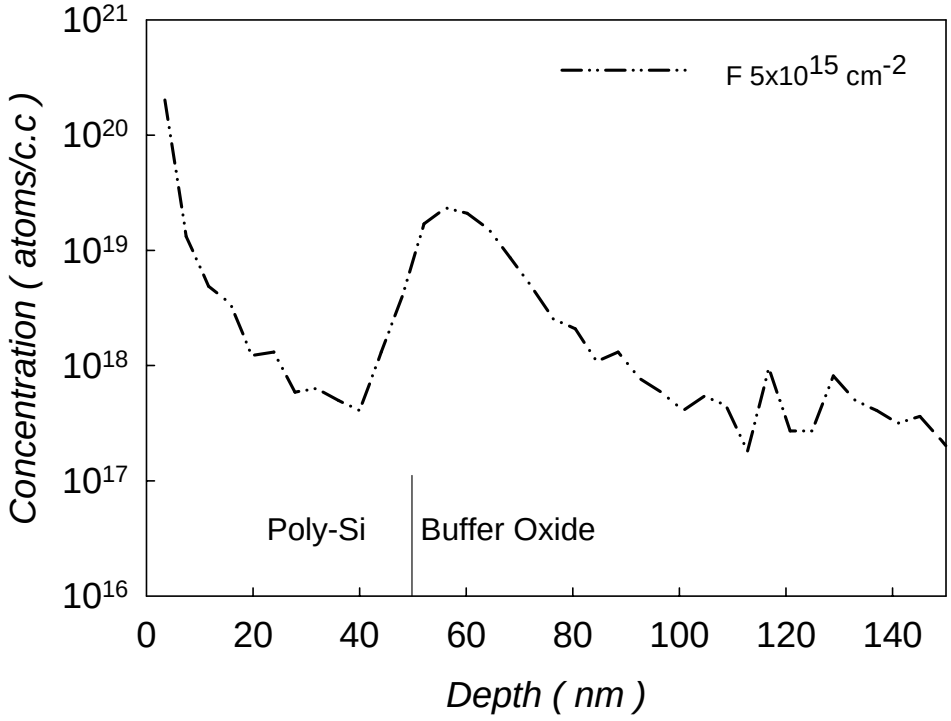

Fig.4-22 Secondary-ion mass spectrometry (SIMS) depth profile with $5x10^{13}$ cm^{-2} fluorine ion implantation doses after excimer laser re-crysatllization.

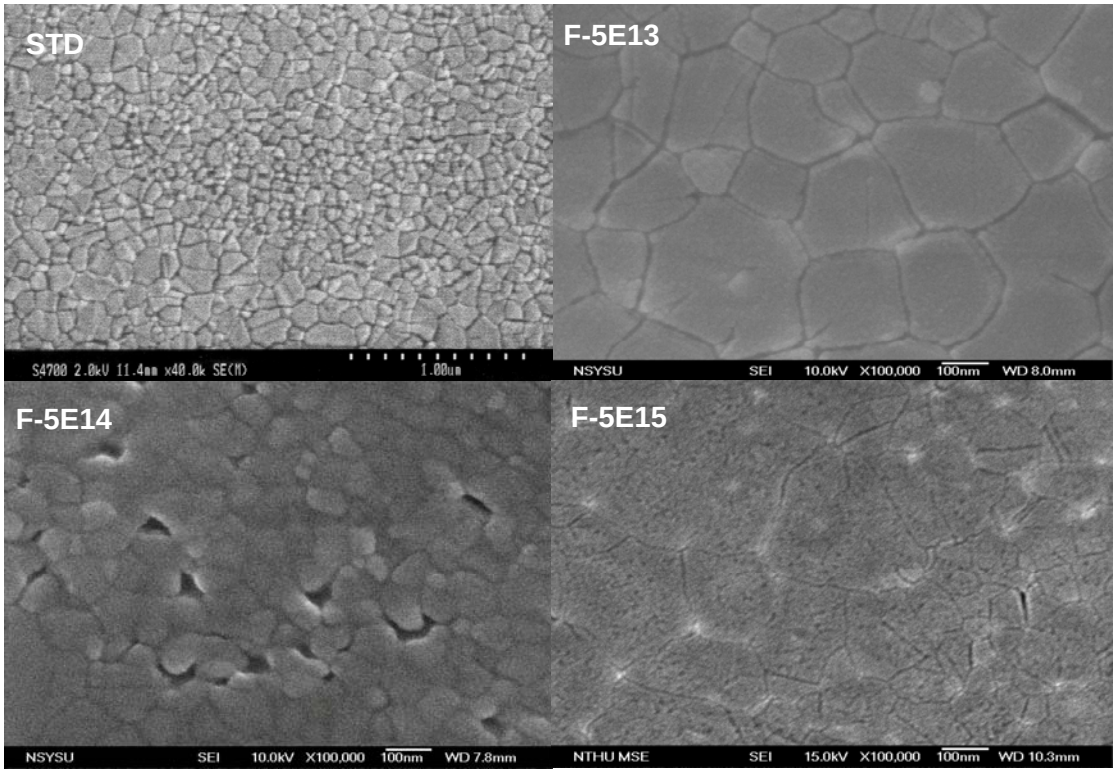

Fig.4-23 The scanning electron microscope (SEM) image of poly-Si grain with different fluorine doses after ELA method. The grain with the $5x10^{13}$ cm^{-2} fluorine ion implantation doses was the largest, and the other grains almost had the same size.

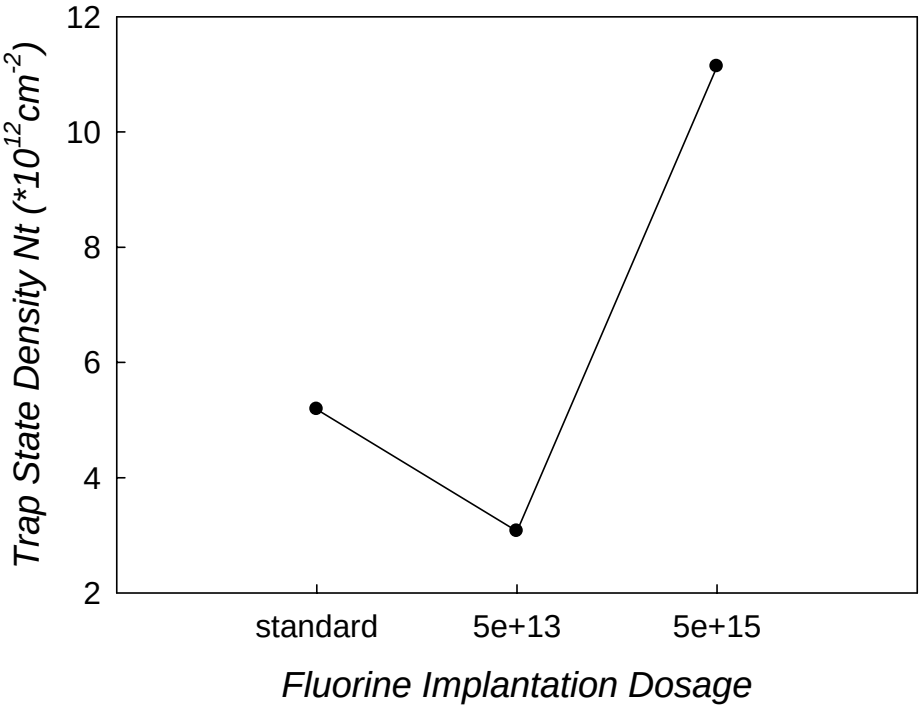

Fig.4-24 Trap state density (*Nt*) versus different fluorine implantation dosage ELA poly-Si TFTs.

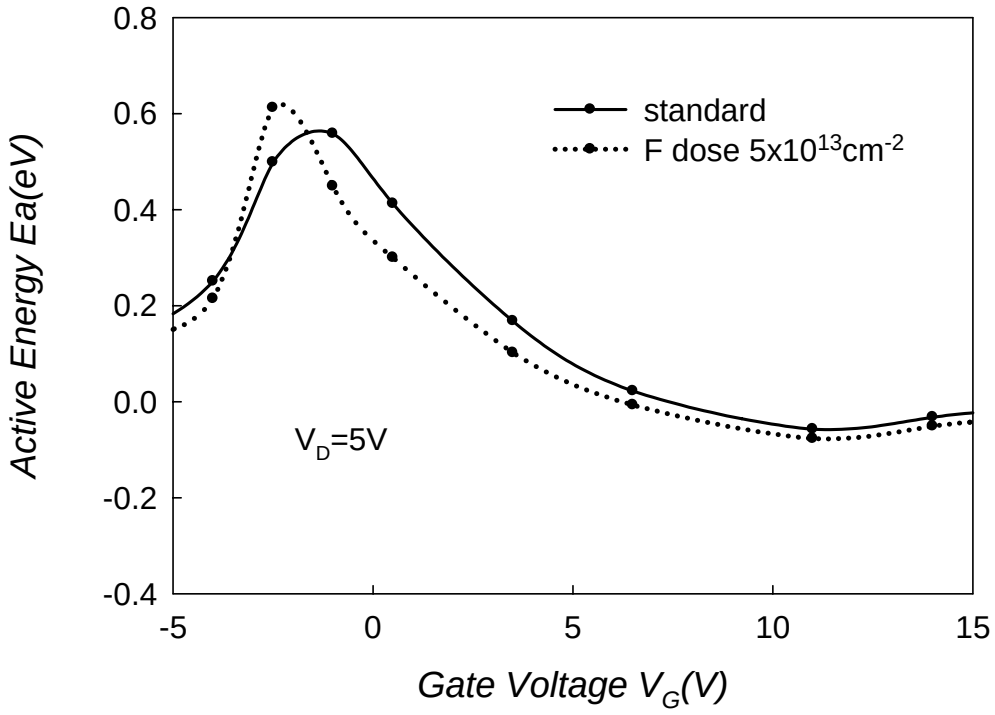

Fig.4-25 The activation energy of drain current as a function of gate voltage measured at V_D=5V for standard and fluorine ion implanted ELA poly-Si TFTs

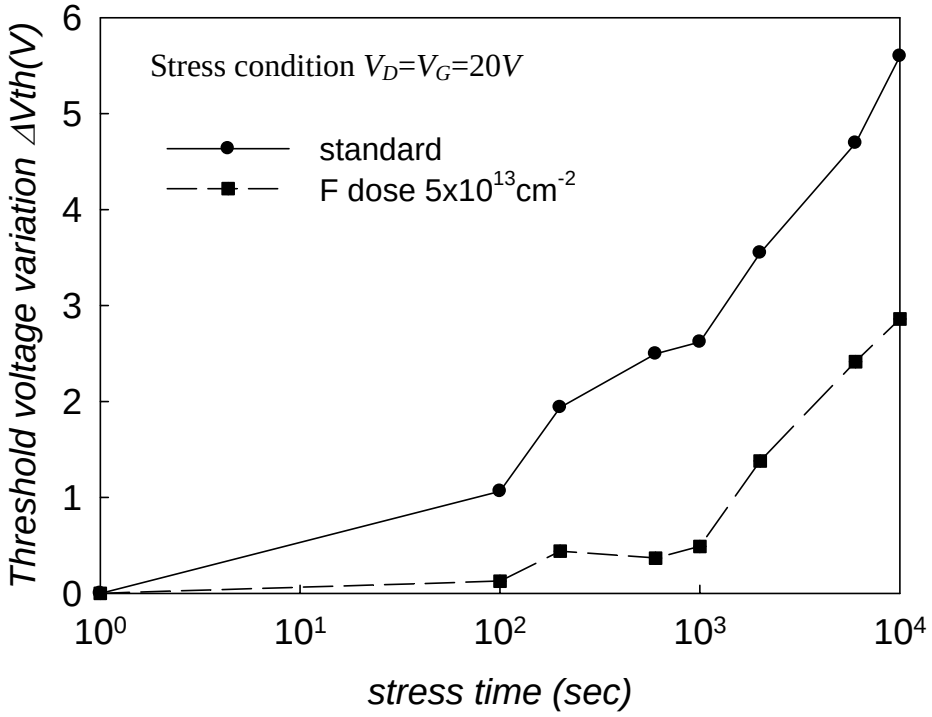

Fig.4-26 Threshold voltage variation ($\triangle$ Vth) of poly-Si ELA TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

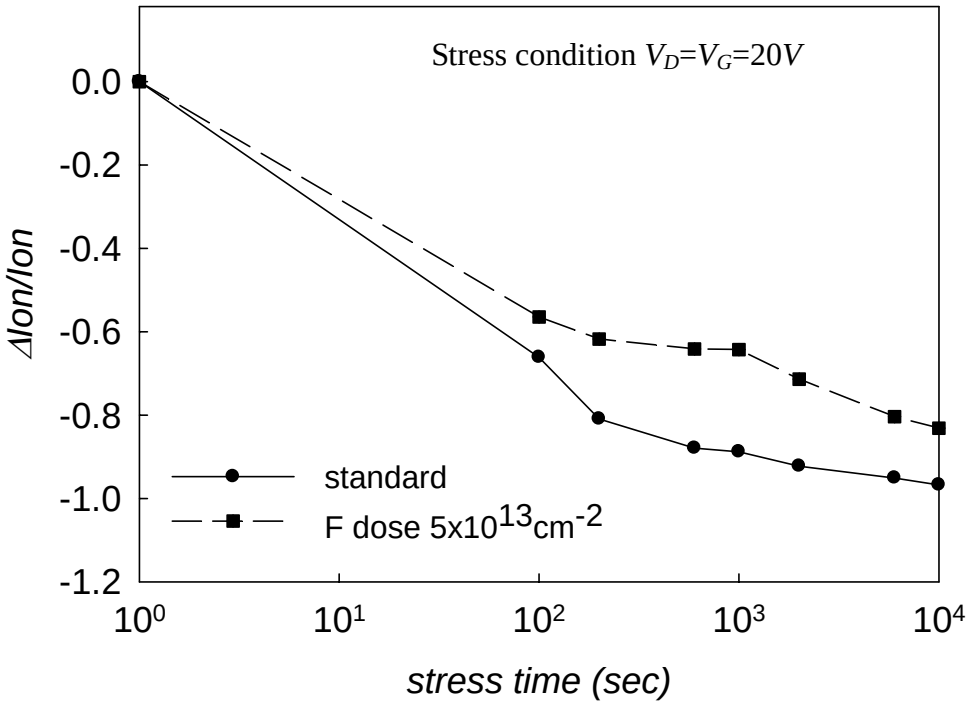

Fig.4-27 On-current degradation of ELA poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage Vd=Vg=20V.

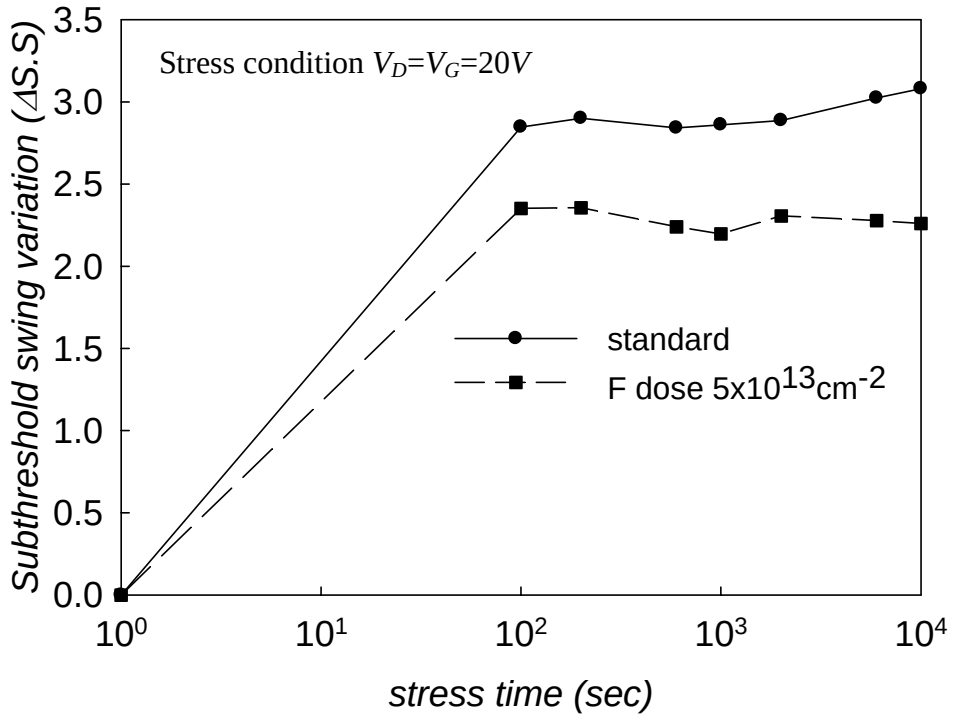

Fig.4-28 Subthreshold swing variation ($\Delta S.S$) of ELA poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

SPC	Mobility (cm^2/VS)	V_{TH} (V)	SS (V/dec.)	Ion / Ioff ($*10^6$)	Nt ($*10^{12}cm^{-2}$)
Standard	19.74	6.24	1.20	26.01	9.48
F dose $5x10^{13}$	54.48	4.78	0.97	87.62	8.37
Improvement(%)	175.99	23.41	19.70	236.64	11.71
ELA	Mobility (cm^2/VS)	V_{TH} (V)	SS (V/dec.)	Ion / Ioff ($*10^6$)	Nt ($*10^{12}cm^{-2}$)
Standard	56.65	3.074	0.61	11.10	5.18
F dose $5x10^{13}$	103.94	1.19	0.30	56.38	3.07
Improvement(%)	83.46	61.21	50.87	408.62	40.79

Table IV The electrical characteristics improvement by fluorine implantation of SPC and ELA poly-Si TFTs

Electrical parameters	**Mainly depending on**
Mobility (μ_{eff})	➢ Trap states in the grain boundaries (tail states)
Threshold voltage (V_{TH})	➢ Trap states in the interface (deep states) ➢ Trap states in the grain boundaries (deep states)
Subthreshold swing (S.S)	➢ Intra-grain defect density (bulk states) ➢ Trap states in the interface (deep states)

Table V The relation between the electrical parameter and the location of the trap states.

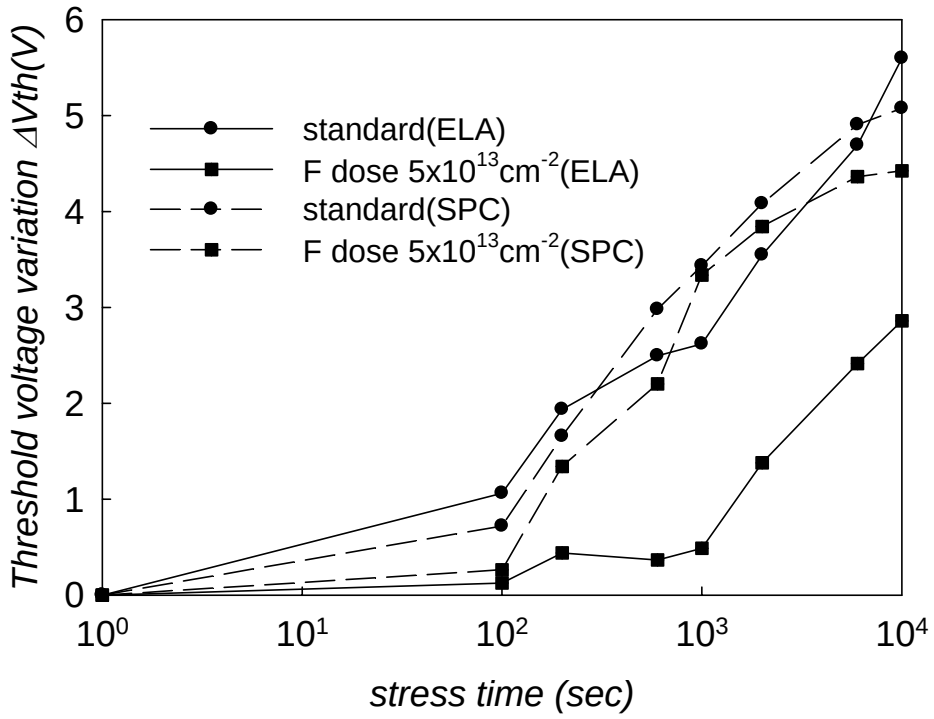

Fig.4-29 Threshold voltage variation ($\triangle$ Vth) of ELA and SPC poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

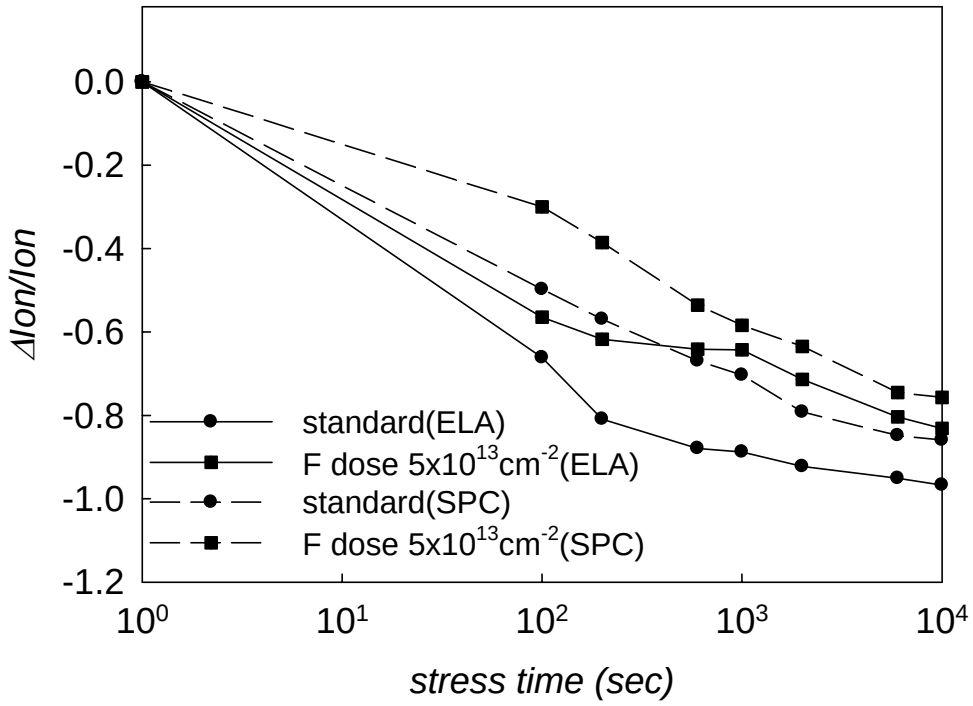

Fig.4-30 On-current degradation of ELA and SPC poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

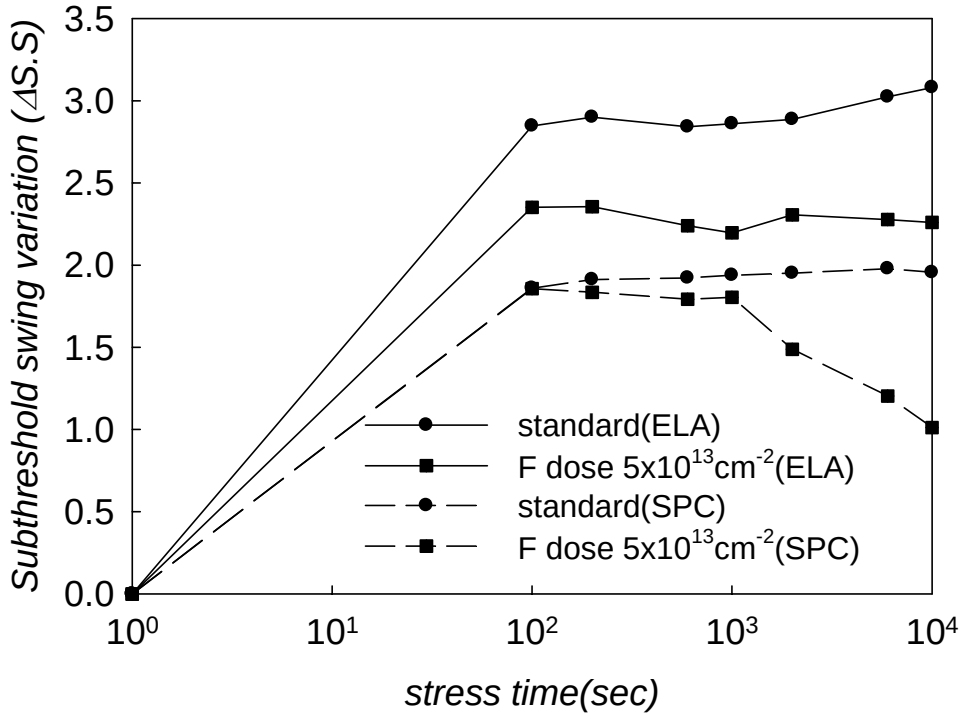

Fig.4-31 Subthreshold swing variation ($\Delta S.S$) of ELA and SPC poly-Si TFTs with/without fluorine implantation versus stress time under a stress voltage V_D=V_G=20V.

簡歷

姓名：楊哲育

性別：男

出生日期：中華民國七十年九月十五日

籍貫：屏東縣

地址：屏東縣屏東市忠孝路 184 巷 16 號

學歷：國立中山大學物理系
88 年 9 月~92 年 6 月

國立交通大學電子工程研究所
92 年 9 月~94 年 6 月

碩士論文：氟離子佈植對低溫多晶矽薄膜電晶體之研究

The Study on Fluorine Ion Implanted Polysilicon Thin Film Transistors