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高介電常數氧化鐠閘極介電層與新穎結構於複晶矽薄膜電晶體之研究

Study on High-κ Pr_2O_3 Gate Dielectric and Novel Structures of Polycrystalline Silicon Thin-Film Transistors

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摘　要

此論文提出多種有效方式來改善複晶矽薄膜電晶體的電性，首先，提出具有高介電常數氧化鐠閘極介電層之固相再結晶複晶矽薄膜電晶體。此外，深入探討應用兩種氟鈍化技術包括氟離子佈值及四氟化碳電漿處理以製備高效能及高可靠度之複晶矽氧化鐠薄膜電晶體。並研究兩種複晶矽晶粒尺寸增大技術於固相再結晶複晶矽薄膜電晶體之應用。最後，發展一個簡單的側壁邊襯技術來製作具有奈米線通道之固相結晶和金屬誘發側向結晶複晶矽薄膜電晶體。

首先，整合氮化鈦金屬閘極和高介電常數氧化鐠閘極介電層來發展高效能之固相再結晶複晶矽薄膜電晶體。應用氧化鐠閘極介電層可得到薄的等效氧化層厚度和高的閘極電容密度並且可以使複晶矽通道區域誘發產生更大量的可移動載子。因此，複晶矽薄膜裡的晶粒邊界缺陷態位會被大量誘導產生的載子迅速的填滿，可以大幅的改善次臨界斜率。即使在沒有額外施加氫化處理製程或採用先進的相結晶技術之下，複晶

矽氧化鐠閘極介電層薄膜電晶體的電性明顯地勝過傳統的複晶矽氧化矽閘極介電層薄膜電晶體。

接著，我們應用兩種氟鈍化技術包括氟離子佈值及四氟化碳電漿處理於複晶矽氧化鐠閘極介電層薄膜電晶體。這些氟鈍化技術可將氟原子引進複晶矽薄膜中及氧化鐠閘極介電極/複晶矽通道界面處來修補晶粒邊界缺陷態位。因此，藉著摻雜氟原子進入複晶矽薄膜中，複晶矽氧化鐠閘極介電層薄膜電晶體的元件電性以及臨界電壓下降特性可大幅的改善，尤其是針對關閉狀態的漏電流改善更加顯著。此外，這些氟鈍化技術也可形成強的矽-氟鍵結以取代一般弱的矽-矽鍵結以及矽-氫鍵結，以增進熱載子應力的免疫力。

其次，我們發展出兩種具有表面成核固相再結晶方式之複晶矽晶粒尺寸增大技術，其中包括氬離子佈植於非晶矽/下層氧化矽界面處以及新穎的懸浮通道結構。在界面處的大量矽晶粒成核機制可被有效抑制住，而成核機制會選擇由較少成核點的非晶矽自由表面處開始，在較少的矽晶粒成核點情況下可以得到較好的複晶矽晶粒特性包含較大晶粒尺寸及較少結構缺陷。因此，利用這些晶粒尺寸增大技術可以顯著的改善複晶矽薄膜電晶體的電性。

在論文的最後，我們發展出利用簡單的側壁邊襯技術且不需要先進的微影製程來形成自我對準的 50 奈米線寬的奈米線通道。探討應用固相再結晶和金屬誘發側向再結晶技術於複晶矽奈米線通道薄膜電晶體的應用。由於固相再結晶複晶矽奈米線通道薄膜電晶體具有三維之類三閘極結構，邊際電場會誘導側壁及角落產生額外的電流貢獻效應以增進閘極對奈米線通道的控制能力。另一方面，金屬誘發側向再結晶複晶矽奈米線通道薄膜電晶體具有較佳的複晶矽晶粒特性，因此具有較好的導通特性以及較低的關閉狀態漏電流。

Study on High-κ Pr_2O_3 Gate Dielectric and Novel Structures of Polycrystalline Silicon Thin-Film Transistors

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ABSTRACT

In this thesis, several effective ways were proposed to improve the electrical performances of polycrystalline silicon thin-film transistors (poly-Si TFTs). First, solid-phase crystallized (SPC) poly-Si TFTs with high-κ Pr_2O_3 gate dielectric were proposed. In addition, applying two kinds of fluorination techniques including fluorine ion implantation and CF_4 plasma treatments to the SPC poly-Si Pr_2O_3 TFTs were deeply investigated. Besides, SPC poly-Si TFTs with two poly-Si grain-size enlargement techniques were demonstrated and characterized. Finally, a simple sidewall spacer technique was developed to fabricate SPC and metal-induced lateral crystallized (MILC) poly-Si TFTs with NW channels.

First, high-performance SPC poly-Si TFTs integrated with TiN metal gate and high-κ Pr_2O_3 gate dielectric have been demonstrated. Using the Pr_2O_3 gate dielectric can obtain thin equivalent-oxide thickness and high gate capacitance density, and then induce much more mobile carriers in the poly-Si channel region. Hence, the grain-boundary trap states in the poly-Si films could be quickly filled up by the large amount of induced carriers to improve the subthreshold swing. The electrical characteristics of the poly-Si Pr_2O_3 gate dielectric TFTs can be greatly improved compared to those of the traditional poly-Si SiO_2 gate

dielectric TFTs even without additional hydrogenation treatments or advanced phase crystallization techniques.

Then, we have incorporated two kinds of fluorination techniques including fluorine ion implantation and CF_4 plasma treatments into the poly-Si Pr_2O_3 gate dielectric TFTs. Utilizing these fluorination techniques, fluorine atoms can be introduced into the poly-Si films and the Pr_2O_3 gate dielectric/poly-Si channel interface to passivate the grain-boundary trap states. Hence, the electrical performances and threshold-voltage rolloff properties of the poly-Si Pr_2O_3 gate dielectric TFTs can be significantly improved by the incorporation of fluorine atoms, in particular, a more obvious enhancement on the decreasing of the off-state leakage currents. Besides, these fluorination techniques also enhance the immunity against hot-carrier stress, due to the formation of strong Si-F bonds in place of weak Si-Si and Si-H bonds.

Next, we have developed two kinds of poly-Si grain-size enhancement techniques associating with surface-nucleation SPC scheme including deep Argon ion implantation into the α-Si/underlying SiO_2 interface and novel floating-channel structure. The silicon grain nucleation at the interface is effectively suppressed, and then the nucleation process with fewer nucleation sites will initiate on the α-Si free surface. Fewer silicon grain nucleation results in better poly-Si grain crystallinity with larger grain size and fewer microstructural defects. The electrical characteristics of the poly-Si TFTs are greatly improved by introducing these poly-Si grain-size enhancement techniques.

Finally, we demonstrate a simple sidewall spacer technique for forming self-aligned 50-nm line-width nanowire (NW) channels without any advanced lithography process. Poly-Si TFTs with NW channels crystallized by SPC and metal-induced lateral crystallization (MILC) techniques are investigated. The SPC poly-Si NW TFTs have excellent gate controllability over the NW channels due to the three-dimensional (3-D) tri-gate-like structure with the sidewall and corner contribution effects. On the other hand, the MILC poly-Si NW TFTs exhibit better turn-on characteristics and lower off-state leakage currents due to the superior poly-Si grain crystallinity.

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Chapter 1

Introduction

1.1 Overview of Polycrystalline Silicon Thin-Film Transistors

Over the past two decades, polycrystalline silicon Thin-film transistors (poly-Si TFTs) have been widely used in many industrial applications, such as high-density static random access memories (SRAMs) [1.1], electrical erasable programming read only memories (EEPROMs) [1.2], linear image sensors [1.3], thermal printer heads [1.4], photo-detector amplifier [1.5], scanner [1.6], and active-matrix liquid-crystal displays (AMLCDs) [1.7]-[1.9]. In particular, the application of AMLCDs is the major driving force to promote and advance the developments of poly-Si TFT technology.

AMLCD is one of the most promising candidates for realizing large-area flat-panel displays. The application of n-channel amorphous silicon (α-Si) TFTs is constrained in the aspect of pixel switching elements. Hence, it is difficult to integrate pixel switching elements and peripheral driving circuits on single glass substrate for system-on-panel (SOP) applications because of the low electron field-effect mobility (typically below 1 cm^2/Vs). Moreover, the electrical properties of p-channel α-Si TFTs are worse than those of n-channel α-Si TFTs, making α-Si TFT technology not practical for CMOS circuits. As a result, poly-Si TFT technology has been steadily growing and become a promising solution for realizing high-performance AMLCD applications due to the advantages of high field-effect mobility, low photocurrents, high driving currents, high CMOS capability, and SOP applications [1.10], [1.11].

The quality of poly-Si films plays a critical role in the device performance and

reliability. Three major crystallization techniques have been proposed to achieve low-temperature poly-Si TFTs, described as follows.

1.1.1 Traditional Solid-Phase Crystallization (SPC)

Solid-phase crystallization (SPC) technique is usually performed at 600 ^{o}C [1.12]-[1.15]. The SPC process is composed of grain nucleation and grain growth. For the traditional SPC of α-Si with homogenous grain nucleation at the α-Si/underlyling SiO_2 interface, the activation energy of the grain growth (3.2 eV) is less than that of the grain nucleation (3.9 eV). Therefore, the amount of the nucleation relative to the grain growth decreases with decreasing temperature. Moreover, such crystallized poly-Si films have a high density of grain-boundary defects and intra-grain defects, which degrade the electrical properties of poly-Si TFTs. An improved SPC technique has been proposed to enlarge the grain size of poly-Si by decreasing the grain nucleation rate even if SPC process is a time-consuming (several hours) process for phase transformation from amorphous into polycrystalline.

1.1.2 Metal-Induced Lateral Crystallization (MILC)

Metal-induced crystallization (MIC) technique with crystallization temperature lower than 600 ^{o}C has been studied in the past using trace metals such as Ni, Ge, Al, Au, and Pb [1.16]-[1.20]. However, the grain size of poly-Si is small compared to the feature size of transistor, and an undesirable metal contamination may be introduced at the channel region, degrading the electrical properties of poly-Si TFTs. In addition, poly-Si film with large grain size can be formed by the crystallization of α-Si through metal-induced lateral crystallization (MILC) technique [1.21]-[1-23]. This MILC technique is simple, less contamination, and can be adopted in three-dimensional (3-D) CMOS integrated circuits. The grain size of resulting poly-Si film is significantly enhanced and much larger than the device dimension.

1.1.3 Excimer-Laser Crystallization (ELC)

Excimer-laser crystallization (ELC) of α-Si film on glass substrate gives a good-quality poly-Si with low defect density and no intra-grain defect. Hence, this technique is thought to

be the most preferable crystallization method for the fabrication of poly-Si TFTs [1.24]-[1.28]. While ELC technique is the most commonly used method to manufacture poly-Si TFTs for display applications, there are many ongoing issues, including high manufacturing cost, uniformity concerns over large areas, narrow process window, high process complexity, rough poly-Si/gate oxide interface, and stability of electric performances, need to be resolved to attain a mature ELC poly-Si TFT technology.

Among these three major crystallization techniques, the most widely used method for poly-Si preparation is the SPC technique. Traditional SPC poly-Si TFT has many advantages over ELC poly-Si TFT, such as simplicity, low-cost batch process, high uniformity, and large area capability. Although the maximum processing temperature of SPC poly-Si TFT is limited by the crystallization temperature of around 600 ^{o}C, the processing temperature is still considered to be acceptable.

Poly-Si material consists of silicon crystallites (grains). Between them, there are regions with high density of impurities, called grain boundaries. Grain-boundary defects and intra-grain defects existing in the poly-Si film result in a large amount of trap states. The detrimental effect of grain boundaries on the electrical performances of poly-Si TFT has been investigated and been well recognized [1.29], [1.30]. At the turn-on state, the trap states can trap carriers to form potential barriers, and thus affect the on-state carrier transport [1.31]. At the turn-off state, the trap states in the depletion region of drain side result in large off-state leakage currents. The generation of leakage currents can be attributed to a thermionic emission at a low electric field and a field-enhanced emission (*i.e.* F-P emission or trap-assisted band-to-band tunneling) at a high electric filed [1.32]. The presence of a high density of trap states at the grain boundaries are thought to be related to the Si dangling bonds and Si strain bonds, resulting in severe degradations on the electrical properties of poly-Si TFTs, such as high threshold voltage, low field-effect mobility, large subthreshold swing, and high leakage currents. The grain-boundary effects can be reduced mainly by two

techniques: (1) by passivating the Si dangling bonds at the grain boundaries with plasma treatments and thus reducing the density of the grain-boundary defects [1.33], [1.34]; (2) by enlarging the grain size of poly-Si and thus reducing the number of grain boundaries present within the active channel of poly-Si TFT.

In addition, the device performances could also be improved by adopting novel device structures, including multiple channel structures [1.35], offset source/drain [1.36], [1.37], lightly doped drain (LDD) [1.38], gate-overlapped LDD (GO-LDD) [1.39]-[1.41], field-induced drain (FID) [1.42], and vertical channel [1.43]. This novel device structures focus on decreasing the electric field near the drain junction, and thus suppresses the off-state leakage currents of poly-Si TFTs.

1.2 Motivation

To realize SOP purposes, integrating pixel switching and peripheral driving ICs on single glass substrate are required [1.44]. However, it is a challenge to develop high-performance poly-Si TFTs for both pixel TFTs and display driving circuits [1.45]. To drive the liquid crystal, pixel TFTs operate at high voltages with low gate-leakage currents. In contrast, TFTs with low operation voltages, low subthreshold swing, high driving capability, and low gate-leakage currents are required for approaching high-speed display driving circuits. However, traditional SPC poly-Si TFTs with continued scaling SiO_2 gate dielectric can increase the driving currents of poly-Si TFTs. But, a thinner SiO_2 gate dielectric cannot still satisfy these demands due to the high gate-leakage currents and poor electrical reliability [1.46]. With the same physical gate-dielectric thickness, introducing high dielectric constant (high-κ) material to replace SiO_2 as the gate dielectric can increase the gate capacitance density and then induce much more mobile carrier density in the channel region. Therefore, several high-κ gate dielectrics including ONO gate stack, Al_2O_3,

HfO_2, and $LaAlO_3$, have been proposed as replacement for SiO_2 gate dielectric to improve the electrical performances of poly-Si TFTs due to better gate controllability [1.47]-[1.50]. Unfortunately, the implementation of ONO gate stack and Al_2O_3 could not effectively improve the device performances due to their lower dielectric constant. On the other hand, these polycrystalline high-κ materials might not be sufficiently stable under post-annealing process. Recent studies reported that thermally robust praseodymium oxide (Pr_2O_3) appeared as a promising high-κ gate dielectric in MOSFET owing to its outstanding dielectric properties, including high dielectric constant value of about 31, ultra-low gate-leakage currents, and superior reliability characteristics [1.51], [1.52]. In Chapter 2, poly-Si TFTs with high-κ Pr_2O_3 gate dielectric are demonstrated and investigated.

Nevertheless, such high gate capacitance density contributes to a high electric field at the gate-to-drain overlap area, resulting in more undesirable gate-induced drain leakage (GIDL) currents [1.53]. To address this GIDL current issue, a hydrogen-based plasma treatment technique is mostly adopted for reducing the trap states because hydrogen atoms can easily passivate the trap states at the poly-Si /gate dielectric interface and in the poly-Si grain boundaries [1.54]-[1.57]. However, the hydrogenated poly-Si TFTs suffer from a serious instability issue due to the easily broken of weak Si-H bonds under electrical stress [1.58]. The other promising strategy, fluorine passivation technique, has been utilized to improve the device performance by eliminating the trap states at the grain boundaries. In addition, strong Si-F bonds, more stable than Si-H bonds, can significantly improve the device reliability under long-term electrical stress [1.59], [1.60]. In Chapter 3 and 4, both fluorine ion implantation and low-temperature CF_4 plasma treatment on poly-Si films are developed to effectively introduce fluorine atoms into the poly-Si film. Incorporating these two fluorine-passivated techniques into poly-Si TFTs with Pr_2O_3 gate dielectric are proposed and studied.

Moreover, the SPC process plays an important role to affect the electrical characteristics

of poly-Si TFTs [1.61]-[1.63]. For the traditional SPC process, an interface-nucleation scehme with too many nucleation sites at the α-Si/underlying SiO_2 interface results in a small grain size and a large number of grain-boundary trap states [1.64]-[1.67]. Thus, many studies have been proposed to improve the microstructure of poly-Si film by introducing oxygen rich region at the α-Si/underlying SiO_2 interface [1.68], [1.69]. The interface nucleation is effectively suppressed, and then the nucleation process with fewer nucleation sites initiating on the top free surface of α-Si film results in large grain size of poly-Si film. In Chapter 4 and 5, two kinds of grain-size enhancement techniques associating with the surface-nucleation scheme, including deep Argon ion implantation into the α-Si/underlying SiO_2 interface and novel floating-channel structure are proposed. Poly-Si TFTs with deep Argon ion implantation and floating-channel structure are demonstrated and investigated.

In addition, a lot of efforts have been put forth to improve the gate controllability and device performance by changing device structure of poly-Si TFTs with complicated steps, such as gate-overlapped lightly doped drain (GO-LDD) TFT [1.70], double-gate TFT [1.71], and gate-all-around TFT [1.72]. Besides, poly-Si TFTs with nano-scale feature sizes have also been proposed to reduce the influences of grain-boundary defects [1.73]-[1.77]. In these studies, the electrical performances of poly-Si TFTs could be remarkably improved by decreasing the channel dimensions to be comparable to, or still smaller than, the grain size. However, poly-Si TFTs with narrow-width channels are directly defined by using costly electron-beam lithography (EBL) technology [1.73]-[1.75], which could not be practicable in flat-panel displays (FPDs). On the other hand, for the poly-Si TFTs with nanowire (NW) channels and multiple-gate configuration reported in [1.76], [1.77], the gate-induced drain leakage (GIDL) currents resulted from large gate-to-drain overlapping area is high and must be addressed by additional processes. In Chapter 6, we demonstrate a simple sidewall spacer technique to fabricate poly-Si TFTs with self-aligned formation of twin NW channels without any expensive photolithography process. Poly-Si TFTs with NW channels

crystallized by traditional SPC technique and advanced MILC technique are proposed and investigated.

1.3 Thesis Organization

This thesis is organized as follows,

In Chapter 1, the overview of poly-Si TFTs and the motivations of this thesis are described.

In Chapter 2, TiN metal gate and high-κ Pr_2O_3 gate dielectric are integrated into the SPC poly-Si TFTs. The integrity of the high-κ Pr_2O_3 gate dielectric is explored. The electrical characteristics and the short-channel effects of the poly-Si TFTs with Pr_2O_3 gate dielectric are studied.

In Chapter 3, two kinds of fluorine passivation effects using fluorine ion implantation and low-temperature CF_4 plasma treatments are applied to the poly-Si TFTs with Pr_2O_3 gate dielectric are investigated. Effects of fluorine ion implantation and various rf powers of CF_4 plasma treatments on the poly-Si films are explored. The electrical characteristics and reliability of the fluorine-passivated poly-Si TFTs with Pr_2O_3 gate dielectric are investigated.

In Chapter 4, deep Argon ion implantation with projection range beyond on the a-Si/underlying SiO_2 interface is proposed to investigate the microstructure of postcrystallized poly-Si film. The electrical characteristics and reliability of SPC poly-Si TFTs with Argon ion implantation are demonstrated and studied.

In Chapter 5, poly-Si TFTs with floating-channel structure crystallized by solid-phase crystallization process are proposed and fabricated. The grain size and trap-state density of poly-Si film with floating-channel structure are analyzed; moreover, the electrical characteristics and reliability of SPC poly-Si TFTs with floating-channel structure are explored and studied.

In Chapter 6, a simple sidewall spacer technique is proposed for the formation of nano-scale channel width (nanowire, NW) without advanced photolithography system. The crystallization of poly-Si NW channels is formed by the SPC and MILC techniques. Effects of gate controllability on the proposed SPC NW TFTs and standard planar TFTs are explored. Besides, the electrical properties of the MILC NW TFTs and the SPC NW TFTs are demonstrated and investigated.

In Chapter 7, conclusions as well as some recommendations for further research are given.

Chapter 2

High-Performance Polycrystalline Silicon Thin-Film Transistors with High-κ Pr_2O_3 Gate Dielectric

2.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention in active-matrix liquid crystal displays (AMLCDs) for the sake of realizing the integration of peripheral driving circuits and pixel switching elements on single glass substrate to accomplish system-on-panel (SOP) purposes [2.1]-[2.3]. High-performance poly-Si TFTs with low operation voltages, low subthreshold swing, high driving capability, and low gate-leakage currents are required for approaching high-speed display driving circuits. However, traditional solid-phase crystallized (SPC) poly-Si TFTs with continued scaling SiO_2 gate dielectric can not satisfy these demands [2.4]. In order to address these issues, integrating metal gate on high dielectric constant (high-κ) gate dielectric with poly-Si TFTs has received lots of attention for maintaining a higher gate capacitance density, a lower gate-leakage current, and a much more induced carrier density [2.5]-[2.11]. Besides, the trap states at poly-Si grain boundaries also could be quickly filled up to improve the subthreshold swing even without additional hydrogenation treatments [2.7]. Therefore, several high-κ gate dielectrics including ONO gate stack, Al_2O_3, HfO_2, and $LaAlO_3$ have been investigated as replacement for SiO_2 gate dielectric to improve the electrical performances owing to better gate controllability [2.8]-[2.11]. Unfortunately, the implementation of ONO gate stack and Al_2O_3 could not effectively improve the device performances due to their lower dielectric constant. On the other hand, these polycrystalline high-κ materials might not be sufficiently

stable under post-annealing process. Recent studies reported that thermally robust praseodymium oxide (Pr_2O_3) appeared as a promising high-κ gate dielectric in MOSFET owing to its outstanding dielectric properties, including high dielectric constant (~31), ultra-low gate-leakage currents, and superior reliability characteristics [2.12], [2.13].

In this chapter, integrating TiN metal gate on high-κ Pr_2O_3 gate dielectric with SPC poly-Si TFTs is successfully demonstrated for the first time. The proposed poly-Si Pr_2O_3 TFTs show outstanding electrical characteristics as compared to poly-Si tetraethoxysilane (TEOS) TFTs; hence, poly-Si Pr_2O_3 TFTs can satisfy the needs of peripheral driving circuit applications with low operation voltages.

2.2 Experiments

The cross section of the proposed poly-Si TFTs with TiN metal gate and Pr_2O_3 gate dielectric is depicted in Fig. 2.1. The detail device fabrication is summarized below. First, a 100-nm amorphous silicon (α-Si) was deposited on 500-nm thermally oxidized Si wafers using low-pressure chemical vapor deposition (LPCVD) system at 550 ^oC [Fig. 2.1(a)]. Subsequently, the SPC annealing process at 600 ^oC for 24 h in N_2 ambient was used to crystallize the α-Si film. After the active regions were defined [Fig. 2.1(b)], a 33.6-nm Pr_2O_3 gate dielectric was deposited by using electron-gun evaporation system, and then annealed at 600 ^oC for 30 min in O_2 ambient to improve thin-film quality. After the deposition of a 200-nm TiN film, a Cl_2 based plasma etching process capable of stopping on the Pr_2O_3 layer was used to pattern the gate electrode [Fig. 2.1(c)]. A self-aligned phosphorous ion implantation was performed, followed by the dopant activation at 600 ^oC for 30 min in N_2 ambient [Fig. 2.1(d)]. After a 300-nm passivation SiO_2 was deposited by plasma-enhanced CVD (PECVD), the definition of contact holes were achieved with the selective wet etching of passivation SiO_2 and Pr_2O_3 by buffered oxide etch (BOE) and H_2SO_4/H_2O_2 solutions

[2.14], respectively [Fig. 2.1(e)]. Finally, the fabricated poly-Si Pr_2O_3 TFTs were sintered at 400 ^oC after the aluminum pad formation [Fig. 2.1(f)]. Moreover, the poly-Si TFTs with a 35-nm TEOS gate dielectric deposited by PECVD were also fabricated with the same process flow for comparison. Note that all the poly-Si TFTs had no hydrogenation treatment in this work.

2.3 Results and Discussion

2.3.1 Pr_2O_3 Gate Dielectric Integrity

The cross-sectional transmission electron microscopy (XTEM) image of the proposed poly-Si TFTs is shown in Fig. 2.2, which indicates a physical thickness of Pr_2O_3 gate dielectric around 33.6 nm with a 1.5-nm interfacial SiO_2-like layer. An accumulation capacitance of 532 nF/cm^2 is achieved for Pr_2O_3 gate dielectric from capacitance-voltage (C-V) measurement as shown in Fig. 2.3. Therefore, the equivalent-oxide thickness (EOT) was extracted to be 6.5 nm. The effective dielectric constant (κ_{Pr2O3}) of Pr_2O_3 gate dielectric was extracted by using a Pr_2O_3/interfacial-SiO_2 series capacitor model, expressed as Eq. (2.1) [2.15].

$$EOT = T_{interficial\text{-}SiO_2} + (k_{interfacial\text{-}SiO_2}/k_{Pr_2O_3}) \times T_{Pr_2O_3} \quad \text{.....Eq. (2.1)}$$

where κ_{Pr2O3} and $\kappa_{interfacial\text{-}SiO2}$ are the dielectric constants for Pr_2O_3 and interfacial-SiO_2 films, respectively, and T_{Pr2O3} and $T_{interfacial\text{-}SiO2}$ are the thicknesses of these films. Based on the relation in Eq. (2.1), the κ_{Pr2O3} was evaluated to be 26.2 by assuming the $\kappa_{interfacial\text{-}SiO2}$ to be 3.9. Moreover, no C-V hysteresis characteristic on Pr_2O_3 gate dielectric occurs after repeating ±4 V forward and reverse stresses for 100 times.

Fig. 2.4 shows the gate current density versus electric field (J-E) characteristic of the Pr_2O_3 gate dielectric film. The J-E characteristic of the Pr_2O_3 gate dielectric was measured by applying a gate voltage, with grounding the source and drain of poly-Si TFTs with Pr_2O_3

gate dielectric. Obviously, the breakdown field of the Pr_2O_3 gate dielectric is around 6.8 MV/cm, which is larger than that of the PECVD TEOS oxide of 5.4 MV/cm. Therefore, such high gate capacitance density, low charge-trapping phenomenon, and high dielectric breakdown field suggest that the Pr_2O_3 film is a promising high-κ gate-dielectric candidate for replacing conventional SiO_2 film in the poly-Si TFTs.

The chemical composition of the Pr_2O_3 gate dielectric was determined by x-ray photoelectron spectroscopy (XPS) measurement. In this perspective, the XPS analysis was performed on a 33.6-nm Pr_2O_3 thin film. The XPS spectra of the Pr3d and O1s core level spectral regions are displayed in Figs. 2.5(a) and 2.5(b), respectively. The Pr3d signals consist of the $3d_{5/2}$ and $3d_{3/2}$ spin-orbit doublets. The main Pr3d XPS peak is centered at 934 eV, and its spin-orbit component is well separated at 954 eV. The shape, binding-energy values, and spin-orbit splitting associated with present Pr_2O_3 features are in agreement with previous reported data and indicate the existence of the Pr_2O_3 phase [2.16]. The shape of O1s XPS feature is quite complicated because of the overlap of different contributions. The visible peak at lower binding energy of 530 eV can be regarded as the Pr-O bonding. At higher binding energy of 533 eV, there is a broad signal due to the overlap of different components associated with SiO_2 and hydroxides, that are formed on the film surface.

2.3.2 Device Characteristics

Fig. 2.6 shows the typical transfer characteristics (I_{DS}-V_{GS}) and transconductanes for the proposed poly-Si TFTs with Pr_2O_3 and TEOS gate dielectric with a dimension of width/length (W/L) = 2 μm/2 μm. The threshold voltage (V_{TH}) is defined as the gate voltage required a normalized drain current of I_{DS} = (W/L)×100 nA at V_{DS} = 0.1 V. The ON/OFF current ratio (I_{ON}/I_{OFF}) is defined as that ratio of the maximum on-state current to the minimum off-state current at V_{DS} = 1 V. The poly-Si Pr_2O_3 TFT exhibits superior electrical performance than poly-Si TEOS TFT, including threshold voltage decreased from 2.28 to

1.27 V, subthreshold swing (S.S.) improved from 1.08 to 0.22 V/dec., field-effect mobility (μ_{FE}) enhanced from 23 to 40 cm^2/V-s, and I_{ON}/I_{OFF} ratio increased from 3.5×10^6 to 10.6×10^6. However, undesirable gate-induced drain leakage (GIDL) currents of the poly-Si Pr_2O_3 TFTs are higher than those of the poly-Si TEOS TFTs, especially under a continuously decreasing gate bias. The inferior GIDL currents may be ascribed to the higher electric field near the drain junction owing to the higher gate capacitance density of the high-κ Pr_2O_3 gate dielectric. The GIDL current issue could be solved by using lightly doped drain (LDD) structure [2.17].

2.3.3 Output Characteristics

Typical output characteristics (I_{DS}-V_{DS}) of the proposed poly-Si Pr_2O_3 TFTs and poly-Si TEOS TFTs are illustrated in Fig. 2.7. The device has a drawn channel length (L) and channel width (W) of 2 μm and 2 μm, respectively. As can be seen, the driving current of the poly-Si Pr_2O_3 TFTs (around 97 μA) is approximately six times larger than that of the poly-Si TEOS TFTs (around 16 μA) at V_{DS} = 4 V and common gate drive of V_{GS}–V_{TH} = 4 V. This driving current enhancement results from the high capacitance density induced higher mobility and smaller threshold voltage for the poly-Si Pr_2O_3 TFTs compared with the poly-Si TEOS TFTs. Also, These excellent performances of poly-Si TFTs can be approached by SPC technique, without extra plasma treatments [2.6], or other advanced phase crystallization techniques with narrow process window [2.18], [2.19]. Hence, this large driving capability is attractive for high-speed peripheral driving IC's applications.

2.3.4 Comparison with Other Researches

The measured and extracted device parameters are summarized in Table 2.1, including the other reported data for the SPC poly-Si TFTs with HfO_2 [2.10] and $LaAlO_3$ [2.11] gate dielectrics. This work provides the thinnest EOT of 6.5 nm realized on SPC poly-Si TFTs

with high-κ gate dielectrics. Without narrow channel-width effect [2.20], the calculated field-effect mobility of the poly-Si Pr_2O_3 TFTs is competed with that of the other reported poly-Si high-κ TFTs. By using refractory metal TiN [2.5], [2.6], the self-aligned implantation and dopant activation can be integrated into poly-Si Pr_2O_3 TFTs after metal gate formation. The higher gate capacitance density of high-κ Pr_2O_3 can quickly fill up the trap states at the grain boundaries in the poly-Si channel. Therefore, the performances of poly-Si Pr_2O_3 TFTs can be further improved, including moderate threshold voltage, lower subthreshold swing, and higher ON/OFF current ratio.

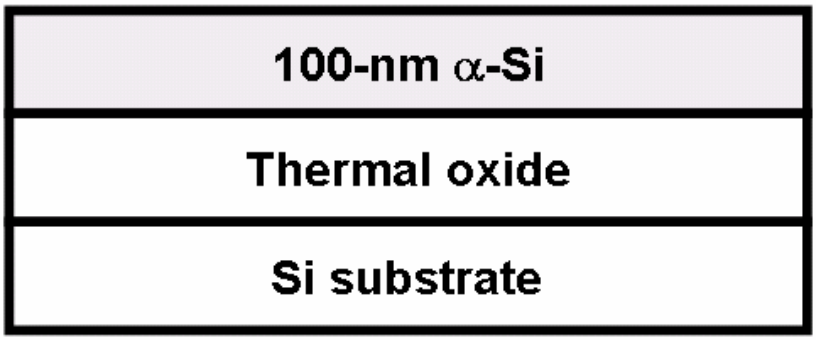
2.3.5 Threshold-Voltage Rolloff

To investigate the short-channel effects of the poly-Si Pr_2O_3 TFTs and poly-Si TEOS TFTs, the threshold-voltage rolloff properties are shown in Fig. 2.8. The threshold voltage of the poly-Si TFTs with SiO_2 gate dielectric is decreased with continuously scaling down channel length, dominated by the reduction of grain-boundary trap states. In contrast, the poly-Si TFTs with Pr_2O_3 gate dielectric exhibit a high gate capacitance density to rapidly fill up the grain-boundary trap states and holds superior turn-on characteristics, and thus the threshold-voltage rolloff property could be well controlled.

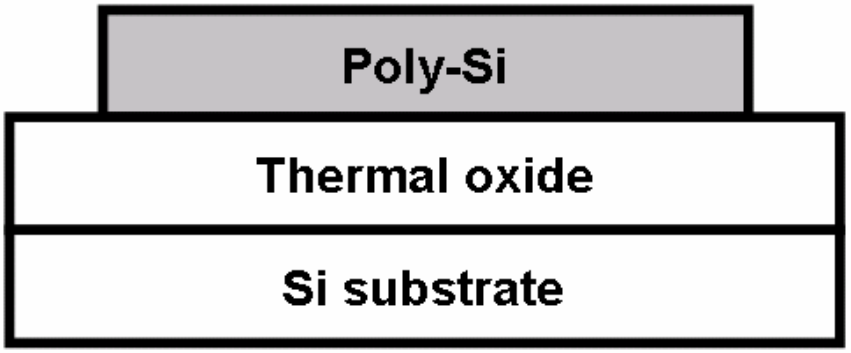
2.4 Summary

High-performance SPC poly-Si TFTs integrated with Pr_2O_3 gate dielectric and TiN metal gate have been successfully demonstrated for the first time. This work provides the thinnest EOT of 6.5 nm from the high gate capacitance density of Pr_2O_3 film. The electrical characteristics of poly-Si Pr_2O_3 TFTs can be effectively improved compared to those of poly-Si TEOS TFTs, including lower threshold voltage, steeper subthreshold swing, higher field-effect mobility, and higher driving current capability, even without additional

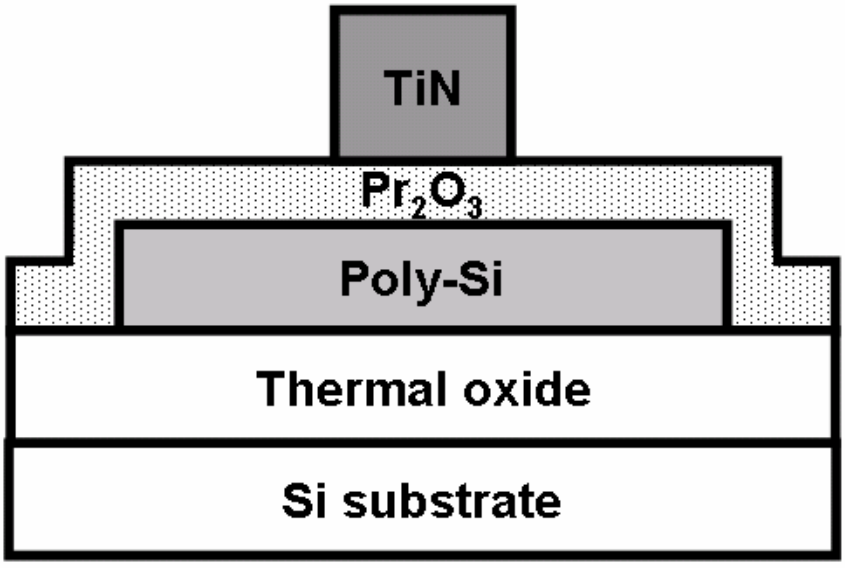
hydrogenation treatments or advanced phase crystallization techniques. Therefore, the proposed poly-Si Pr_2O_3 TFT technology is a promising candidate for future high-speed display driving circuit applications.



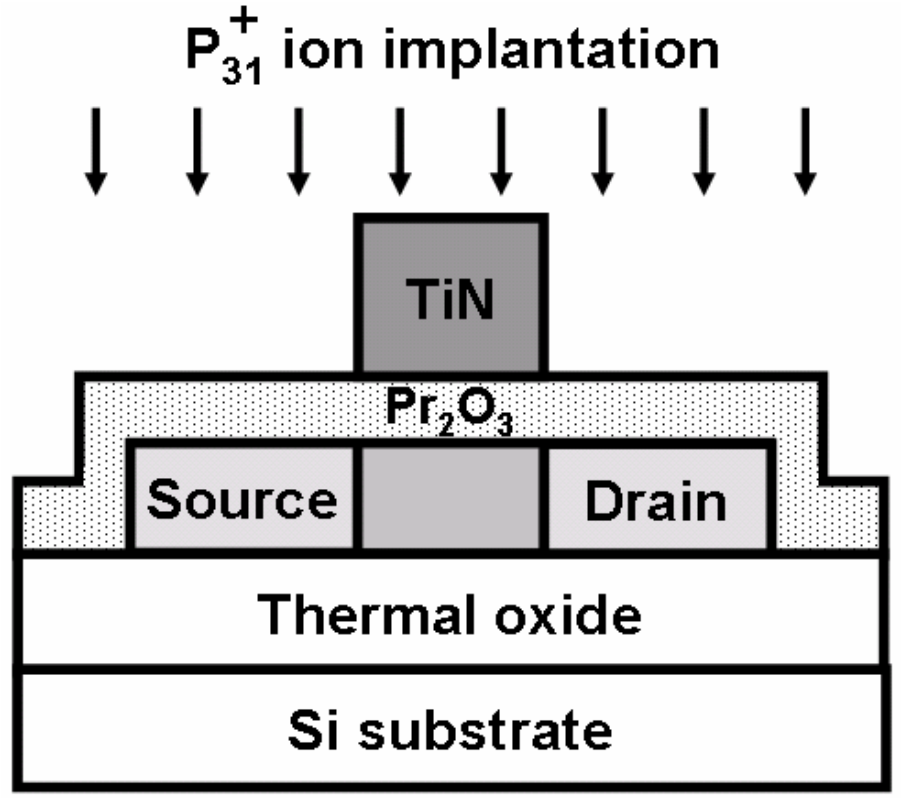
(a) Thermal oxidation, and α-Si deposition.



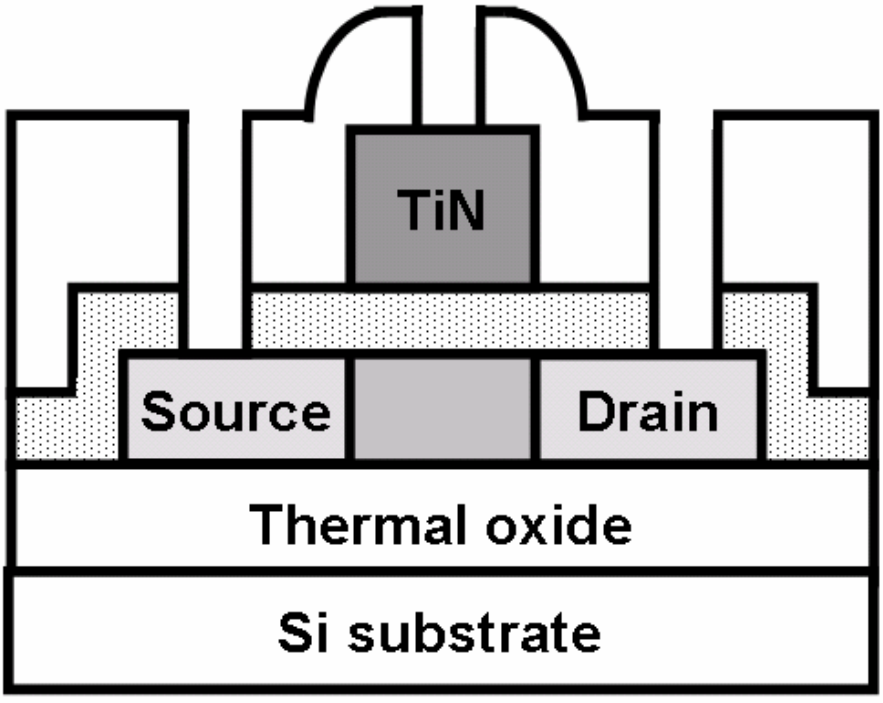
(b) Solid-phase crystallization of α-Si, and patterning of active region.



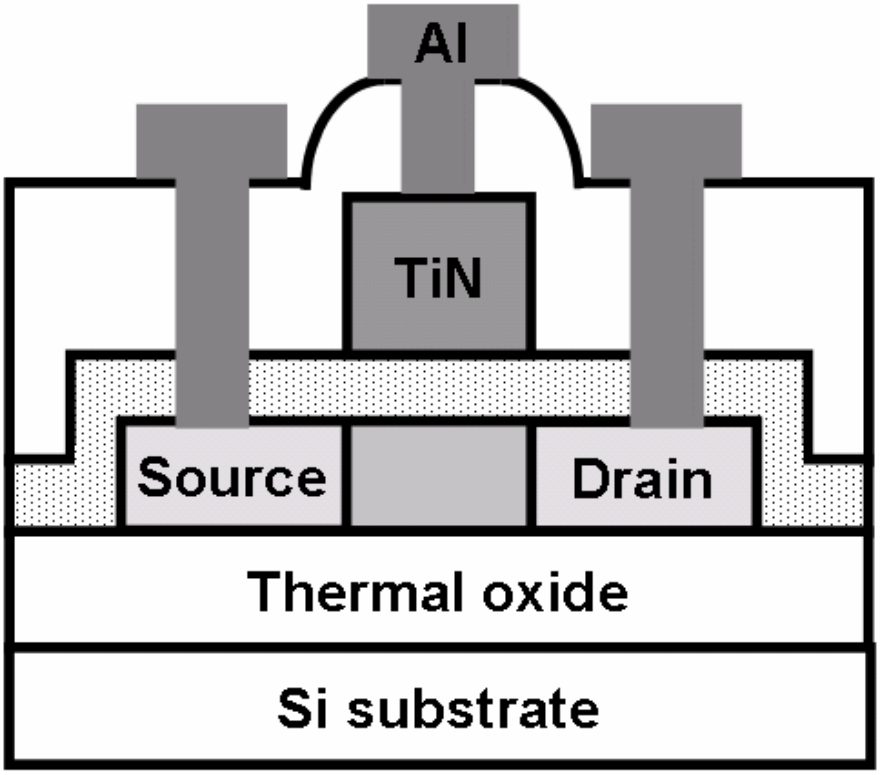
(c) Pr_2O_3 deposition and densification, TiN deposition, and patterning of gate electrode.



(d) Self-aligned phosphorus ion implantation, and dopant activation.



(e) Passivation oxide deposition, and patterning of contact hole.



(f) Al deposition, patterning of metal pad, and thermal sintering.

Fig. 2.1 Schematic process flows of the poly-Si TFTs with TiN metal gate and Pr_2O_3 gate dielectric.

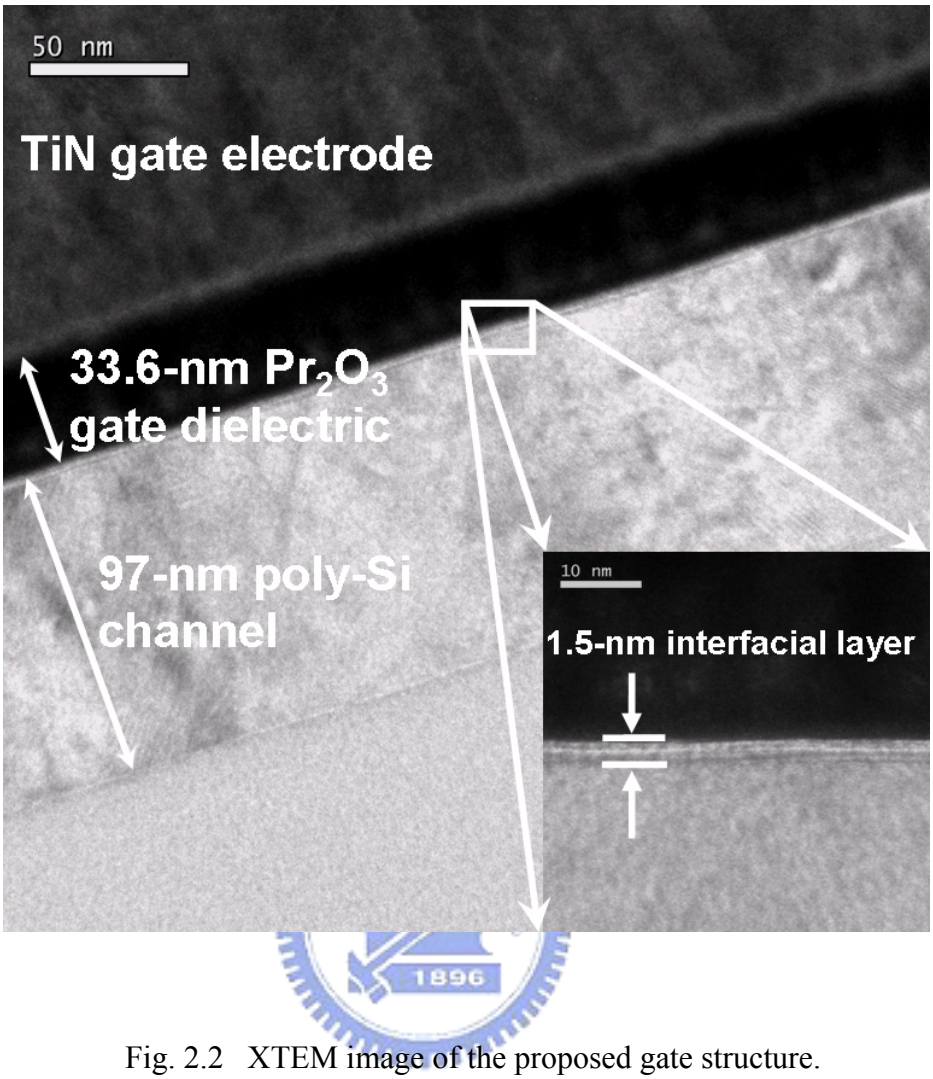


Fig. 2.2 XTEM image of the proposed gate structure.

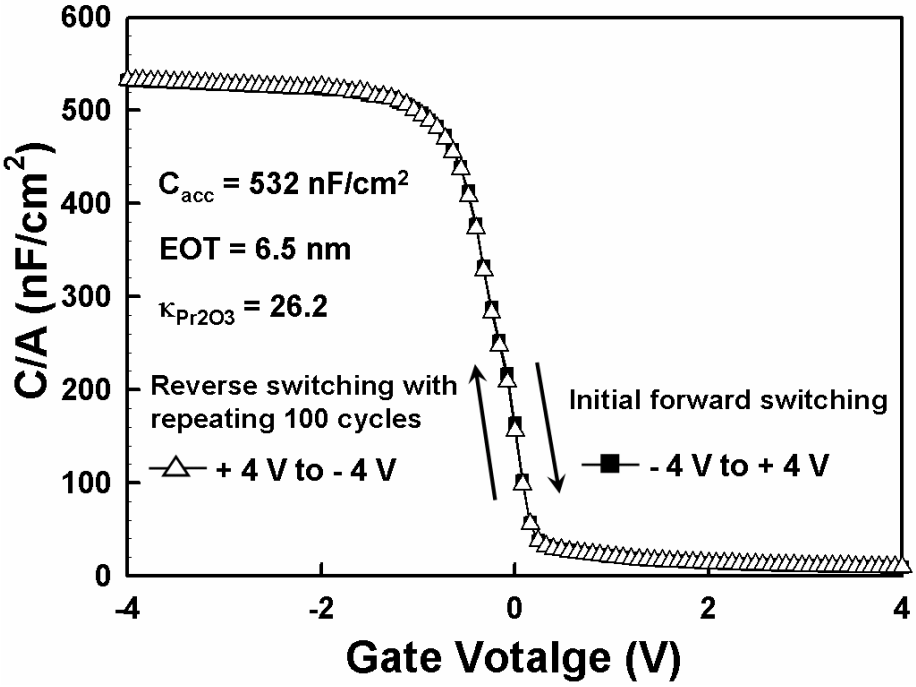


Fig. 2.3 The capacitance-voltage measurement of the Pr_2O_3 gate dielectric after repeating ± 4 V forward and reverse stresses for 100 times.

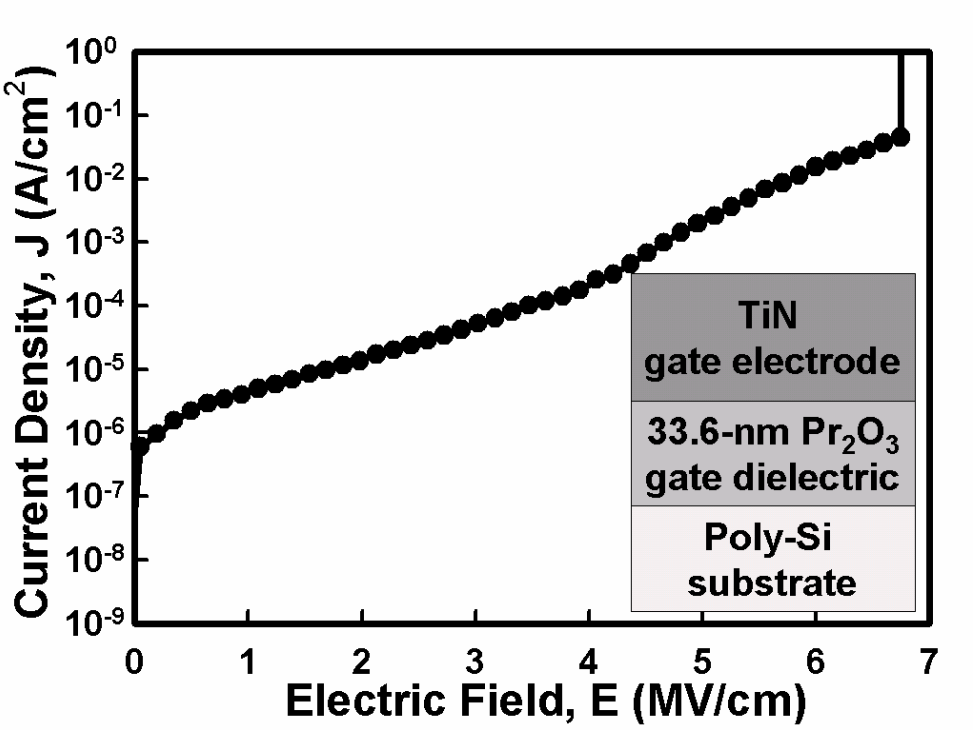
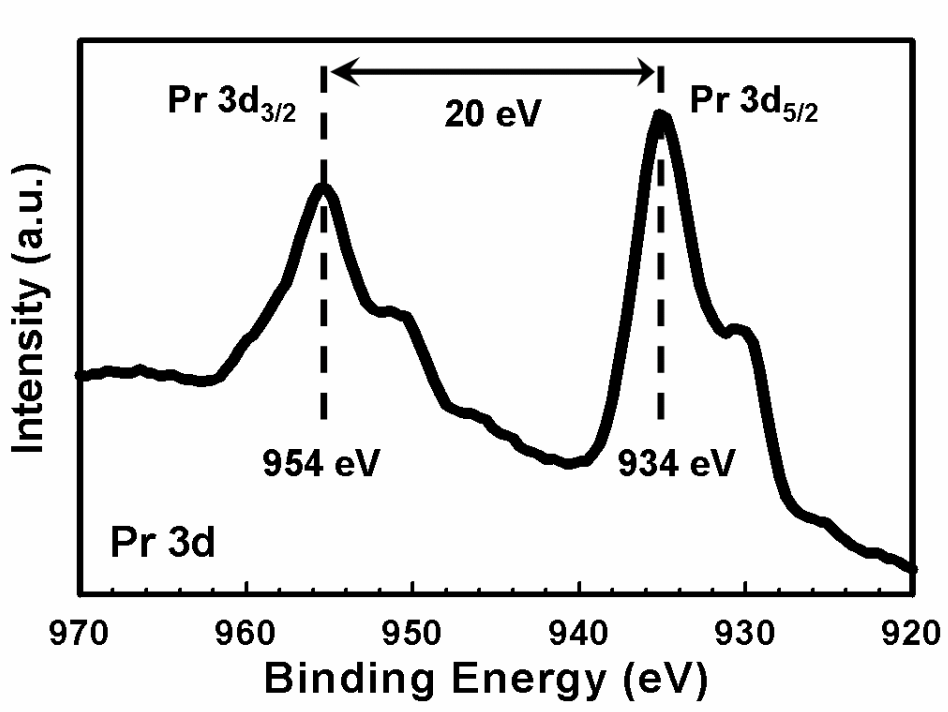
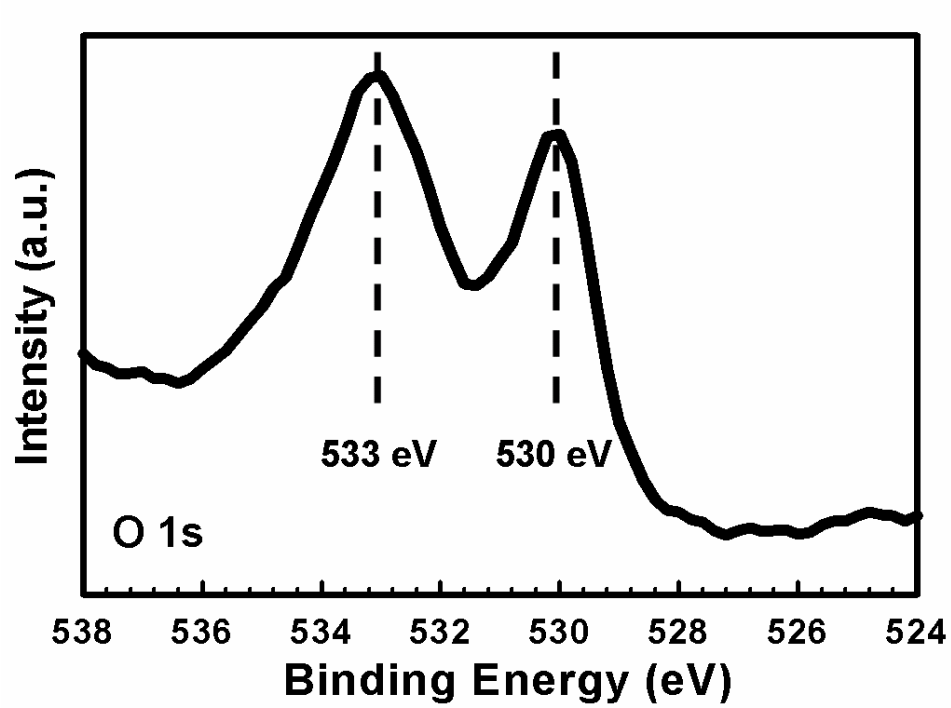


Fig. 2.4 Gate-current density versus electric field (J-E) characteristic of the poly-Si TFTs with TiN metal gate and Pr_2O_3 gate dielectric.



(a) XPS spectra of Pr3d core level.



(a) XPS spectra of O1s core level.

Fig. 2.5 The XPS spectra of Pr3d and O1s for the Pr_2O_3 gate dielectric.

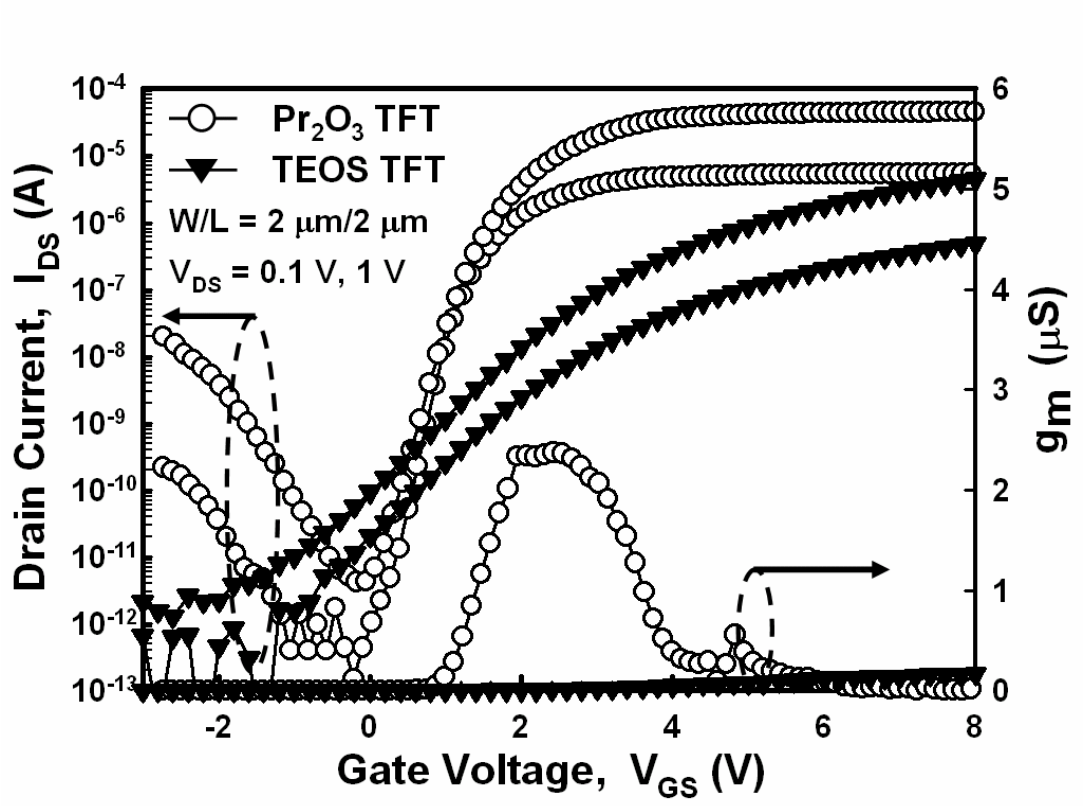


Fig. 2.6 Typical transfer characteristics of the proposed poly-Si Pr_2O_3 TFTs and the poly-Si TEOS TFTs with a dimension of W/L = 2 μm/2 μm.

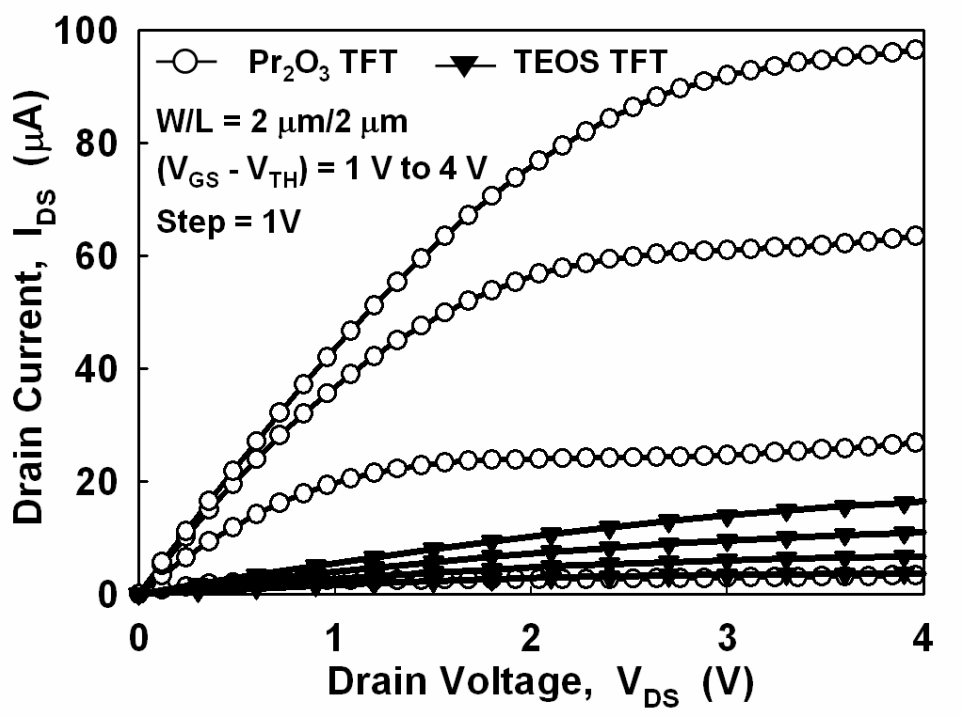


Fig. 2.7 Output characteristics of the proposed poly-Si Pr_2O_3 TFTs and the poly-Si TEOS TFTs with a dimension of W/L = 2 μm/2 μm.

Table 2.1 Electrical characteristics comparison for SPC poly-Si TFTs with various gate dielectrics, including Pr_2O_3 as well as TEOS oxide from this work, HfO_2, and $LaAlO_3$.

SPC poly-Si TFT with various gate dielectrics	Pr_2O_3 [This work]	HfO_2 [10]	$LaAlO_3$ [11]	PECVD TEOS [This work]
$T_{Physical}$/ EOT	33.6 nm/ 6.5 nm	27.7 nm/ 7.3 nm	50 nm/ 8.7 nm	35 nm/ 42.6 nm
W/L (μm)	2/2	0.1/1	100/4	2/2
V_{TH} (V)	1.27	0.3	1.2	2.28
S.S. (V/decade)	0.22	0.28	0.31	1.08
μ_{EF} (cm^2/V-s)	40	39	40	23
I_{ON}/I_{OFF} ratio (10^6)	10.6	9.7	1.5	3.5

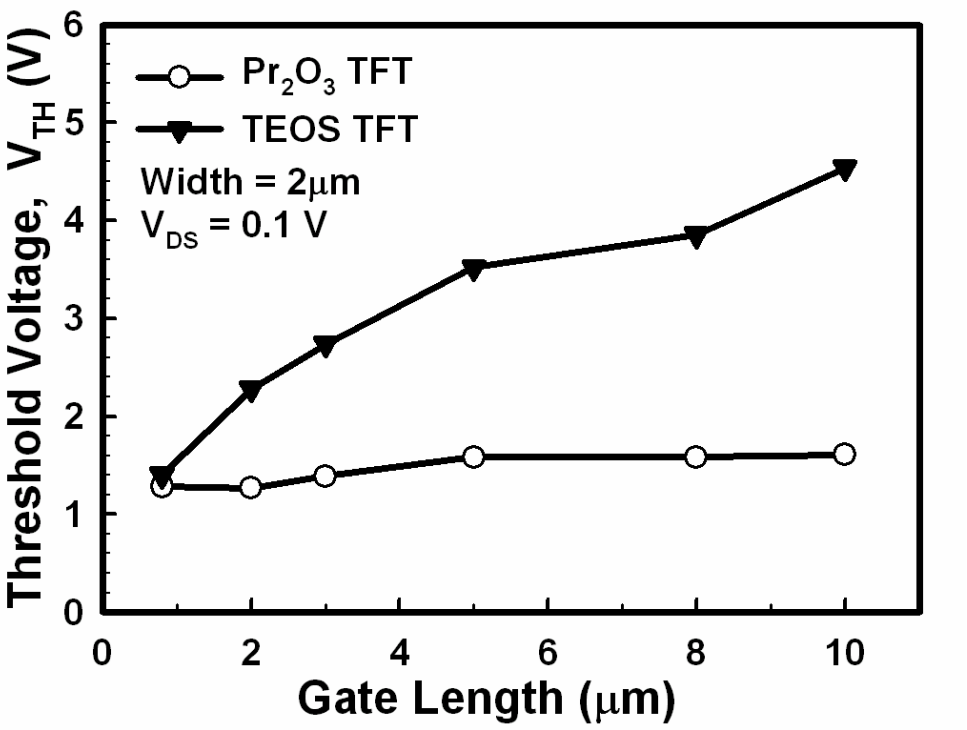


Fig. 2.8 Threshold-voltage rolloff propoerties of the proposed poly-Si Pr_2O_3 TFTs and the poly-Si TEOS TFTs at V_{DS} = 0.1 V.

Chapter 3

Characterizing Fluorine-Ion Implant and CF_4 Plasma Treatment Effects on Polycrystalline Silicon Thin-Film Transistors with Pr_2O_3 Gate Dielectric

3.1 Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) have received a considerable attention in fields such as large-area electronic applications including linear image sensors and active-matrix liquid crystal displays (AMLCDs) [3.1], [3.2]. The major application of poly-Si TFTs in AMLCDs lies in integrating the peripheral driving circuits and the pixel switching elements on the same glass substrate to realize system-integration-on-panel (SOP) technology [3.3]. The complicated process can be greatly simplified and then the fabrication cost also can be reduced by realizing SOP technology. Because poly-Si TFTs are usually fabricated on inexpensive glass substrate, low-temperature process is required for the realization of commercial flat-panel displays (FPDs). The solid-phase crystallization (SPC) process with maximum process temperature limiting to 600 °C is widely used to recrystallize amorphous silicon film due to its low production cost and good grain-size uniformity [3.4]. However, it is difficult to develop high-performance and high-reliability poly-Si TFTs that are applicable for both pixel switching elements and peripheral driving circuits. Pixel switching elements require TFTs to operate at high voltages as well as low gate-leakage currents to drive the liquid crystals. In contrast, TFTs with good electrical characteristics including low operation voltages, low subthreshold swings, high driving currents, and low gate-leakage currents are necessary for achieving the peripheral driving circuit applications.

However, the electrical properties of the SPC poly-Si TFTs are not good enough to meet the requirements of driving circuits. The SPC poly-Si TFTs with thinner physical thickness of SiO_2 gate dielectric can increase the gate capacitance density to enhance the driving capability, but higher gate-leakage currents could be introduced by the thinner SiO_2 gate dielectric, which would unavoidably degrade the device performances [3.5].

In order to address this issue, incorporating high-κ gate dielectrics into poly-Si TFTs can increase the gate capacitance density and then induce more mobile carriers in the channel region. To reach the same value of gate capacitance density, the physical thickness of high-κ gate dielectrics can be thicker than that of SiO_2 gate dielectrics. Therefore, poly-Si TFTs with high-κ gate dielectrics can improve the gate controllability for enhancing the driving currents and suppressing the gate-leakage currents. Several high-κ materials including ONO gate stack, Al_2O_3, and Ta_2O_5, were proposed to replace conventional SiO_2 to serve as the gate dielectrics of poly-Si TFTs [3.6]-[3.8]. However, the performance enhancement of the foregoing poly-Si TFTs is restricted by the lower dielectric constant of ONO gate stack as well as Al_2O_3 ($\kappa < 9$) and the narrow bandgap of Ta_2O_5. Recently, praseodymium oxide (Pr_2O_3) becomes a promising high-κ gate-dielectric candidate in MOSFET due to its high dielectric constant value of about 31, low gate-leakage currents, good dielectric properties, and superior thermal stability [3.9], [3.10]. Poly-Si TFTs incorporating Pr_2O_3 as gate dielectric have been proposed in our previous work [3.11], Chapter 2, which resolved the issues mentioned previously.

However, such high gate capacitance density would contribute to a high electric field at the gate-to-drain overlap area, resulting in rather high field-enhanced emission rates via the grain-boundary trap states. Therefore, poly-Si TFTs with high-κ gate dielectrics would suffer from more undesirable gate-induced drain leakage (GIDL) currents [3.12]. To address this GIDL current issue, various techniques including hydrogen plasma treatments and fluorine ion implantation on poly-Si films have been applied to greatly improve the device

performances by reducing the trap-state densities [3.13]-[3.16]. However, the hydrogenated poly-Si TFTs suffer from a serious instability issue due to the easily broken of weak Si-H bonds under electrical stress [3.14]. Another promising strategy, fluorine ion implantation, has been utilized to improve the device performances by effectively eliminating the trap states at the grain boundaries. In addition, strong Si-F bonds, more stable than Si-H bonds, formed in the poly-Si film and at the poly-Si/gate dielectric interface can significantly improve the device reliability under long-term electrical stress [3.15], [3.16]. However, the fluorine ion implantation method has troublesome problems in large-area electronics and subsequent high-temperature annealing is also required to activate the implanted fluorine ions and cure implant-indcued damages.

In this chapter, two kinds of simple, effective, and process-compatible fluorine-passivation techniques, fluorine ion implantation and low-temperature CF_4 plasma treatments, have been utilized to introduce the fluorine ions into the poly-Si films for eliminating the trap states. CF_4 plasma-treated process is more uncomplicated than fluorine-implanted process because of the lack of fluorine ion implantation and additional annealing step. We have successfully integrated these two kinds of fluorine-passivation techniques into the poly-Si TFTs with Pr_2O_3 gate dielectric and characterized their electrical and reliability characteristics.

3.2 Experiments

Fig. 3.1 illustrates the key fabrication steps for the proposed poly-Si Pr_2O_3 TFTs with fluorine ion implantation and CF_4 plasma treatments. First, we describe the fluorine ion implantation process as follows. A 50-nm undoped amorphous silicon (α-Si) layer was deposited on a thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550 ^{o}C [Fig. 3.1(a-1)]. Following, the fluorine

ion implantation was realized with the accelerating energy and dosage at 10 keV and 5×10^{12} cm^{-2}, respectively [Fig. 3.1(b-1)]. The fluorine ions were implanted into the α-Si layer with the projection range locating at the middle of the α-Si film. Subsequently, a solid-phase crystallization (SPC) process was performed at 600 ^{o}C for 24 h in N_2 ambient for phase transformation from amorphous to polycrystalline and activation of fluorine-ion dopants. Individual active regions were patterned and defined [Fig. 3.1(c-1)]. A 40-nm Pr_2O_3 gate dielectric was deposited by electron-beam evaporation system, and densified at 600 ^{o}C for 30 min in O_2 ambient to improve the gate-dielectric quality. Second, we depict the CF_4 plasma treatment technique as follows. A 100-nm α-Si layer was deposited on a thermally oxidized Si wafer [Fig. 3.1(a-2)], and then followed by the realization of SPC process and the definition of individual active region [Fig. 3.1(b-2)]. After RCA clean process, a CF_4 plasma treatment process was applied on the recrystallizaed poly-Si film by plasma-enhanced CVD (PECVD) system at 350 ^{o}C [Fig. 3.1(c-2)]. The chamber pressure and flow rate of CF_4 reaction gas were 400 mtorr and 80 sccm, respectively. To investigate the effect of CF_4 plasma treatments on the poly-Si Pr_2O_3 TFTs, various radio frequency (rf) powers of 0 W, 10 W, and 20 W, with a constant treating time of 20 s, were used to perform the CF_4 plasma treatments. A 33.6-nm Pr_2O_3 gate dielectric was deposited by electron-beam evaporation, followed by a realization of thermal annealing treatment at 600 ^{o}C for 30 min in O_2 ambient. Afterwards, the fluorine-implanted and CF_4 plasma-treated poly-Si films were performed with the same following processes. After a 200-nm TiN film was deposited, a Cl_2 based dry etching process capable of stopping on the Pr_2O_3 layer was used to pattern the gate electrode [Fig. 3.1(d-1) and 3.1(d-2)]]. A self-aligned phosphorous ion implantation was performed to dope the source/drain regions and then the dopant was activated by the thermal budget of 600 ^{o}C for 30 min [Fig. 3.1(e)]. After a 300-nm passivation SiO_2 layer was deposited by PECVD system at 300 ^{o}C, the contact holes were opened by a two-step wet etching process. The 300-nm passivation SiO_2 layer and the Pr_2O_3 layer were etched away by a buffered

oxide etch (BOE) solution and a H_2SO_4/H_2O_2 mixture solution, respectively [Fig. 3.1(f)]. Since the H_2SO_4/H_2O_2 mixture solution has rather high etching selectivity of the Pr_2O_3 film to the passivation SiO_2 layer, the Pr_2O_3 film can be completely etched away by an excess of overetching. Finally, a typical 400-nm Al metallization completed the fabrication process [Fig. 3.1(g)]. For comparison, the control poly-Si Pr_2O_3 TFTs without the fluorine ion implantation step and the CF_4 plasma treatment, rf power of 0 W, were also prepared with the same process flow. In order to study the fluorine-passivation effects on the poly-Si Pr_2O_3 TFTs, no additional hydrogen plasma treatment and thermal sintering process were performed after the Al electrode formation.

3.3 Results and Discussion

3.3.1 Fluorine-Ion Implant Effect on Pr_2O_3 TFTs

3.3.1.1 Pr_2O_3 Gate Dielectric Integrity

The cross-sectional transmission electron microscopy (XTEM) image of the integrated Pr_2O_3 gate dielectric on the fluorine-implanted poly-Si TFTs is depicted in Fig. 3.2. From the XTEM image, the physical thicknesses of the Pr_2O_3 gate dielectric and the poly-Si channel are around 40 nm and 48 nm, respectively. The higher resolution XTEM image near the Pr_2O_3/poly-Si interface displayed in the inset of Fig. 3.2 exhibits an around 1.5-nm SiO_2-like interfacial layer between the Pr_2O_3 gate dielectric and poly-Si channel. A metal-oxide-semiconductor (MOS) capacitor with Pr_2O_3 gate dielectric on single-crystalline Si wafer was also fabricated to obtain the gate capacitance density of Pr_2O_3 gate dielectric. Fig. 3.3 shows typical capacitance-voltage (C-V) characteristics of the MOS capacitor at 1 MHz. The MOS capacitor has the same gate-dielectric thickness as the proposed TFT device has. An accumulation gate capacitance density (C_{acc}) at applied gate voltage of $V_G = -4$ V is 463 nF/cm^2. Therefore, the equivalent-oxide thickness (EOT) of the Pr_2O_3 gate dielectric

extracted from the accumulation gate capacitance density is 7.4 nm. The effective dielectric constant of the Pr_2O_3 gate dielectric was extracted by using a series capacitance of Pr_2O_3 gate dielectric and SiO_2-like interfacial layer according to the series capacitor model [3.17], expressed as Eq. (3.1).

$$EOT = T_{interfacial\ layer} + (\kappa_{interfacial\ layer}/\kappa_{Pr_2O_3}) \times T_{Pr_2O_3} \quad \text{.....Eq. (3.1)}$$

where κ_{Pr2O3} and $\kappa_{interfacial\ layer}$ are the dielectric constants of Pr_2O_3 gate dielectric and SiO_2-like interfacial layer, respectively, and T_{Pr2O3} and $T_{interfacial\ layer}$ are the thicknesses of these films. Here, the T_{Pr2O3} and $T_{interfacial\ layer}$ are assumed to be 40 nm and 1.5 nm, respectively, and the $\kappa_{interfacial\ layer}$ is assumed to be 3.9 to simplify the calculation. Based on the relation in Eq. (3.1), the effective dielectric constant of the Pr_2O_3 gate dielectric (κ_{Pr2O3}) is extracted to be 26. The inset in Fig. 3.3 shows the hysteresis characteristics of the Pr_2O_3 gate dielectric upon sweeping from accumulation to inversion (–4 V to 4 V) and then sweeping back (4 V to –4 V). The Pr_2O_3 gate dielectric demonstrates a negligible hysteresis characteristic of 7.2 mV. Therefore, such high gate capacitance density, and low charge-trapping phenomenon suggest that the Pr_2O_3 film is a promising high-κ gate-dielectric candidate for replacing conventional SiO_2 film in the poly-Si TFTs.

3.3.1.2 Evidence of Fluorine Incorporation

Fourier transform infrared spectroscopy (FTIR) and secondary ion mass spectroscopy (SIMS) analyses were utilized to verify the fluorine existing in the poly-Si film. The FTIR spectra of the fluorine-implanted and control poly-Si films after SPC process are shown in Fig. 3.4(a). The main peak of functional group Si-F bonds is clearly observed at around 930 cm^{-1} in the fluorine-implanted poly-Si film [3.18]. The stronger peak of Si-O bond is derived from the underlying thermal SiO_2 substrate. Therefore, Si-F bonds are formed in the poly-Si film by utilizing fluorine ion implantation. Moreover, Fig. 3.4(b) shows the SIMS profiles of

fluorine and praseodymium atoms for the fluorine-implanted poly-Si film. It was apparently observed that considerable fluorine ions were detected in the poly-Si film and, in particular, two obvious fluorine peaks were piled up at the Pr_2O_3 gate dielectric/poly-Si channel and the poly-Si channel/underlying thermal SiO_2 interfaces. Note that the incorporated and piled-up fluorine ions in the poly-Si film and at the Pr_2O_3/poly-Si interface would bring about an effective passivation of deep trap states and interface states, resulting in fewer Si dangling bonds and Si strain bonds.

3.3.1.3 Device Characteristics

Fig. 3.5 shows the transfer characteristics (I_{DS}-V_{GS}) of the poly-Si Pr_2O_3 TFTs with and without fluorine ion implantation. The measurements are performed at two different drain voltages of V_{DS} = 0.1 V and 1 V. The drawn channel width (W) and channel length (L) are 10 μm and 5 μm, respectively. The parameters of the devices, including threshold voltage (V_{th}), field-effect mobility (μ_{FE}), and subthreshold swing (S.S.) are extracted at V_{DS} = 0.1 V, whereas the maximum off-state leakage currents ($I_{off, max}$) and maximum on-state currents (I_{on}) are defined at V_{DS} = 1 V. The on/off current ratio (I_{on}/I_{off}) is defined as the ratio of the maximum on-state currents to the minimum off-state leakage currents at V_{DS}= 1 V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of I_{DS} = (W/L)×100 nA. The detailed device parameters of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs are summarized in Table 3.1.

Accordingly, the electrical performances of the fluorine-implanted poly-Si Pr_2O_3 TFT are remarkably improved compared to those of the control poly-Si Pr_2O_3 TFTs. With the fluorine ion implantation, the poly-Si Pr_2O_3 TFTs exhibit significant performance improvements in terms of drastically decreased threshold voltage from 1.57 to 0.65 V and reduced subthreshold swing from 320 to 216 mV/dec. It is known that the deep trap states, associated with the Si dangling bonds, accompanied with many energy states near the middle

of Si bandgap, would strongly affect the threshold voltage and subthreshold swing [3.13]. Therefore, introducing fluorine ions into the poly-Si film by fluorine ion implantation can effectively terminate the deep trap states at the grain boundaries. In addition, the maximum on-state currents and on/off current ratio of the fluorine-implanted poly-Si Pr_2O_3 TFTs are also superior to those of the control poly-Si Pr_2O_3 TFTs. The corresponding on/off current ratios for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs are 1.6×10^7 and 3.4×10^6, respectively. The on/off current ratio of the fluorine-implanted poly-Si Pr_2O_3 TFTs is approximately five times larger than that of the control poly-Si Pr_2O_3 TFTs.

Fig. 3.5 also shows the relation between the field-effect mobility and gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. The field-effect mobility is extracted from the transconductance value at $V_{DS} = 0.1$ V. As can be seen, the maximum field-effect mobility of the fluorine-implanted poly-Si Pr_2O_3 TFTs is higher than that of the control poly-Si Pr_2O_3 TFTs. With the fluorine ion implantation, the poly-Si Pr_2O_3 TFT shows approximately 105 % enhancement in the maximum field-effect mobility. Note that the tail states near the Si bandedge resulted from the strain bonds in the poly-Si and at the Pr_2O_3/poly-Si interface would greatly affect the field-effect mobility [3.13]. This feature implies that the fluorine ion implantation treatment can not only passivate the Si dangling bonds but also relieve the Si strain bonds. The proposed poly-Si TFTs crystallized by SPC technique can demonstrate good electrical performances even without additional hydrogen plasma treatments or other advanced phase crystallization techniques with narrow process window [3.19], [3.20].

However, incorporating high-κ gate dielectric into poly-Si TFT would contribute to a higher electric field at the gate-to-drain overlap area, exhibiting higher field-enhanced emission rates via the grain-boundary trap states. Thus, the control poly-Si Pr_2O_3 TFTs would suffer from more undesirable gate-induced drain leakage (GIDL) currents, especially under continuously decreasing gate voltage. The GIDL current of the fluorine-implanted

poly-Si Pr_2O_3 TFTs (2.6×10^{-10}) is much lower than that of the control poly-Si Pr_2O_3 TFTs (1.2×10^{-8}), under applied voltages of V_{GS} = –2 V and V_{DS} = 1 V. This observation suggests that the incorporation of fluorine ions into the poly-Si film can effectively passivate the trap states, thereby resulting in lower GIDL currents under a high electric field.

3.3.1.4 Trap-State Density

In order to verify the effect of fluorine passivation, the grain-boundary trap-state density (N_{trap}) was calculated from the square root of the slope of $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ plot according to the grain-boundary trapping model proposed by Proano et al. [3.21]. Fig. 3.6 exhibits the $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ and the extracted grain-boundary trap-state densities at V_{DS} = 0.1 V and high gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. It can be found that the fluorine-implanted poly-Si Pr_2O_3 TFT shows a N_{trap} of 4.58×10^{12} cm^{-2}, whereas the control poly-Si Pr_2O_3 TFT possesses a N_{trap} of 1.44×10^{13} cm^{-2}. This result implies that the fluorine ions can effectively passivate the present grain-boundary trap states in the poly-Si film, thereby exhibiting improved device performances. Combined with the SIMS profiles, we believe that the passivation effect is due to the piled-up and accumulated fluorine ions at the Pr_2O_3/poly-Si interface and in the poly-Si film.

3.3.1.5 Output Characteristics and Activation Energy

Fig. 3.7 shows the output characteristics (I_{DS}-V_{DS}) of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. As can be seen, with the fluorine ion implantation, the poly-Si Pr_2O_3 TFT exhibits a significant enhancement in the on-state driving current under common gate drive of $V_{GS}-V_{TH}$ = 2, 3, and 4 V. The fluorine passivation of trap states would result in a higher field-effect mobility, thus exhibiting an obvious improvement on the driving capability.

Fig. 3.8 illustrates the activation energy (E_A) of drain current as a function of gate voltage at V_{DS} = 1 V for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. E_A was extracted by the measurements of I_{DS}-V_{GS} characteristics at various temperatures ranging from 25 to 150 ^oC [3.22]. E_A represents the carrier transport barrier across the grain boundaries in the poly-Si film. In the turned-off state, the value of E_A reflects the required energy for field-enhanced emission of carriers via the trap states, whereas in the turned-on state, the value of E_A reflects the carrier transport barrier height caused by the trap states within the poly-Si channel. The fluorine-implanted poly-Si Pr_2O_3 TFT exhibits a higher E_A in the turned-off state, but a lower E_A in the turned-on state, as compared to the control poly-Si Pr_2O_3 TFT. It should be noted that the trap states can be effectively terminated by the incorporation of fluorine ions into the poly-Si film. Moreover, a steeper curve can be found in the subthreshold region for the fluorine-implanted poly-Si Pr_2O_3 TFTs, thereby demonstrating well terminated interface states by the fluorine ion implantation. This implication is well-consistent with the above extracted data of trap-state density.

3.3.1.6 Short-Channel Effect

To investigate the short-channel effect of poly-Si Pr_2O_3 TFTs with and without fluorine ion implantation, the average and statistical distributions of threshold voltage as a function of channel length with a fixed channel width of 10 μm are shown in Fig. 3.9. The number of sampling devices characterized under each condition is 20. The vertical bars in Fig. 3.9 indicate the minimum and maximum values of the devices characteristics and the circle as well as triangular symbol present the average values. The threshold voltage of poly-Si TFTs with traditional SiO_2 gate dielectrics is decreased with continuously scaling down channel length, called the threshold-voltage rolloff effect, dominated by the reduction of grain-boundary trap states [3.23]. In contrast, the poly-Si Pr_2O_3 TFTs with a high gate capacitance density can rapidly fill up the grain-boundary trap states and then maintain superior

turned-on characteristics, demonstrating a better threshold-voltage rolloff property. In addition, as the channel length scales down, fluctuations of threshold voltage by the variation of the number of grain boundaries in the poly-Si channel become more significant in the control poly-Si Pr_2O_3 TFTs. This is reasonable and is related to the inherent grain structure contained in the poly-Si channels [3.24]. Therefore, using the fluorine ions to passivae the trap states can not only decrease the average threshold voltage but also minimize the fluctuation of threshold voltage.

3.3.1.7 Device Reliability

Additionally, hot-carrier stress was performed to investigate the electrical reliability of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. The TFT devices with a dimension of W/L = 10 μm/10 μm were bias stressed at V_{DS} = 4 V and V_{GS} = 4 V for 1000s to examine the hot-carrier stress immunity. The threshold-voltage shift (ΔV_{th}) and on-current variation (δI_{on}) over stress time for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs are shown in Figs. 3.10 and 3.11, respectively. The ΔV_{th} and δI_{on} were defined as $V_{th,\ stressed} - V_{th,\ initial}$ and $(I_{on,\ stressed} - I_{on,\ initial})/I_{on,\ initial} \times 100$ %, respectively, where the index of initial and stressed represents the measured values before and after stresses. Hot-carrier multiplication near the drain side causes the degradation of threshold voltage and on current. The poly-Si Pr_2O_3 TFT with fluorine ion implantation shows less degradation on threshold voltage and on current. Notably, the threshold-voltage shift and on-current variation of the fluorine-implanted poly-Si Pr_2O_3 TFT after 1000 s stress are found to be 0.7 V and 26 %, which are superior to those of the control poly-Si Pr_2O_3 TFT (1.5 V and 72 %, respectively). It has been reported that the degradation of electrical characteristics induced by hot-carrier stress can be attributed to the following two reasons: the generation of Pr_2O_3/poly-Si interface states and the formation of Si dangling bonds from the breaking of weak Si-Si or Si-H bonds in the poly-Si channel [3.14]. Therefore, introducing fluorine ions into the poly-Si film by fluorine

ion implantation would bring about the passivation of trap states and the formation of strong Si-F bonds in place of weak Si-Si and Si-H bonds, thereby leading to great improvements in the electrical reliability.

3.3.2 CF_4 Plasma Treatment Effects on Pr_2O_3 TFTs

3.3.2.1 Pr_2O_3 Gate Dielectric Integrity

Fig. 3.12 shows the XTEM image of the integrated Pr_2O_3 gate dielectric on the CF_4 plasma-treated poly-Si TFTs. The physical thicknesses of the Pr_2O_3 gate dielectric and the poly-Si channel are around 33.6 nm and 97 nm, respectively. The higher resolution XTEM image around the Pr_2O_3/poly-Si interface displayed in the inset of Fig. 3.12 exhibits an about 1.5-nm SiO_2-like interfacial layer. Fig. 3.13 shows typical C-V characteristics of the MOS capacitor with Pr_2O_3 gate dielectric on single-crystalline Si wafer at 1 MHz. The MOS capacitor has the same gate-dielectric thickness as the propsoed TFT device has. An accumulation gate capacitance density (C_{acc}) at applied gate voltage of $V_G = -4$ V is 532 nF/cm^2. Therefore, the equivalent-oxide thickness (EOT) and the dielectric constant of the Pr_2O_3 gate dielectric are extracted to be 6.5 nm and 26.2, respectively. The 6.5-nm EOT is the thinnest thickness reported on TFT fields so far. The inset in Fig. 3.13 shows a negligible hysteresis characteristic of 5.7 mV upon sweeping from accumulation to inversion (–4 V to 4 V) and then sweeping back (4 V to –4 V), indicating it is a promising gate-dielectric candidate for poly-Si TFTs.

3.3.2.2 Device Characteristics

Figs. 3.14 and 3.15 illustrate the transfer characteristics (I_{DS}-V_{GS}) of the poly-Si Pr_2O_3 TFTs with various rf powers of 0-W (control sample), 10-W, and 20-W CF_4 plasma treatments, which were measured at $V_{DS} = 0.1$ V and 1 V, respectively. The drawn channel

width (W) and channel length (L) are 10 μm and 10 μm, respectively. The device parameters, including threshold voltage (V_{th}), field-effect mobility (μ_{FE}), and subthreshold swing (S.S.) are extracted at V_{DS} = 0.1 V. The extracted key device parameters of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments are summarized in Table 3.2. The poly-Si Pr_2O_3 TFT with 10-W CF_4 plasma treatment exhibits better subthreshold and on-state characteristics compared to that without (0-W) and with 20-W CF_4 plasma treatments. The threshold voltages for the poly-Si Pr_2O_3 TFTs with 0-W, 10-W, and 20-W CF_4 plasma treatments are 1.58, 1.27, and 1.93 V, respectively. Also, the subthreshold swings for the poly-Si Pr_2O_3 TFTs with 0-W, 10-W, and 20-W CF_4 plasma treatments are 276, 232, and 318 mV/dec., respectively. This tendency indicates that introducing fluorine atoms into the poly-Si layer by an appropriate rf power of 10-W CF_4 plasma treatment can effectively passivate the grain-boundary trap states to greatly improve the on-state characteristics.

Although the fluorine passivation of trap states is found to greatly improve the subthreshold and on-state characteristics, the minimum off-state leakage current of the poly-Si Pr_2O_3 TFTs with CF_4 plasma treatments is not suppressed sufficiently. Similar data have been previously reported in the poly-Si TFTs with fluorine ion implantation technique [3.15]. Poly-Si TFTs with high-κ gate dielectrics show higher off-state gate-induced drain leakage (GIDL) currents, resulted from the higher electric field near the gate-to-drain overlap area, compared to those with SiO_2 gate dielectrics [3.12]. Notably, as the gate voltage continuously decreases to V_{GS} = −3 V, the maximum off-state GIDL current ($I_{GIDL, max}$) of the poly-Si Pr_2O_3 TFT with 10-W CF_4 plasma treatment (0.53 nA) is more than one order in magnitude lower than that without CF_4 plasma treatment (control sample) (8.75 nA). In addition, the maximum on-state current and on/off current ratio of the 10-W CF_4 plasma-treated poly-Si Pr_2O_3 TFT are also better than those of the 0-W and 20-W samples. The on/off current ratio of the 10-W CF_4 plasma-treated poly-Si Pr_2O_3 TFT (9.6×10^6) is approximately 2.5 times larger than that of the 0-W (control) sample (3.9×10^6). Therefore,

using CF_4 plasma treatment can introduce the fluorine atoms into the poly-Si film to effectively passivate the grain-boundary trap states, leading to better off-state characteristics.

Additionally, the field-effect mobility versus gate voltage for the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments is also shown in Fig. 3.14. The filed-effect mobility is extracted from the transconductance value measured at V_{DS} = 0.1 V. The maximum field-effect mobility of the poly-Si Pr_2O_3 TFTs with 0-W, 10-W, and 20-W CF_4 plasma treatments are 28.33, 43.48 and 21.28 cm^2/V-s, respectively. Note that the maximum field-effect mobility is improved by 10-W CF_4 plasma treatment but degraded by 20-W CF_4 plasma treatment. This result also confirms that the incorporated fluorine atoms by an appropriate rf power of 10-W CF_4 plasma treatment provide fluorine passivation effects on Si dangling bonds and Si strain bonds in the poly-Si channel and at the Pr_2O_3/poly-Si interface.

3.3.2.3 Evidence of Fluorine Incorporation

The evidence of the fluorine incorporation into the poly-Si film can be firmly demonstrated with the SIMS analysis. Fig. 3.16 shows the SIMS depth profiles of the fluorine and praseodymium atoms for the poly-Si films with 0-W, 10-W, and 20-W CF_4 plasma treatments. It was clearly observed that considerable fluorine atoms were detected in the poly-Si and, in particular, an obvious fluorine peak was located at the Pr_2O_3 gate dielectric/poly-Si channel interface. The SIMS analysis shows an increased concentration of fluorine atoms at the Pr_2O_3/poly-Si interface with increasing the rf power. Note that the piled-up fluorine atoms at the Pr_2O_3/poly-Si interface by using CF_4 plasma treatment provide an effective termination of grain-boundary trap states and interface trap states.

3.3.2.4 Grain-Boundary and Interface Trap-State Density

To verify the fluorine termination of grain-boundary trap states by using CF_4 plasma

treatments, the effective grain-boundary trap-state density (N_{trap}) was evaluated according to the grain-boundary trapping model [3.21]. Fig. 3.17 exhibits the $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves in the strong inversion at V_{DS} = 0.1 V for the poly-Si Pr_2O_3 TFTs with 0-W, 10-W, and 20-W CF_4 plasma treatments. The effective grain-boundary trap-state density was calculated from the square root of the slope of $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$. For the cases of the applied rf power of 0 W, 10 W, and 20 W, the effective grain-boundary trap-state densities are found to be 1.35×10^{13}, 9.44×10^{12}, and 1.47×10^{13} cm^{-2}, respectively. It is observed that there is an optimal rf powers of 10-W CF_4 plasma treatment for the reduction of grain-boundary trap states. Although the 20-W sample exhibits higher concentration of fluorine atoms than the 10-W sample, as shown in the SIMS depth profiles, the grain-boundary trap states are slightly increased with increasing the rf power to 20 W.

To further investigate the fluorine passivation of interface trap states near the Pr_2O_3 gate dielectric/poly-Si channel interface, the effective interface trap-state densities (N_{it}) were calculated from the subthreshold swing (S.S.) without considering the depletion capacitance, expressed as Eq. (3.2) [3.25].

$$N_{it} = \left[\left(\frac{S.S.}{\ln 10}\right)\left(\frac{q}{kT}\right)\right]\left(\frac{C_{acc}}{q}\right) \quad \text{.....Eq. (3.2)}$$

where C_{acc} is the gate capacitance density of Pr_2O_3 gate dielectric. The N_{it} values for the 0-W, 10-W, and 20-W CF_4 plasma-treated poly-Si Pr_2O_3 TFTs are 1.49×10^{13}, 1.25×10^{13}, and 1.71×10^{13} cm^{-2}, respectively. This result reveals that the interface trap states near the Pr_2O_3/poly-Si interface could be greatly passivated by using an appropriate rf power of 10-W CF_4 plasma treatment. Combined with the SIMS profiles, we believe that the passivation effect is due to the accumulated fluorine atoms at the Pr_2O_3/poly-Si interface.

3.3.2.5 Plasma-Induced Device Degradation

However, there is a non-ideal result that the 20-W CF_4 plasma treatment on the poly-Si

film shows detrimental effects on the electrical performances of the fabricated TFT device. As is well known, CF_4 gas dissociated into reactive fluorine radicals by rf gas discharge is a commonly used etching species, thereby etching the exposed poly-Si film [3.26]. The reason for the degradation of electrical properties could be attributed to the plasma-etching induced electrical damages to the poly-Si film. The effect of degradation on the poly-Si film completely dominates the effect of fluorine passivation on the trap states in the 20-W CF_4 plasma-treated sample, resulting in degraded electrical performances. Fortunately, the variations of the thicknesses of the poly-Si films before and after CF_4 plasma treatments measured by ellipsometer are negligible, and thus the thinning effect of the poly-Si films by CF_4 plasma treatment is excluded. According to previous reports, the surface morphology of the poly-Si channel film has been reported to affect the electrical characteristics and reliability of TFT devices [3.27]. To investigate the degradation on the on-state characteristics of the 20-W CF_4 plasma-treated sample, the surface morphology of poly-Si films was analyzed by atomic force microscopy (AFM). Fig. 3.18 (a)-(c) shows the AFM images of the poly-Si films with 0-W, 10-W, and 20-W CF_4 plasma treatments, respectively. The average root-mean-square (RMS) values of surface roughness for the poly-Si films with 0-W, 10-W, and 20-W CF_4 plasma treatments are 0.25 nm, 0.31 nm, and 0.47 nm, respectively. Clearly, the poly-Si film with 20-W CF_4 plasma treatment shows the roughest surface morphology, demonstrating severest plasma-etching induced damage to the integrity of the poly-Si channel film. The performance degradation on the 20-W CF_4 plasma-treated sample might be ascribed to that the effect of increasing surface roughness as well as serious plasma damage completely dominates the effect of fluorine passivation.

3.3.2.6 Activation Energy

Fig. 3.19 shows the activation energy (E_A) of drain current as a function of gate voltage at V_{DS} = 0.1 V for the poly-Si Pr_2O_3 TFTs without (0-W), and with 10-W and 20-W CF_4

plasma treatments. The extracted E_A of the optimal rf power of 10-W CF_4 plasma-treated poly-Si Pr_2O_3 TFT is higher in the turn-off state and lower in the turn-on state, as compared with the 0-W (control) and 20-W samples. Introducing fluorine atoms into the poly-Si film by 10-W CF_4 plasma treatment can effectively passivate the trap states, thereby reducing the trap-assisted leakage currents in the turn-off state and improving the carrier transport efficiency in the turn-on state. Besides, in the subthreshold region, a steeper slope is obtained in the 10-W CF_4 plasma-treated sample. This verifies that the interface trap states in the 10-W CF_4 plasma-treated sample are fewer than those in the 0-W and 20-W CF_4 plasma-treated samples. The implication is consistent with the above extracted data of trap-state density.

3.3.2.7 Short-Channel Effect

To investigate the short-channel effect of the poly-Si Pr_2O_3 TFTs with and without 10-W CF_4 plasma treatment, the average and statistical distributions of threshold voltage as a function of channel length with a fixed channel width of 10 μm are shown in Fig. 3.20. The number of sampling devices characterized under each condition is 20. The vertical bars in the figure indicate the minimum and maximum values of threshold voltage and the circle as well as square symbol presents the average values. The threshold voltage of the poly-Si TFTs with conventional SiO_2 gate dielectrics is decreased with continuously scaling down channel length. In contrast, the poly-Si TFTs with Pr_2O_3 gate dielectrics possess high gate capacitance density to rapidly fill up the grain-boundary trap states and then maintain superior turned-on characteristics, demonstrating superior threshold-voltage rolloff properties. In addition, as the channel length scales down, fluctuations of threshold voltage by the variation of the number of grain boundaries in the poly-Si channel become severer for the control poly-Si Pr_2O_3 TFT. This is reasonable and is related to the inherent grain structure contained in the poly-Si channels. The trap states at the grain boundaries can be greatly

terminated by incorporating the fluorine atoms into the poly-Si film, leading to smaller fluctuations of threshold voltage. Therefore, integrating Pr_2O_3 gate dielectrics and fluorine-plasma passivation technique into the poly-Si TFTs can not only suppress the threshold-voltage rolloff properties but also reduce the fluctuations of threshold voltage.

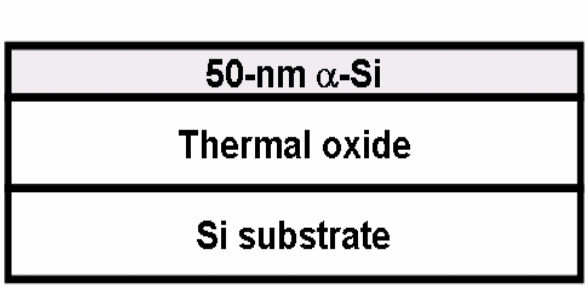
3.3.2.8 Device Reliability

Finally, the influence of electrical stress on the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments is examined. Figs. 3.21 and 3.22 show the threshold-voltage shift and on-current variation as a function of hot-carrier stress time for the poly-Si Pr_2O_3 TFTs with 0-W, 10-W, and 20-W CF_4 plasma treatments. The TFT devices were biased at V_{GS} = 6 V and V_{DS} = 6 V. The CF_4 plasma-treated samples show smaller threshold-voltage shift and on-current variation than the control sample. Notably, the threshold-voltage shift and on-current variation of the poly-Si Pr_2O_3 TFT with 10-W CF_4 plasma treatment are found to be 1.84 V and 16.06 % after 1000 s stress, which are superior to those without CF_4 plasma treatment (4.72 V and 38.34 %, respectively). Thus, introducing fluorine atoms into the poly-Si film by CF_4 plasma treatment would result in the passivation of trap states and the formation of strong Si-F bonds in place of weak Si-H bonds, exhibiting superior endurance against hot-carrier stress.

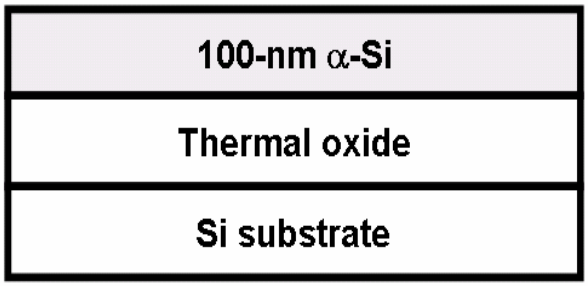
3.4 Summary

We have incorporated two kinds of fluorination techniques including fluorine ion implantation and CF_4 plasma treatments into the poly-Si Pr_2O_3 TFTs. Pr_2O_3 gate dielectric can achieve thin equivalent-oxide thickness and high gate capacitance density. Utilizing these fluorination techniques, fluorine atoms can be introduced into the poly-Si films and the Pr_2O_3 gate dielectric/poly-Si channel interface to passivate the grain-boundary trap states.

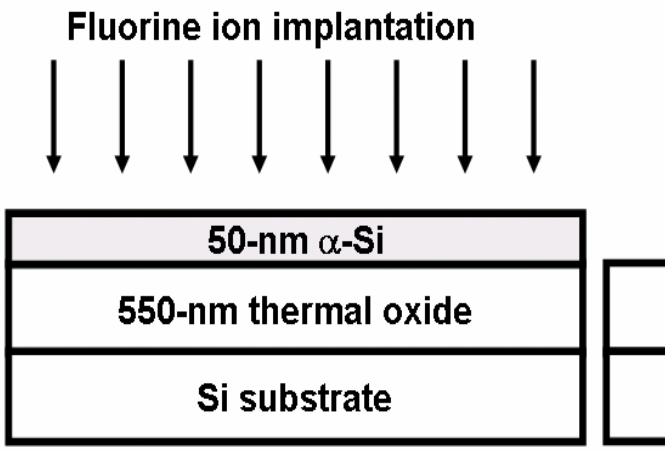
Hence, the electrical performances and threshold-voltage rolloff properties of the poly-Si Pr_2O_3 TFTs can be significantly improved. Besides, these fluorination techniques also enhance the immunity against hot-carrier stress, due to the formation of strong Si-F bonds. It is concluded that the integration of these effective fluorination techniques and Pr_2O_3 gate dielectric into the poly-Si TFTs could be available for achieving AMLCD applications.



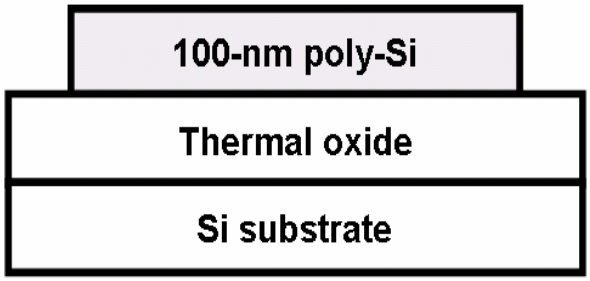
(a-1) Thermal oxidation, and 50-nm α-Si deposition.



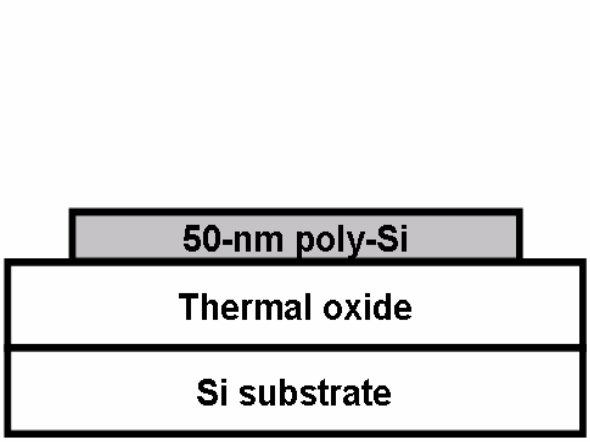
(a-2) Thermal oxidation, and 100-nm α-Si deposition.



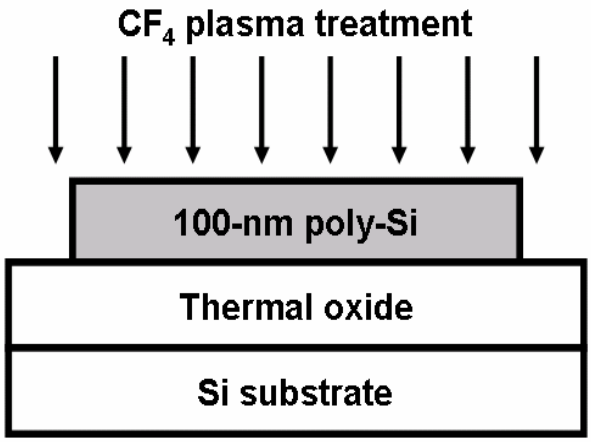
(b-1) Fluorine ion implants into α-Si film.



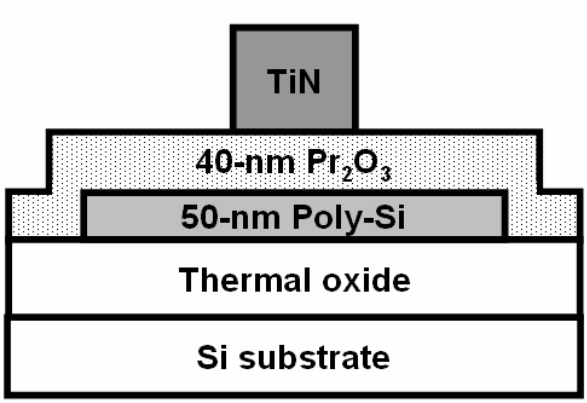
(b-2) Solid-phase crystallization of α-Si, and patterning of active region.



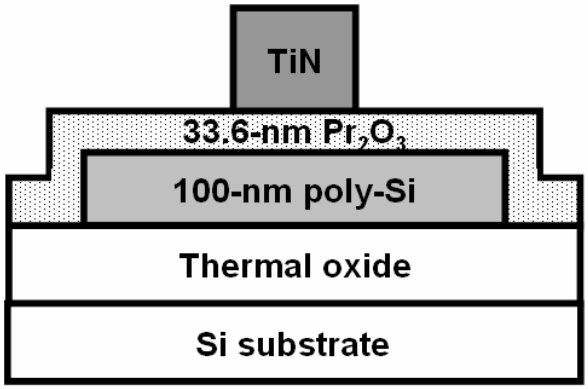
(c-1) Solid-phase crystallization of α-Si, and patterning of active region.



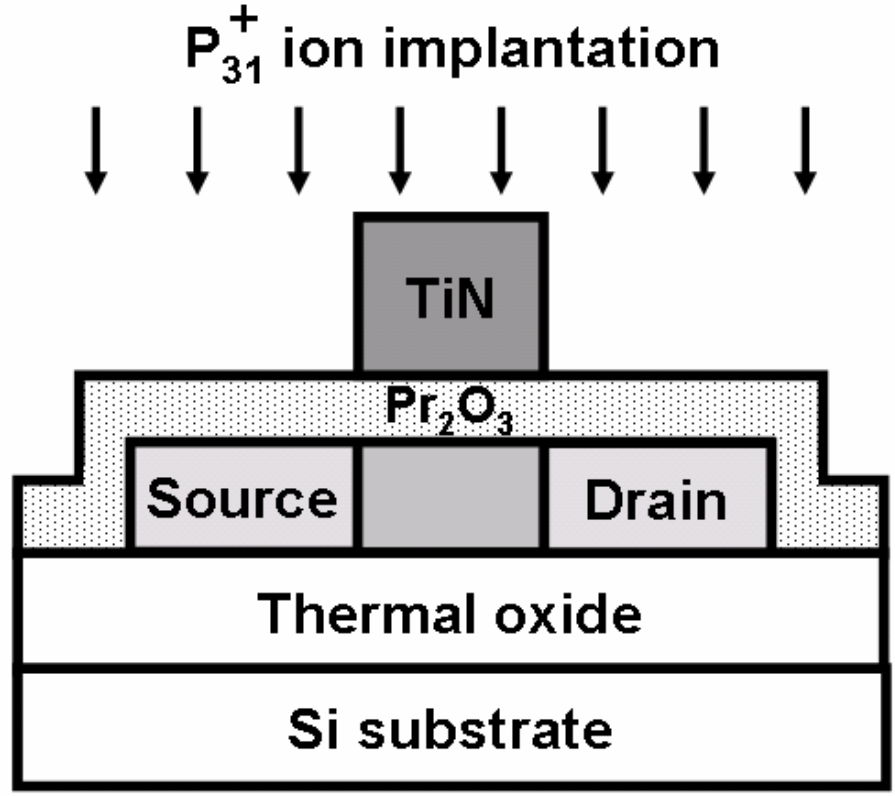
(c-2) Perform CF_4 plasma treatment on poly-Si film.



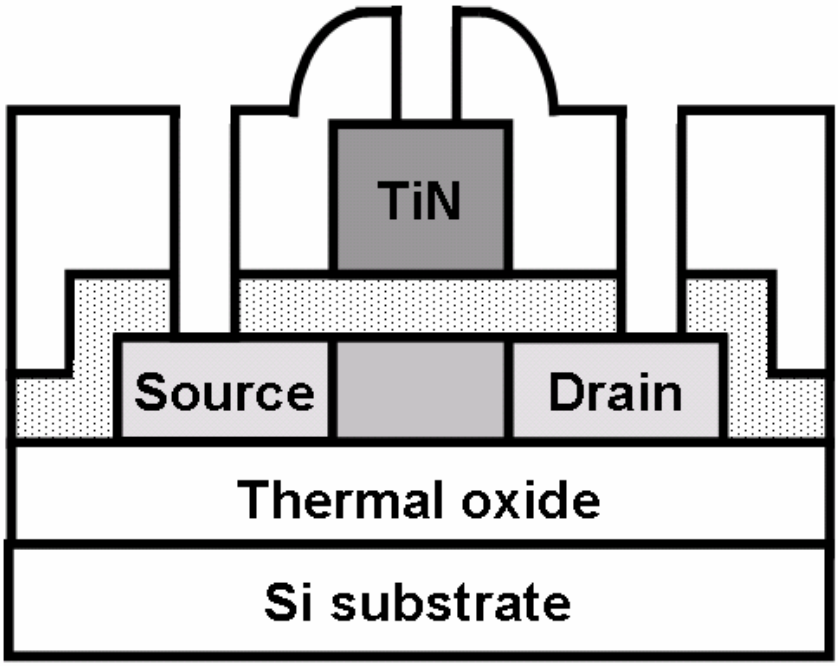
(d-1) 40-nm Pr_2O_3 deposition, densification, and TiN gate formation.



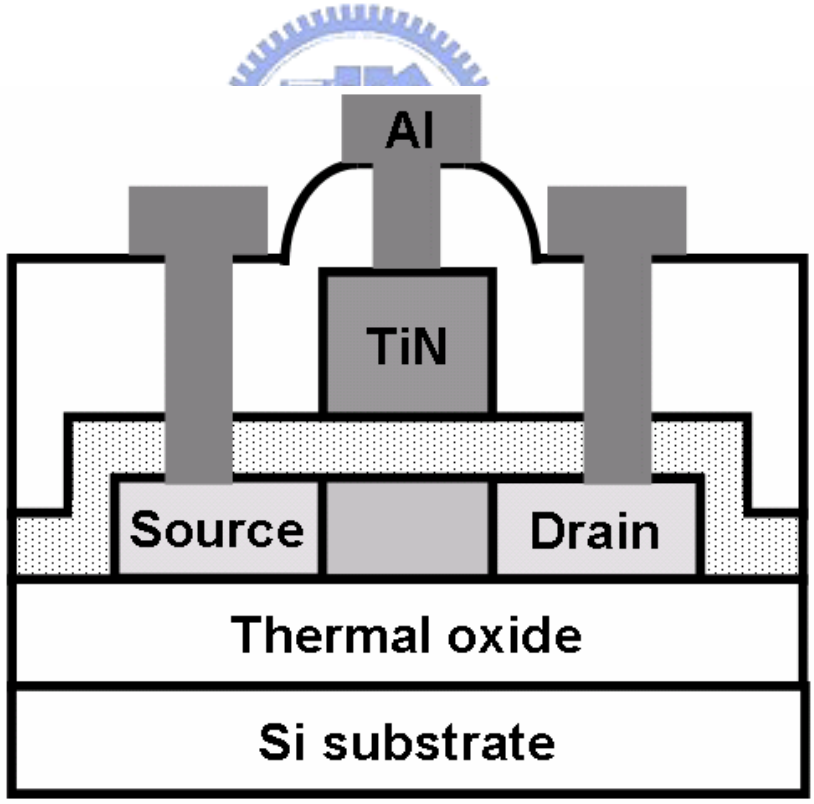
(d-2) 33.6-nm Pr_2O_3 deposition, densification, and TiN gate formation.



(e) Self-aligned phosphorus ion implantation, and dopant activation.



(f) Passivation oxide deposition, and patterning of contact hole.



(g) Al electrode deposition and patterning.

Fig. 3.1 Schematic key fabrication steps for the proposed Pr_2O_3 gate dielectric TFTs on the fluorine-implanted and the CF_4 plasma-treated poly-Si films.

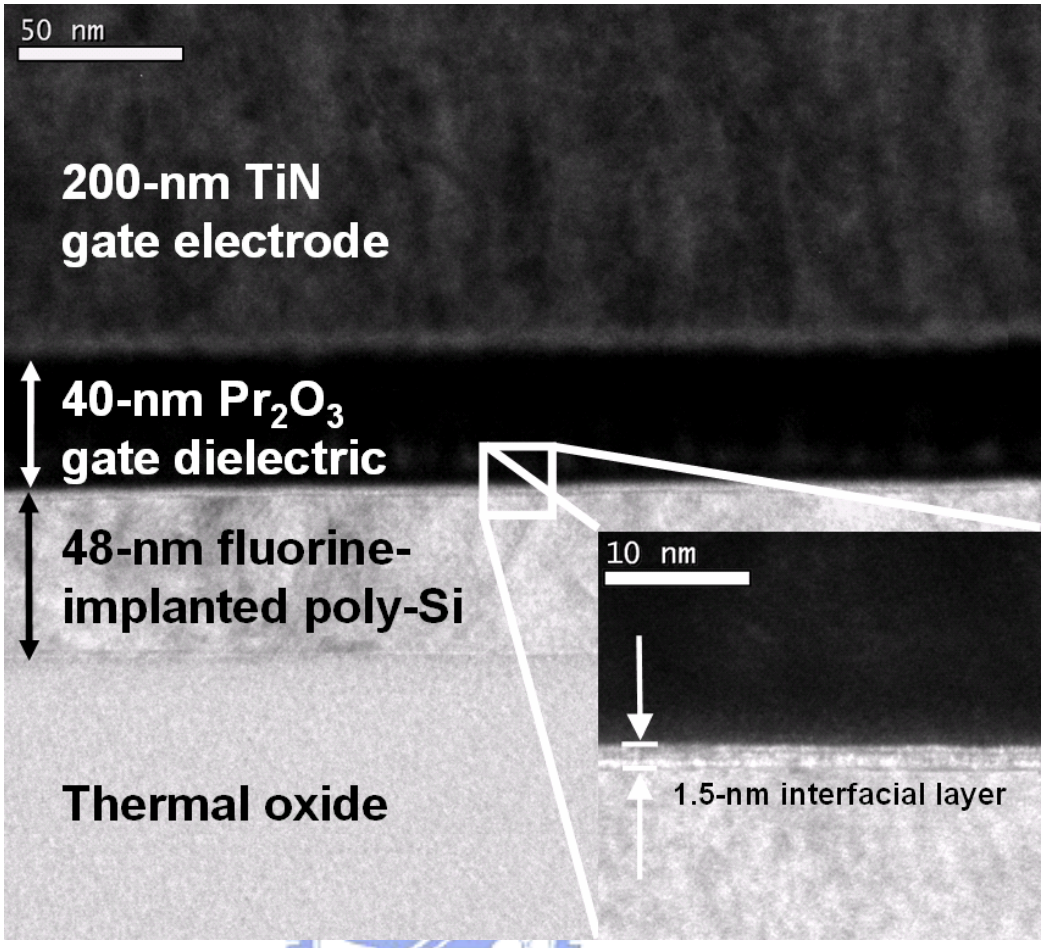


Fig. 3.2 Cross-sectional TEM image of the proposed Pr_2O_3 gate dielectric TFTs on the fluorine-implanted poly-Si film.

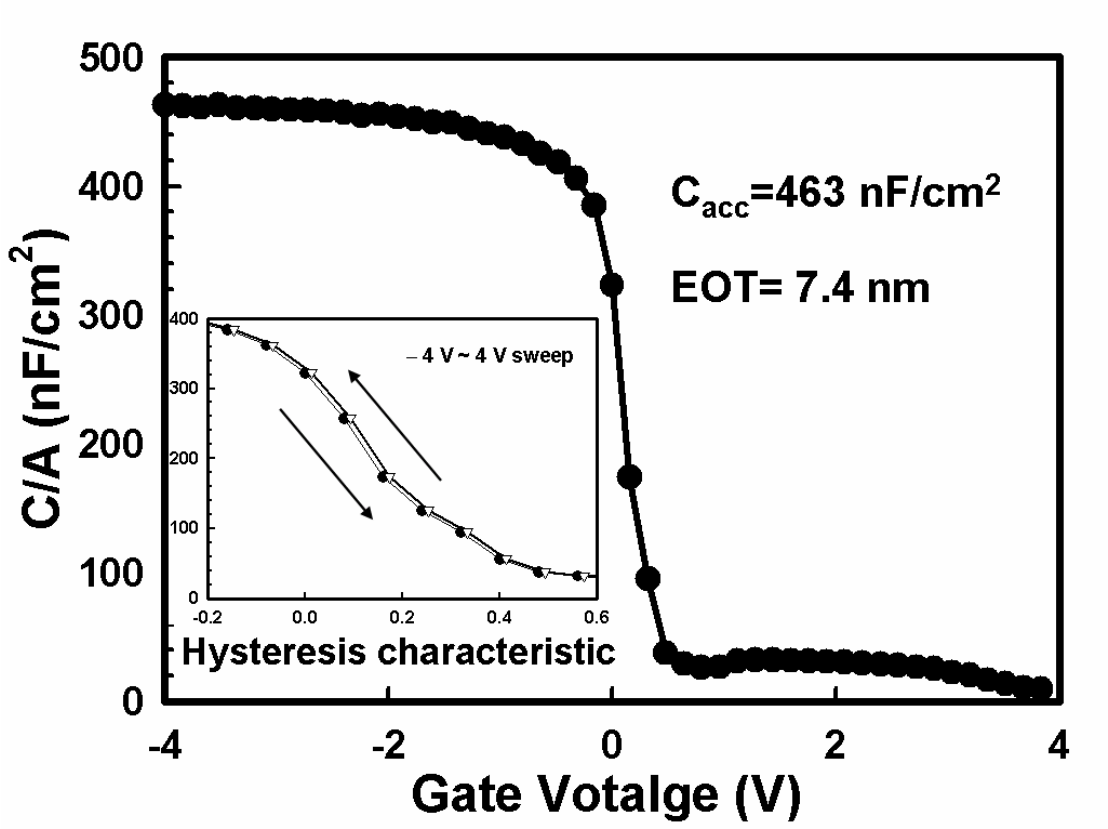
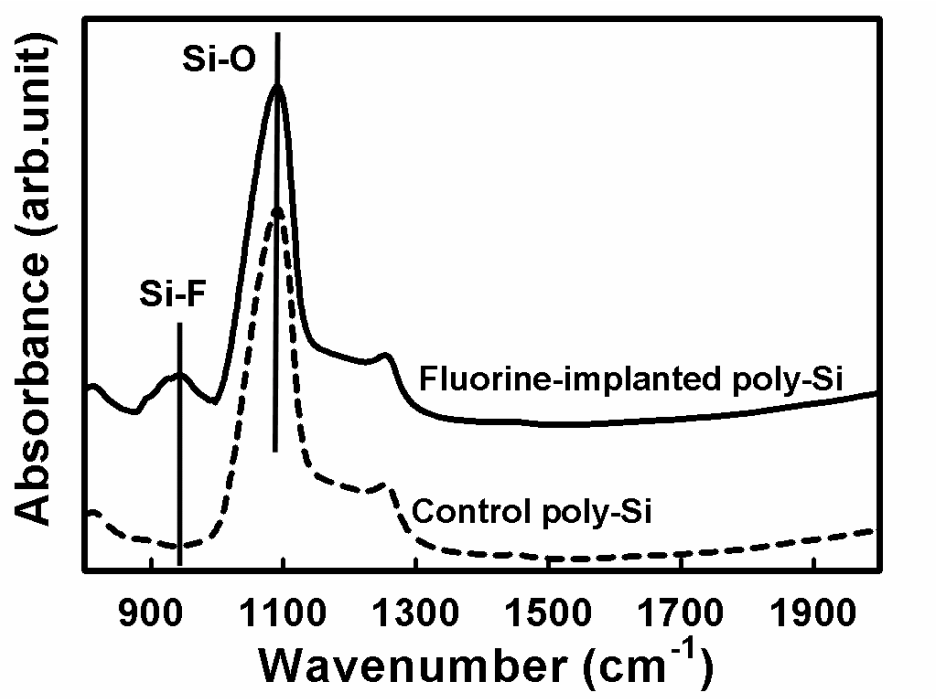
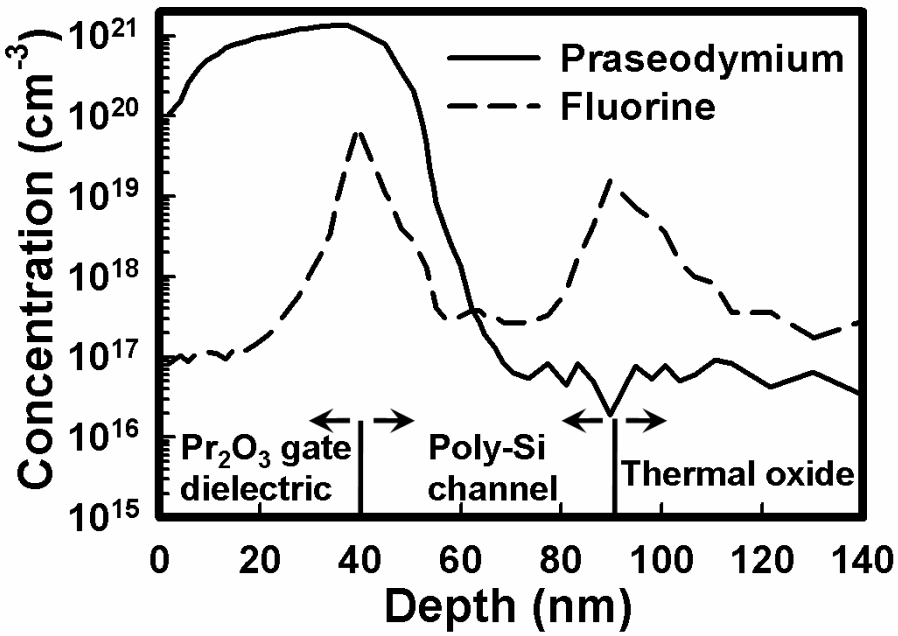


Fig. 3.3 Typical C-V characteristic of the Pr_2O_3 gate dielectric. The inset shows the hysteresis characteristic of the Pr_2O_3 gate dielectric.



(a) FTIR spectra of the poly-Si film with and without fluorine ion implantation.



(b) SIMS depth profiles of the fluorine-implanted poly-Si TFTs with Pr_2O_3 gate dielectric.

Fig. 3.4 FTIR spectra of the poly-Si films with and without fluorine ion implantation and SIMS depth profiles of the fluorine-implanted poly-Si Pr_2O_3 TFTs.

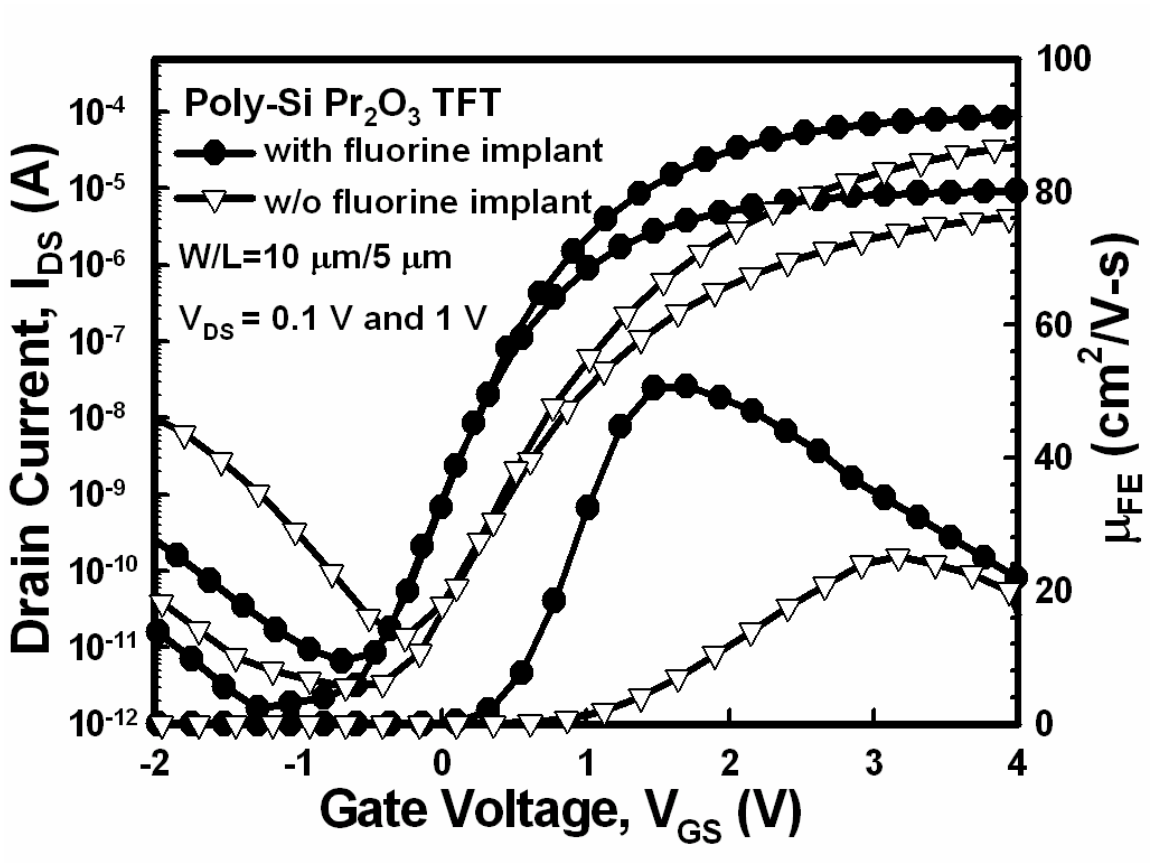


Fig. 3.5 Transfer characteristics of the poly-Si Pr_2O_3 TFTs with and without fluorine ion implantation.

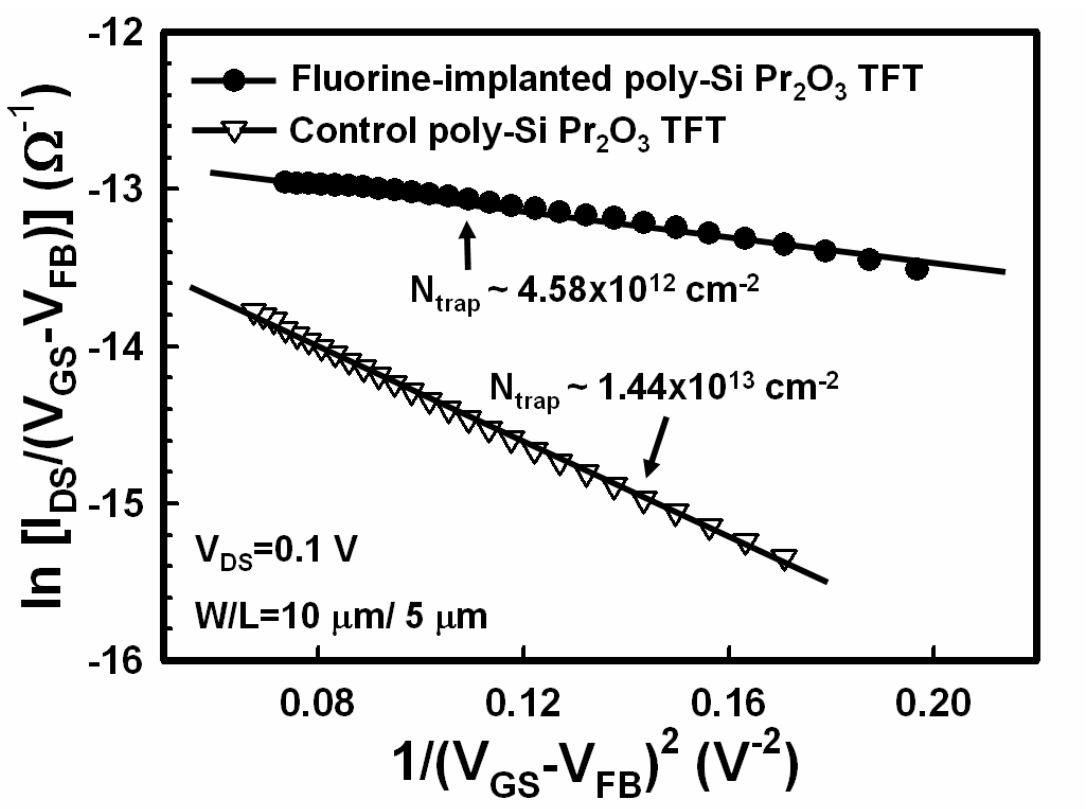


Fig. 3.6 Polt of $\ln[I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ at V_{DS} = 0.1 V and high gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

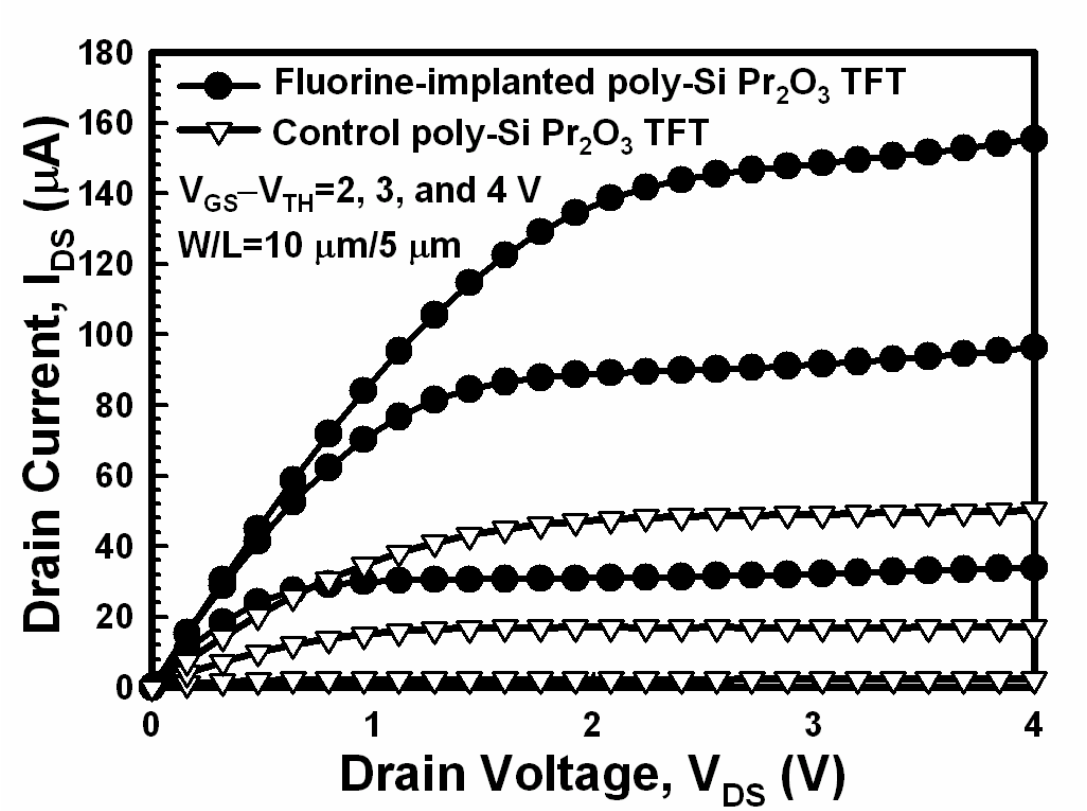


Fig. 3.7 Output characteristics of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

Table 3.1. Electrical characteristics comparison of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

Key Parameters	V_{th} (V)	μ_{FE} (cm^2/V-s)	S.S. (mV/dec)	$I_{off, max}$ at V_{DS}=1 V V_{GS}= –2 V	I_{on}/I_{off} at V_{DS}=1 V
Fluorine-implanted Pr_2O_3 TFT	0.65	51.5	216	2.6×10^{-10}	1.6×10^{7}
Control Pr_2O_3 TFT	1.57	25.1	320	1.2×10^{-8}	3.4×10^{6}

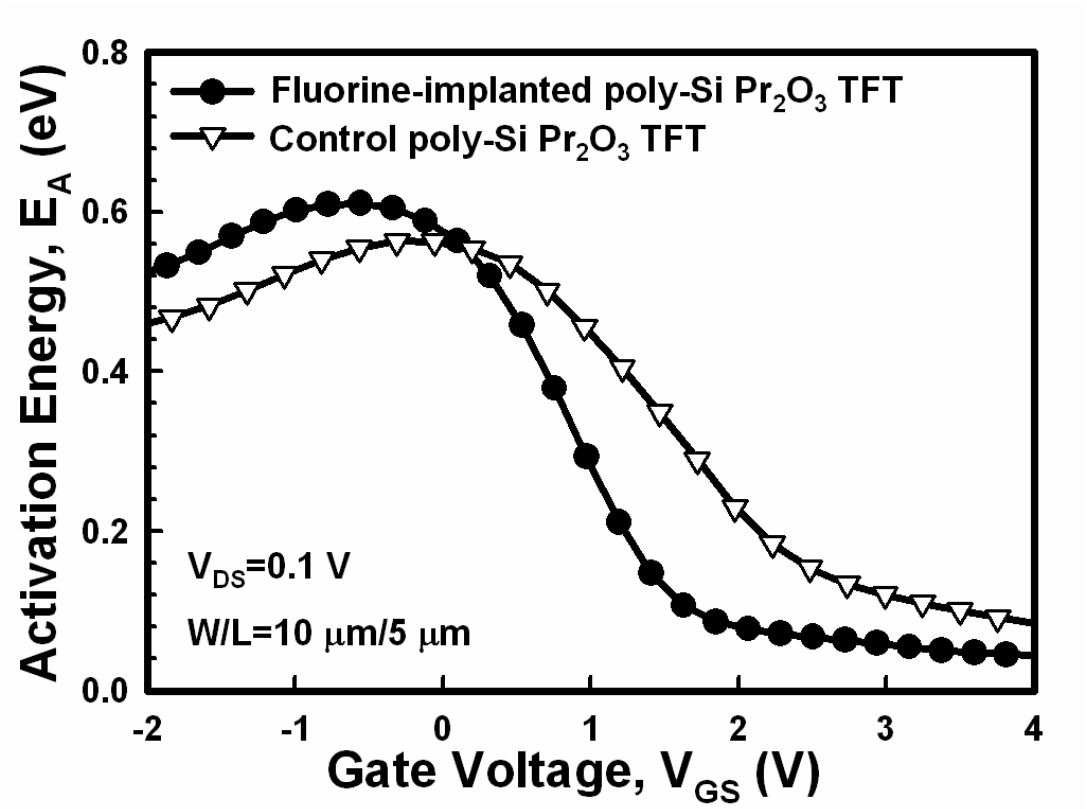


Fig. 3.8 Activation energy versus gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

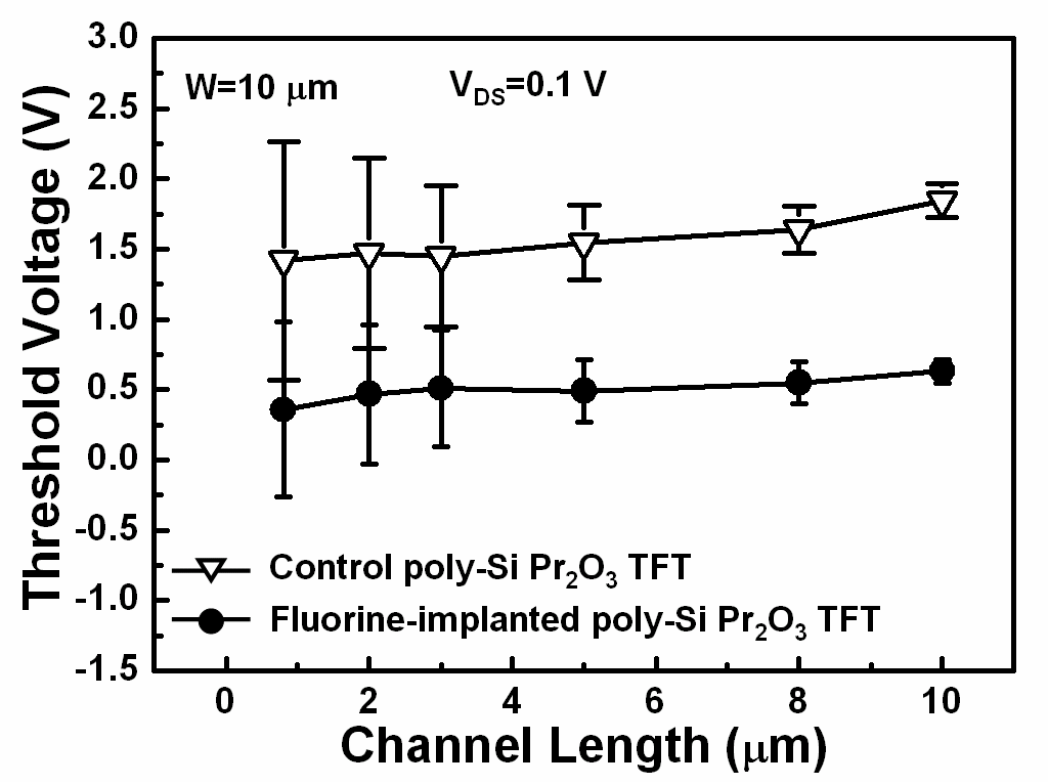


Fig. 3.9 Threshold-voltage rolloff characteristics for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

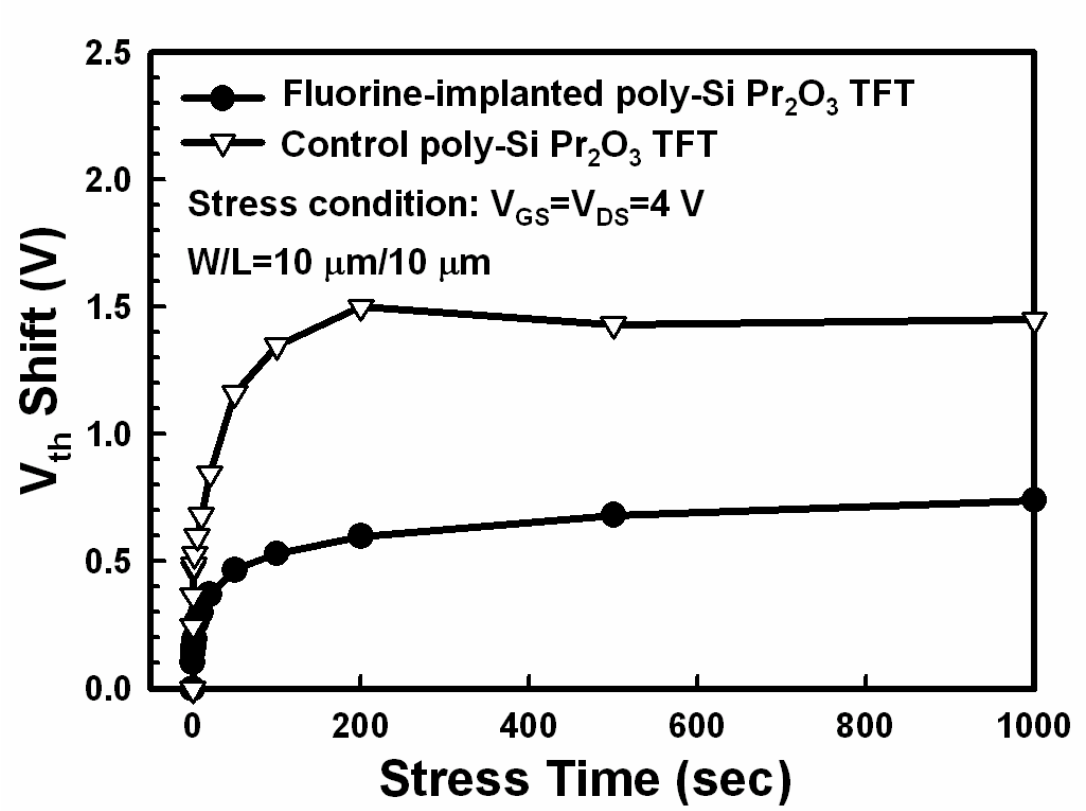


Fig. 3.10 Threshold-voltage shift over hot-carrier stress time for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

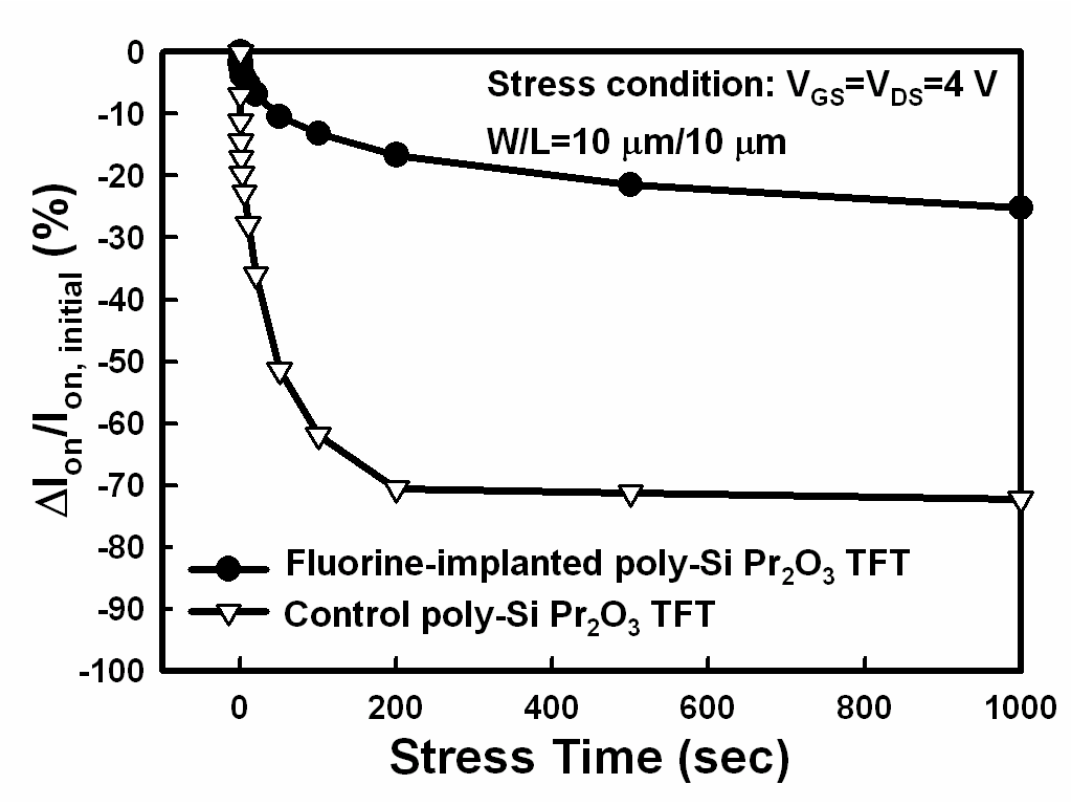


Fig. 3.11 On-current variation over hot-carrier stress time for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

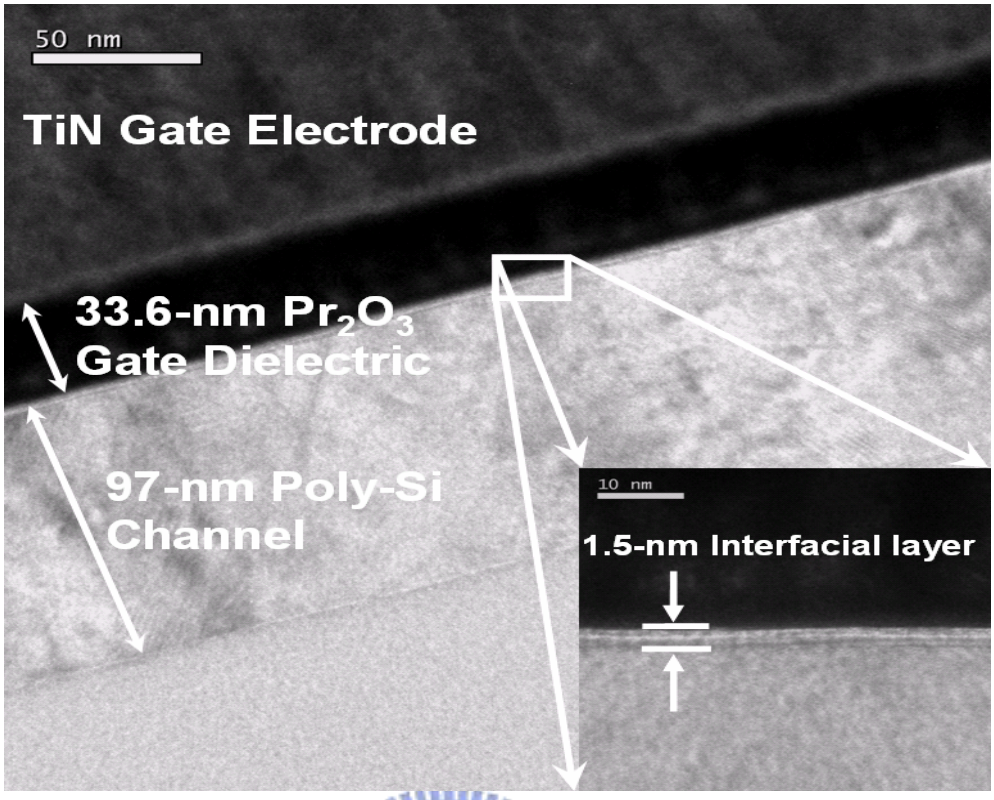


Fig. 3.12 Cross-sectional TEM image of the proposed Pr_2O_3 gate dielectric TFTs on the CF_4 plasma-treated poly-Si film.

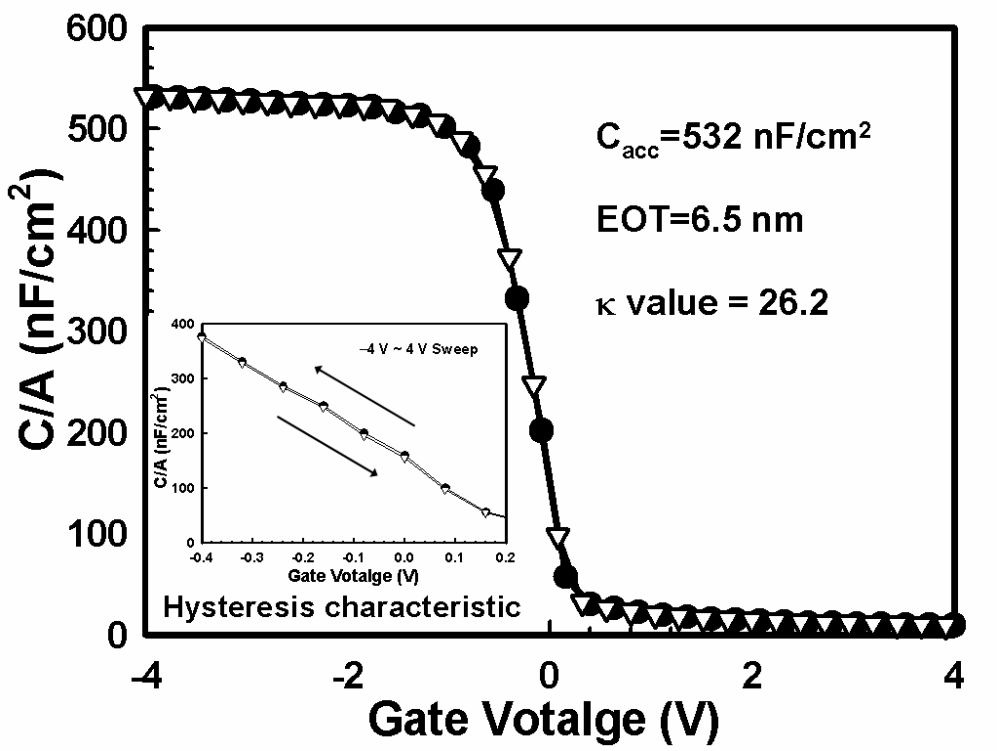


Fig. 3.13 Typical C-V characteristic of the Pr_2O_3 gate-dielectric MOS capacitor. The inset shows the hysteresis characteristic of the Pr_2O_3 gate dielectric.

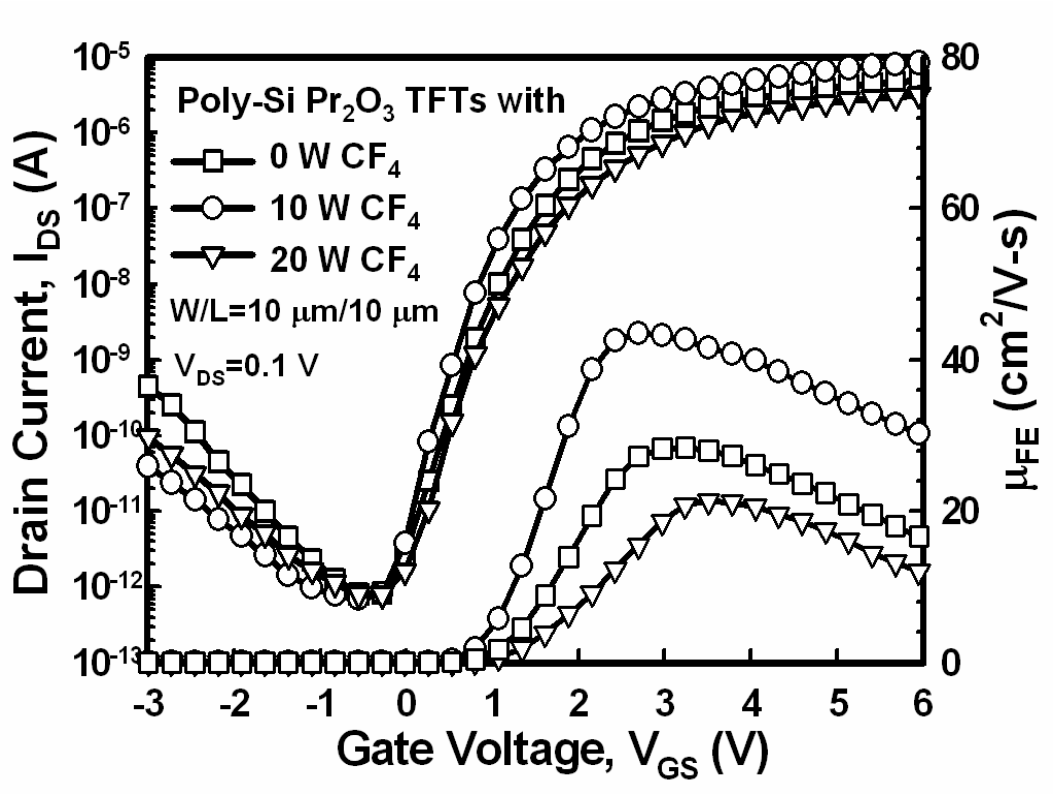


Fig. 3.14 Transfer characteristics of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments at V_{DS} = 0.1 V.

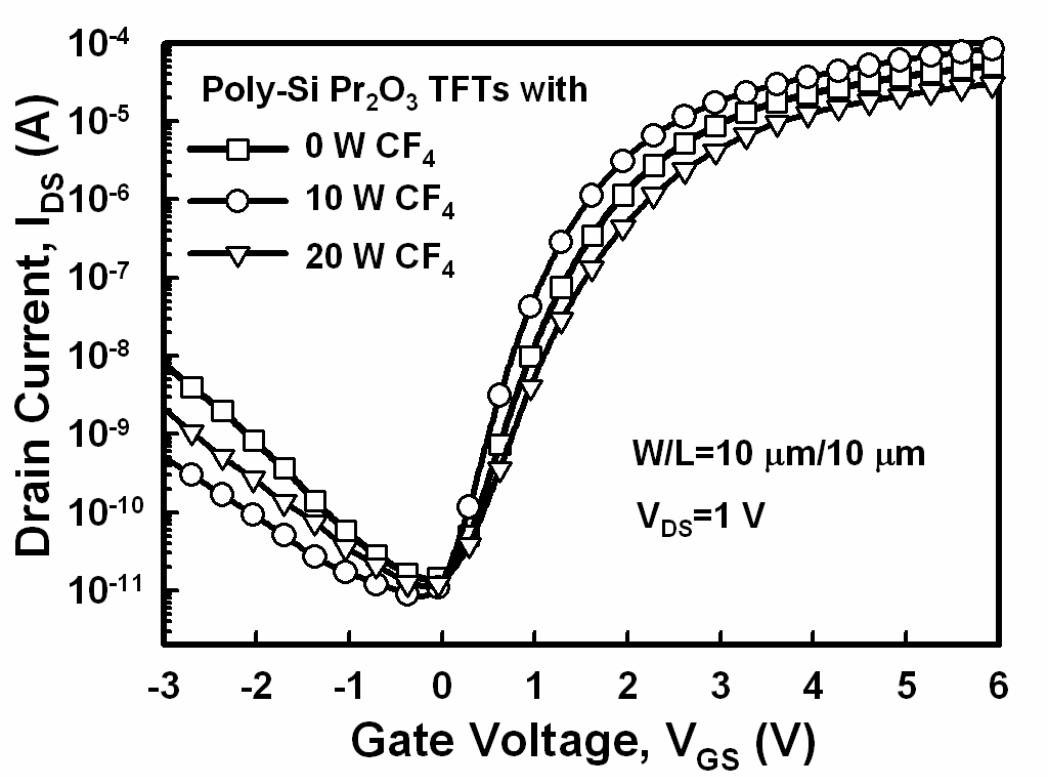


Fig. 3.15 Transfer characteristics of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments at V_{DS} = 1 V.

Table 3.2 Key device parameters for the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

Parameter	V_{th} (V)	S.S. (mV/dec)	μ_{FE} ($cm^2/V \cdot s$)	$I_{GIDL, max}$ (nA)	I_{on}/I_{off} (10^6)
Control	1.58	276	28.33	8.75	3.9
10 W	1.27	232	43.48	0.53	9.6
20 W	1.93	318	21.28	1.95	2.7

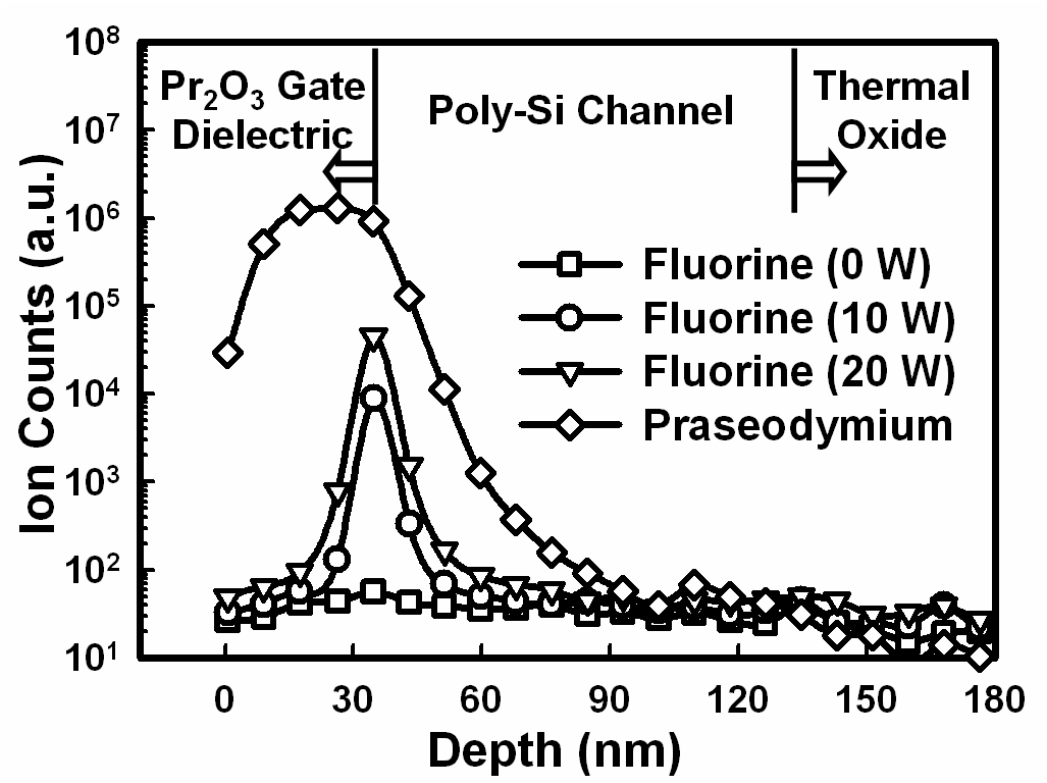


Fig. 3.16 SIMS depth profiles of the fluorine and praseodymium atoms for the poly-Si films with various rf powers of CF_4 plasma treatments.

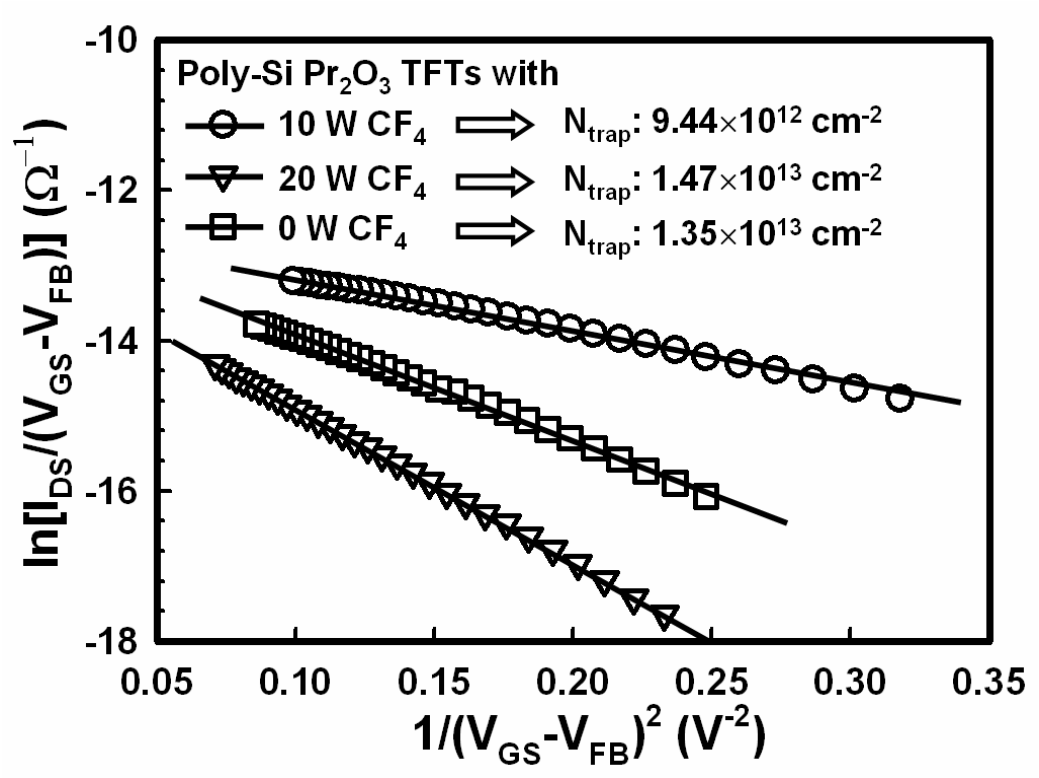
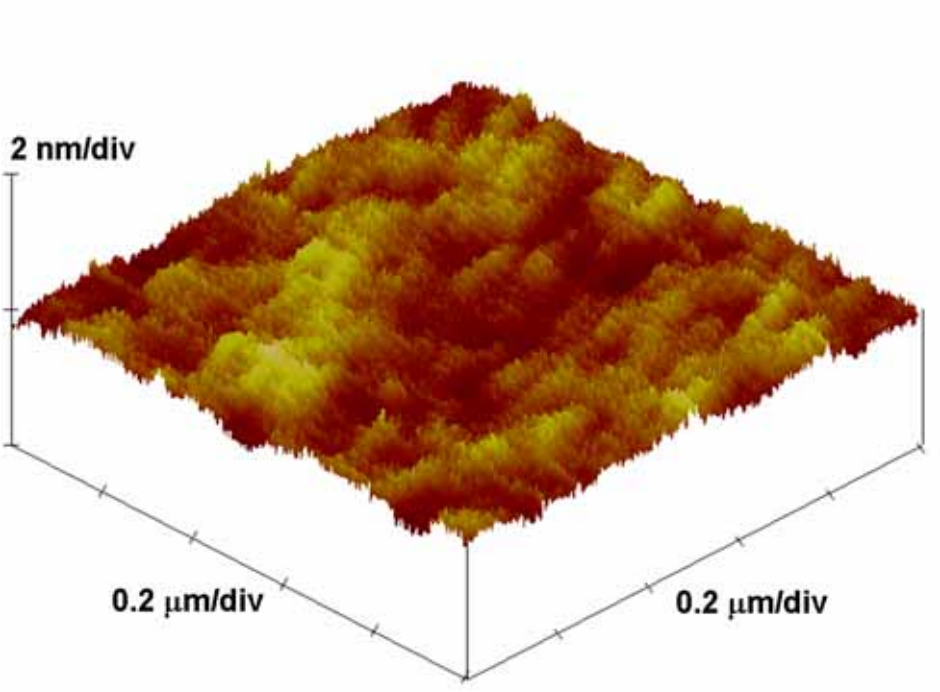
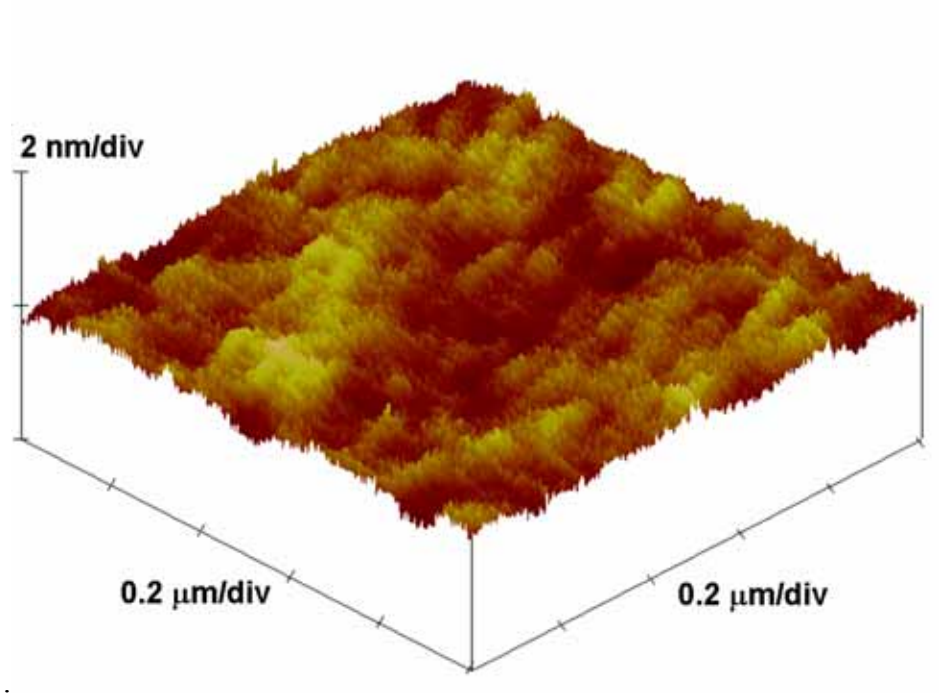


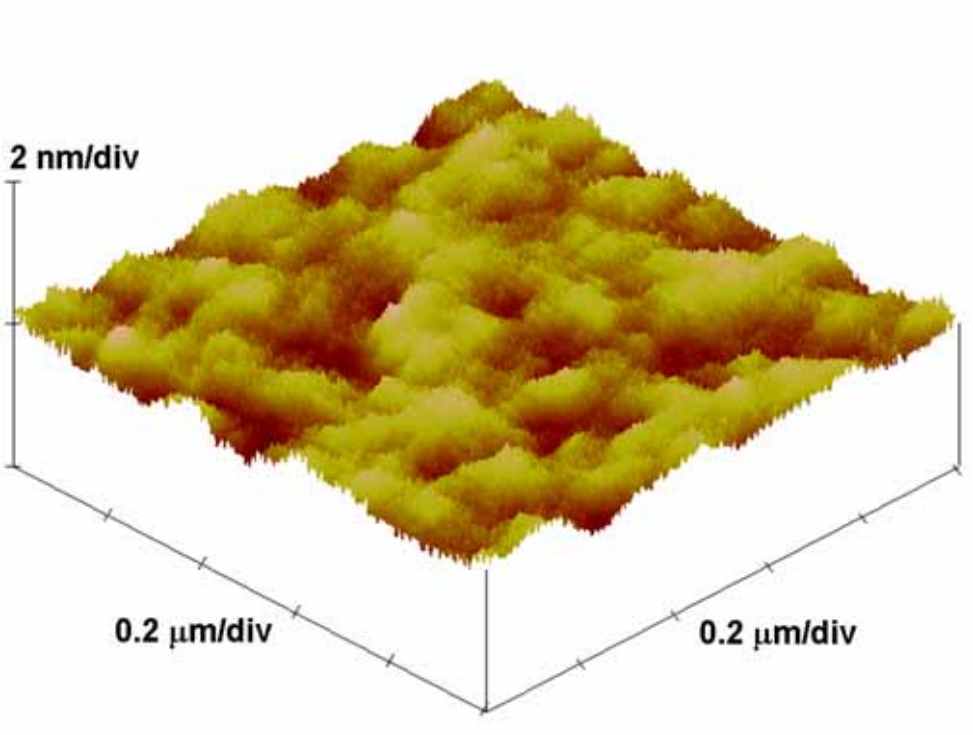
Fig. 3.17 Plot of $\ln[I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ under strong inversion at V_{DS} = 0.1 V for the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.



(a) AFM image of the poly-Si film with rf power of 0-W CF_4 plasma treatment (control). The RMS value of the poly-Si surface roughness is 0.25 nm.



(b) AFM image of the poly-Si film with rf power of 10-W CF_4 plasma treatment. The RMS value of the poly-Si surface roughness is 0.31 nm.



(c) AFM image of the poly-Si film with rf power of 20-W CF_4 plasma treatment. The RMS value of the poly-Si surface roughness is 0.47 nm.

Fig. 3.18 AFM images of the poly-Si films with various rf powers of 0-W, 10-W, and 20-W CF_4 plasma treatments.

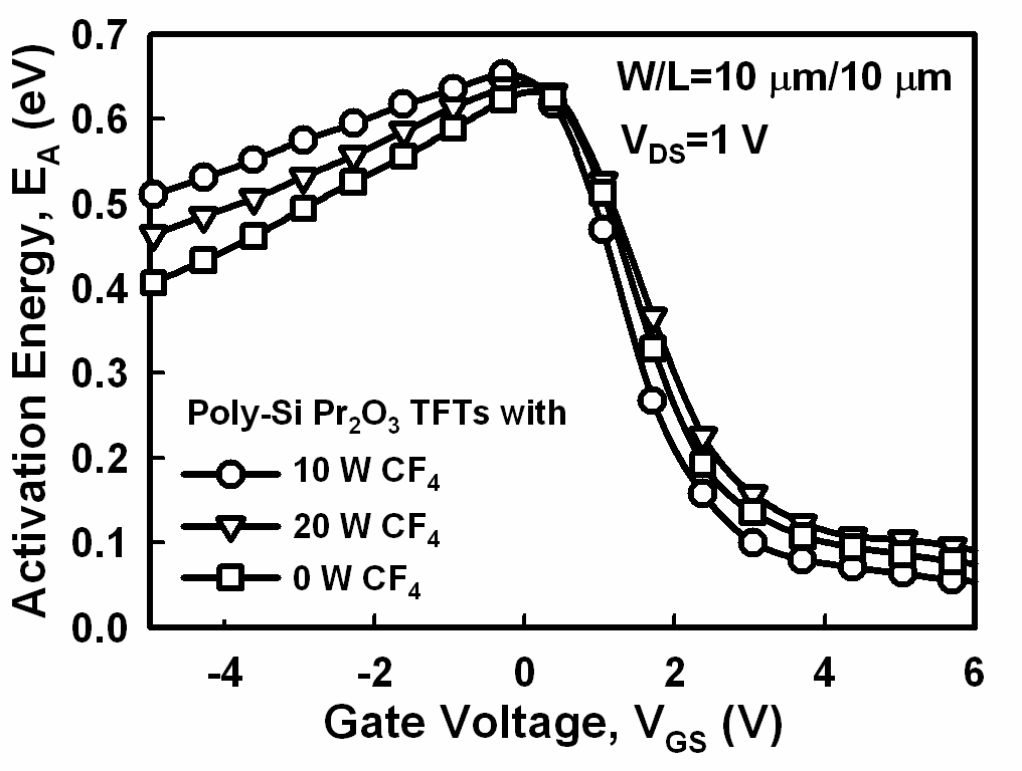


Fig. 3.19 Activation energy (E_A) of the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

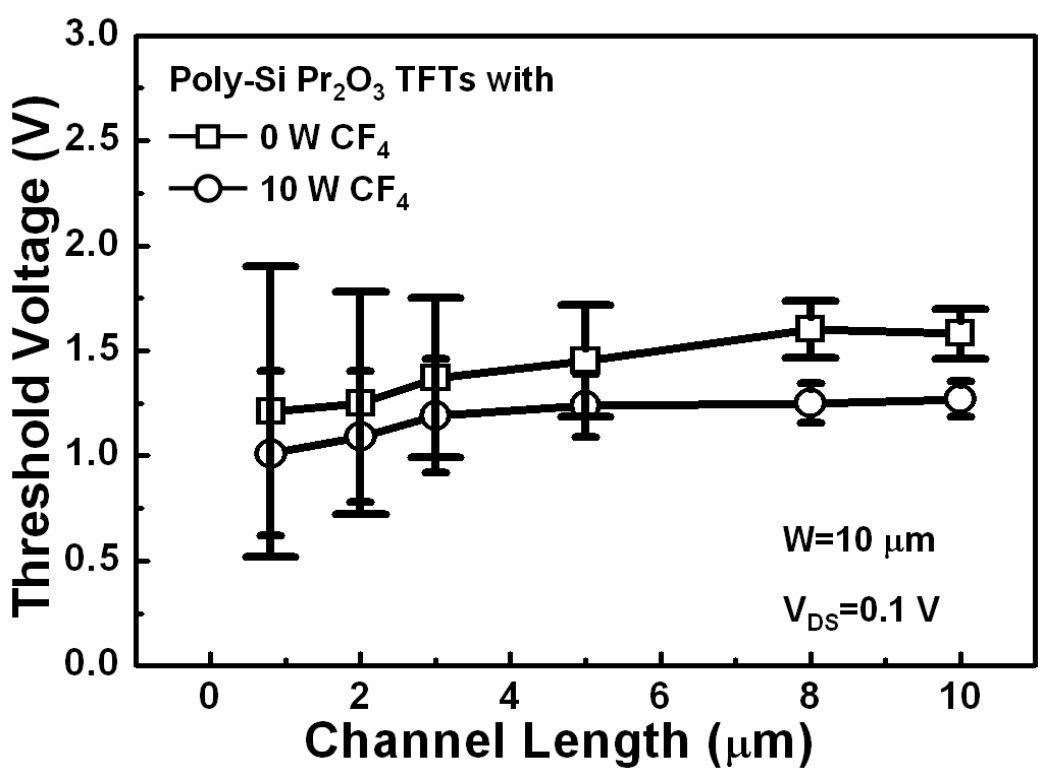


Fig. 3.20 Threshold-voltage rolloff characteristics of the poly-Si Pr_2O_3 TFTs with 0-W and 10-W CF_4 plasma treatments.

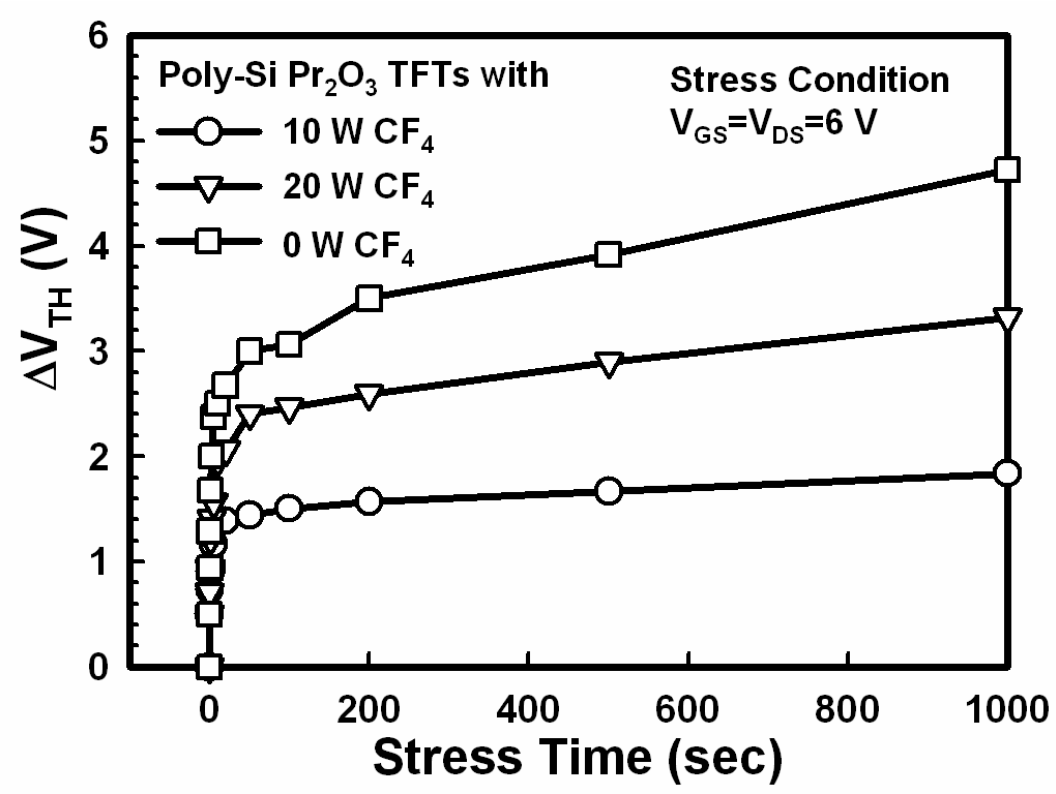


Fig. 3.21 Threshold-voltage shift versus hot-carrier stress time for the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

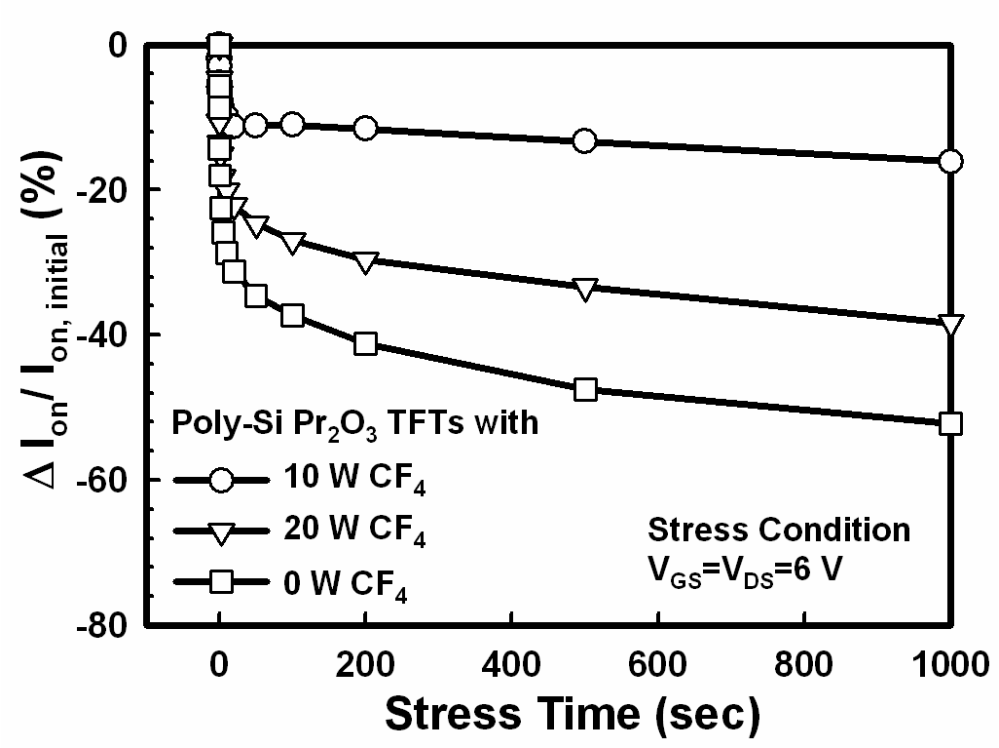


Fig. 3.22 On-current variation versus hot-carrier stress time for the poly-Si Pr_2O_3 TFTs with various rf powers of CF_4 plasma treatments.

Chapter 4

Effect of Argon-Ion Implant on Solid-Phase Crystallized Polycrystalline Silicon Thin-Film Transistors

4.1 Introduction

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFT) are widely used for active-matrix liquid crystal displays (AMLCDs) on glass substrates [4.1], [4.2]. However, a difficult technological challenge is to develop high-performance poly-Si TFTs that are useful for both pixel switching elements and peripheral driving circuits [4.3]. To achieve high-performance poly-Si TFTs on inexpensive glass substrate, low-temperature technology is required for realizing flat-panel displays (FPDs) owing to the maximum process temperature of lower than 600 ^{o}C. The solid-phase crystallization (SPC) process is widely used for phase transformation from amorphous to polycrystalline due to its low fabrication cost and good grain-size uniformity. However, the electrical characteristics of SPC poly-Si TFTs are strongly dependent on the microstructure of poly-Si film. In particular, the trap states in the poly-Si grains and grain boundaries acted as scattering centers and midgap traps are known to degrade the carrier's transport properties and increase the off-state leakage current [4.4]-[4.6]. Consequently, reducing these trap states becomes the primary way for achieving high-performance poly-Si TFTs. Hydrogen plasma treatment is a widely used method to passivate the trap states of the poly-Si film and improve the electrical performances of devices in modern TFT manufacturing [4.7], [4.8]. However, the

hydrogenated poly-Si TFTs suffer from a serious reliability issue due to the easily broken of weak Si-H bonds at the grain boundaries. Therefore, the SPC process plays an important role to affect the electrical characteristics of poly-Si TFTs [4.9]-[4.11]. However, the traditional SPC process is an interface-nucleation scheme generating too many nucleation sites at the amorphous silicon/underlying oxide (α-Si/SiO_2) interface resulting in a small grain size and a large number of grain-boundary trap states [4.12]-[4.15]. Thus, many efforts have been attempted to increase the grain size and to reduce the trap-state density of the poly-Si film [4.16]-[4.19].

Modified SPC processes with surface-nucleation scheme were proposed to improve the microstructure of poly-Si film by introducing oxygen doping at the α-Si/SiO_2 interface [4.16], [4.17]. It has been known that oxygen retards the crystallization process of an oxygen-implanted α-Si film during the solid-phase epitaxial regrowth [4.18]. When the interfacial grain nucleation is effectively suppressed, the grain nucleation process will initiate at another preferable nucleation site on the top free surface of α-Si film [4.16], [4.17]. Because of fewer nucleation sites at the top free surface of α-Si film, the larger grain size of poly-Si could be obtained. However, the oxygen doping during α-Si deposition causes particle contamination issue to possibly affect the electrical characteristics of poly-Si TFTs [4.16], and it also need complicated processes during α-Si deposition [4.17]. Recently, Wu *et al*. also proposed that retardation of silicon grain nucleation at the α-Si/SiO_2 interface could enlarge the grain size of poly-Si [4.19]. The decreased silicon grain nucleation rate could be attributed to that recoiled oxygen atoms from the SiO_2 substrate by deep Si implantation will accumulate at the α-Si/SiO_2 interface. Among aforesaid processes, an oxygen-rich layer is introduced at the α-Si/SiO_2 interface by various methods to verify the grain-size enhancement of poly-Si film, but they have not been successfully adopted for TFT fabrication.

In this chapter, a modified surface-nucleation SPC scheme with the grain-size

enhancement achieved by deep Argon ion implantation is proposed. It is expected that the heavy Argon (atomic weight of 40) ion implantation could induce more recoiled oxygen atoms at the α-Si/SiO_2 interface with a lower implantation dosage. Therefore, the crystallinity of SPC poly-Si could be further enhanced, and the performances and reliability of poly-Si TFTs with Argon ion implantation also could be improved.

4.2 Experiments

The schematic diagram of the fabrication processes of the poly-Si TFTs with Argon ion implantation is shown in Fig. 4.1. First, a 100-nm undoped amorphous silicon (α-Si) film was deposited on a 500-nm thermal oxide (SiO_2) covered Si wafer by low-pressure chemical vapor deposition (LPCVD) system at 550 ^oC [Fig. 4.1(a)]. Following, the Argon ions were implanted through the 100-nm α-Si film with the accelerating energy and dosage at 90 keV and 1×10^{12} cm^{-2}, respectively [Fig. 4.1(b)]. With the 90-keV accelerating energy, the projected range of Argon ions was located beyond the α-Si/thermal SiO_2 interface. Subsequently, the Argon-implanted α-Si layer was recrystallized at 600 ^oC for 24 h in N_2 ambient for phase transformation from amorphous into polycrystalline. After individual active regions were patterned [Fig. 4.1(c)], a 50-nm tetraethylorthosilicate (TEOS) oxide was deposited to serve as the gate dielectric, and a 200-nm poly-Si was deposited and patterned for the gate electrode [Fig. 4.1(d)]. A self-aligned phosphorous ion implantation was preformed to dope the source/drain (S/D) and gate with the dosage and energy of 5×10^{15} cm^{-2} and 40 keV, respectively [Fig. 4.1(e)]. And then, the S/D dopants were activated at 600 ^oC for 12 h in N_2 ambient. Following, a 300-nm passivation SiO_2 was deposited by plasma-enhanced CVD (PECVD) system, and then the contact holes were patterned and etched by buffer-oxide etchant (BOE) solution. Aluminum (Al) electrode was deposited and then patterned as metal pads [Fig. 4.1(f)]. Finally, a thermal sintering process was performed

at 350 ^{o}C for 30 min. Control poly-Si TFTs without Argon ion implantation were also fabricated for comparison.

4.3 Results and Discussion

4.3.1 Material Analyses

The scanning electron microscopy (SEM) images of solid-phase crystallized (SPC) poly-Si films for the Argon-implanted and control samples after secco etching are shown in Figs. 2.2(a) and 2.2(b), respectively. The SEM images apparently reveal the difference in their grian size between the Argon-implanted and control samples. The average grain sizes of poly-Si for the Argon-implanted and control poly-Si samples are approximately 100 nm and 20 nm, respectively. The enhancement on the silicon grain size is descried as follows. Because the silicon atoms are bounded to underlying thermal SiO_2, the rearrangement and volume contraction of silicon atoms at the beginning of crystallization process would produce a large magnitude of tensile stress at the α-Si/SiO_2 interface in the control poly-Si film [4.16]. Many silicon nucleation sites related crystalline defects including microtwins and stacking faults are introduced in order to relieve the tensile stress. Therefore, the grain size of poly-Si obtained from many silicon nucleation sites is rather small. In contrast, in the case of the Argon-implanted poly-Si film, because the interface-nucleation rate is almost suppressed, the stress generated from the surface nucleation is easily relieved from the top free surface. Consequently, the silicon nucleation sites associated with crystalline defects are reduced, resulting in larger silicon grain size and better grain crystallinity in the Argon-implanted poly-Si film.

The x-ray diffraction (XRD) patterns of the Argon-implanted and control poly-Si films after SPC annealing are shown in Fig. 4.3. The SPC poly-Si film has two preferred orientations, the dominant orientation of Si (111) and the other orientation of Si (110),

reported by Aoyama *et al*. [4.20]. The intensity of the preferred orientation of Si (111) and Si (110) in the Argon-implanted poly-Si film is apparently sharper and higher than that in the control poly-Si film. Therefore, the sharper and higher intensity of XRD peaks proved the crystallinity of poly-Si film in the Argon-implanted sample can be improved compared to that in the control sample. The reason why the Argon-implanted poly-Si film has better crystallinity could be ascribed as following. When heavy Argon ions are implanted through the α-Si film with the projected range located beyond the α-Si/SiO_2 interface, many recoiled-oxygen atoms from the SiO_2 substrate will accumulate at the α-Si/SiO_2 interface. The presence of recoiled-oxygen atoms is believed to reduce the nucleation sites at the α-Si/SiO_2 interface [4.16]- [4.19], which suppresses the interface-nucleation rate of Si atoms, and thereby to result in the nucleation of silicon grain from the top free surface of α-Si layer, called surface-nucleation scheme.

To prove the recoiled-oxygen existing at the α-Si/SiO_2 interface, the secondary ion mass spectroscopy (SIMS) analysis is performed. Fig. 4.4 shows the SIMS depth profiles of oxygen atoms for the Argon-implanted and control α-Si films. The SIMS depth profile shows that an oxygen-rich region is observed near at the α-Si/SiO_2 interface after the Argon implantation. Consequently, when the interface-nucleation rate is suppressed but the surface-nucleation scheme is dominated, the large silicon grains could be formed after Argon implantation treatment.

4.3.2 Device Characteristics

Typical transfer characteristics of the Argon-implanted and control poly-Si TFTs are shown in Fig. 4.5. The measurements were performed at two drain voltages of V_{DS} = 0.5 V and 5 V, and the drawn channel length (L) and channel width (W) are 10 μm and 10 μm, respectively. The electrical parameters of these devices, including threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), and subthreshold swing (S.S.) were extracted at V_{DS} = 0.5 V,

whereas the maximum on current (I_{ON}), minimum off current (I_{OFF}), and ON/OFF current ratio (I_{ON}/I_{OFF}) were defined at V_{DS} = 5 V. The threshold voltage is defined as the gate voltage required to yield a normalized drain current of I_{DS} = (W/L)×100 nA. The major electrical parameters of these poly-Si TFTs are summarized in Table 4.1. Obvious performance improvements are achieved for the Argon-implanted poly-Si TFTs. The threshold voltage and subthreshold swing of the Argon-implanted poly-Si TFT are 1.73 V and 750 mV/dec, whereas the control poly-Si TFT has the value of 5.75 V and 1290 mV/dec, respectively. The threshold voltage and subthreshold swing of the Argon-implanted poly-Si TFT are found to be superior to those of the control one. Some studies reported that the deep trap states originated from the Si dangling bonds, which have energy states near the middle of the silicon bandgap, would greatly influence the threshold voltage and subthreshold swing [4.21]. The poly-Si film with surface-nucleated scheme can improve the crystallinity of silicon, resulting in decreasing the grain boundaries with decreasing the Si dangling bonds in the poly-Si film. In addition, the leakage current of the Argon-implanted poly-Si TFT was smaller than that of the control one. As is well-known, the traps assisted band-to-band tunneling resulted from the high electric field near the drain junction results in the leakage current [4.22]. The result suggests that fewer grain boundaries exist in the Argon-implanted poly-Si film, and thus the leakage current under a high electric field can be reduced.

Fig. 4.5 also shows the field-effect mobility as a function of gate voltage for the Argon-implanted and control poly-Si TFTs. The field-effect mobility is calculated from the transconductance at V_{DS} = 0.5 V. In Fig. 4.5, the maximum field-effect mobility of the Argon-implanted poly-Si TFT has approximately 74 % improvement compared to that of the control one. Because Argon ion is a noble gas which could not react with Si dangling bonds or contribute any dopant species, the improved performances cannot be ascribed to the Argon passivation effect on the grain-boundary trap states and dopant-induced threshold voltage variation. Therefore, the main reason for the field-effect mobility improvement may be

further attributed to the enhancement of grain size and the reduction of grain boundaries, thereby leading to a better microstructure crystallinity of silicon grain in the Argon-implanted poly-Si film.

4.3.3 Trap-State Density and Activation Energy

The grain-boundary trap-state density (N_{trap}) of the Argon-implanted and control poly-Si TFTs could be extracted according to the grain-boundary trapping model proposed by Levinson and Proano [4.23], [4.24]. Fig. 4.6 shows the plot of $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ at V_{DS} = 0.5 V and high gate voltage. N_{trap} is estimated from the slopes of these curves. It can be found that the Argon-implanted poly-Si TFT exhibits a N_{trap} of around 3.44×10^{12} cm^{-2}, whereas the control one possess a N_{trap} of 6.48×10^{12} cm^{-2}. This result further confirms that Argon implantation treatment can reduce grain-boundary trap states in the poly-Si film due to the enlarged grain size and the reduced grain boundaries.

Fig. 4.7 illustrates the activation energy (E_A) of drain current as a function of gate voltage measured at V_{DS} = 5 V for the Argon-implanted and control poly-Si TFTs. E_A was extracted by the measurement of I_{DS}–V_{GS} characteristics at various temperatures from 25 to 150 ^oC. E_A represents the carrier transportability, which is related to the barrier height in the poly-Si channel [4.25]. The Argon-implanted poly-Si TFT exhibits a higher E_A in turned-off state but a lower E_A in turned-on state, as compared to the control poly-Si TFT. The result infers that Argon implantation treatment can obtain a better crystallinity of silicon grain with reduced trap-state density. Moreover, a steeper curve can be found in the subthreshold region, which proves that the interface quality of the Argon-implanted poly-Si TFT is better than that of the control one.

4.3.4 Threshold-Voltage Rolloff

To investigate the short-channel effect of the poly-Si TFTs, the threshold voltages of the

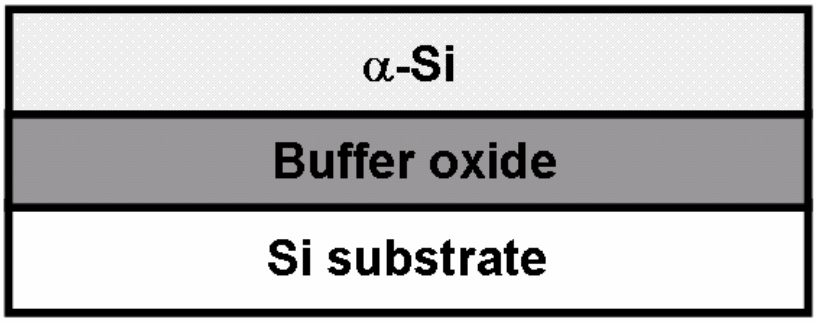
Argon-implanted and control poly-Si TFTs with their channel width (W) of 10 μm as a function of channel length (L) are shown in Fig. 4.8. The threshold voltage of the control poly-Si TFTs is decreased with decreasing the channel length, dominated by the reduction of the grain-boundary trap states, called threshold voltage rolloff effect, [4.26], [4.27]. Nevertheless, in the case of the Argon-implanted poly-Si TFT, its threshold-voltage rolloff effect could be well suppressed because it has fewer grain-boundary trap states in the poly-Si channel film. Moreover, the Argon implantation treatment also leads to a smaller threshold voltage due to the reduced grain-boundary trap states.

4.3.5 Device Reliability

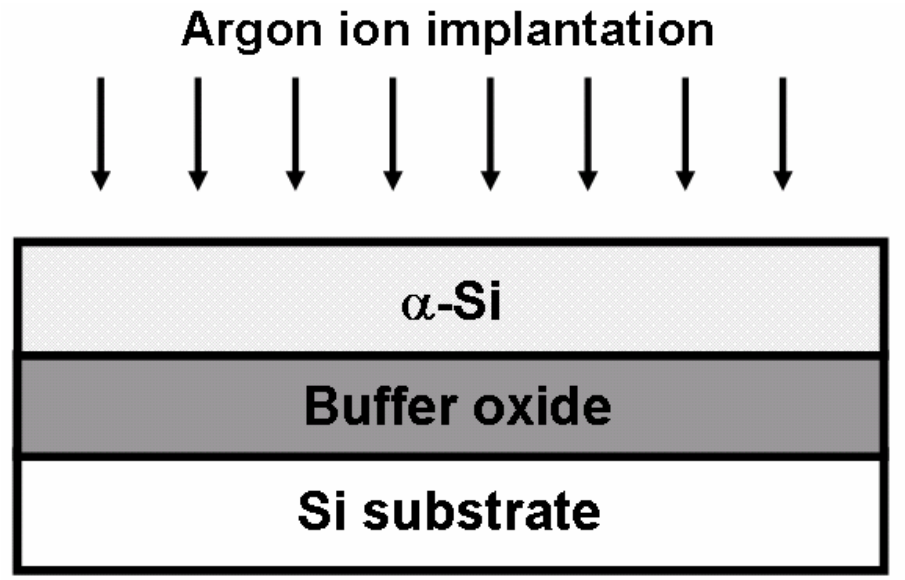
Additionally, hot-carrier stress was carried out to investigate the device reliability. The Argon-implanted and control poly-Si TFTs were stressed at V_{DS} = 20 V and V_{GS} = 20 V for 10000 s. The variations of threshold voltage (ΔV_{TH}) over hot-carrier stress time are shown in Fig. 4.9. Hot carrier multiplication occurred at the drain side of poly-Si TFTs causes the degradation of threshold voltage. Notably, the variation of V_{TH} of the Argon-implanted poly-Si TFT is smaller than that of the control poly-Si TFTs after stress time of 10000 s. It has been reported that the degradations of V_{TH} caused by hot-carrier stress could be attributed to two reasons: the generation of interface states at the poly-Si channel/gate dielectric interface and the formation of deep trap states originated from the broken of weak Si-Si or Si-H bonds at the grain boundaries [4.28], [4.29]. The result hints that the poly-Si film with Argon implantation treatment forms larger grain size accompanied with fewer grain boundaries. Therefore, the Argon-implanted poly-Si TFTs with fewer grain boundaries in its channel film possess a superior hot-carrier endurance.

4.4 Summary

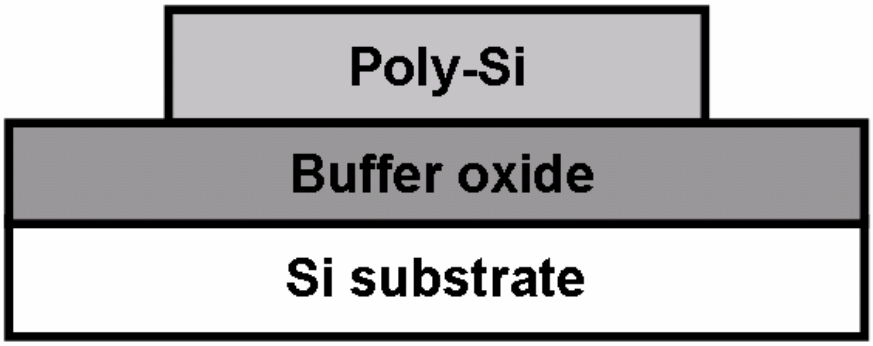
In summary, we have investigated the modified SPC of α-Si film with surface-nucleation scheme by heavy Argon ion implantation. The interface-nucleation rate is suppressed in the Argon-implanted α-Si film, resulting in a better microstructural quality of poly-Si films. The electrical characteristics of the poly-Si TFTs, including threshold voltage, subthreshold swing, field-effect mobility, trap-state density, and ON/OFF current ratio, are significantly improved using Argon ion implatation technique. In addition, the Argon-implanted poly-Si TFTs also present a higher immunity against the hot-carrier stresses attributing to larger grain size of poly-Si film with fewer grain-boundary defects. Therefore, the Argon-implanted poly-Si TFTs are not only compatible with conventional fabrication processes but also possessing superior electrical characteristics for large flat-panel display applications.



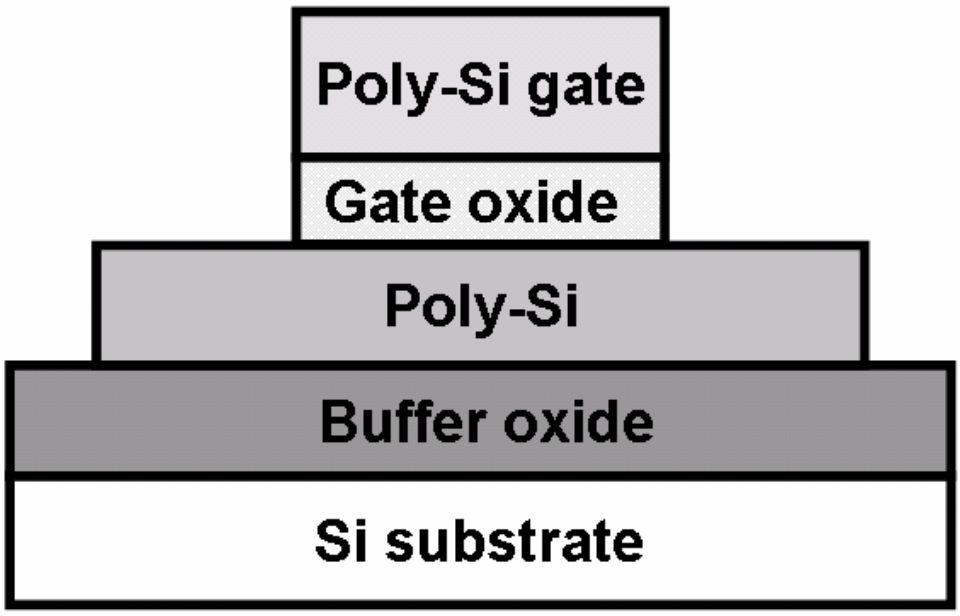
(a) Thermal oxidation, and α-Si deposition.



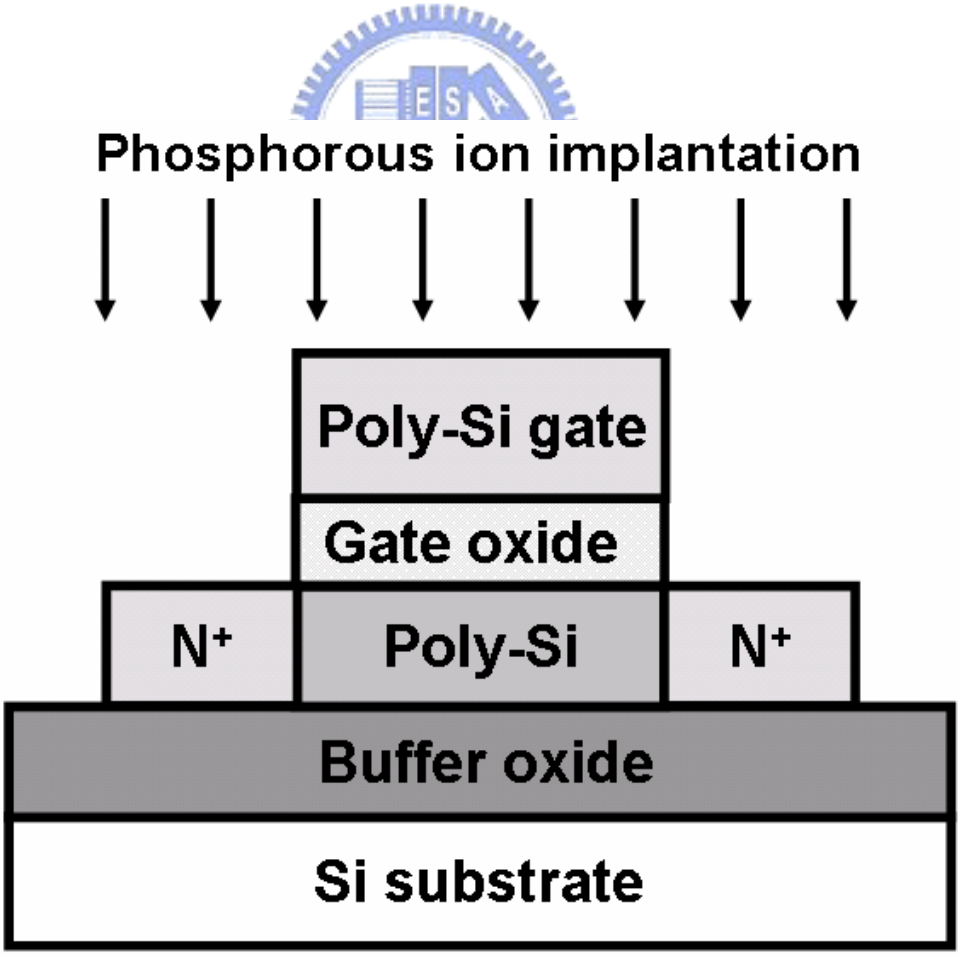
(b) Argon ion implantation with projected range located beyond α-Si/buffer oxide interface.



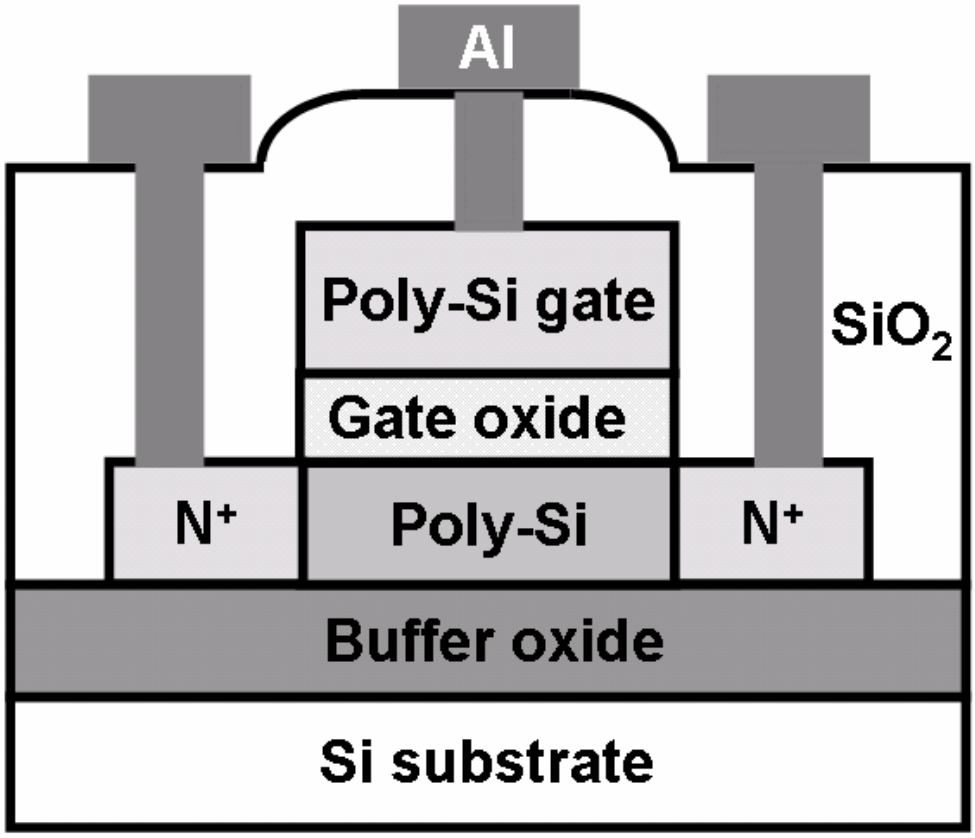
(c) Solid-phase crystallization of α-Si, and patterning of active region.



(d) Gate oxide and poly-Si gate deposition, and patterning of gate electrode.

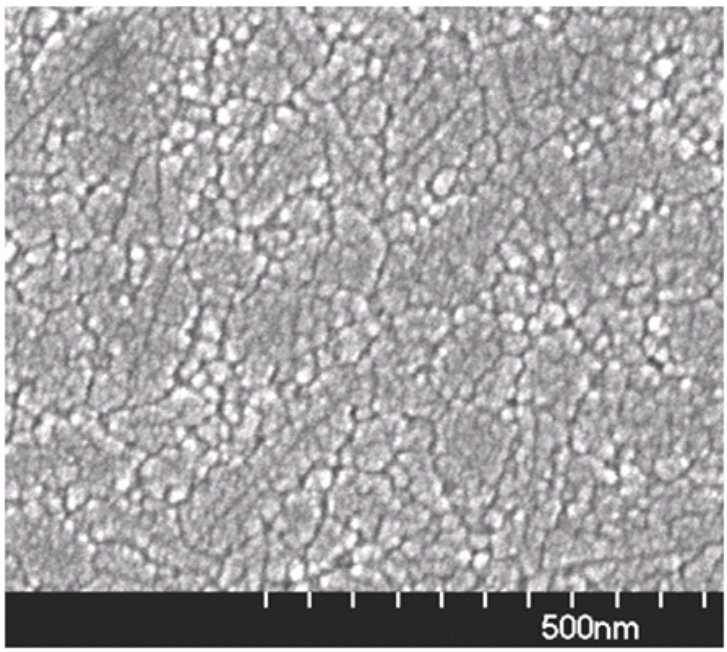


(e) Self-aligned phosphorous ion implantation, and dopant activation.

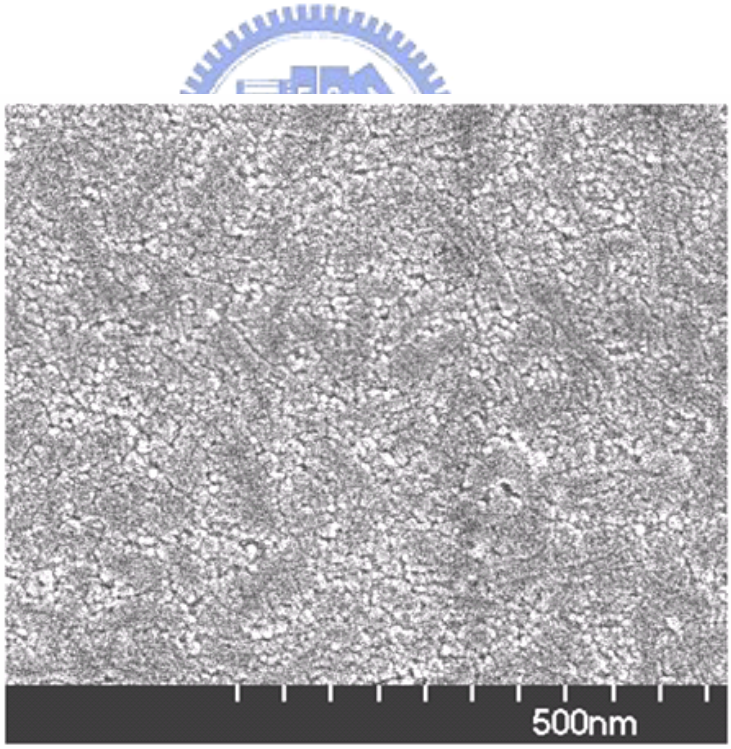


(f) Passivation oxide deposition, patterning of contact hole, and formation of metal pad.

Fig. 4.1. Schematic diagram of the fabrication processes of the poly-Si TFTs with Argon ion implantation.



(a) SEM image of the Argon-implanted poly-Si film.



(b) SEM image of the control poly-Si film.

Fig. 4.2. SEM images of the secco-etched poly-Si films with and without Argon ion implantation after SPC process.

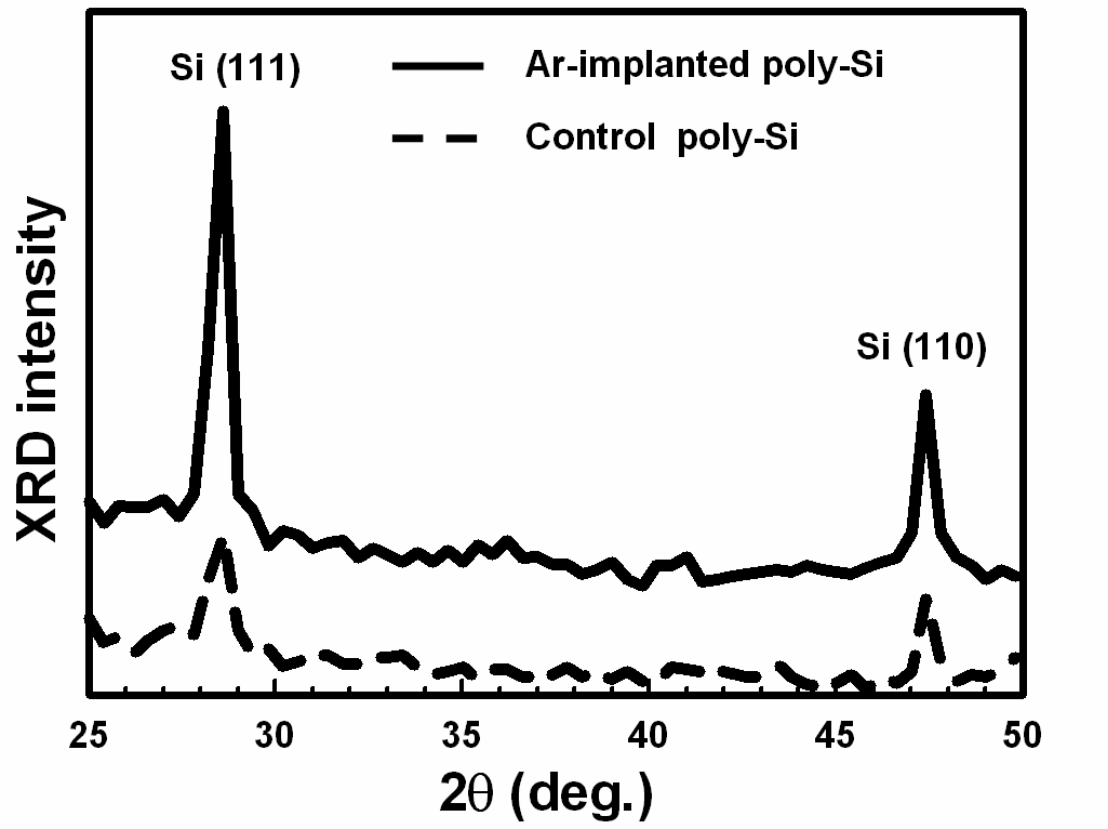


Fig. 4.3. XRD patterns of the Argon-implanted and control poly-Si films after SPC process.

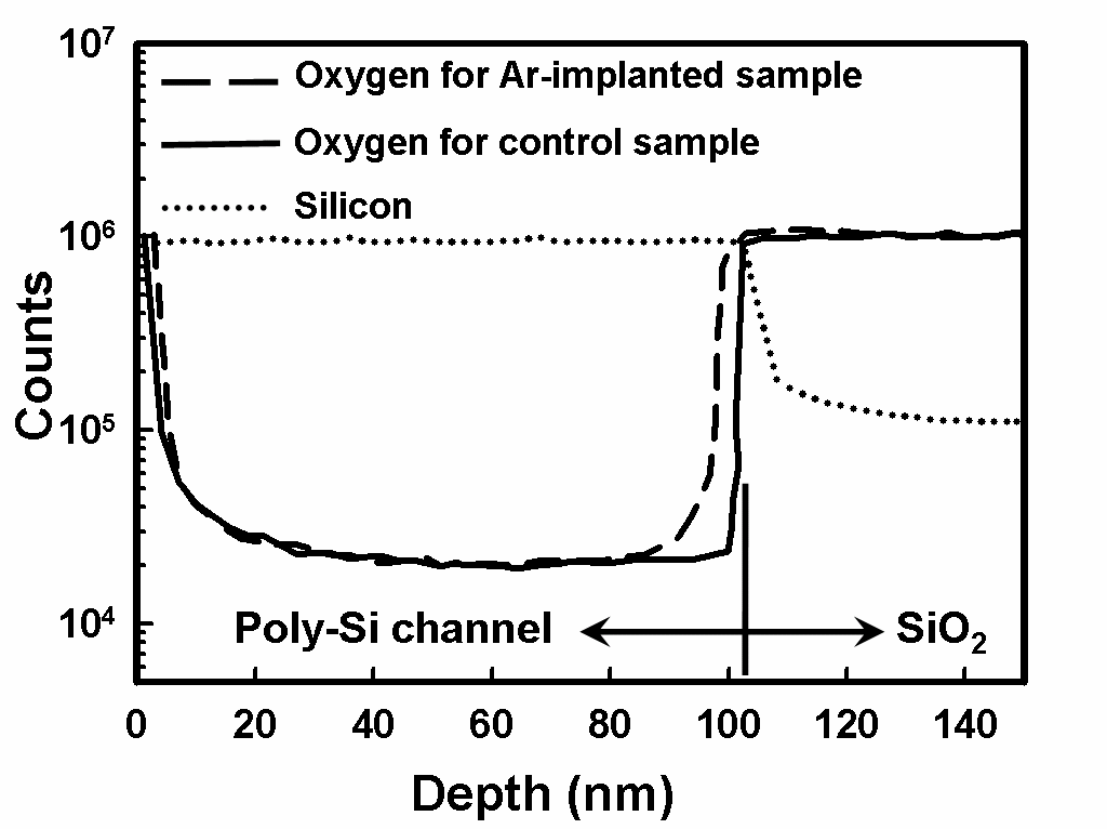


Fig. 4.4. The SIMS depth profiles of oxygen and silicon for the Argon-implanted and control α-Si samples.

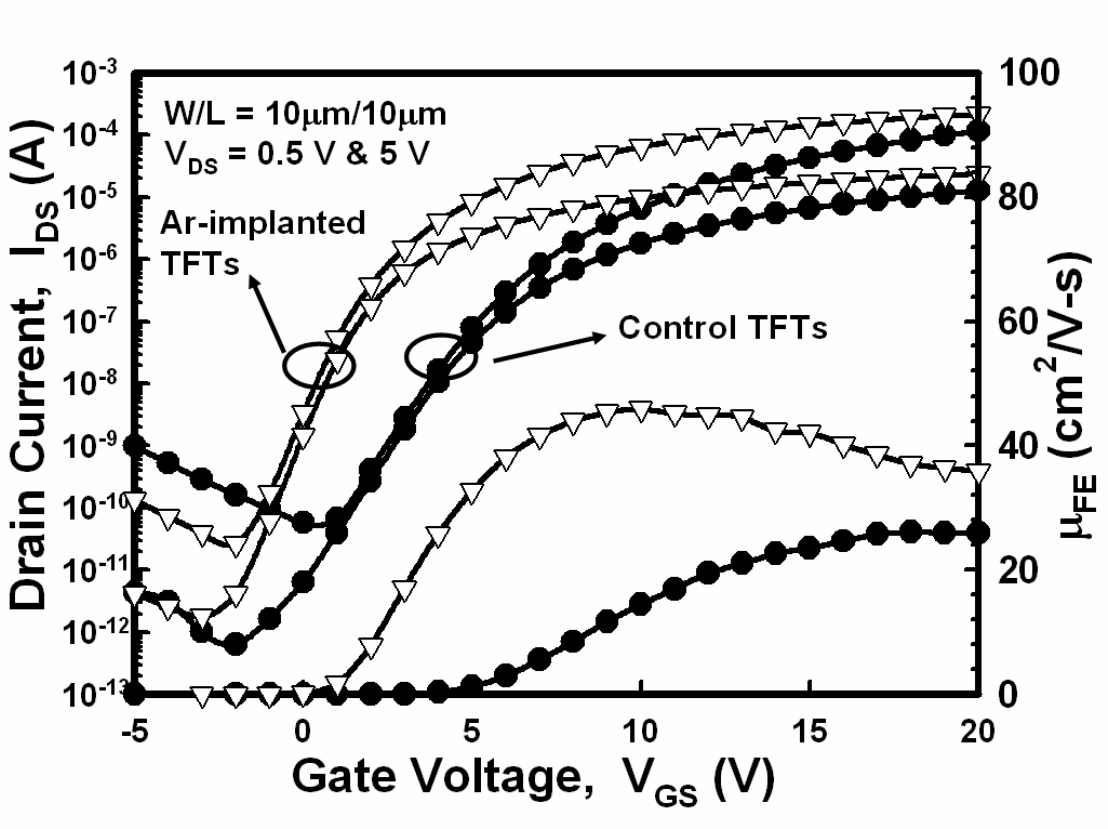


Fig. 4.5. Typical transfer characteristics of the Argon-implanted and control poly-Si TFTs at V_{DS} = 0.5 V and 5 V.

Table 4.1 Devices characteristics comparison of the Argon-implanted and control poly-Si TFTs with a dimension of W/L = 10 μm/10 μm.

Key parameters	Control TFTs	Ar-implanted TFTs
Threshold Voltage (V)	5.75	1.73
Subthreshold swing (V/dec)	1.29	0.75
Field-effect mobility (cm^2/V-s)	26.5	46.1
Trap state density	6.48×10^{12}	3.44×10^{12}
ON/OFF current ratio	6.67×10^{6}	1.11×10^{7}

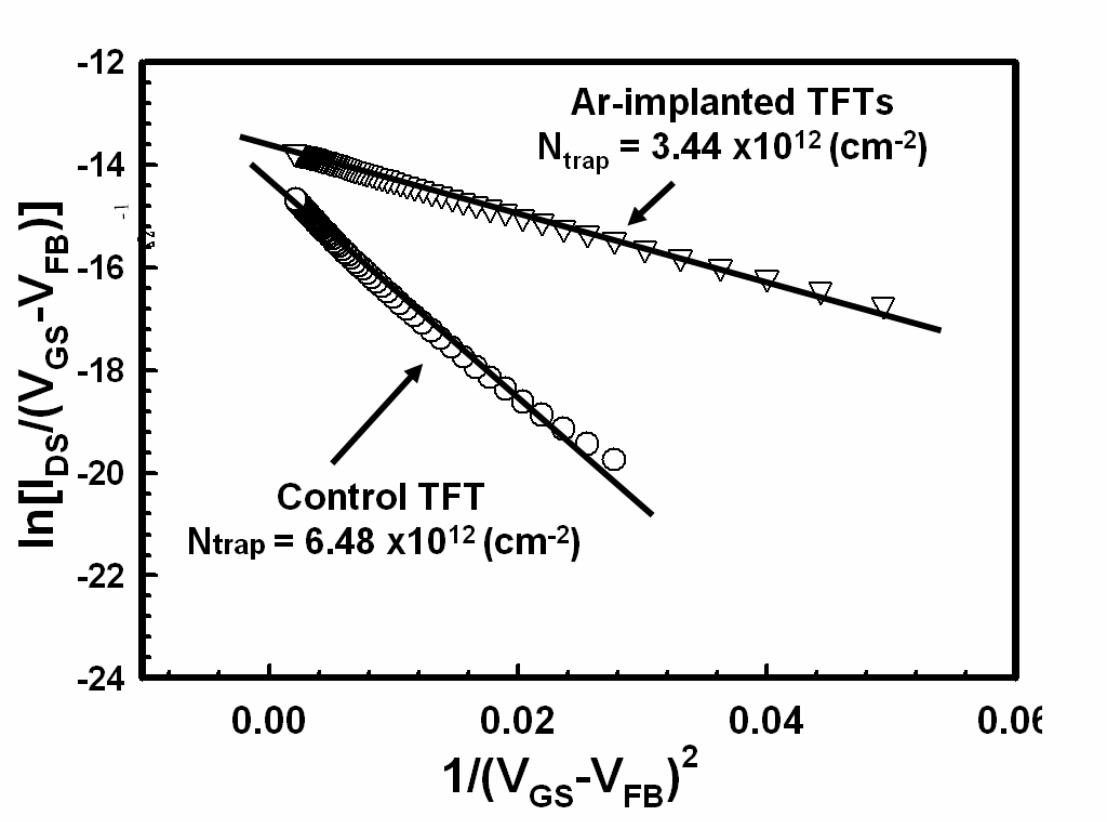


Fig. 4.6. Plot of $\ln[(I_{DS}/V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ and the extracted grain-boundary trap-state densities for the Argon-implanted and control poly-Si TFTs.

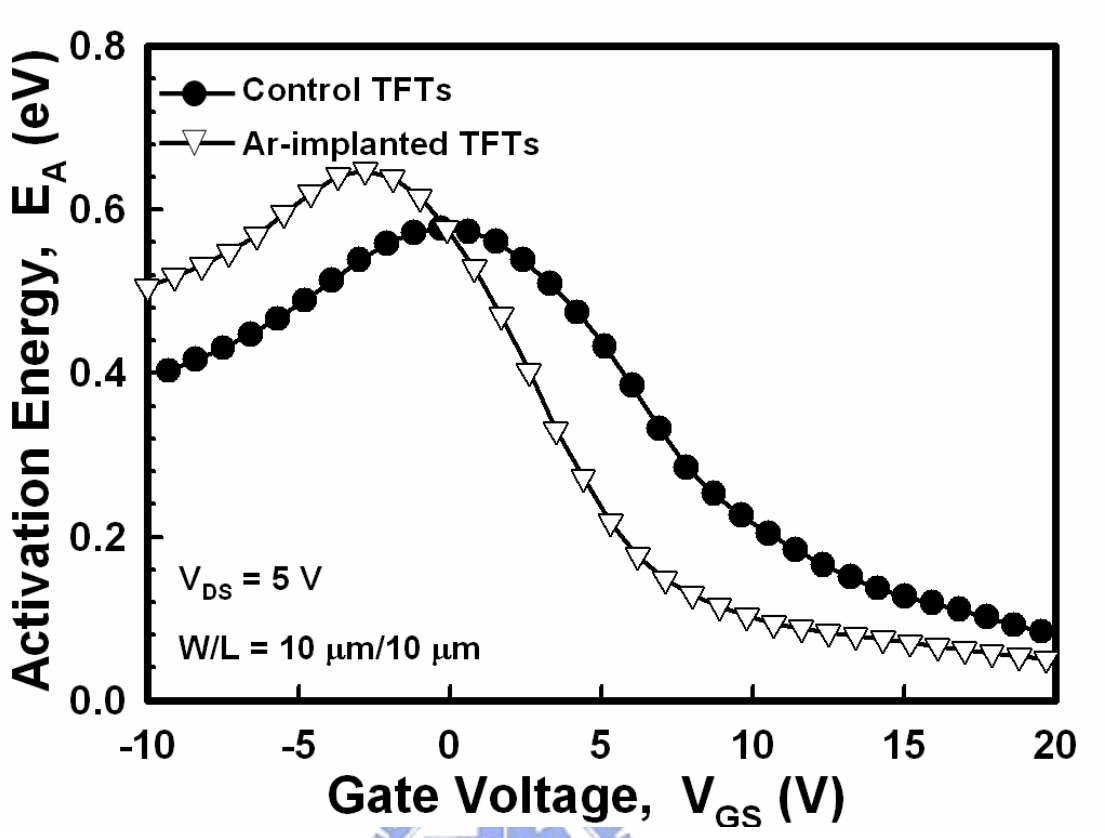


Fig. 4.7. Activation energy (E_A) of the Argon-implanted and control poly-Si TFTs.

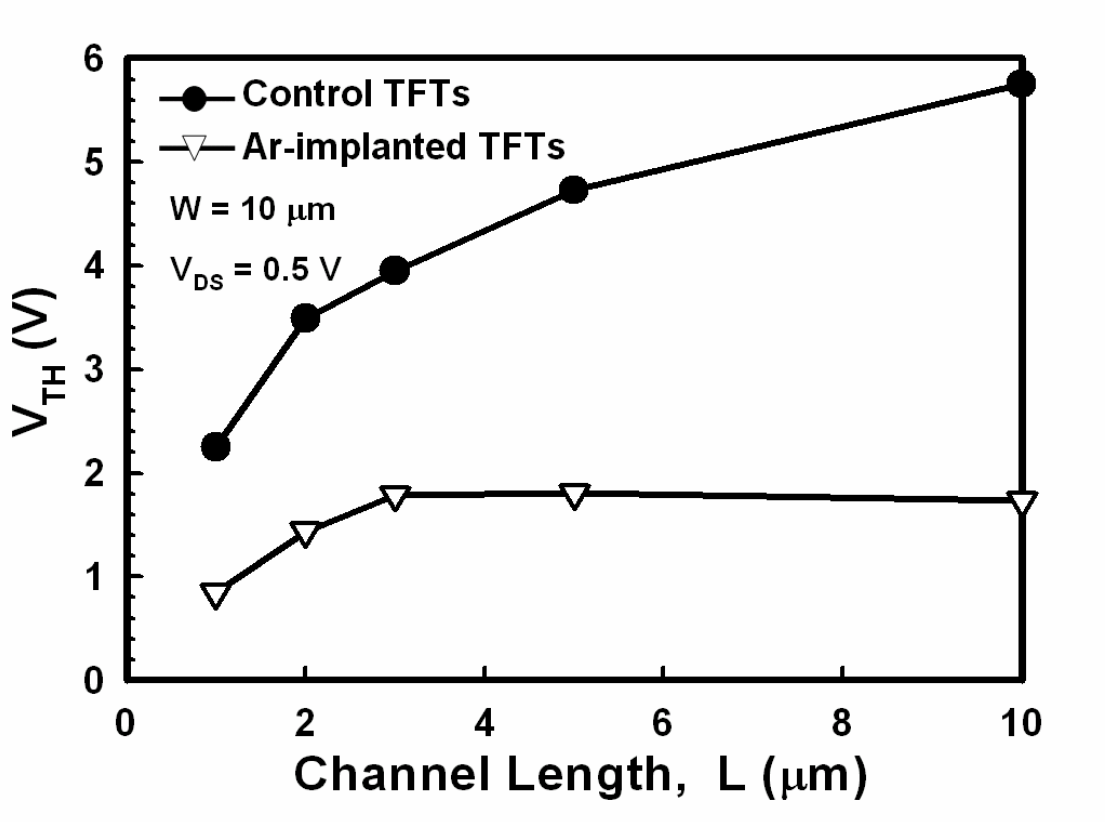


Fig. 4.8. Threshold-voltage rolloff of the Argon-implanted and control poly-Si TFTs at V_{DS} = 0.5 V.

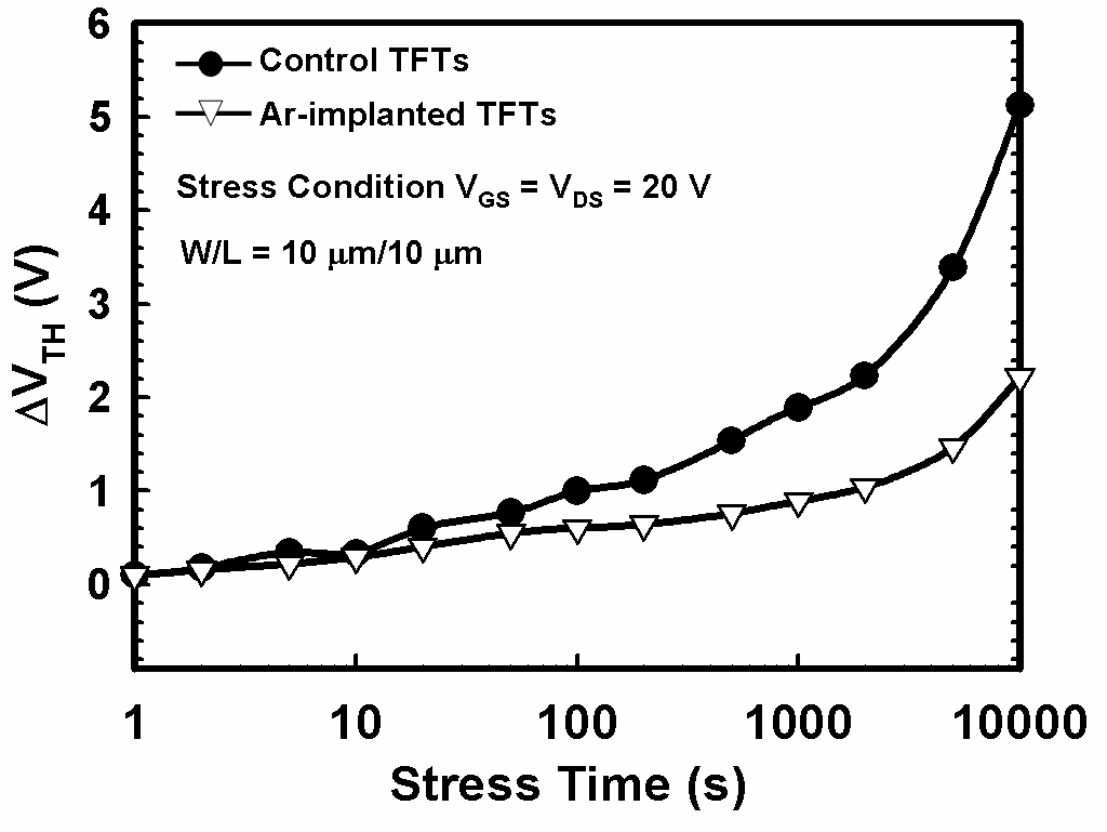


Fig. 4.9. Variation of threshold voltage as a function of stress time for the Argon-implanted and control poly-Si TFTs.

Chapter 5

High-Performance Solid-Phase Crystallized Polycrystalline Silicon Thin-Film Transistors with Floating-Channel Structure

5.1 Introduction

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used for active-matrix liquid crystal displays (AMLCDs). High-performance and superior-reliability poly-Si TFTs have the potential to realize the integration of peripheral driving circuits and pixel switching elements on single glass substrate [5.1], [5.2]. To fabricate poly-Si TFTs on an inexpensive glass substrate, low-temperature technology is required for realizing flat-panel displays (FPDs) owing to the maximum process temperature of being lower than 600 ^{o}C. The solid-phase crystallization (SPC) process is widely used for phase transformation from amorphous to polycrystalline due to its low fabrication cost and good grain-size uniformity. However, the electrical characteristics of SPC poly-Si TFTs are strongly correlated to the microstructure of poly-Si channel film. It is well known that the presence of a large number of grain boundaries and intragranular defects acting as scattering centers and midgap traps in the poly-Si film degrades the electrical properties of poly-Si TFTs [5.3], [5.4]. Therefore, the SPC process plays an important role in determining the device performance. Unfortunately, the traditional SPC process is an interface-nucleation scheme generating too many nucleation sites at the amorphous silicon/underlying oxide (α-Si/SiO_2) interface, resulting in a smaller poly-Si grain size and many grain-boundary

defects [5.5], [5.6]. Various techniques have been employed to improve the device performance either by reducing the trap-state density [5.7], [5.8] or increasing the grain size of SPC poly-Si film [5.9], [5.12]. The hydrogen plasma treatment is widely used to reduce the trap-state density due to the passivation of trap states. Although hydrogen plasma treatment can improve the electrical performances, it is difficult to control the optimal processing time for satisfactory performance improvements. In addition, the hydrogenated poly-Si TFTs also suffer from a serious instability in their electrical characteristics under long-term electrical stress due to the easy breaking of weak Si-H bonds at the grain boundaries [5.13]. Recently, many modified SPC processes associated with surface-nucleation scheme were proposed to improve the microstructure of poly-Si film by utilizing oxygen doping at the α-Si/underlying SiO_2 interface [5.9], [5.11]. It has been known that oxygen atoms retard the crystallization process of an oxygen-implanted α-Si film during solid-phase epitaxial regrowth [5.12]. As interface nucleation is effectively suppressed by the incorporation of oxygen atoms at the α-Si/SiO_2 interface, the nucleation process will initiate at another preferable nucleation site on the top free surface of the α-Si film. Because of fewer nucleation sites at the top free surface of the α-Si film, a larger poly-Si grain size can be obtained. However, these modified surface-nucleation SPC processes mentioned previously require relatively complicated fabrication procedures, and they are not practical for TFT applications.

In this chapter, we take advantage of the modified SPC process with surface-nucleation scheme proposed by Bo et al. [5.14], and then design the self-aligned formation of a floating-channel structure without any additional sacrificial pattern to form the air gap. Experimental results also confirm that the grain size and trap-state density of the poly-Si film with floating-channel structure are markedly improved; moreover, relatively better electrical characteristics are also achieved. Therefore, the proposed fabrication procedure for floating-channel poly-Si TFTs (FC poly-Si TFTs) is very simple and low cost. It is also

reproducible and compatible with existing poly-Si TFT manufacturing processes.

5.2 Experiments

Figs. 5.1(a) and 5.1(g) depict the bird's eye and cross-sectional views of the proposed FC poly-Si TFT, respectively. The schematic diagram of the fabrication processes is illustrated in Figs. 5.1(b)-5.1(g). First, a 150-nm silicon nitride (Si_3N_4) layer, a 20-nm tetraethooxysilane (TEOS) oxide, and a 50-nm α-Si film were successively deposited by low-pressure chemical vapor deposition (LPCVD) to serve as buffered layer, dummy oxide, and channel film [Fig. 5.1(b)], respectively. After individual α-Si active regions were anisotropically patterned and defined, an isotropic wet etching was performed using buffer oxide etchant (BOE) solution with a constituent ratio of HF : NH_4F = 7 : 1 to remove the dummy TEOS oxide to form the floating-channel α-Si region [Fig. 5.1(a) and Fig. 5.1(c)]. The etching rates of BOE for dummy TEOS oxide and α-Si were 15 nm/s and 0.4 nm/min, respectively. Therefore, the dummy TEOS oxide was etched for 90 s to make sure the floating-channel structure could be easily created between the large areas of source/drain pads. Subsequently, the α-Si film with a floating-channel structure was recrystallized at 600 °C for 24 h in N_2 ambient for phase transformation from amorphous to polycrystalline [Fig. 5.1(d)]. After Radio Corporation of America (RCA) cleaning, a 100-nm TEOS oxide and a 150-nm poly-Si film were deposited to serve as the gate dielectric and gate electrode, respectively [Fig. 5.1(e)]. A self-aligned phosphorous ion implantation was performed at dosage and energy values of 5×10^{15} cm^{-2} and 15 keV, respectively [Fig. 5.1(f)]. A 300-nm passivation SiO_2 layer was deposited by plasma-enhanced CVD (PECVD), followed by the realization of dopant activation at 600 °C for 12 h and the definition of contact holes. Finally, a 400 nm Al electrode was deposited and patterned [Fig. 5.1(g)]. An NH_3 plasma treatment was performed at 350 °C for 30 min after the Al electrode formation. For comparison,

conventional poly-Si TFTs (CN poly-Si TFTs) without the removal of dummy TEOS oxide were also fabricated [Fig. 5.1(h)]. Therefore, the distinction between the Si atoms unbounded and bounded to the underlying dummy TEOS oxide could be easily observed for the poly-Si films with floating-channel and conventional structures, respectively.

5.3 Results and Discussion

5.3.1 Material Analyses

A cross-sectional transmission electron microscopy (XTEM) image of the proposed FC poly-Si TFT structure is shown in Fig. 5.2. From the XTEM image, it is clearly observed that the thicknesses of the floating-channel poly-Si film and the air gap are 47 and 20 nm, respectively. Thus, there really exists a floating-channel poly-Si film on the air gap.

SEM images of poly-Si films used in the FC poly-Si TFTs and CN poly-Si TFTs after secco etching are shown in Fig. 5.3(a) and 5.3(b), respectively. These images obviously show that the average grain sizes of poly-Si films for the FC poly-Si TFT and CN poly-Si TFT are approximately 150 and 50 nm, respectively. The result indicates that a better polycrystalline structure with larger grain size and fewer intragranular defects can be obtained in the floating-channel poly-Si film.

5.3.2 Device Characteristics

Fig. 5.4 presents typical transfer characteristics (I_{DS}-V_{GS}) of the FC poly-Si TFTs and CN poly-Si TFTs. The measurements are performed at two different drain voltages of V_{DS} = 0.5 V and 3 V. The drawn channel width (W) and channel length (L) are 1 μm and 10 μm, respectively. The parameters of the devices, including threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), and subthreshold swing (SS), are extracted at V_{DS} = 0.5 V, whereas the maximum on-state driving current (I_{ON}) is defined at V_{DS} = 3 V. The ON/OFF current ratio

(I_{ON}/I_{OFF}) is defined as the ratio of the maximum on-state driving current to the minimum off-state leakage current at V_{DS} = 3 V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of I_{DS} = (W/L)×100 nA at V_{DS} = 0.5 V. The measured and extracted device parameters of the FC poly-Si TFTs and CN poly-Si TFTs are summarized in Table 5.1. Accordingly, the electrical properties of the FC poly-Si TFTs are significantly improved compared with those of the CN poly-Si TFTs. The threshold voltage and subthreshold swing of the FC poly-Si TFTs are 1.62 V and 264 mV/dec, whereas the CN poly-Si TFTs has values of 6 V and 971 mV/dec, respectively. The threshold voltage and subthreshold swing of the FC poly-Si TFTs are found to be superior to those of the CN poly-Si TFTs. Some studies indicated that the Si dangling bonds originating from the deep trap states have energy states near the middle of the Si bandgap, greatly affecting the threshold voltage and subthreshold swing [5.3]. The floating-channel poly-Si film with the surface-nucleation scheme can improve the poly-Si crystallinity with fewer trap states at the grain boundaries. In addition, the maximum on-state driving current and ON/OFF current ratio of the FC poly-Si TFTs are better than those of the CN poly-Si TFTs. The FC poly-Si TFTs exhibit approximately one order of magnitude enhancement in the maximum on-state driving current compared with the CN poly-Si TFTs at V_{GS} = 20 V and V_{DS} = 3 V. Moreover, the ON/OFF current ratio of the FC poly-Si TFTs is about eight times larger than that of the CN poly-Si TFTs. The result suggests that there must be larger poly-Si grains existing in the floating-channel poly-Si film, and thereby the subthreshold and on-state characteristics can be significantly improved.

Fig. 5.4 also shows the field-effect mobility versus gate voltage for the FC and CN poly-Si TFTs. The field-effect mobility is calculated from the transconductance at V_{DS} = 0.5 V. As can be seen, the maximum field-effect mobility of the FC poly-Si TFTs is around three times higher than that of the CN poly-Si TFTs. Note that the strain bonds associated with the tail states near the silicon band edge in the poly-Si film, and at the gate dielectirc/poly-Si

interface greatly affect the field-effect mobility. The improvement on the field-effect mobility could be attributed to the enhancement of grain size and the reduction of grain boundaries, thereby leading to better poly-Si grain crystallinity in the floating-channel poly-Si film.

5.3.3 Trap-State Density and Output Characteristics

To verify the effect of poly-Si grain enhancement, the effective trap-state density (N_{trap}) was extracted from the square root of the slope of $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ plots according to the grain-boundary trapping model proposed by Levinson et al [5.15]. Fig. 5.5 shows the $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ characteristics at V_{DS} = 0.5 V and a high gate voltage for the FC and CN poly-Si TFTs. It can be found that the FC poly-Si TFT exhibits a N_{trap} of 7.1×10^{11} cm^{-2}, whereas the CN poly-Si TFT possesses a N_{trap} of 1.36×10^{12} cm^{-2}. This result further confirms that the floating-channel poly-Si film has much fewer grain boundaries and microstructure defects than the conventional poly-Si film due to the enlarged grain size.

Fig. 5.6 shows the output characteristics (I_{DS}-V_{DS}) of the FC and CN poly-Si TFTs. As can be seen, the FC poly-Si TFT exhibits a great enhancement in the driving current at V_{DS} = 10 V and common gate driving voltages of $V_{GS}-V_{TH}$ = 3, 6, 9, and 12 V. The improvement can be attributed to the field-effect mobility and threshold voltage of the FC poly-Si TFTs being higher and lower than those of the CN poly-Si TFTs.

5.3.4 Interface Nucleation v.s. Surface Nucleation

These electrical performance improvements strongly related to the crystallinity of poly-Si film could be qualitatively explained as follows. While using the traditional SPC process with interface-nucleation scheme to crystallize α-Si into poly-Si, the rearrangement of interfacial Si atoms and volume contraction of bulk Si film induce tensile stress at the

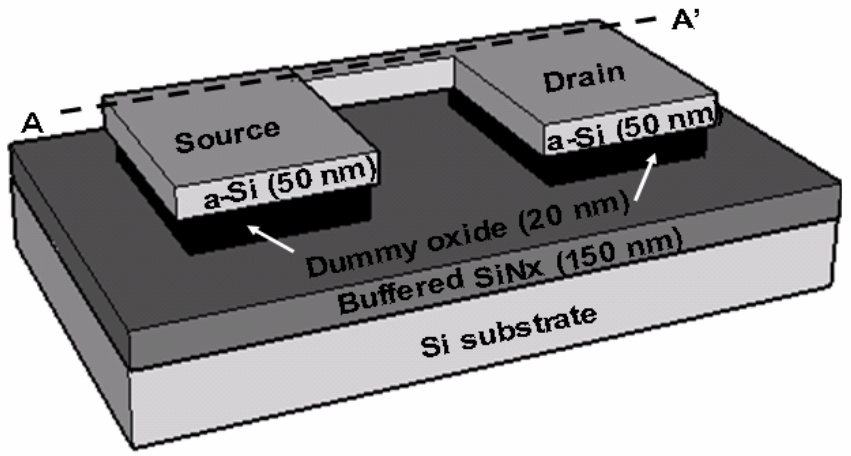
α-Si film/underlying SiO_2 interface. Hence, a large number of crystalline defects, such as microtwins and dislocations, are generated to relieve the tensile stress. Following, numerous nucleation sites could be produced to result in smaller poly-Si grain size [5.11], [5.14]. Nevertheless, in the case of poly-Si film with a floating-channel structure in this work, the removal of underlying dummy TEOS oxide makes the Si atoms barely bound. As a result, the stress formed during the crystallization process could be easily relieved from the free Si surface pursing for fewer nucleation sites, thereby yielding good-quality poly-Si film with lower trap-state density and larger poly-Si grain size.

5.3.5 Device Reliability

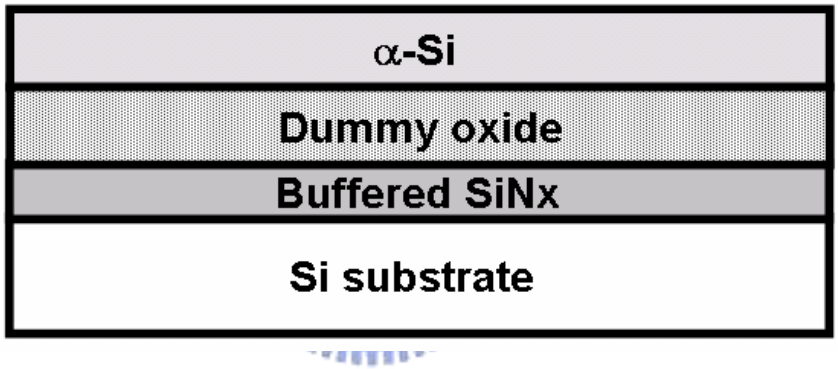
Additionally, hot-carrier stress analysis was applied to investigate the device reliability. The poly-Si TFT devices were bias-stressed at V_{DS} = 20 V and V_{GS} = 20 V for 10^4 s to examine the hot-carrier stress immunity. The threshold-voltage shifts over hot-carrier stressing time for the FC and CN poly-Si TFTs are shown in Fig. 5.7. Hot-carrier multiplication occurring on the drain side of poly-Si TFTs causes the degradation of threshold voltage. The poly-Si TFT with a floating-channel structure shows less degradation in threshold voltage. Notably, the threshold-voltage shift of the FC poly-Si TFTs after a stress time of 10^4 s is found to be 3 V, which is superior to that of the CN poly-Si TFTs (5.4 V). It has been reported that the degradations of threshold voltage caused by hot-carrier stress could be attributed to two reasons: the generation of interface states at the gate dielectric/poly-Si interface and the formation of deep trap states originating from the broken of weak Si-H bonds at the grain boundaries [5.13]. The result indicates that the poly-Si film with floating-channel structure crystallized by SPC process demonstrates a good-quality poly-Si film with larger grain size and fewer grain boundaries, resulting in better hot-carrier endurances.

5.4 Summary

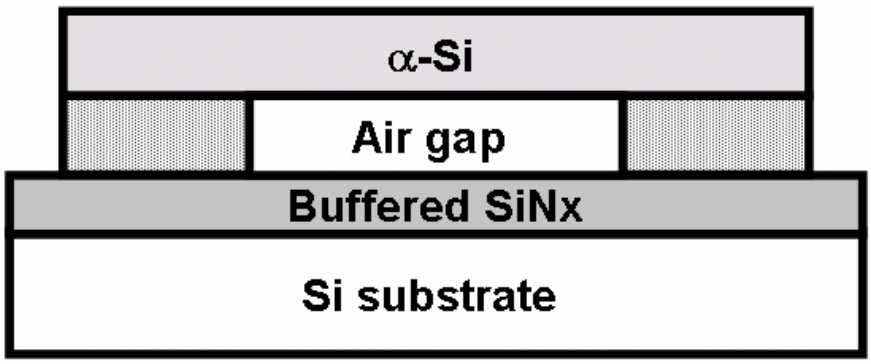
In this study, we have demonstrated that the α-Si film with floating-channel structure crystallized by SPC process exhibits a better crystallinity of poly-Si film with larger grain size and fewer microstructural defects. Poly-Si TFTs with the self-aligned formation of the floating-channel active region is firstly proposed. The electrical characteristics of the FC poly-Si TFTs, including threshold voltage, subthreshold swing, field-effect mobility, ON/OFF current ratio, and hot-carrier immunity are significantly improved. Therefore, the proposed FC poly-Si TFTs are not only compatible with existing manufacturing processes but also possess superior electrical properties for large flat-panel display applications.



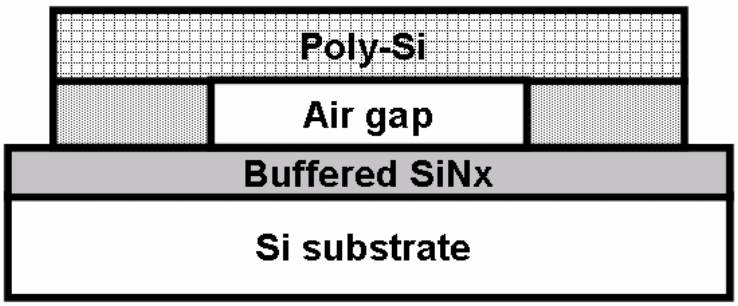
(a) Bird's eye view of the FC poly-Si TFTs



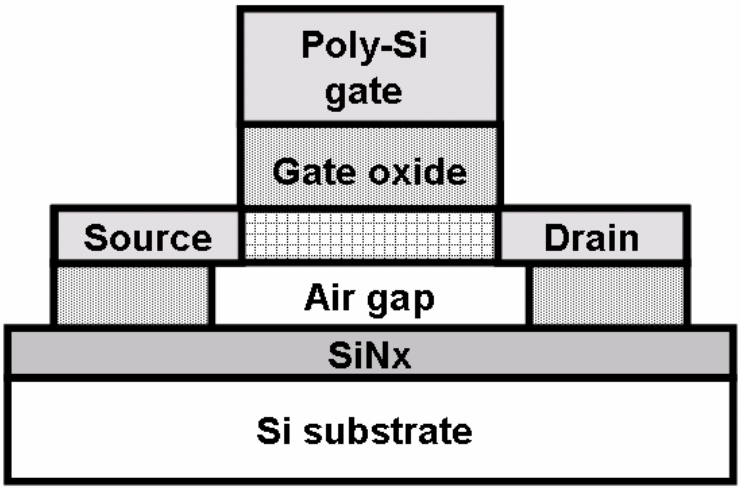
(b) Buffered SiNx, dummy oxide, and α-Si deposition.



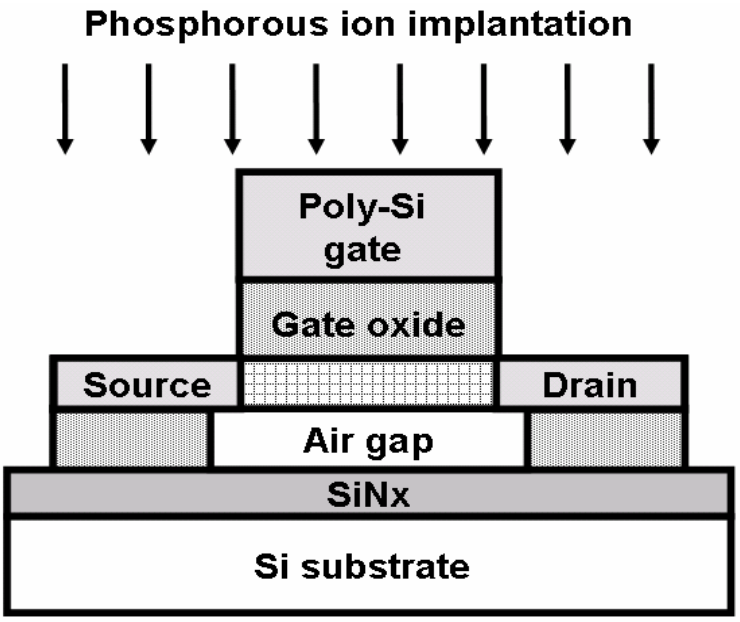
(c) Definition of active region, anisotropic dry etching of α-Si, and isotropic wet etching of dummy oxide to form floating-channel α-Si structure.



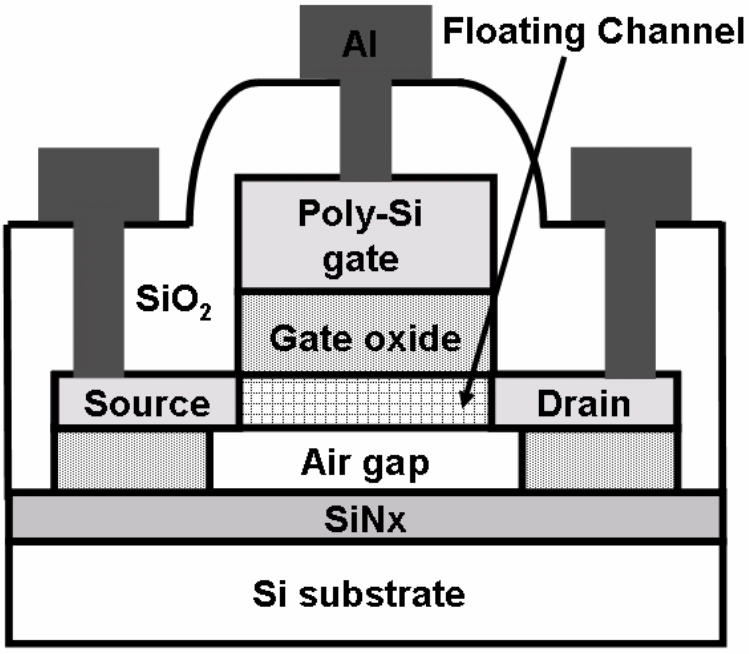
(d) Solid-phase crystallization of α-Si, and then form floating-channel poly-Si.



(e) Gate oxide and poly-Si gate deposition, and patterning of gate electrode.

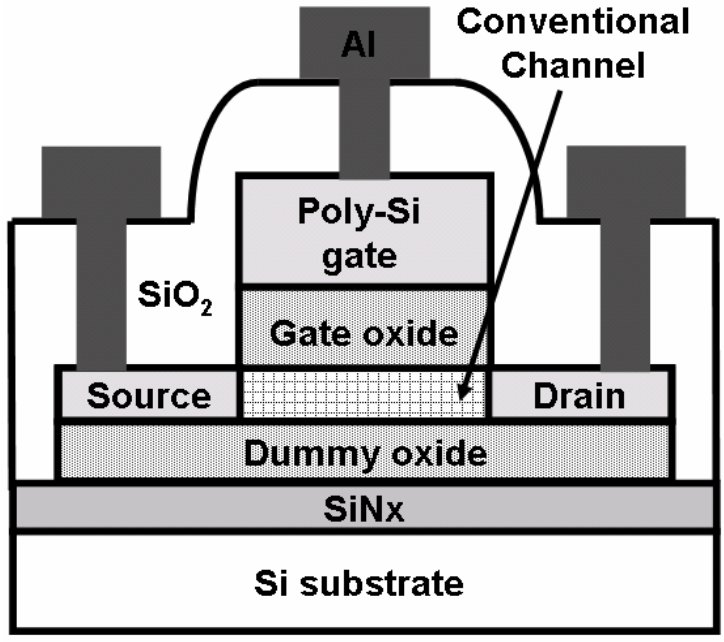


(f) Self-aligned phosphorous ion implantation, and dopant activation.



(g) Passivation oxide deposition, patterning of contact hole, and formation of metal pad.

(Cross-sectional view of the FC poly-Si TFTs)



(h) Cross-sectional view of the CN poly-Si TFTs.

Fig. 5.1 Schematic diagram of the fabrication processes of the poly-Si TFTs with floating-channel structure.

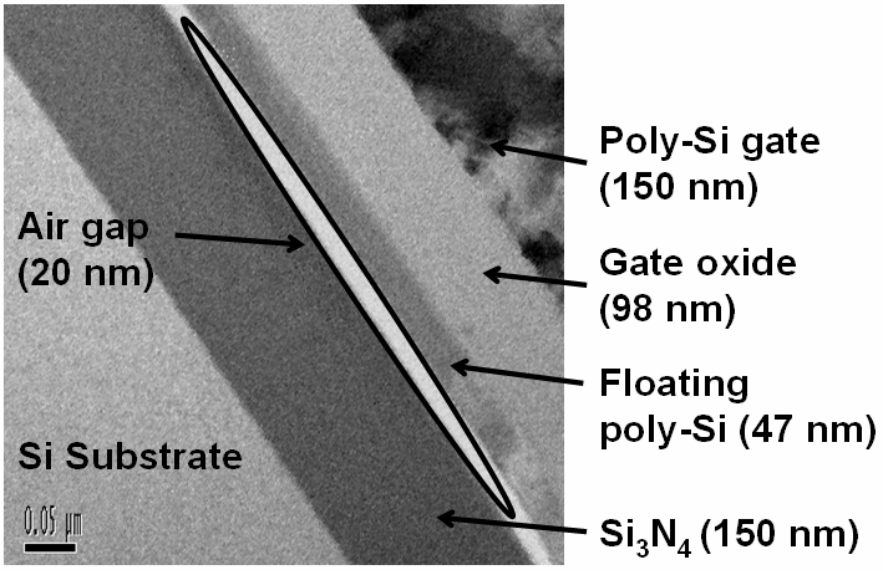
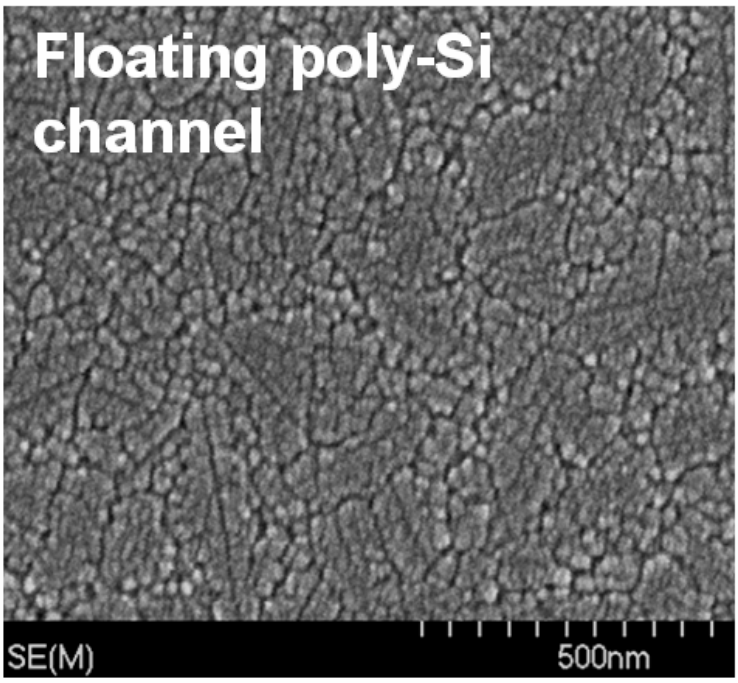
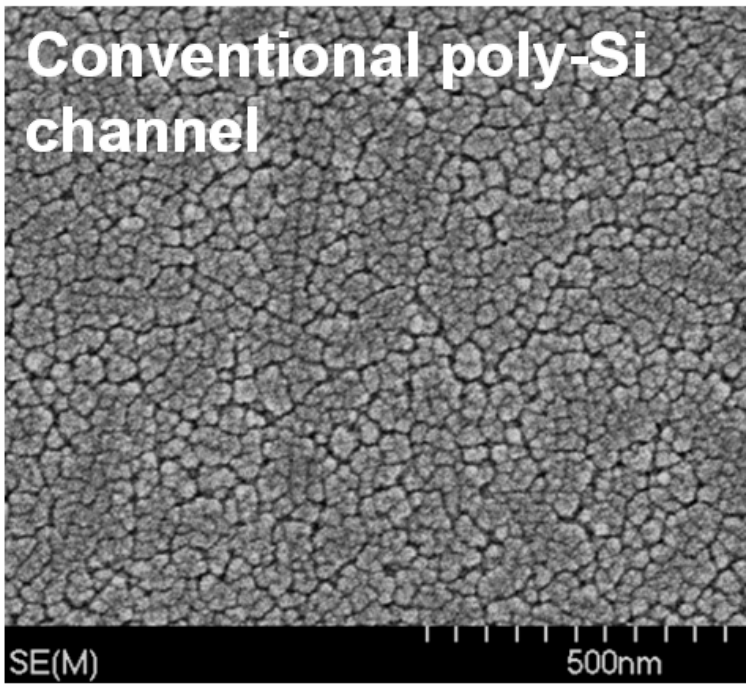


Fig. 5.2 Cross-sectional TEM image of the FC poly-Si TFTs.



(a) SEM image of the floating-channel poly-Si film.



(b) SEM image of the conventional poly-Si film.

Fig. 5.3 SEM images of the secco-etched poly-Si films with and without floating-channel structure after SPC process.

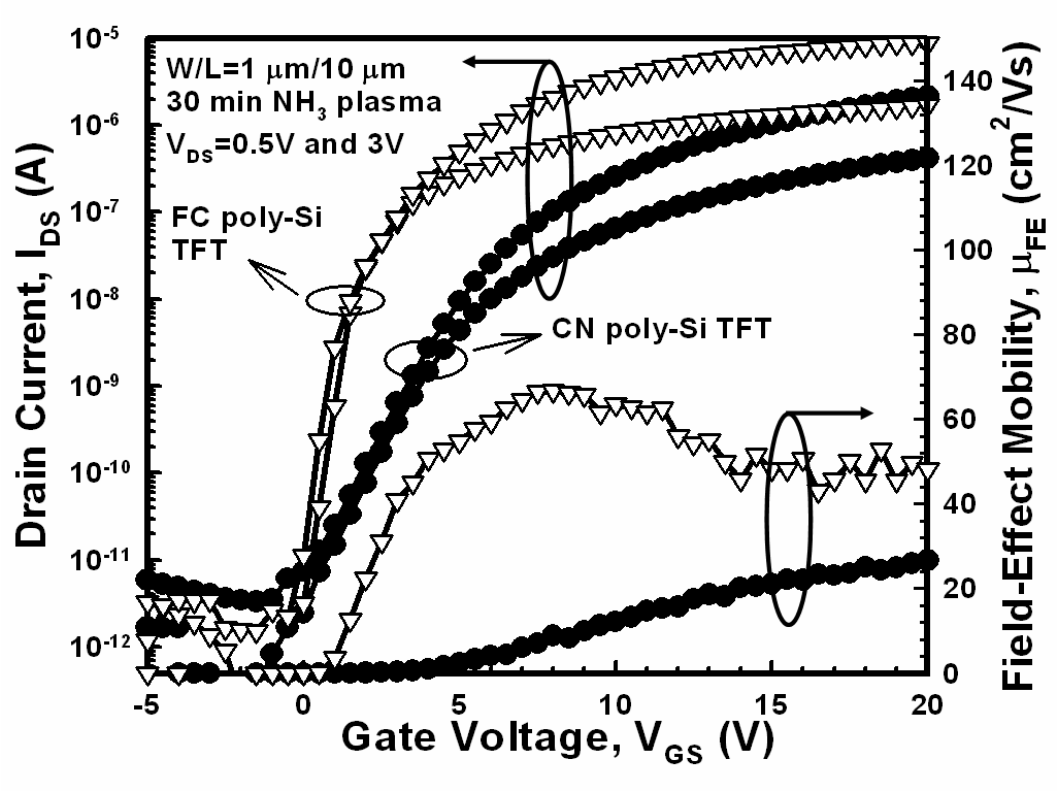


Fig. 5.4 Typical transfer characteristics and the extracted field-effect mobility for the FC and CN poly-Si TFTs with a dimension of W/L = 1 μm/10 μm.

Table 5.1 Comparison of device characteristics for the FC and CN poly-Si TFTs with a dimension of W/L = 1 μm/10 μm.

	FC poly-Si TFT	CN poly-Si TFT
Threshold voltage (V)	1.62	6
Subthreshold swing (mV/dec)	264	971
Field-effect mobility ($cm^2V^{-1}s^{-1}$)	66.9	21.1
Maximum on-state current (A)	8.9×10^{-6}	1.5×10^{-6}
ON/OFF current ratio	5.8×10^{6}	6.8×10^{5}

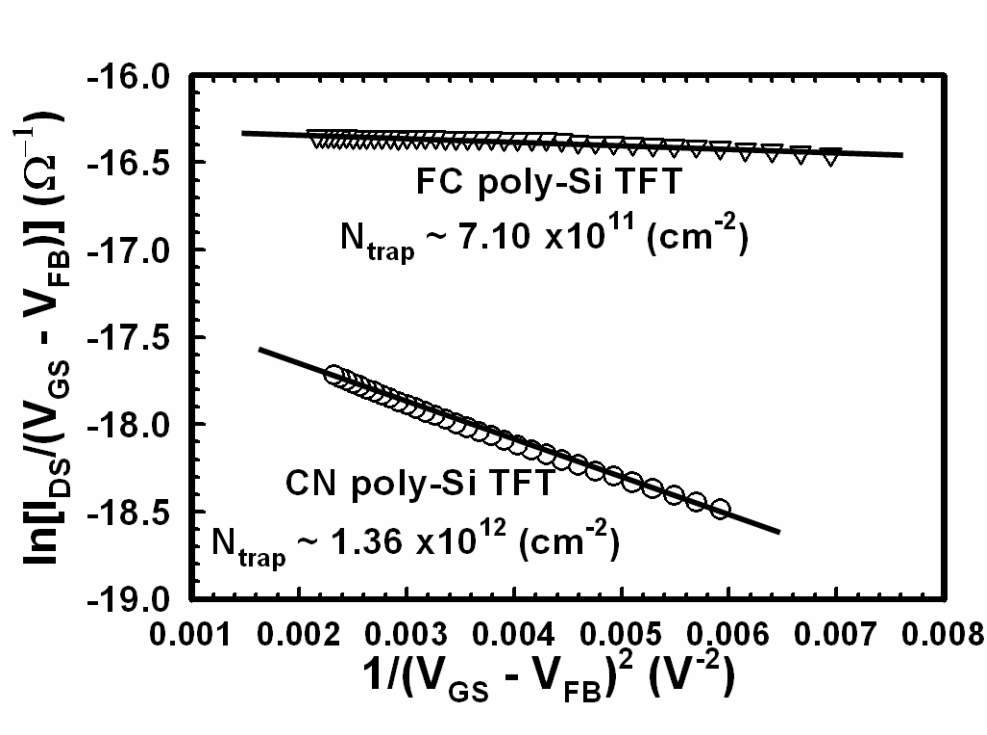


Fig. 5.5 Plot of $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ and the extracted trap-state density (N_{trap}) for the FC and CN poly-Si TFTs. I_{DS} was measured at $V_{DS} = 0.5$ V.

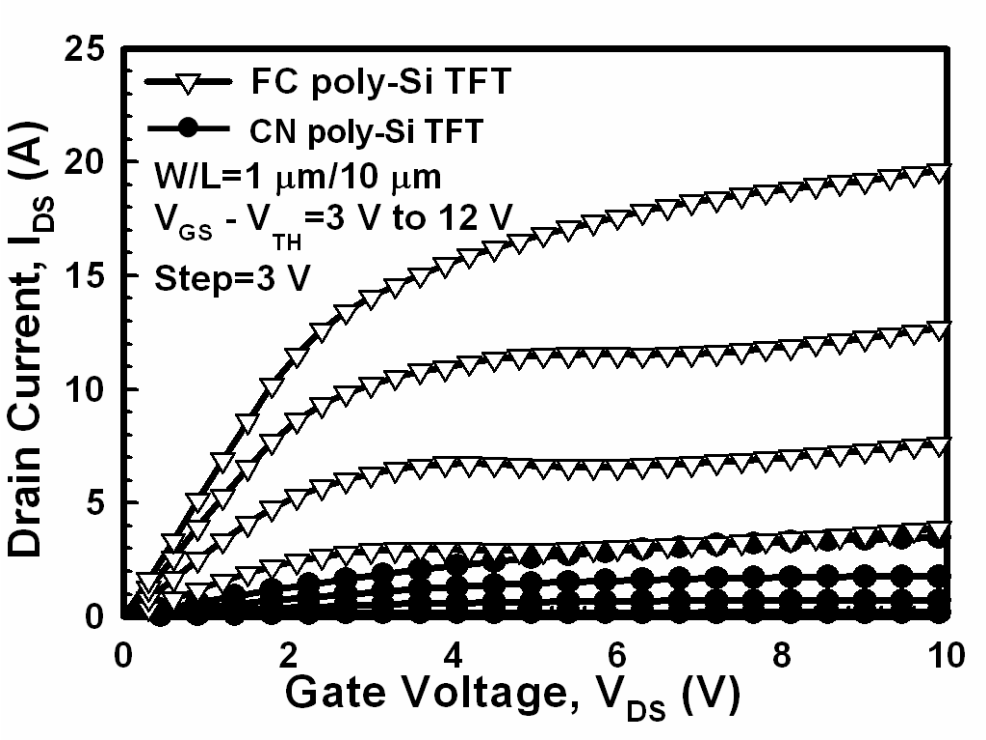


Fig. 5.6 Output characteristics of the FC and CN poly-Si TFTs with a dimension of W/L = 1 μm/10 μm.

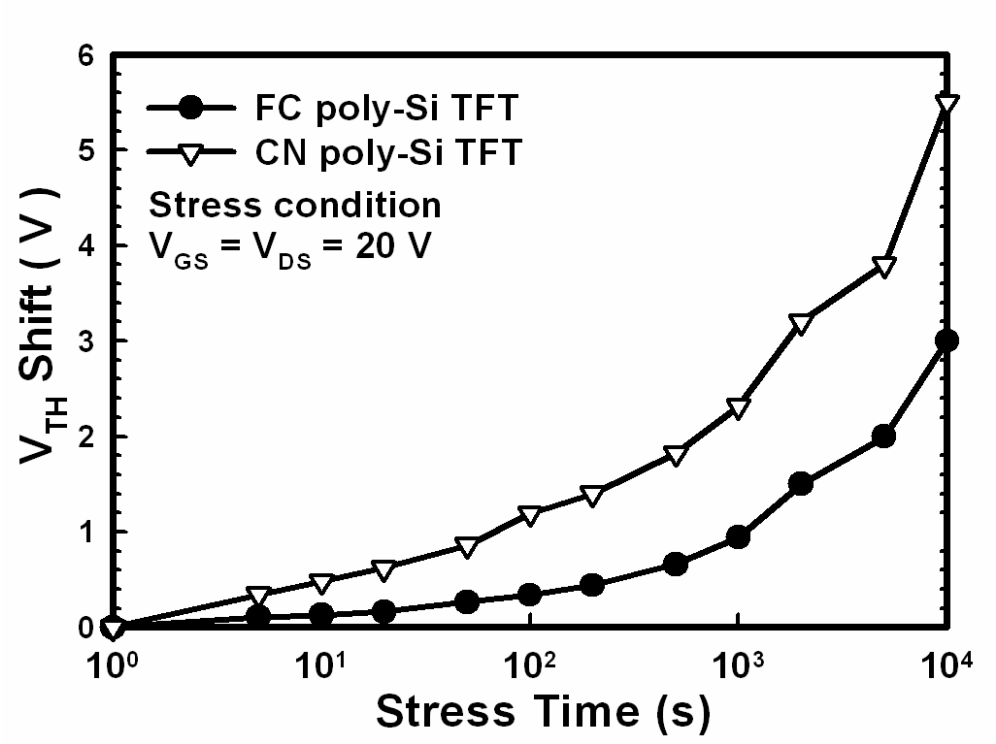


Fig. 5.7 Threshold-voltage shift versus hot-carrier stress time for the FC and CN poly-Si TFTs.

Chapter 6

Polycrystalline Silicon Thin-Film Transistors with Nanowire Channel Fabricated by Sidewall Spacer Technique

6.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much considerable attention because they could be integrated with peripheral driving circuits and pixel switching elements on a low-cost glass substrate for active-matrix liquid-crystal display (AMLCD) applications [6.1], [6.2]. Also, poly-Si TFTs have the potential to be used in three-dimensional (3-D) circuits, including vertically integrated SRAMs [6.3] and DRAMs [6.4]. To improve the performances of poly-Si TFTs, several advanced crystallization techniques such as excimer-laser crystallization (ELC) [6.5] and metal-induced lateral crystallization (MILC) [6.6]-[6.8] have been developed to produce high-quality poly-Si film with large grain size and low microstructural defect density. However, the most widely used ELC technique still has many issues to be addressed for further developments. MILC technique is a low-cost batch process and also attractive for obtaining needlelike poly-Si grain with grain boundary parallel to the crystallization direction. Though considerable grain length can be obtained by MILC, the grain width achieved is still smaller than the device channel width, which can't realize poly-Si TFTs with nearly single-grain active channel.

Recently, a lot of efforts have been put forth to enhance the gate controllability over the poly-Si channel by changing the device structures of poly-Si TFTs. Several device structures such as gate-overlapped lightly doped drain (GO-LDD) [6.9], double gate [6.10], and gate all

around [6.11] have been proposed to improve the device performances. However, these proposed device structures involve much more complicated fabrication steps, and are not practicable for poly-Si TFT manufacturing. Moreover, poly-Si TFTs with nano-scale feature sizes have also been proposed to reduce the influence of grain-boundary defects [6.12]-[6.16]. In these studies, the electrical performances of poly-Si TFTs could be remarkably improved by decreasing the channel dimensions to be comparable to, or still smaller than, the poly-Si grain size. However, the poly-Si TFTs with narrow-width channels directly defined using costly electron-beam lithography (EBL) technology could not be practicable in flat-panel displays (FPDs) [6.12]-[6.14]. On the other hand, for the poly-Si TFTs with nanowire (NW) channels and multiple-gate configuration reported in [6.15], [6.16], a undersiable gate-induced drain leakage (GIDL) current resulted from large gate-to-drain overlapping area is found and must be addressed by additional processes. Furthermore, in order to form tri-gate structure with NW channels, the extra top metal gate and bottom Si-substrate gate accompanied with high-temperature thermal oxide and rapid thermal processing are used [6.14], [6.15], which are difficult to process in LCD production line.

In this chapter, we propose a simple sidewall spacer technique to form self-aligned twin poly-Si NW, directly served as the channel regions of poly-Si TFTs, without any expensive photolithograpy process. Poly-Si TFTs with nanowire channels are crystallized by traditional solid-phase crystallization and advanced metal-induced lateral crystallization techniques. All processes are compatible with modern LCD production line, and suitable for system-on-panel (SOP) applications in the future.

6.2 Experiments

The key fabrication steps and the schematic top view of the proposed poly-Si NW TFTs are shown in Figs. 6.1(a)-(g) and (h), respectively. Firstly, a 150-nm SiN_X and a 100-nm

tetraethooxysilane (TEOS) SiO_X were deposited by plasma-enhanced chemical vapor deposition (PECVD) system to serve as the starting substrate and the dummy oxide layer, respectively [Fig. 6.1(a)]. After patterning and etching to be the dummy oxide stripe, a 100-nm amorphous silicon (α-Si) layer was conformally deposited by low-pressure CVD (LPCVD) at 550 °C [Fig. 6.1(b)], and then anisotropically etched to form square-coil α-Si sidewall spacer in a self-aligned manner [Fig. 6.1(c)]. The feature size of the α-Si spacer could be well controlled by turning dry etching condition and readily shrunk into nanoscale dimension without advanced photolithography technology. The α-Si sidewall spacer was then crystallized by traditional solid-phase crystallization technique at 600 °C for 24 h in N_2 ambient to transform amorphous into polycrystalline. At the same time, to investigate the effect of metal-induced lateral crystallization technique on the proposed poly-Si NW TFT, a 200-nm low-temperature oxide (LTO) was deposited and patterned to expose the MILC window [Fig. 6.1(d)]. A 10-nm nickel (Ni) layer was deposited, and lateral crystallization was subsequently carried out at 550 °C for 24 h in N_2 ambient. After the MILC process, the remaining Ni and LTO as well as dummy oxide stripe were etched away by hot sulfuric acid and hydrofluoric acid, respectively, and then the square-coil poly-Si NW was reserved [Fig. 6.1(e)]. Then, a 33-nm TEOS gate oxide and a 250-nm n^+ poly-Si were deposited and patterned to form the gate electrode [Fig. 6.1(f)]. Next, a self-aligned phosphorus ion implantation was performed at 15 keV to a dose of 5×10^{15} cm^{-2} to dope the source/drain regions, followed by the dopant activation at 600 °C for 12 h in N_2 ambient. Finally, typical passivation layer deposition, contact hole opening, and metal pad formation completed the device fabrication [Fig. 6.1(g)].

6.3 Results and Discussion

6.3.1 Material Analyses

Fig. 6.2 (a) shows the cross-sectional transmission electron microscopy (XTEM) image of the proposed poly-Si NW TFTs having a couple of NW channels. Here, such test structure with small dimension of 300-nm distance is used to make the illustration more clear. The fractional enlarging plot of poly-Si NW channel is shown in Fig. 6.2(b). Because the poly gate electrode pattern is perpendicularly across the poly-Si NW channels, a couple of active NW channels would be formed after removing the dummy oxide stripe in the proposed poly-Si NW TFTs. From the cross-sectional TEM image, the vertical sidewall thickness (T_{Si}) and horizontal width (W_{Si}) are approximately 50 nm. The aspect ratio T_{Si}/W_{Si} of the active NW channel in the poly-Si NW TFTs (approximately equals to one) is larger than that of large-width channel in the standard planar poly-Si TFTs (much smaller than one). Such high aspect ratio means that the gate electrode forms in a tri-gate-like structure with well electrostatic controllability on channel potential due to sidewall and corner contribution effects [6.17], [6.18].

6.3.2 Device Characteristics of SPC NW TFTs

Typical transfer characteristics (I_{DS}-V_{GS}) of the SPC poly-Si NW TFTs with and without 1-hr NH_3 plasma treatment are compared and shown in Fig. 6.3. The effective channel width of the poly-Si NW TFTs is defined as the twice horizontal width ($2\times W_{Si}$) of 100 nm parallel on starting substrate, which is the same definition in other reports on TFT field [6.12]-[6.14]. The ON/OFF current (I_{ON}/I_{OFF}) ratio is the ratio of the maximum on-state current to the minimum off-state current at V_{DS} = 0.5 V. The threshold voltage (V_{TH}) is defined as the gate voltage required to achieve a normalized drain current of I_{DS} = (W/L)×100 nA at V_{DS} = 0.5 V. The threshold voltage (V_{TH}), subthreshold swing (S.S.), field-effect mobility, and ON/OFF current ratio are summarized in Table 6.1. After NH_3 plasma treatment for 1 hr, the threshold voltage is scaled down from 2.2 V to 0.3 V, the field-effective mobility (μ_{FE}) can be improved from 46.7 cm^2/V-s to 63.5 cm^2/V-s, the

subthreshold swing (S. S.) is also decreased from 570 mV/dec to 170 mV/dec, and the ON/OFF current ratio could be increased one order magnitude. In addition, the gate-induced drain leakage (GIDL) current could be suppressed near half order magnitude at V_{DS} = 3 V and V_{GS} = –4 V.

6.3.3 Standard TFTs v.s. NW TFTs

Fig. 6.4 shows the normalized I_{DS}-V_{GS} curves of the standard planar poly-Si TFTs and the proposed poly-Si NW TFTs with 1-hr NH_3 plasma treatment. The electrical performances of the poly-Si NW TFTs are superior to those of the standard planar poly-Si TFTs, including higher on-state current, lower threshold voltage, and steeper subthreshold swing. The enhancement on the on-state current for the poly-Si NW TFTs can be ascribed to the fact that the inversion layer at the triangle-like corner region turns on earlier than that on the channel surface due to the stronger fringing electric field. Hence, additional current contributed from the triangle-like corner region results in the increase of the on-state current. The performance enhancements of the poly-Si NW TFTs are due to the increased effective channel width and the better gate controllability over the channel potential by the tri-gate-like structure.

6.3.4 Hydrogenation Effect

Besides excellent gate controllability due to the 3-D tri-gate-like feature, the effect of grain boundaries in poly-Si NW film also plays an important role. As the poly-Si TFTs are scaled down, the number of grain boundaries is decreased to dominate on the threshold voltage decreasing [6.19], [6.20]. So, in the poly-Si NW channel, the fewer grain boundaries make lower threshold voltage for ploy-Si TFTs, which obtains higher driving current under the same operational condition. On the other hand, according to the poly-Si model [6.21], the effective field-effect mobility (μ_{EF}) could be given as Eq. (6.1):

$$\mu_{EF} = \frac{1}{1+(\mu_G/\mu_{GB})[nL_{GB}/L]\exp[qV_b/kT]} \quad \text{.....Eq. (6.1)}$$

where μ_{EF} is the effective field-effect mobility, L_{GB} is the average grain-boundary length, $n = L/L_{GB}$ is the average grain boundary number, and L_{GB} is the average intragrain length. If the active channel is shrunk down to nano-scale dimension, the n value would be decreased to increase the value of μ_{EF} [6.19], [6.21]. Finally, fewer grain boundaries in poly-Si NW channels also make effectively passivated deep trap states by NH_3 plasma treatments. Therefore, the high-performance poly-Si NW TFT with NH_3 plasma treatment could be achieved by utilizing a simple spacer formation technology and suitable for LCD practical manufacturing.

6.3.5 SPC NW TFTs v.s. MILC NW TFTs

Fig. 6.5 shows the transfer characteristics of the proposed poly-Si TFTs with NW channels crystallized by MILC and SPC techniques at V_{DS} = 0.5 V and 3 V. The TFT device composed from a couple of NW channels has a nominal channel length (L) of 1 μm and an effective channel width (W) of 100 nm ($2\times W_{Si}$). The threshold voltage (V_{TH}), subthreshold swing (S.S.), and field-effect mobility are extracted at V_{DS} = 0.5 V, whereas the maximum off-state gate-induced drain leakage (GIDL) current ($I_{GIDL,\ max}$) and on/off current ratio (I_{on}/I_{off}) are extracted at V_{DS} = 3 V. The key device parameters are summarized in Table 6.2. Accordingly, the threshold voltage and the subthreshold swing of the MILC NW TFTs are 0.1 V and 199 mV/dec., respectively, which are superior to 2.7 V and 594 mV/dec. of the SPC NW TFTs. Notably, the maximum GIDL current of the MILC NW TFTs is more than one order in magnitude lower than that of the SPC NW TFTs. The on/off current ratio of the MILC NW TFTs (4.7×10^7) is much higher than that of the SPC NW TFTs (3.2×10^6). Additionally, compared to the SPC NW TFT, the MILC NW TFT has an obvious enhancement in the maximum field-effect mobility from 42 to 156 cm^2/V-s. It should be

noted that the major performance improvements in the MILC NW TFTs are due to the alignment of poly-Si grains in a direction parallel to the current flows. Also, the growth of poly-Si grains perpendicular to the channel direction is effectively limited by the nano-scale channel width of 50 nm. Therefore, the effects of parallel grain boundaries could be relieved by decreasing the channel width to be comparable to, or even smaller than the poly-Si grain size. However, the grain boundaries are still randomly oriented in the SPC NW TFTs.

6.3.5 Trap-State Density

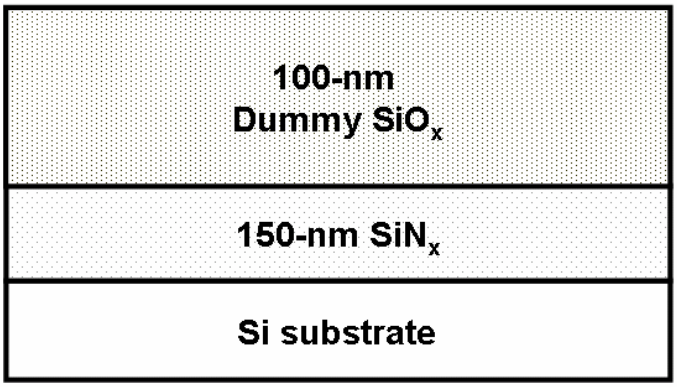
In order to verify the reduction of grain-boundary defects in the MILC poly-Si NW channel, the effective trap-state density (N_{trap}) was calculated from the square root of the slope of $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ plot, which was proposed by Proano et al. [6.22], as shown in Fig. 6.6. It is observed that the MILC poly-Si NW TFT shows much reduced effective trap-state density from 1.13×10^{13} to 5.67×10^{12} cm^{-2}, as compared to the SPC poly-Si NW TFT. This figure strongly implies that the MILC technique can obtain a good-quality poly-Si film with larger grain size and fewer microstructural defects.

6.3.6 Threshold-Voltage Rolloff

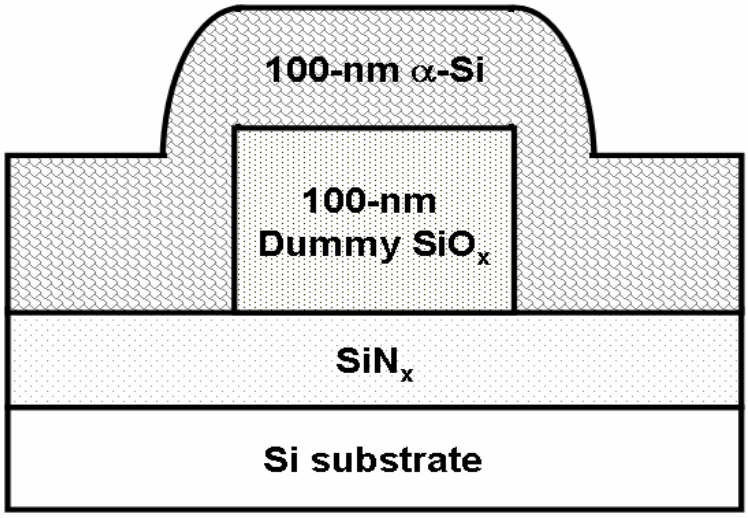
Additionally, to examine the grain crystallinity of the poly-Si NW channels with different crystallization techniques, the threshold-voltage rolloff properties of the MILC NW TFTs and the SPC NW TFTs are compared in Fig. 6.7. Apparently, the SPC NW TFT exhibits a serious threshold-voltage rolloff property, which is dominated by the decreasing of randomly distributed grain boundaries contained in the channel [6.23]. But a much more improved scaling characteristic is observed in the MILC NW TFTs, which could be ascribed to the fabrication of entire device on a nearly single-crystalline grain; therefore, compared to the SPC NW TFTs, the MILC NW TFTs could not only relieve the effects of grain boundaries but also achieve a lower threshold voltage.

6.4 Summary

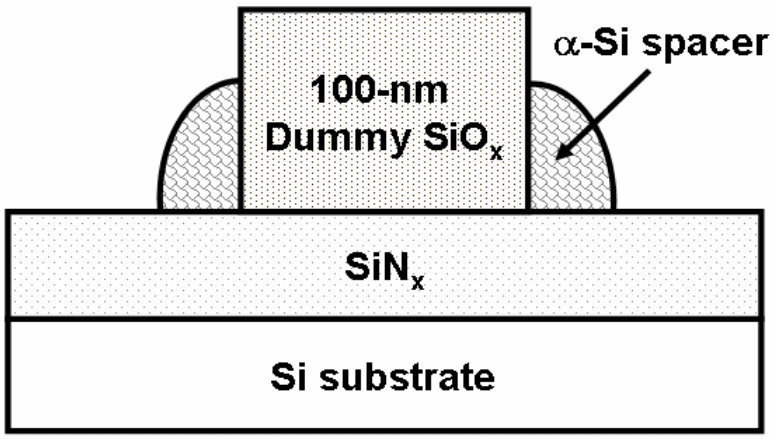
We have demonstrated a simple, low cost, and self-aligned sidewall spacer technique to fabricate the poly-Si TFTs with NW channels crystallized by solid-phase crystallization and metal-induced lateral crystallization techniques. The 50-nm NW channel could be easily realized by anisotropically etched without extra mask or advanced photolithography system. The proposed SPC poly-Si NW TFT has excellent gate controllability due to the tri-gate-like structure with the sidewall and corner contribution effects. Also, for the poly-Si NW channels, effectively passivated deep trap states by NH_3 plasma treatment also improve the electrical characteristics of poly-Si TFTs. On the other hand, the MILC poly-Si NW TFT not only depicts improved turn-on characteristics by forming superior grain crystallinity of poly-Si films but also maintains a low off-state leakage current by reducing the microstructural defects. Moreover, superior short-channel characteristics are also achieved, which might be explained by the formation of single-crystalline grain in the entire channel region. Therefore, the MILC poly-Si NW TFTs could be a promising candidate for AMLCD applications.



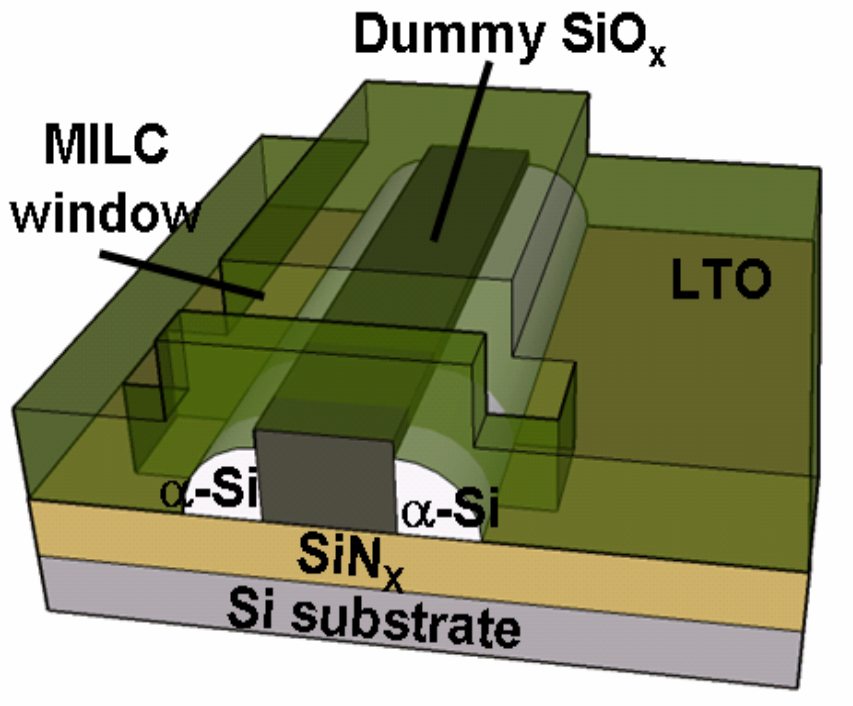
(a) 150-nm SiNx, and 100-nm dummy SiOx deposition.



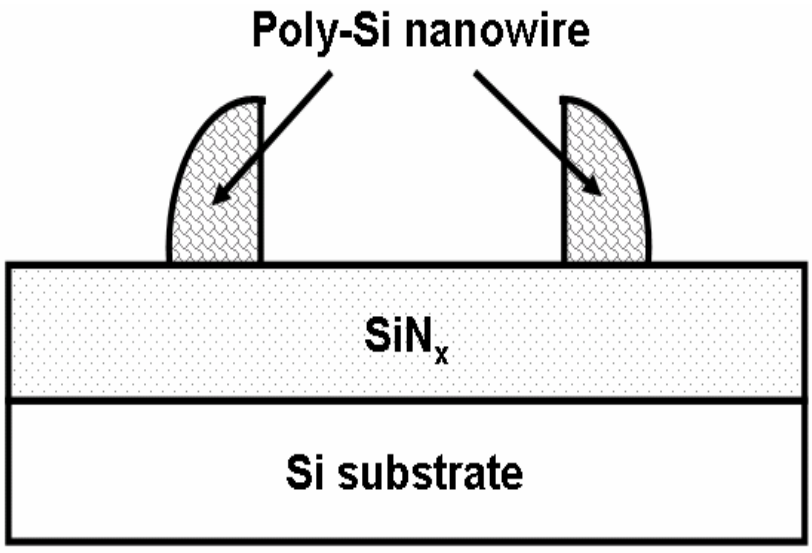
(b) Patterning of dummy SiOx stripe, and then 100-nm α-Si deposition.



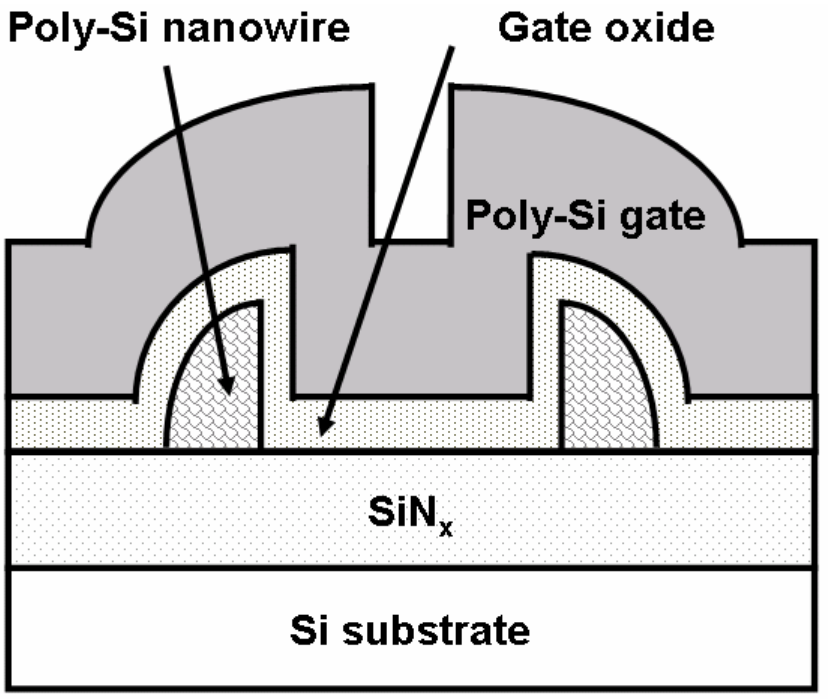
(c) Anisotropically dry etching of α-Si to form α-Si sidewall spacer.



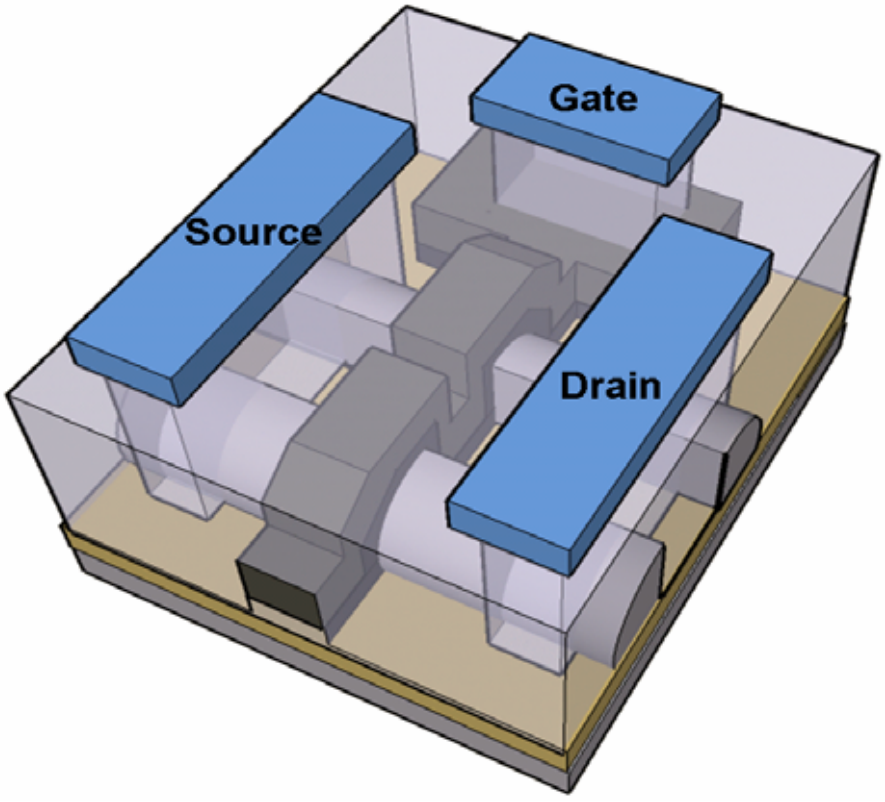
(d) Low-temperature oxide deposition, patterning of MILC window, seeded Ni deposition, and realization of metal-induced lateral crystallization process.



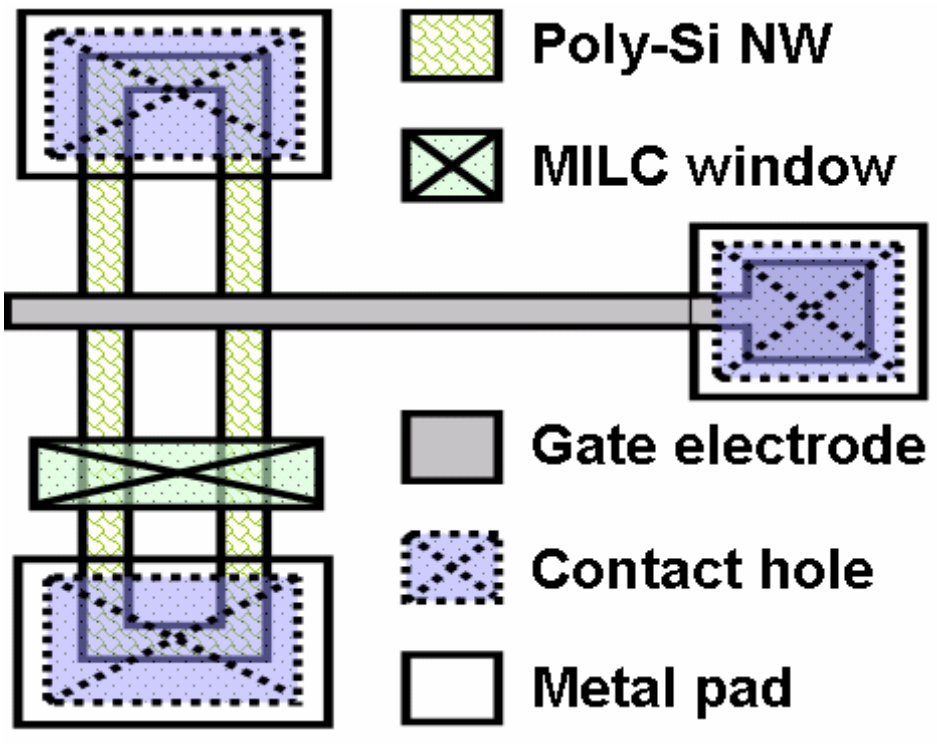
(e) Removal of unreacted Ni and LTO as well as dummy SiOx stripe to from twin poly-Si nanowire.



(f) Gate oxide and poly-Si gate deposition

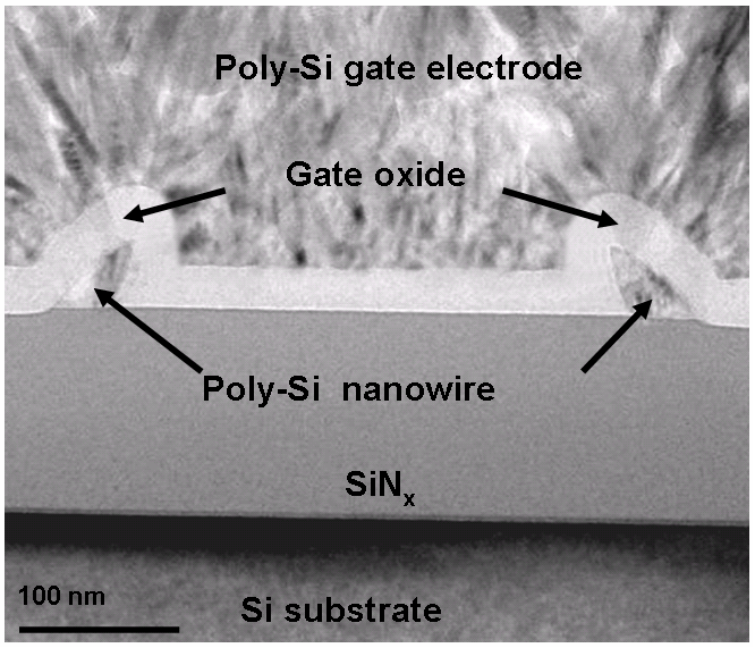


(g) Bird's eye view of the final device structure.

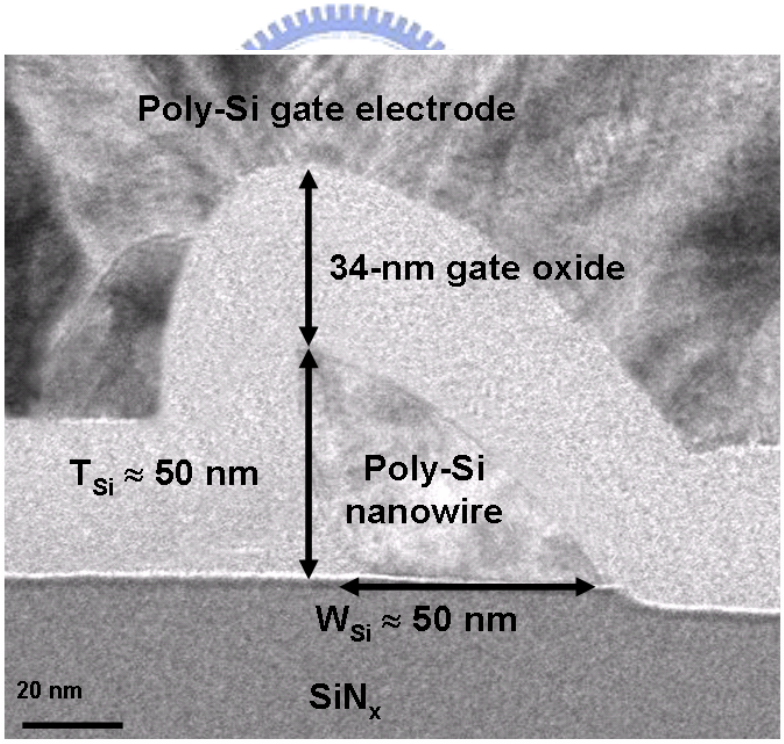


(h) The schematic layout of the MILC poly-Si NW TFTs.

Fig. 6.1. Schematic diagrams of the key fabrication steps of the SPC and MILC poly-Si NW TFTs.



(a) The cross-sectional TEM image of the poly-Si NW TFTs.



(b) The fractional enlarging plot in (a)

Fig. 6.2. The cross-sectional TEM image of the poly-Si NW TFTs having a couple of NW channels.

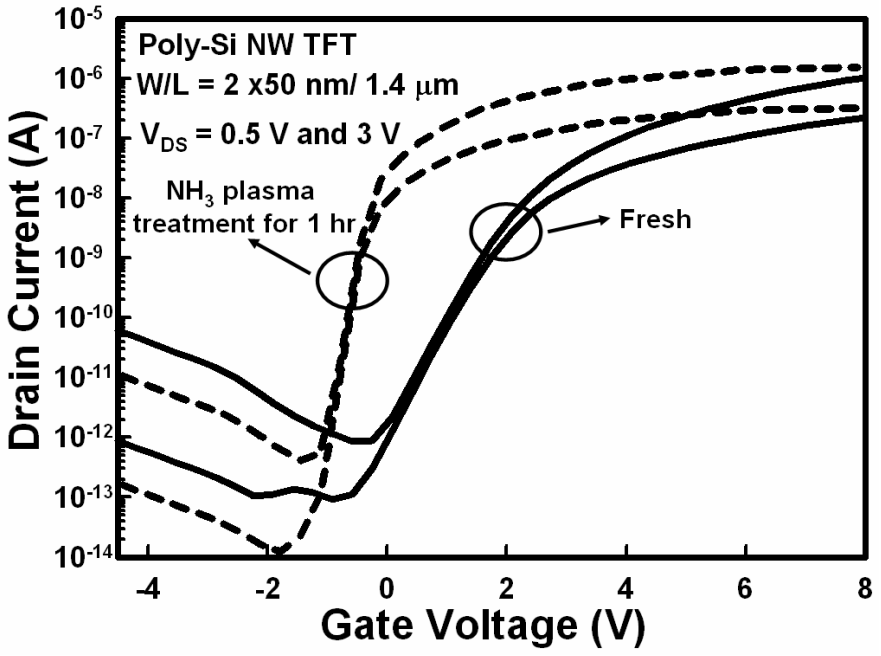


Fig. 6.3. Typical transfer characteristics of the SPC poly-Si NW TFTs with and without 1-hr NH_3 plasma treatment.

Table 6.1 Comparison of the electrical characteristics of the fresh NW TFT and the 1-hr NH_3-treated NW TFT.

	V_{TH} (V)	μ_{FE} (cm^2/V-s)	S.S. (mV/dec)	I_{ON}/I_{OFF} (V_{DS} = 0.5V)
Fresh NW TFT	2.2	46.7	570	$2.0x10^6$
NH_3-treated NW TFT	0.3	63.5	170	$3.5x10^7$

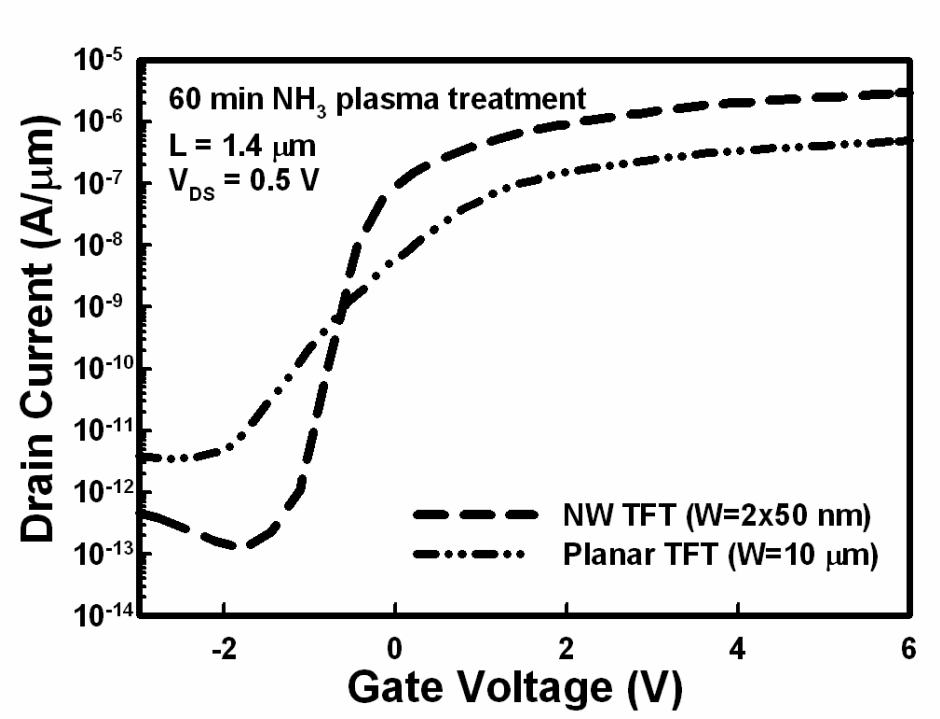


Fig. 6.4. Comparison of the normalized transfer characteristics for the standard planar TFT and the NW TFT.

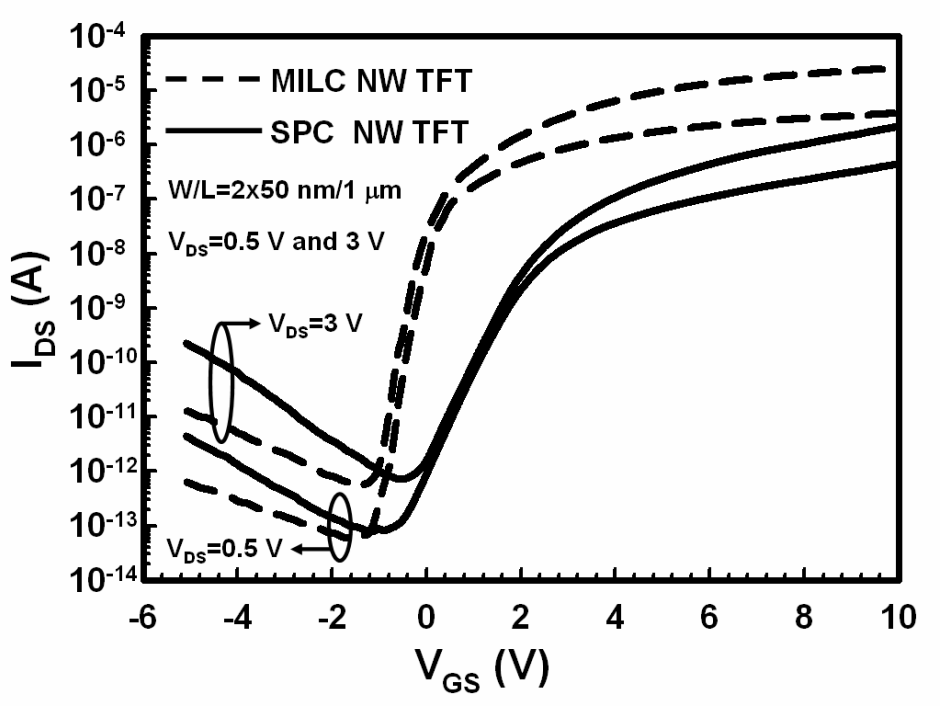


Fig. 6.5. Typical transfer characteristics of the MILC NW TFT and the SPC NW TFT with L = 1 μm and W = 2×50 nm.

Table 6.2 Comparison of the electrical performances of the MILC NW TFT and the SPC NW TFT.

Key parameters	SPC NW TFT	MILC NW TFT
Threshold voltage, V_{TH} (V)	2.7	0.1
Subthreshold swing, S.S. (mV/dec.)	594	199
Field-effect mobility, m_{FE} (cm^2/V-s)	42	156
Maximum GIDL current, $I_{GIDL,\ max}$ (A)	2.39×10^{-10}	1.18×10^{-11}
On/off current ratio, I_{on}/I_{off}	3.2×10^{6}	4.7×10^{7}

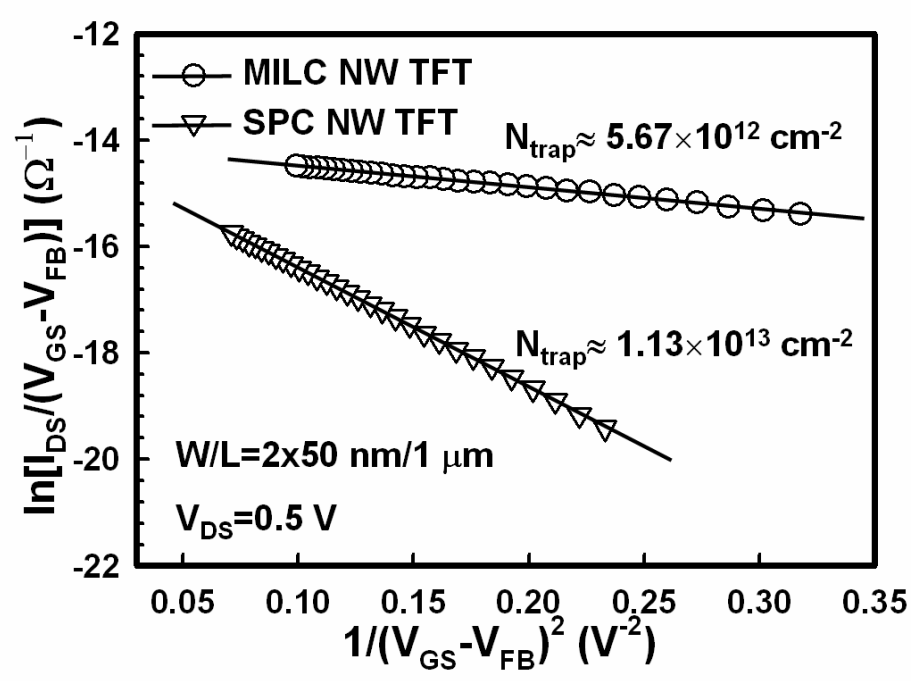


Fig. 6.6. Plot of $\ln[I_{DS}/(V_{GS}-V_{FB})$ versus $1/(V_{GS}-V_{FB})^2$ curves at V_{DS} = 0.5 V and the extracted effective trap-state density.

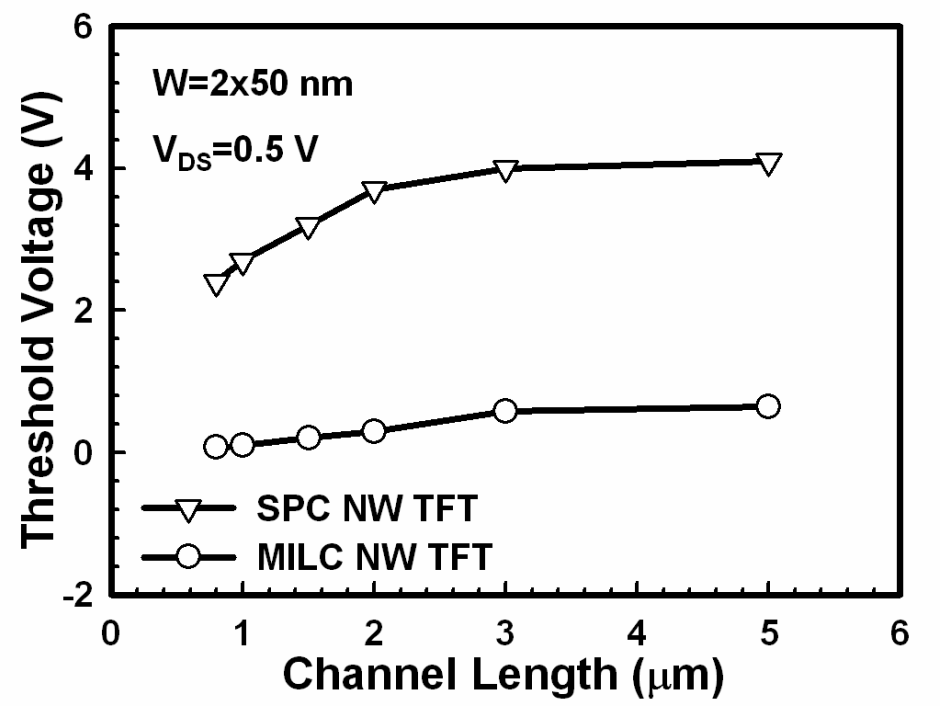


Fig. 6.7. Threshold-voltage rolloff of the MILC NW TFT and the SPC NW TFT with channel length (L) varying from 5 μm to 0.8 μm, the channel width (W) is kept at 2×50 nm.

Chapter 7

Conclusions and Further Recommendations

7.1 Conclusions

In this thesis, SPC poly-Si TFTs with high-κ Pr_2O_3 gate dielectric were proposed. And various fluorine passivation techniques, including fluorine ion implantation and CF_4 plasma treatments, applied to the SPC poly-Si TFTs with high-κ Pr_2O_3 gate dielectric were comprehensively studied. In addition, SPC poly-Si TFTs with two poly-Si grain-size enlargement techniques were demonstrated and characterized. Finally, a simple sidewall spacer technique was developed to fabricate poly-Si NW TFTs crystallized by SPC and MILC techniques. The main results of these studies are summarized as below:

In Chapter 2, high-performance SPC poly-Si TFTs integrated with TiN metal gate and high-κ Pr_2O_3 gate dielectric have been successfully demonstrated for the first time. This work provides the thinnest EOT of 6.5 nm from the high gate capacitance density of Pr_2O_3 film. The electrical characteristics of the poly-Si TFTs with Pr_2O_3 gate dielectric (poly-Si Pr_2O_3 TFTs) can be effectively improved compared to those of poly-Si TFTs with SiO_2 gate dielectric (poly-Si SiO_2 TFTs), including lower threshold voltage, steeper subthreshold swing, higher field-effect mobility, and higher driving current capability, even without additional hydrogenation treatments or advanced phase crystallization techniques. Therefore, the proposed poly-Si Pr_2O_3 TFT technology is a promising candidate for high-speed display driving circuit applications.

In Chapter 3, we have incorporated two kinds of fluorination techniques including fluorine ion implantation and CF_4 plasma treatments into the poly-Si Pr_2O_3 TFTs. Pr_2O_3 gate

dielectric can achieve thin equivalent-oxide thickness and high gate capacitance density. Utilizing these fluorination techniques, fluorine atoms can be introduced into the poly-Si films and the Pr_2O_3 gate dielectric/poly-Si channel interface to passivate the grain-boundary trap states. Hence, the electrical performances and threshold-voltage rolloff properties of the poly-Si Pr_2O_3 TFTs can be significantly improved. Besides, these fluorination techniques also enhance the immunity against hot-carrier stress, due to the formation of strong Si-F bonds. It is concluded that the integration of these effective fluorination techniques and Pr_2O_3 gate dielectric into the poly-Si TFTs could be available for achieving AMLCD applications.

In Chapter 4, we have investigated the solid-phase crystallization of α-Si film with reduced nucleation sites created by heavy Argon ion implantation. It has been found the interface-nucleation rate was suppressed by introducing implant-induced recoiled oxygen at the α-Si/SiO_2 interface so that the microstructural quality of poly-Si films could be improved after SPC process. The electrical characteristics of the poly-Si TFTs, including threshold voltage, subthreshold swing, field-effect mobility, and ON/OFF current ratio, are greatly improved by using the Argon ion implatation technique. In addition, the Argon-implanted poly-Si TFTs also present a higher immunity against the hot-carrier stresses attributing to larger grain size of poly-Si film with fewer grain boundaries defects. Therefore, the Argon-implanted poly-Si TFTs are not only compatible with conventional fabrication processes but also possessing superior electrical characteristics for large flat-panel display applications.

In Chapter 5, we have demonstrated that the α-Si film with floating-channel structure crystallized by SPC process exhibits a better crystallinity of poly-Si film with larger grain size and fewer microstructural defects. Poly-Si TFTs with the self-aligned formation of the floating-channel active region is firstly proposed. The electrical characteristics of the FC poly-Si TFTs, including threshold voltage, subthreshold swing, field-effect mobility,

ON/OFF current ratio, and hot-carrier immunity are significantly improved. Therefore, the proposed FC poly-Si TFTs are not only compatible with existing manufacturing processes but also possess superior electrical properties for large flat-panel display applications.

In Chapter 6, we have demonstrated a simple, low cost, and self-aligned sidewall spacer technique to fabricate the poly-Si TFTs with NW channels crystallized by solid-phase crystallization and metal-induced lateral crystallization techniques. The 50-nm NW channel could be easily realized by anisotropically etched without extra mask or advanced photolithography system. The proposed SPC poly-Si NW TFT has excellent gate controllability due to the tri-gate-like structure with the sidewall and corner contribution effects. Also, for the poly-Si NW channels, effectively passivated deep trap states by NH_3 plasma treatment also improve the electrical characteristics of poly-Si TFTs. On the other hand, the MILC poly-Si NW TFT not only depicts improved turn-on characteristics by forming superior grain crystallinity of poly-Si films but also maintains a low off-state leakage current by reducing the microstructural defects. Moreover, superior short-channel characteristics are also achieved, which might be explained by the formation of single-crystalline grain in the entire channel region. Therefore, the MILC poly-Si NW TFTs could be a promising candidate for AMLCD applications.

7.2 Further Recommendations

There are some interesting and important topics about poly-Si TFTs that are worthy to be further investigated:

(1) As described in Chapter 2, high-κ Pr_2O_3 gate dielectric is a good gate-dielectric candidate for high-performance poly-Si TFTs. However, the off-state gate-induced drain leakage (GIDL) currents of the poly-Si Pr_2O_3 TFTs are somewhat large. The inferior GIDL currents and the on-state electrical characteristics could be further

improved by using different device structures such as lightly doped drain (LDD) and field-induced drain (FID), and adopting advanced crystallization techniques such as metal-induced lateral crystallization (MILC) and excimer-laser crystallization (ELC).

(2) Deposition of high-κ gate dielectric by electron-beam evaporation system is a promising method to characterize the dielectric quality. However, the fabrication of poly-Si TFTs with electron-beam deposited gate dielectric may be limited due to the large-scale glass substrate. Metal-organic chemical vapor deposition (MOCVD) based system or so-gel spin coating method could be promising ways to deposit any pure high-κ, mixed high-κ, and mixed silicates gate dielectrics for further studies.

(3) In Chapter 3, CF_4 plasma treatments provide a good passivation of trap states near the Pr_2O_3 gate dielectric/poly-Si channel interface. However, in this thesis, the fluorine radicals are generated by conventional PECVD systems. High-density plasma (HDP) and electron-cyclotron resonance (ECR) plasma are suggested to further dissociate the CF_4 molecule into fluorine radicals, and thus improve the efficiency of fluorine passivation. Furthermore, introducing fluorine radicals from remote plasma system can avoid plasma-induced damage in the poly-Si film. Some further studies on the CF_4 plasma treatments can be done by adopting these plasma systems.

(4) In Chapter 4 and 5, the electrical performances of the SPC poly-Si TFTs can be improved by utilizing these two kinds of poly-Si grain-size enlargement techniques. The increase of poly-Si grain size usually accompanies the decrease of trap-state density. Integrating high-κ gate dielectric and these grain-size enhancement techniques into poly-Si TFTs to further improve the electrical characteristics is worthy to be studied.

(5) In Chapter 6, a simple sidewall spacer technique is utilized to fabricate poly-Si NW TFTs. The gate electrode with a naturally tri-gate-like structure can exhibit a good electrostatic controllability on the channel potential due to the stronger fringing electric

field. Using tunnel oxide/trapping nitride/blocking oxide (ONO) to replace the traditional gate oxide in the poly-Si NW TFTs may be a feasible way for achieving nonvolatile memory applications.

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Chapter 1

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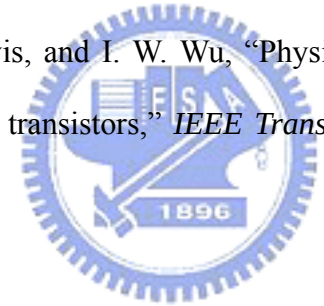

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論文題目: 高介電常數氧化鐠閘極介電層與新穎結構於複晶矽薄膜電晶體之研究

Study on High-κ Pr_2O_3 Gate Dielectric and Novel Structures of Polycrystalline Silicon Thin-Film Transistors

Publication Lists

1. International Journal:

[1]. **Chia-Wen Chang**, Chih-Kang Deng, Che-Lun Chang, and Tan-Fu Lei, "Enhanced Performance and Reliability for Solid Phase Crystallized Poly-Si TFTs with Argon ion implantation," ***J. Electrochem. Soc.***, Vol. 154, No. 11, pp. J375–J378, 2007.

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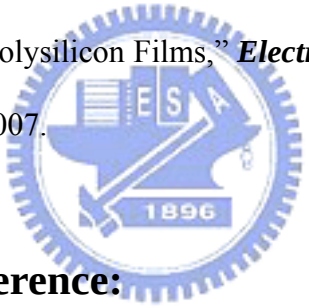

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4. Patents:

[1]. 低製造成本之奈米線通道鰭式薄膜電晶體應用在液晶顯示器，申請中華民國、大陸地區、美國發明專利中。